TECHNICAL MANUAL

LSISAS1064 PCI-X to 4-Port Serial Attached SCSI/SATA Controller

October 2005

Version 3.2

LSI LOGIC®

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Preface

This book is the primary reference and technical manual for the LSISAS1064 PCI-X to 4-Port Serial Attached SCSI/SATA Controller. It contains a complete functional description for the LSISAS1064, as well as the physical and electrical specifications for the LSISAS1064.

Audience

This document assumes that you are familiar with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the LSISAS1064 for use in a system
- Engineers who are designing the LSISAS1064 into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, provides an overview of the LSISAS1064 features and capabilities.
- Chapter 2, **Functional Description**, provides a detailed functional description of the LSISAS1064 operation. This chapter describes the LSISAS1064 implementations of the PCI, PCI-X, and SAS specifications.
- Chapter 3, **Signal Description**, provides a detailed signal description for the LSISAS1064.
- Chapter 4, **PCI Host Register Description**, provides a bit level description of the host interface registers.
- Chapter 5, **Specifications**, provides the electrical and physical specifications for the LSISAS1064.

- Appendix A, **Register Summary**, provides a register map for the LSISAS1064.

Related Publications

LSI Logic Documents
Fusion-MPT™ Device Management User's Guide, Version 2.0, DB15-000186-02

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InterNational Committee on Information Technology Standards (INCITIS) T10 Technical Committee
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Global Engineering Documents
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Serial ATA Working Group
http://www.serialata.org
Email: info@serialata.org

Philips I^2C Bus Specification
http://www.semiconductors.philips.com

SFF-8485 Serial GPIO Bus Specification
http://www.sffcommittee.org

Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive. Signals that are active LOW end with a "/."

Hexadecimal numbers are indicated by the prefix "0x" —for example, 0x32CF. Binary numbers are indicated by the prefix "0b" —for example, 0b0011.0010.1100.1111.

Revision History

Revision	Date	Remarks
Final Version 3.2	9/2005	Updated external memory diagrams. Removed references to Serial EEPROM as it is not supported with this device.
Final Version 3.1	3/2005	Added I^2C and SFF-8485 specifications to the list of references. Updated IR wording in Chapter 1. Added SAS version 1.1 feature compliance statement to Chapter 1. Updated Section 2.8, "Multi-ICE Test Interface," by removing the TST_RST/ signal from the test header pinout. Corrected a typo in Table 4.1. Added a footnote to Table 5.2.
Final Version 3.0	11/2004	Added 2 kV ESD information.
Preliminary Version 2.0	11/2004	Updated PCI and Power Management specification revision numbers. Updated PCI 5 V tolerance information. Updated ZCR information. Updated REFCLK_B signal description. Updated operating conditions data. Updated signal power data.
Advance Version 0.3	1/2004	Updated Table 4.5, the PCI-X Command register default value, and the PCI-X Status register default value.
Advance Version 0.2	12/2003	Initial release of document.

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Chapter 1
Introduction

The LSISAS1064 is a four-port 3.0 Gbit/s SAS/SATA controller that is compliant with the Fusion-MPT™ architecture, provides a PCI-X interface, and supports the Integrated RAID™ solution. This chapter contains the following sections:

1.1 General Description

The LSISAS1064 controller brings 3.0-Gbit/s SAS performance to host adapter, workstation, and server designs, making it easy to add a SAS interface to any PCI or PCI-X[1] system. The LSISAS1064 integrates four high-performance SAS/SATA phys and a 64-bit, 133 MHz PCI-X bus master DMA core. Each of the four phys on the LSISAS1064 is capable of 3.0 Gbit/s and 1.5 Gbit/s SAS link rates, and 3.0 Gbit/s and 1.5 Gbit/s SATA link rates. The LSISAS1064 supports the SAS protocol as described in the Serial Attached SCSI Standard, version 1.0, as well as SAS 1.1 features, such as support for the BROADCAST (SES) primitive and support for SATA port selectors. The controller also supports the Serial ATA (SATA) protocol defined by the Serial ATA specification,

1. In some instances, this manual references PCI-X explicitly. References to the PCI bus may be inclusive of both the PCI specification and PCI-X addendum, or may only refer to the PCI bus depending on the operating mode of the device.

version 1.0a. SATA II is an extension to SATA 1.0a. LSI Logic SAS/SATA controllers also support the following SATA II features:

- 3.0 Gbit/s SATA
- Staggered spin-up
- Hot Plug
- Native Command Queuing
- Activity and fault indicators per phy
- Port Selector (for dual-port drives)

Supporting both the SAS and SATA interfaces, the LSISAS1064 is a versatile controller that provides the backbone of both server and high-end workstation environments. LSI Logic produces the LSISAS1064 using the Gflx™ process technology.

Each port on the LSISAS1064 supports SAS and SATA devices using the SAS Serial SCSI Protocol (SSP), Serial Management Protocol (SMP), Serial Tunneling Protocol (STP), and SATA. The SSP protocol enables communication with other SAS devices. SATA enables the LSISAS1064 to communicate with other SATA devices. The SMP protocol communicates topology management information directly with an attached SAS expander device, such as the LSISASx12. STP enables the LSISAS1064 to communicate with a SATA device through an attached expander.

The LSISAS1064 supports a 133 MHz, 64-bit PCI-X bus. With the exception that the PCI interface is not tolerant of 5 V PCI, the interface is backward compatible with all revisions of the PCI/PCI-X bus. The LSISAS1064 supports PCI-X split completion cycles and 32-bit or 64-bit data bursts with variable burst length. The LSISAS1064 supports the *PCI-X Addendum to the Peripheral Components Interface Specification, Revision 2.0,* and the *Peripheral Components Interface Specification, Revision 3.0*.

Figure 1.1 shows a direct-connect configuration. Figure 1.2 provides an example of the LSISAS1064 configured with an LSISASx12 expander.

Figure 1.1 LSISAS1064 Direct-Connect Example Application

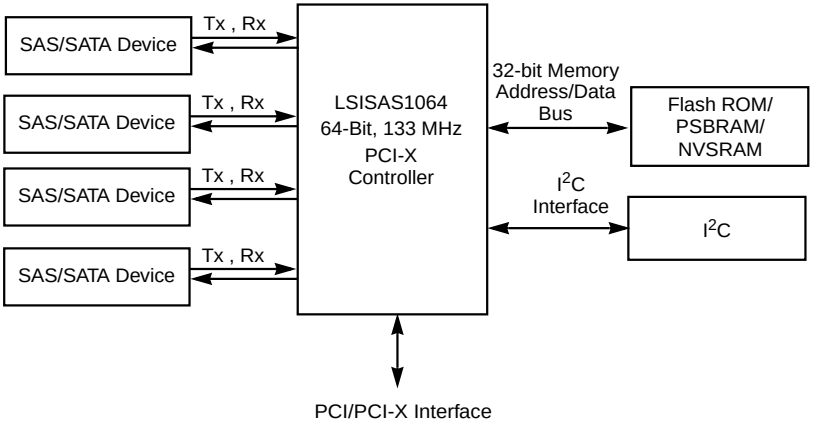
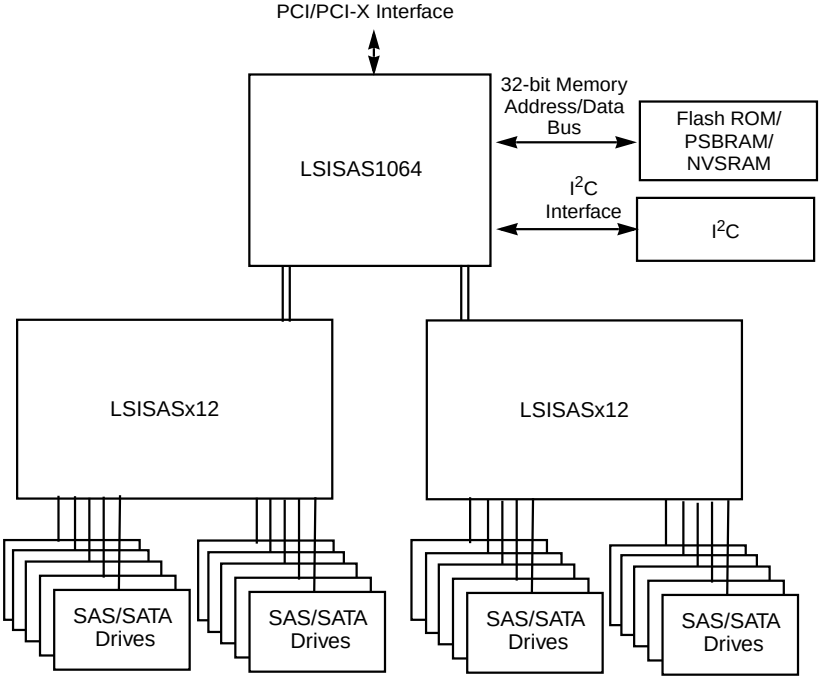


Figure 1.2 LSISAS1064 Controller and LSISASx12 Expander Example Application



The LSISAS1064 employs an ARM926 processor to meet the data transfer flexibility requirements of the host interface PCI-X specifications.

The LSISAS1064 is based on the Fusion-MPT (Message Passing Technology) architecture, which features a performance based message passing protocol that off loads the host CPU by completely managing all I/Os and minimizes system bus overhead by coalescing interrupts. The Fusion-MPT architecture requires only a thin, easy to develop device drivers that is independent of the I/O bus. LSI Logic provides these device drivers.

The LSISAS1064 supports a 32-bit external memory bus. The external memory controller block provides an interface for Flash ROM, NVSRAM, and PSBRAM devices. Most configurations use a Flash ROM to store firmware, configuration information, and persistent data information.

The LSISAS1064 supports the Integrated RAID solution, which is a highly integrated, low cost RAID implementation. It is designed for systems requiring redundancy and high availability, but not needing a full-featured RAID implementation. The Integrated RAID solution includes Integrated Mirroring™ (IM) technology and Integrated Striping™ (IS) technology. IM technology provides physical mirroring of eight physical drives. IM technology requires an NVSRAM to support write journaling. IS technology enables data striping across up to eight physical drives. The Integrated RAID solution is OS independent, easy to install and configure, supports up to eight drives at RAID Level 0, and does not require a special driver. The runtime operation of the Integrated RAID solution is transparent to the operating system. A single firmware build supports all Integrated RAID capabilities. The LSISAS1064 also provides Zero Channel RAID (ZCR) support.

The IR firmware requires a configuration mechanism, which enables configuration of the mirroring attributes during initial setup or reconfiguration after hardware failures or changes in the system environment. Use the LSI Logic BIOS Configuration Utility or the IM DOS Configuration Utility to configure the IR firmware attributes. Host based status software monitors the state of the mirrored drives and reports error conditions as they arise.

1.2 Benefits of SAS

SAS is a serial, point-to-point, enterprise-level device interface that leverages the proven SCSI protocol set. SAS is a convergence of the

advantages of SATA, SCSI, and FC, and is the future mainstay of the enterprise and high-end workstation storage markets. SAS offers a higher bandwidth per pin than parallel SCSI, and improves signal and data integrity.

The SAS interface uses the proven SCSI command set to ensure reliable data transfers, while providing the connectivity and flexibility of point-to-point serial data transfers. The serial transmission of SCSI commands eliminates clock skew challenges. The SAS interface provides improved performance, simplified cabling, smaller connectors, lower pin count, and lower power requirements when compared to parallel SCSI.

SAS controllers leverage a common electrical and physical connection interface that is compatible with Serial ATA technology. The SAS and SATA protocols use a thin, 7-wire connector instead of the 68-wire SCSI cable or 26-wire ATA cable. The SAS/SATA connector and cable are easier to manipulate, allow connections to smaller devices, and do not inhibit airflow. The point-to-point SATA architecture eliminates inherent difficulties created by the legacy ATA master-slave architecture, while maintaining compatibility with existing ATA firmware.

The LSISAS1064 can function as an SSP initiator, an SSP target, an SMP initiator, an STP initiator, or a SATA initiator. The LSISAS1064 uses SSP to communicate with other SAS devices, and uses SMP to communicate topology management information with other SAS devices. STP communicates with SATA devices by tunneling through SAS expanders directly to the SATA device or by using the SATA protocol to communicate directly with the SATA device.

1.3 Benefits of the Fusion-MPT Architecture

The Fusion-MPT architecture provides an open architecture that is ideal for SAS, SATA, SCSI, Fibre Channel, and other emerging interfaces. The I/O interface is interchangeable at the system and application level; embedded software uses the same device interface for different bus implementations, just as application software uses the same storage management interfaces for different bus implementations. LSI Logic provides Fusion-MPT device drivers that are binary compatible between SAS, SATA, Fibre Channel, and Ultra320 SCSI interfaces.

The Fusion-MPT architecture improves overall system performance by requiring only a thin device driver, which off loads the intensive work of managing I/Os from the system processor to the LSISAS1064. The use of thin, easy to develop, common OS device drivers accelerates time to market by reducing device driver development and certification times.

The Fusion-MPT architecture provides an interrupt coalescing feature. Interrupt coalescing allows an I/O controller to send multiple reply messages in a single interrupt to the host processor. Sending multiple reply messages per interrupt reduces context switching of the host processor and maximizes the host processor efficiency, which results in a significant improvement of system performance. To use the interrupt coalescing feature, the host processor must be able to accept and manage multiple replies per interrupt.

The Fusion-MPT architecture also provides built-in device driver stability since the device driver need not change for each revision of the LSISAS1064 silicon or firmware. This architecture is a reliable, constant interface between the host device driver and the LSISAS1064. Changes within the LSISAS1064 are transparent to the host device driver, operating system, and user. The Fusion-MPT architecture also saves the user significant development and maintenance effort since it is not necessary to alter or redevelop the device driver when a revision of the LSISAS1064 device or firmware occurs.

1.4 Benefits of PCI-X

PCI-X doubles the maximum clock frequency of the conventional PCI bus. The *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0*, defines enhancements to the proven *PCI Local Bus Specification, Revision 3.0*. PCI-X provides more efficient data transfers by enabling registered inputs and outputs, improves buffer management by including transaction information with each data transfer, and reduces bus overhead by restricting the use of wait states and disconnects. PCI-X also reduces host processor overhead by providing a wide range of error recovery implementations.

The LSISAS1064 supports up to a 133 MHz, 64-bit PCI-X bus and is backwards compatible with previous versions of the PCI/PCI-X specification. Per the PCI-X addendum, the LSISAS1064 includes

transaction information with all PCI-X transactions to enable more efficient buffer management schemes. Each PCI-X transaction contains a transaction sequence identifier (Tag), the identity of the initiator, and the number of bytes in the sequence. The LSISAS1064 clocks PCI-X data directly into and out of registers, which creates a more efficient data path. The LSISAS1064 increases bus efficiency since it does not insert wait states after the initial data phase when acting as a PCI-X target and never inserts wait states when acting as a PCI-X initiator.

1.5 Benefits of GigaBlaze® Transceivers

The GigaBlaze transceivers provide the physical layer for the LSISAS1064 controller and are a proven component of LSI Logic semiconductor expertise. The Gflx GigaBlaze transceivers are the fifth generation of the LSI Logic GigaBlaze core. The GigaBlaze transceivers provide full-duplex, point-to-point communications channels that can operate at 3.0/1.5 Gbits/s SAS/SATA transfer rates.

The integrated GigaBlaze transceivers perform the 8b/10b conversion that is necessary for SAS and SATA transfers, without burdening either the LSISAS1064 ARM® processor or the host interface. The transmitter accepts parallel data, serializes it, and transmits it on the differential TX+/TX- signals. The receiver recovers the clock and deserializes the data from the bitstream that it receives on the RX+/RX- signals. Because the transceiver and receiver operate independently, the GigaBlaze transceivers can send and receive data simultaneously, which maximizes system performance. The GigaBlaze transceivers also provide integrated internal termination.

1.6 Summary of LSISAS1064 Features

This section provides a summary of the LSISAS1064 features and benefits. It contains information on SAS Features, SATA Features, PCI Performance, Integration, Usability, Flexibility, Reliability, and Testability.

1.6.1 SAS Features

This section describes the SAS features.

- Provides 4 fully independent phys
- Each phy supports 3.0 Gbits/s and 1.5 Gbits/s SAS data transfers
- Supports SSP to enable communication with other SAS devices
- Supports SMP to communicate topology management information
- Provides a serial, point-to-point, enterprise-level storage interface
- Simplifies cabling between devices
- Provides a scalable interface that supports up to 128 devices through multiple expanders
- Supports wide ports consisting of 2, 3, or 4 phys
- Supports narrow ports consisting of a single phy
- Transfers data using SCSI information units

1.6.2 SATA Features

This section describes the SATA features.

- Supports SATA data transfers of 3.0 Gbit/s and 1.5 Gbits/s
- Supports STP data transfers of 3.0 Gbits/s and 1.5 Gbits/s
- Provides a serial, point-to-point storage interface
- Simplifies cabling between devices
- Eliminates the Master-Slave construction used in parallel ATA
- Allows addressing of multiple SATA targets through an expander
- Allows multiple initiators to address a single target (in a fail-over configuration) through an expander

1.6.3 PCI Performance

The LSISAS1064 supports these PCI features:

- 133 MHz, 64-bit PCI/PCI-X interface that:
  - Operates up to 133 MHz PCI-X
  - Operates at 33 MHz or 66 MHz PCI
  - Supports 32-bit or 64-bit data transfers

  - Supports 32-bit or 64-bit addressing through Dual Address Cycles (DAC)
  - Provides a theoretical 1066 Mbytes/s PCI bandwidth
  - Supports 3.3 V PCI, and is not 5 V PCI tolerant
  - Complies with the *PCI Local Bus Specification*, Revision 3.0
  - Complies with the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0
  - Complies with the *PCI Power Management Interface Specification*, Revision 1.2
  - Complies with the *PC2001 Specification*
- Provides unequaled performance through the Fusion-MPT architecture
- Provides high throughput and low CPU utilization to off load the host processor
- Uses a dedicated ARM926 processor
- Presents a single electrical load to the PCI Bus
- Reduces Interrupt Service Routine (ISR) overhead with interrupt coalescing
- Supports Message Signaled Interrupts (MSI) and MSI-X
- Supports 32-bit or 64-bit data bursts with variable burst lengths
- Supports the PCI Cache Line Size register
- Supports the PCI Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands
- Supports the PCI-X Memory Read Dword, Split Completion, Memory Read Block, Memory Write Block commands
- Supports up to 16 PCI-X Split Transaction cycles

1.6.4 Integration

These features make the LSISAS1064 easy to integrate:

- Supports backwards compatibility with previous revisions of the PCI specification, with the exception that the LSISAS1064 does not support 5 V PCI

- Provides a full 32-bit or 64-bit PCI-X DMA bus master
- Reduces time to market with the Fusion-MPT architecture
  - Single driver binary for SAS/SATA, SCSI, and Fibre Channel products
  - One firmware build supports all Integrated RAID capabilities
  - Thin, easy to develop drivers
  - Reduced integration and certification effort

1.6.5 Usability

This section describes the usability features.

- Simplifies cabling with point-to-point, serial architecture
- Smaller, thinner cables do not restrict airflow
- Provides drive spin-up sequencing control
- Provides up to two LED signals for each phy to indicate link activity and faults
- Provides an Inter-IC (I^2C) interface for enclosure management

1.6.6 Flexibility

These features increase the flexibility of the LSISAS1064:

- Supports a Flash ROM interface, a nonvolatile RAM (NVSRAM) interface, and a pipelined synchronous burst SRAM (PSBRAM) interface
- Offers a flexible programming interface to tune I/O performance
- Allows mixed connections to SAS or SATA targets
- Leverages compatible connectors for SAS and SATA connections
- Allows grouping of up to 4 phys to form a wide port
- Allows programming of the World Wide Name

1.6.7 Reliability

These features enhance the reliability of the LSISAS1064:

- Uses proven GigaBlaze transceivers

- Isolates the power and ground of I/O pads and internal chip logic
- Provides 2 kV ESD protection
- Provides latch-up protection
- Has a high proportion of power and ground pins
- Integrated RAID solution provides Integrated Mirroring technology and Integrated Striping technology
- Supports Zero Channel RAID

1.6.8 Testability

These features enhance the testability of the LSISAS1064:

- Offers JTAG boundary scan
- Provides a UART interface for debugging
- Offers ARM Multi-ICE® technology for debugging the ARM9™ processor
- Offers I^2C port to output debug information

Chapter 2
Functional Description

This chapter provides a subsystem level overview of the LSISAS1064, a discussion of the Fusion-MPT architecture, and a functional description of the LSISAS1064 interfaces. This chapter contains the following sections:

The LSISAS1064 is a four port 3.0 Gbit/s SAS controller that is compliant with the Fusion-MPT architecture, provides a PCI-X interface, and supports Integrated RAID solution. The LSISAS1064 supports version 3.0 of the *PCI Local Bus Specification*, revision 2.0 of the *PCI-X Addendum to the PCI Local Bus Specificatio*n, version 1.0 of the ANSI *Serial Attached SCSI* standard, and version 1.0a of the *Serial ATA* standard.

The LSISAS1064 employs the LSI Logic Fusion-MPT architecture to ensure robust system performance, to provide binary compatibility of host software between the LSI Logic SAS/SATA, SCSI, and Fibre Channel products, and to significantly reduce software development time. Refer to the *Fusion-MPT Device Management User’s Guide* for more information on the Fusion-MPT architecture.

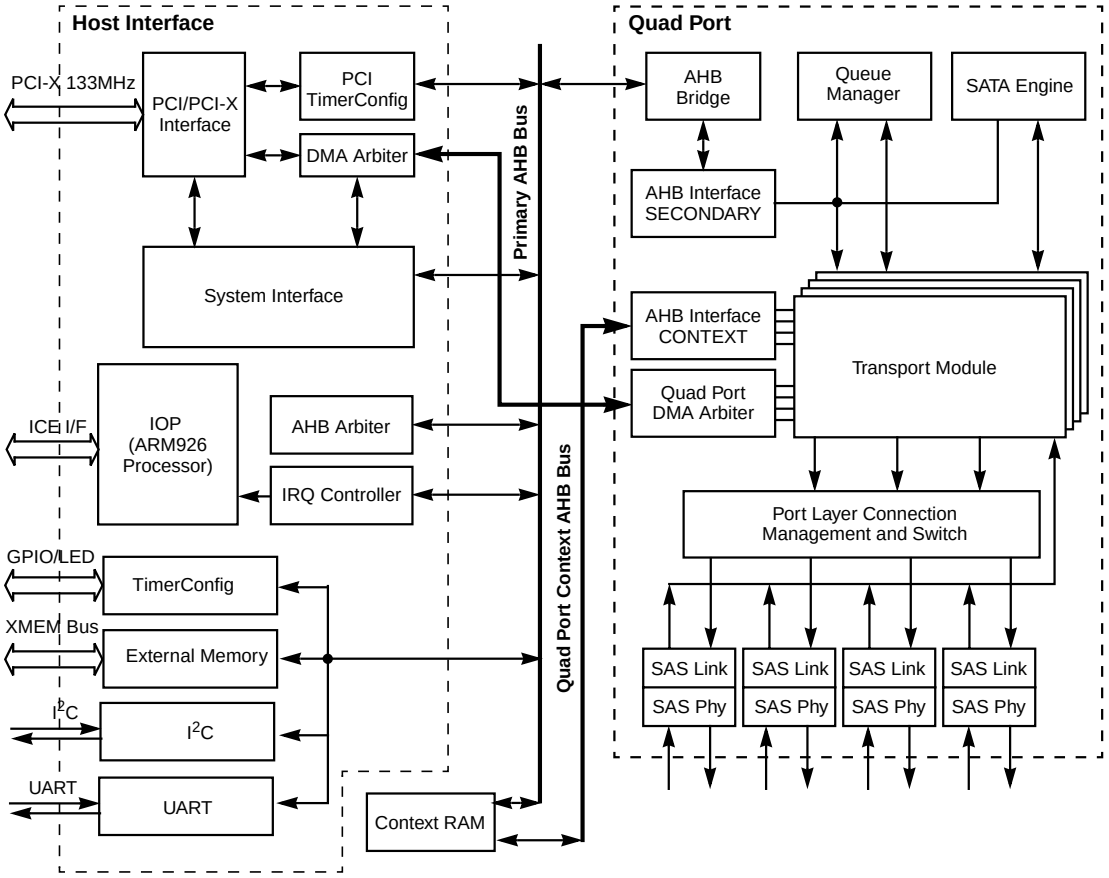
2.1 Block Diagram Description

The LSISAS1064 consists of two major modules and a context RAM. The two major modules are the host interface module and the Quad Port module. The modules consist of the following components:

- Host Interface Module
  - PCI/PCI-X Interface
  - System Interface
  - IOP (ARM926 processor)
  - PCI Timer and Configuration
  - Timer and Configuration
  - DMA Arbiter
  - External Memory Interface
  - I^2C
  - UART
- Quad Port
  - Queue Manager
  - SATA Engine
  - Four Transport Modules
  - Port Layer Connection Management and Switch
  - Four SAS Links and four SAS Phys
- Context RAM

Figure 2.1 illustrates the relationship between these modules. The following sections describe each submodule.

Figure 2.1 LSISAS1064 Controller Block Diagram



2.1.1 Host Interface Module Description

The host interface module provides an interface between the host driver and the Quad Port. The host interface module controls system DMA transfers and the host side of the LSI Logic Fusion-MPT architecture. The host interface module contains the PCI/PCI-X interface, system interface, PCI timer and configuration, DMA arbiter, IOP, I^2C, TimerConfig, UART, and external memory blocks. This section provides a detailed explanation of the host interface submodules.

2.1.1.1 PCI/PCI-X Interface

The LSISAS1064 provides a PCI-X interface that supports up to a 64-bit, 133 MHz PCI-X bus. The LSISAS1064 PCI interface is backward compatible with previous implementations of the PCI specification, with the exception that the LSISAS1064 does not support 5 V PCI. For more information on the PCI interface, refer to Section 2.3, "PCI Functional Description."

2.1.1.2 System Interface

In combination with the IOP, the system interface supports the Fusion-MPT architecture. The system interface efficiently passes messages between the LSISAS1064 and the host using a high-performance, packetized mailbox architecture. The LSISAS1064 system interface coalesces PCI interrupts to minimize traffic on the PCI bus and maximize system performance. The system interface contains five hardware FIFOs for the message queuing lists: Request Free FIFO, Request Post FIFO, Reply Free FIFO, Reply Post FIFO, and High Priority Request FIFO. The LSISAS1064 contains control logic for the FIFOs, while the messages are stored in the context RAM or in external memory.

All host accesses to the IOP, external memory, and timer and configuration subsystems pass through the system interface and use the primary bus. The host system initiates data transactions on the primary bus with the system interface registers. PCI Memory Space [0] and the PCI I/O Base Address registers identify the location of the system interface register set. Chapter 4, "PCI Host Register Description," provides a bit level description of the system interface register set.

2.1.1.3 IOP

The LSISAS1064 I/O processor controls the system interface and manages the host side of the Fusion-MPT architecture without host processor intervention, which frees the host processor for other tasks. The LSISAS1064 I/O processor (IOP) is a 32-bit ARM926 RISC processor that provides instruction and data requests to streamline operations and increase performance.

2.1.1.4 PCI Timer and Configuration

This PCI Timer and Configuration module supports the PCI configuration register space, an industry-standard and a power-on reset (POR).

2.1.1.5 Timer and Configuration

This block supports the LSISAS1064 LED and GPIO interfaces. There are a total of nine LED signals on the LSISAS1064. Each of the four phys has an LED signal to indicate activity on the link and an LED signal to indicate an error on the link. The GPIO interface contains four independent GPIO signals. The LED signals can also be configured as GPIO signals. This block provides an firmware heartbeat LED. This block also supports internal timing adjustments and power-on sense configuration options.

2.1.1.6 DMA Arbiter

The LSISAS1064 provides the ability to transfer system memory blocks to and from local memory through the descriptor-based DMA arbiter and router.

2.1.1.7 External Memory

The external memory controller block provides an interface for Flash ROM, NVSRAM, and PSBRAM devices. The external memory bus provides a 32-bit memory bus, parity checking, and chip select signals for PSBRAM, NVSRAM, and Flash ROM.

Typical system configurations require a Flash ROM to store firmware, configuration information, and persistent data information.

2.1.1.8 I^2C

The LSISAS1064 contains an Inter-IC (I^2C) interface that communicates with peripherals. This interface is also referred to as an industry standard 2-wire interface (ISTWI). The I^2C block operates as either a master or a slave on the bus and sustains data rates up to 400 Kbits/s. The I^2C block accomplishes byte-wise bidirectional data transfers by using either an interrupt or a polling handshake at the completion of each byte. The style and operation of this interface closely follows the de facto standard for a

two-wire serial interface chip. The I^2C block controls all bus timing and performs bus-specific sequences.

2.1.1.9 UART

The UART provides test and debug access to the LSISAS1064.

2.1.2 Quad Port

The Quad Port module in the LSISAS1064 implements the SSP, SMP, and STP/SATA protocols, and manages the four SAS/SATA PHYs. The following subsections describe the Quad Port module. Refer to Section 2.4, “SAS Functional Description,” for an operational description of the LSISAS1064 SAS ports.

2.1.2.1 Transport Module

The transport modules transmit frames to and from the port layer and implement the STP, SSP, and SMP protocols. There are four instances of the transport module, one for each SAS/SATA phy on the LSISAS1064.

2.1.2.2 Queue Manager

The queue manager is responsible for managing various queue structures that support the SSP, SMP, and STP protocols. The queue structures are the primary means for the IOP to initiate I/Os to the hardware, and for the hardware to notify the IOP of I/O status.

2.1.2.3 SATA Engine

The SATA engine provides information to the transport modules to enable handling of SATA commands. The SATA engine tracks queued commands per device and provides these tags to the SATA transport layer blocks.

2.1.2.4 Port Layer Connection Manager and Switch

The port layer connection monitor and switch manages transmission requests from the transport modules and originates connection requests to the SAS links. It is also responsible for handling SAS wide port configurations.

2.1.2.5 SAS Link and Phy

The LSISAS1064 uses the Gflx GigaBlaze transceivers to implement the SAS link. The SAS link layer manages SAS connections between initiator and target ports, data clocking, and CRC checking on received data. The SAS link is also responsible for starting a link reset sequence.

The SAS phys interface to the physical layer, perform serial-to-parallel conversion of received data and parallel-to-serial conversion of transmit data, manage phy reset sequences, and perform 8b/10b encoding.

2.1.2.6 Quad Port DMA Arbiter

The quad port arbiter interfaces with the host interface DMA arbiter and determines bus priority between each of the four ports for DMA transfers.

2.1.3 Context RAM

The context RAM is a memory that is shared between the host interface module and the quad port module. The context RAM contains the message frames, the FIFOs, and a portion of the firmware.

2.2 Fusion-MPT Architecture Overview

The Fusion-MPT architecture provides two I/O methods for the host system to communicate with the IOP: the system interface doorbell and the message queues.

The system interface doorbell is a simple message passing mechanism that allows the PCI host system and IOP to exchange single 32-bit Dword messages. When the host system writes to the doorbell, the LSISAS1064 hardware generates a maskable interrupt to the IOP, which can then read the doorbell value and take the appropriate action. When the IOP writes a value to the doorbell, the LSISAS1064 hardware generates a maskable interrupt to the host system. The host system can then read the doorbell value and take the appropriate action.

There are two, 32-bit message queues: the request message queue and the reply message queue. The host uses the request queue to request an action by the LSISAS1064, and the LSISAS1064 uses the reply queue to return status information to the host. The request message

queue consists of the request post FIFO. The reply message queue consists of both the reply post FIFO and the reply free FIFO. The context RAM contains the message queues. The Fusion-MPT architecture also provides a High Priority Request FIFO to provide high priority request free messages to the host on reads and to accept high priority request post messages from the host on writes.

Communication using the message queues occurs through request messages and reply messages. Request message frame descriptors are pointers to the request message frames and are passed through the request post FIFO. The request message frame data structure is up to 128 bytes in length and includes a message header and a payload. The header uniquely identifies the message. The payload contains information that is specific to the request. Reply message frame descriptors have one of two formats and are passed through the reply post FIFO. When indicating the successful completion of a SCSI I/O, the IOP writes the reply message frame descriptor using the Context Reply format, which is a message context. If a SCSI I/O does not complete successfully, the IOP uses the Address Reply format. In this case, the IOP pops a reply message frame from the reply free FIFO, generates a reply message describing the error, writes the reply message to system memory, and writes the address of the reply message frame to the reply post FIFO. The host can then read the reply message and take the appropriate action.

The doorbell mechanism provides both a communication path that interrupts the host system device driver and an alternative communication path to the message queues. Since data transport through the system doorbell occurs a single Dword at a time, use the LSISAS1064 message queues for normal operation and data transport.

2.3 PCI Functional Description

The host PCI interface complies with the *PCI Local Bus Specification, Version 3.0* and the *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0*. The LSISAS1064 supports a 133 MHz, 64-bit PCI-X bus. The LSISAS1064 provides support for 64-bit addressing with Dual Address Cycle (DAC). The LSISAS1064 does not support 5 V PCI signaling.

2.3.1 PCI Addressing

The three physical address spaces the PCI specification defines are:

- PCI Configuration Space
- PCI I/O Space for operating registers
- PCI Memory Space for operating registers

The following sections describe the PCI address spaces.

2.3.1.1 PCI Configuration Space

The PCI Configuration Space is a contiguous 256 x 8-bit set of addresses. The system BIOS initializes the configuration registers using PCI configuration cycles. The LSISAS1064 decodes C_BE[3:0]/ to determine if a PCI cycle intends to access the configuration register space. The IDSEL signal behaves as a chip select signal that enables access to the configuration register space only. The LSISAS1064 ignores configuration read/write cycles when IDSEL is not asserted.

Bits AD[10:8] address the PCI Function Configuration Space (AD[10:8] = 0b000). The LSISAS1064 does not respond to any other encodings of AD[10:8]. Bits AD[7:2] select one of the 64 Dword registers in the device's PCI Configuration Space. Bits AD[1:0] determine if the configuration command is a Type 0 Configuration Command (AD[1:0] = 0b00) or a Type 1 Configuration Command (AD[1:0] = 0b01). Since the LSISAS1064 is not a PCI Bridge device, all PCI Configuration Commands designated for the LSISAS1064 must be Type 0. C_BE[3:0]/ address the individual bytes within each Dword and determine the type of access to perform.

2.3.1.2 PCI I/O Space

The PCI specification defines I/O Space as a contiguous 32-bit I/O address that all system resources share, including the LSISAS1064. The I/O Base Address register determines the 256-byte PCI I/O area that the PCI device occupies.

2.3.1.3 PCI Memory Space

The LSISAS1064 contains two PCI memory spaces: PCI Memory Space [0] and PCI Memory Space [1]. PCI Memory Space [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. The LSISAS1064 requires 64 Kbytes of memory space.

The PCI specification defines memory space as a contiguous 64-bit memory address that all system resources share. The Memory [0] Low and Memory [0] High registers determine which 64 Kbyte memory area PCI Memory Space [0] occupies. The Memory [1] Low and Memory [1] High registers determine which 64 Kbyte memory area PCI Memory Space [1] occupies.

2.3.2 PCI Commands and Functions

Bus commands indicate to the target the type of transaction the master is requesting. The master encodes the bus commands on the C_BE[3:0]/ lines during the address phase. The PCI bus command encodings appear in Table 2.1.

Table 2.1 PCI/PCI-X Bus Commands and Encodings[1]

C_BE[3:0]/	PCI Command	PCI-X Command	Supports as Master	Supports as Slave
0b0000	Interrupt Acknowledge	Interrupt Acknowledge	No	No
0b0001	Special Cycle	Special Cycle	No	No
0b0010	I/O Read	I/O Read	Yes	Yes
0b0011	I/O Write	I/O Write	Yes	Yes
0b0100	Reserved	Reserved	N/A	N/A
0b0101	Reserved	Reserved	N/A	N/A
0b0110	Memory Read	Memory Read Dword	Yes	Yes
0b0111	Memory Write	Memory Write	Yes	Yes
0b1000	Reserved	Alias to Memory Read Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1001	Reserved	Alias to Memory Write Block	PCI: N/A PCI-X: No	PCI: N/A PCI-X: Yes
0b1010	Configuration Read	Configuration Read	No	Yes
0b1011	Configuration Write	Configuration Write	No	Yes

Table 2.1 PCI/PCI-X Bus Commands and Encodings[1] (Cont.)

C_BE[3:0]/	PCI Command	PCI-X Command	Supports as Master	Supports as Slave
0b1100	Memory Read Multiple	Split Completion	Yes	Yes[2]
0b1101	Dual Address Cycle	Dual Address Cycle	Yes	Yes
0b1110	Memory Read Line	Memory Read Block	Yes	Yes[2]
0b1111	Memory Write and Invalidate	Memory Write Block	Yes	Yes[3]

1. The LSISAS1064 ignores reserved commands as a slave and never generates them as a master.
2. When acting as a slave in the PCI mode, the LSISAS1064 supports this command as the PCI Memory Read command.
3. When acting as a slave in the PCI mode, the LSISAS1064 supports this command as the PCI Memory Write command.

The following sections describe how the LSISAS1064 implements these commands.

2.3.2.1 Interrupt Acknowledge Command

The LSISAS1064 ignores this command as a slave and never generates it as a master.

2.3.2.2 Special Cycle Command

The LSISAS1064 ignores this command as a slave and never generates it as a master.

2.3.2.3 I/O Read Command

The I/O Read command reads data from an agent mapped in the I/O address space. When decoding I/O commands, the LSISAS1064 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSISAS1064 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.4 I/O Write Command

The I/O Write command writes data to an agent mapped in the I/O address space. When decoding I/O commands, the LSISAS1064 decodes the lower 32 address bits and ignores the upper 32 address bits. The LSISAS1064 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.5 Memory Read Command

The LSISAS1064 uses the Memory Read command to read data from an agent mapped in the memory address space. The target can perform an anticipatory read if such a read produces no side effects. The LSISAS1064 supports this command when operating in the PCI bus mode.

2.3.2.6 Memory Read Dword Command

The Memory Read Dword command reads up to a single Dword of data from an agent mapped in the memory address space and can only be initiated as a 32-bit transaction. The target can perform an anticipatory read if such a read produces no side effects. The LSISAS1064 supports this command when operating in the PCI-X bus mode.

2.3.2.7 Memory Write Command

The Memory Write command writes data to an agent mapped in the memory address space. The target assumes responsibility for data coherency when it returns “ready.” The LSISAS1064 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.8 Alias to Memory Read Block Command

This command is reserved for future implementations of the PCI specification. The LSISAS1064 never generates this command as a master. When a slave, the LSISAS1064 supports this command using the Memory Read Block command.

2.3.2.9 Alias to Memory Write Block Command

This command is reserved for future implementations of the PCI specification. The LSISAS1064 never generates this command as a master. When a slave, the LSISAS1064 supports this command using the Memory Write Block command.

2.3.2.10 Configuration Read Command

The Configuration Read command reads the configuration space of a device. The LSISAS1064 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the

LSISAS1064 by asserting its IDSEL signal when AD[1:0] equal 0b00. During the address phase of a configuration cycle, AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] address the PCI function Configuration Space (AD[10:8] = 0b000). The LSISAS1064 treats AD[63:11] as logical don't cares.

2.3.2.11 Configuration Write Command

The Configuration Write command writes the configuration space of a device. The LSISAS1064 never generates this command as a master, but does respond to it as a slave. A device on the PCI bus selects the LSISAS1064 by asserting its IDSEL signal when bits AD[1:0] equal 0b00. During the address phase of a configuration cycle, bits AD[7:2] address one of the 64 Dword registers in the configuration space of each device. C_BE[3:0]/ address the individual bytes within each Dword register and determine the type of access to perform. Bits AD[10:8] decode the PCI function Configuration Space (AD[10:8] = 0b000). The LSISAS1064 treats AD[63:11] as logical don't cares.

2.3.2.12 Memory Read Multiple Command

The Memory Read Multiple command is identical to the Memory Read command, except it additionally indicates that the master intends to fetch multiple cache lines before disconnecting. The LSISAS1064 supports PCI Memory Read Multiple functionality when operating in the PCI mode and determines when to issue a Memory Read Multiple command instead of a Memory Read command.

Burst Size Selection – The Read Multiple command reads multiple cache lines of data during a single bus ownership. The number of cache lines the LSISAS1064 reads is a multiple of the cache line size, which Revision 3.0 of the PCI specification provides. The LSISAS1064 selects the largest multiple of the cache line size based on the amount of data to transfer.

2.3.2.13 Split Completion Command

Split transactions in PCI-X replace the delayed transactions in conventional PCI. The LSISAS1064 supports up to 16 outstanding split

transactions when operating in the PCI-X mode. A split transaction consists of at least two separate bus transactions: a split request, which the requester initiates, and one or more split completion commands, which the completer initiates. Revision 2.0 of the PCI-X addendum permits split transaction completion for the Memory Read Block, Alias to Memory Read Block, Memory Read Dword, Interrupt Acknowledge, I/O Read, I/O Write, Configuration Read, and Configuration Write commands. When operating in the PCI-X mode, the LSISAS1064 supports the Split Completion command for all of these commands except the Interrupt Acknowledge command, which the LSISAS1064 neither responds to nor generates.

2.3.2.14 Dual Address Cycles (DAC) Command

The LSISAS1064 performs Dual Address Cycles (DAC), per the *PCI Local Bus Specification, Version 3.0*. The LSISAS1064 supports this command when operating in either the PCI or PCI-X bus mode.

2.3.2.15 Memory Read Line Command

This command is identical to the Memory Read command except it additionally indicates that the master intends to fetch a complete cache line. The LSISAS1064 supports this command when operating in the PCI mode.

2.3.2.16 Memory Read Block Command

The LSISAS1064 uses this command to read from memory. The LSISAS1064 supports this command when operating in the PCI-X mode.

2.3.2.17 Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except it additionally guarantees a minimum transfer of one complete cache line. The master uses this command when it intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size register. The LSISAS1064 determines when to issue a Write and Invalidate command instead of a Memory Write command and supports this command when operating in the PCI bus mode.

Alignment – The LSISAS1064 uses the calculated line size value to determine if the current address aligns to the cache line size. If the address does not align, the LSISAS1064 bursts data using a noncache command. If the starting address aligns, the LSISAS1064 issues a Memory Write and Invalidate command using the cache line size as the burst size.

Multiple Cache Line Transfers – The Memory Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The LSISAS1064 issues a burst transfer as soon as it reaches a cache line boundary. The PCI Local Bus specification states that the transfer size must be a multiple of the cache line size. The LSISAS1064 selects the largest multiple of the cache line size based on the transfer size. When the DMA buffer contains less data than the value Cache Line Size register specifies, the LSISAS1064 issues a Memory Write command on the next cache boundary to complete the data transfer.

2.3.2.18 Memory Write Block Command

The LSISAS1064 uses this command to burst data to memory. The LSISAS1064 supports this command when operating in the PCI-X bus mode.

2.3.3 PCI Arbitration

The LSISAS1064 contains an independent bus mastering function. The system interface bus mastering function manages DMA operations as well as the request and reply message frames.

2.3.4 PCI Cache Mode

The LSISAS1064 supports an 8-bit Cache Line Size register. The Cache Line Size register provides the ability to sense and react to nonaligned addresses corresponding to cache line boundaries. The LSISAS1064 determines when to issue a PCI cache command (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate), or PCI noncache command (Memory Read or Memory Write command).

2.3.5 PCI Interrupts

The LSISAS1064 signals an interrupt to the host processor either using PCI interrupt pins (INTA/ and ALT_INTA/), or Message Signaled Interrupts (MSI and MSI-X). The Interrupt Request Routing Mode bits in the Host Interrupt Mask register configure the routing of each interrupt to either the INTA/ and/or the ALT_INTA/ pin.

MSI is an optional feature that enables a device to signal an interrupt by writing to a specified address. MSI-X is an extension of the MSI that increases the number of available message vectors, allows software aliasing of message vectors, and allows each message vector to use an independent address and data value. If using MSI or MSI-X, the LSISAS1064 does not signal interrupts on INTA/ or ALT_INTA/. Note that enabling MSI or MSI-X to mask PCI interrupts is a violation of the PCI specification. The LSISAS1064 implements its own MSI and MSI-X register sets. The MSI functionality is managed through the MSI register set, and the MSI-X functionality is managed through the MSI-X register set. The PCI specification prohibits system software from simultaneously enabling MSI and MSI-X.

The Host Interrupt Mask register also prevents the assertion of a PCI interrupt to the host processor by selectively masking reply interrupts and system doorbell interrupts. This register masks both pin-based and MSI-based interrupts.

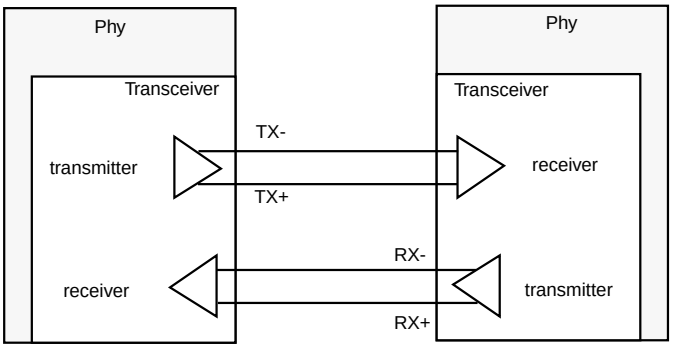
2.3.6 Power Management

The LSISAS1064 complies with the *PCI Power Management Interface Specification, Revision 1.2,* and the *PC2001 System Design Guide*. The LSISAS1064 supports the D0, D1, D2, $D3_{hot}$, and $D3_{cold}$ power states. D0 is the maximum power state, and D3 is the minimum power state. Power State D3 is further categorized as $D3_{hot}$ or $D3_{cold}$. Powering the device off places it in the $D3_{cold}$ Power State.

2.4 SAS Functional Description

The LSISAS1064 provides four SAS/SATA phys. Each phy can form one side of the physical link in a connection with a phy on a different SAS/SATA device. The physical link contains four wires that form two differential signal pairs. One differential pair transmits signals, while the other differential pair receives signals. Both differential pairs operate simultaneously, and allow concurrent data transmission in both the receive and the transmit directions. Figure 2.2 shows two phys that are attached with a physical link.

Figure 2.2 Transceivers within a Phy

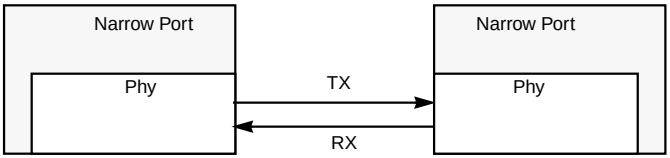


Phys are contained within ports. A port can contain a single phy or can contain multiple phys. A narrow port contains a single phy, while a wide port contains multiple phys. The LSISAS1064 supports wide ports that contain up to four phys. Any of the LSISAS1064 ports can combine to form a wide port. Since each phy within a wide port can transmit data at 3.0 Gbit/s SAS, increasing the number of phys in a port increases the data transfer rate. Combining the four phys on the LSISAS1064 into a wide port enables bandwidths of up to 12.0 Gbits/s.

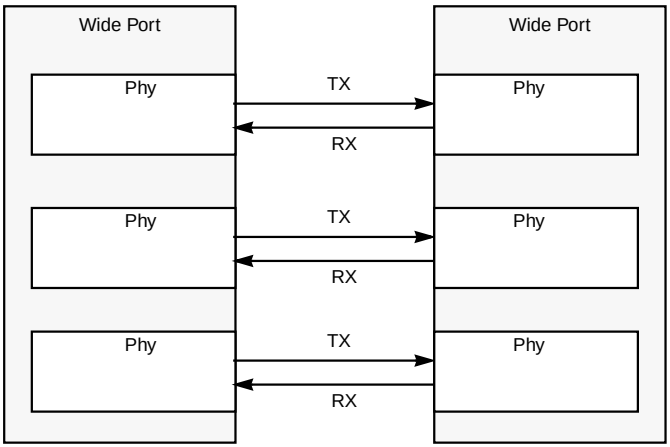
A link between two narrow ports is a narrow link. A link between two wide ports is a wide link. Figure 2.3 illustrates a narrow link and a wide link. The wide link contains three phys in each port.

Figure 2.3 Narrow and Wide Links

a. Narrow Link Containing One Phy in each Port



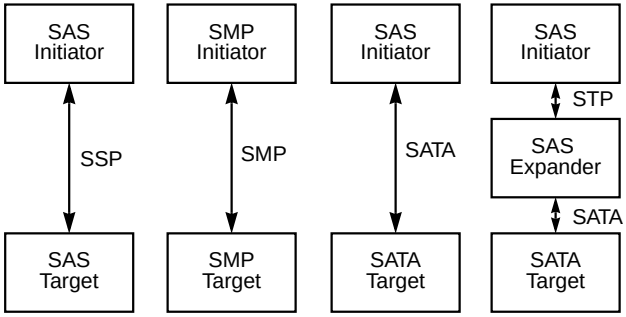
b. Wide Link Containing Three Phys in each Port



Each phy on the LSISAS1064 can function as an SSP Initiator, an SSP target, an SMP initiator, an STP initiator, or a SATA Initiator. A phy can function in only one role during a connection, but function in different roles during different connections. The LSISAS1064 uses SSP to communicate with other SAS devices, and uses SMP to communicate management information with other SAS devices. STP communicates with SATA devices in a SAS domain by tunneling through SAS expanders to the SATA device. The LSISAS1064 can also use SATA to communicate with other SATA devices.

Figure 2.4 illustrates the uses of the SSP, STP, and SMP protocols.

Figure 2.4 SSP, STP, and SMP Protocol Usage



2.5 External Memory Interface

The external memory control block provides a direct slave interface between the internal primary AHB bus and an external 32-bit memory interface. This interface is for accessing external Flash ROM and NVSRAM devices. Because the LSISAS1064 uses a 32-bit multiplexed address/data bus, designs using the LSISAS1064 do not require latches or CPLD devices to construct memory addresses.

2.5.1 Memory Requirements

The memory requirements for the LSISAS1064 depend on the board design and application. Several board design possibilities and their respective memory requirements are presented as follows.

- System board implementation
  - If the system uses the firmware download boot procedure, external memory may be required depending on the system implementation.
  - If the system does not use the firmware download boot procedure, then the LSISAS1064 requires only a Flash ROM.
- Host Bus Adapter (HBA) implementation
  - The LSISAS1064 requires only a Flash ROM.
- Intelligent IOP implementation

  - The LSISAS1064 has no memory requirements in this configuration, assuming that the intelligent IOP can download the firmware image to the LSISAS1064 and store the persistent data.
- Integrated RAID implementation
  - The LSISAS1064 requires a Flash ROM for Integrated RAID implementations.
  - The LSISAS1064 requires an NVSRAM for all Integrated Mirroring implementations.

The LSISAS1064 does not require a PSBRAM for any board design or application.

2.5.2 Flash ROM Controller

The LSISAS1064 Flash ROM interface provides access to nonvolatile code and parameter storage for both the embedded ARM core and the host system. An 8-bit wide Flash ROM is optional if the LSISAS1064 is not the boot device, and a suitable driver exists to initialize the LSISAS1064 and download its code. The Flash ROM interface:

- uses an 8-bit data bus
- reads 4 bytes from the Flash ROM and returns the resulting 32-bit Dword for each Dword read request
- writes a single data byte/word for each Flash ROM write request

Byte lane 3 of the LSISAS1064 external memory bus (MAD[31:24]) connects to the 8-bit data bus on the Flash ROM. BWE[3]/ provides the write enable signal for the Flash ROM. MOE[1]/ enables the Flash ROM to drive data.

The LSISAS1064 determines the Flash ROM addressable space during the Power-On Sense configuration. If the Flash ROM addressable space is 64 Kbytes or less, then the LSISAS1064 defines only the middle (MAD[15:8]) and lower (MAD[7:0]) address ranges during a read or write. If the Flash ROM addressable space is 128 Kbytes or greater, then the LSISAS1064 defines the upper (MAD[23:16]), middle (MAD[15:8]), and lower (MAD[7:0]) address ranges.

The firmware requirements for the Flash ROM are:

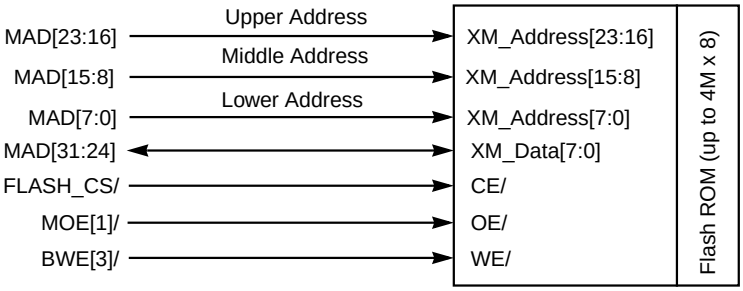
- 1 Mbyte (1 Mbit x 8) or larger Flash ROM size

- Uniform sector and/or boot block sector
- 64 Kbyte maximum sector size
- Intel/Sharp extended command set and/or AMD/Fujitsu extended command set programming algorithms

The Fusion-MPT firmware for the LSISAS1064 supports all CFI Flash parts and a limited set of non-CFI Flash parts. Contact the LSI Logic or OEM representative for a current list of supported non-CFI Flash parts.

Figure 2.5 provides a diagram of a Flash ROM configuration.

Figure 2.5 Flash ROM Block Diagram



Flash Signature Recognition – The LSISAS1064 implements a Flash ROM signature recognition mechanism to determine whether the Flash ROM contains a valid image. The Flash ROM can be present and not contain a valid image either before its initial programming or during board testing.

The first access to the Flash ROM is a 16-byte burst read beginning at Flash ROM address 0x000000. The LSISAS1064 compares the values read to the Flash ROM signature values in Table 2.2. If the signature values match, the LSISAS1064 performs the instruction located at Flash ROM address 0x000000. If the signature values do not match, the LSISAS1064 records an error and ignores the Flash ROM instruction. The Flash ROM signature does not include the first 3 bytes of Flash ROM memory because these bytes contain a branch offset instruction.

Table 2.2 Flash ROM Signature Value

Flash ROM Address	Flash ROM Signature Values			
Bytes [3:0]	0xEA	XX	XX	XX

Table 2.2 Flash ROM Signature Value (Cont.)

Flash ROM Address	Flash ROM Signature Values			
Bytes [7:4]	0x5A	0xEA	0xA5	0x5A
Bytes [11:8]	0xA5	0x5A	0xEA	0xA5
Bytes [15:12]	0x5A	0xA5	0x5A	0xEA

2.5.3 NVSRAM Controller

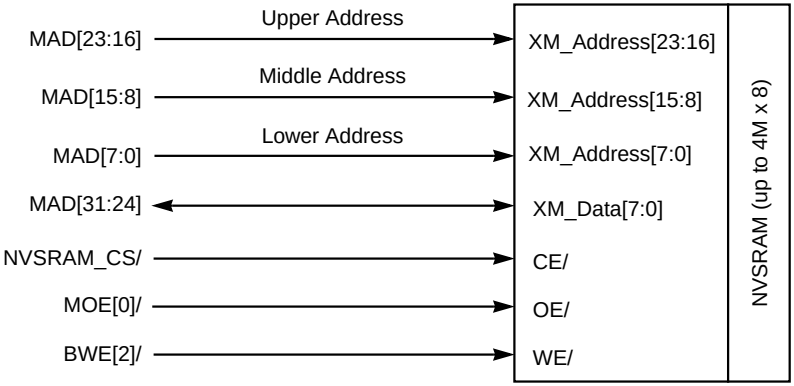
The LSISAS1064 provides a NVSRAM interface that supports write journaling in Integrated Mirroring applications or provides memory space for firmware code overflow.

This interface provides up to 24 address bits to address an NVSRAM; however, the LSISAS1064 supports NVSRAM capacities of up to 128 Kbytes. The NVSRAM interface:

- uses an 8-bit data bus
- writes a Dword, word, or byte according to the write cycle
- reads 4 bytes from the NVSRAM and returns the resulting 32-bit Dword for each AHB Dword read request

Byte lane 3 of the LSISAS1064 external memory bus (MAD[31:24]) connects to the 8-bit data bus of the NVSRAM. BWE[2]/ provides the write enable signal for the NVSRAM. The MOE[0]/ signal enables the attached NVSRAM to drive data. Figure 2.6 provides an example NVSRAM configuration.

Figure 2.6 NVSRAM Block Diagram



2.6 Zero Channel RAID

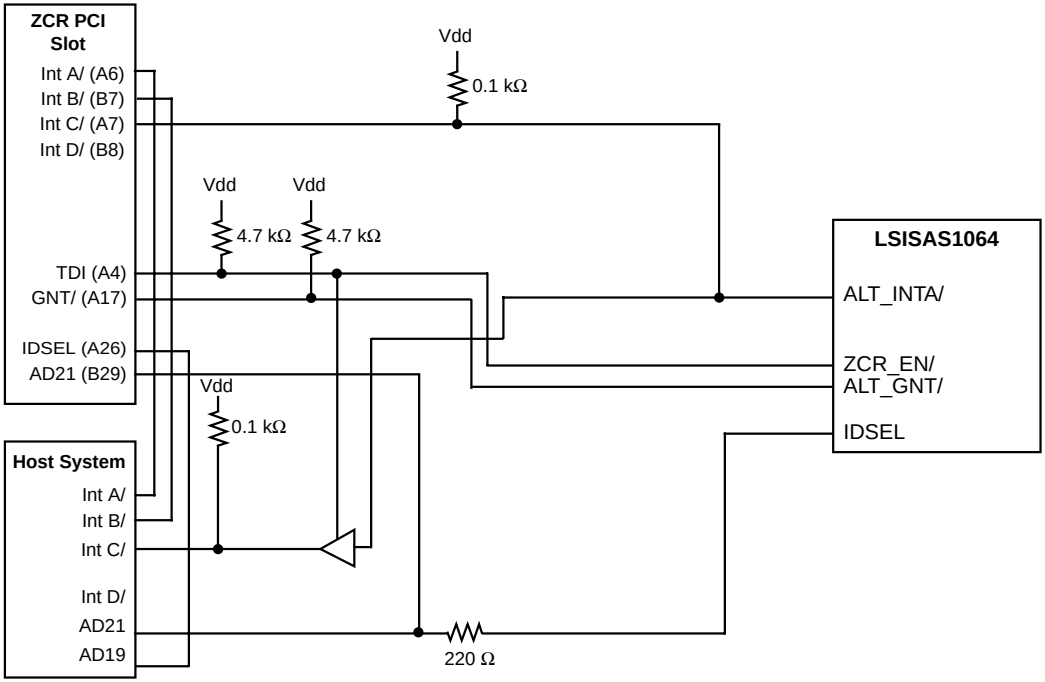
Zero channel RAID (ZCR) capabilities enable the LSISAS1064 to respond to accesses from a PCI RAID controller card or chip that is able to generate ZCR cycles. The LSISAS1064's ZCR functionality is controlled through the ZCR_EN/ and the ALT_GNT/ signals. Both of these signals have internal pull-ups and are active LOW.

The ZCR_EN/ signal enables ZCR support on the LSISAS1064. Pulling ZCR_EN/ HIGH disables ZCR support on the LSISAS1064 and causes the LSISAS1064 to behave as a normal PCI-X to SAS controller. When ZCR is disabled, the ALT_GNT/ signal has no effect on the LSISAS1064 operation.

Pulling ZCR_EN/ LOW enables ZCR operation. When ZCR is enabled, the LSISAS1064 responds to PCI configuration cycles when the ALT_GNT/ signal is asserted. Connect the ALT_GNT/ pin on the LSISAS1064 to the PCI GNT/ signal of the external I/O processor. This allows the I/O processor to perform PCI configuration cycles to the LSISAS1064 when the I/O processor is granted the PCI bus. This configuration also prevents the system processor from accessing the LSISAS1064 PCI configuration registers.

Figure 2.7 illustrates how to connect the LSISAS1064 to enable ZCR. Notice that the LSISAS1064 does not require the 2:1 mux.

Figure 2.7 ZCR Circuit Diagram for the LSISAS1064



Note: To maintain proper interrupt mapping, select the address line for use as IDSEL on the LSISAS1064 to be +2 address lines above IDSEL on ZCR slot.

2.7 Universal Asynchronous Receiver/Transmitter (UART)

The LSISAS1064 provides an industry standard UART interface. The UART performs serial-to-parallel conversion on data characters received from a peripheral device or modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU has access to UART status at any time during functional operation. The status information includes the type and condition of the transfer operations being performed by the UART, and any error conditions such as parity, overrun, framing, or break interrupt.

The LSISAS1064 UART is compatible with the standard 16550 UART, with the following exceptions:

- Uses speed sense logic to automatically determine the speed of a connected modem.

- Does not support 5-bit and 6-bit characters
- Does not support 1.5 stop bits
- Provides additional registers to support the speed sense logic
- Provides a synchronous interface to allow access to internal registers and FIFOs

2.8 Multi-ICE Test Interface

Include a 20-pin header to access the ARM Multi-ICE signals through the ICE JTAG post. The header has a 100 mil spacing between posts. The connector is a 20-way header that mates with IDC sockets that are mounted on a ribbon cable. This header enables LSI Logic to debug the board design. Table 2.3 provides the header pinout. If it is not possible to include a header, route the ARM Multi-ICE signals to through-holes. **LSI Logic considers access to the ARM Multi-ICE signals essential to all board designs.**

Include pull-up resistors on the signals that require a pull-up (TRST_ICE/, TDI_ICE, TMS_ICE, TCK_ICE) and on pin 15. In addition, include GND and VDD_33.

Table 2.3 ARM Multi-ICE Header Pinout

Pin	Signal	Pin	Signal
1	VDD (3.3 V)	2	VDD (3.3 V)
3	TRST_ICE/[1]	4	VSS
5	TDI_ICE[1]	6	VSS
7	TMS_ICE[1]	8	VSS
9	TCK_ICE[1]	10	VSS
11	RTCK_ICE	12	VSS
13	TDO_ICE	14	VSS
15	NC[1]	16	VSS
17	NC	18	VSS
19	NC	20	VSS

1. Connect a 4.7 kΩ resistor between this pin and 3.3 V.

Chapter 3
Signal Description

This chapter describes the input and output signals of the LSISAS1064, and consists of the following sections:

A slash (/) at the end of a signal indicates that the signal is active LOW. When the slash is absent, the signal is active HIGH. NC designates a No Connect signal.

3.1 Signal Organization

The LSISAS1064 has eight major interfaces:

- PCI Bus Interface
- PCI-Related Interface
- Compact PCI Interface

- SAS Interface
- Memory Interface
- Communication Interface
- Configuration and GPIO Interface
- JTAG and Test Interface

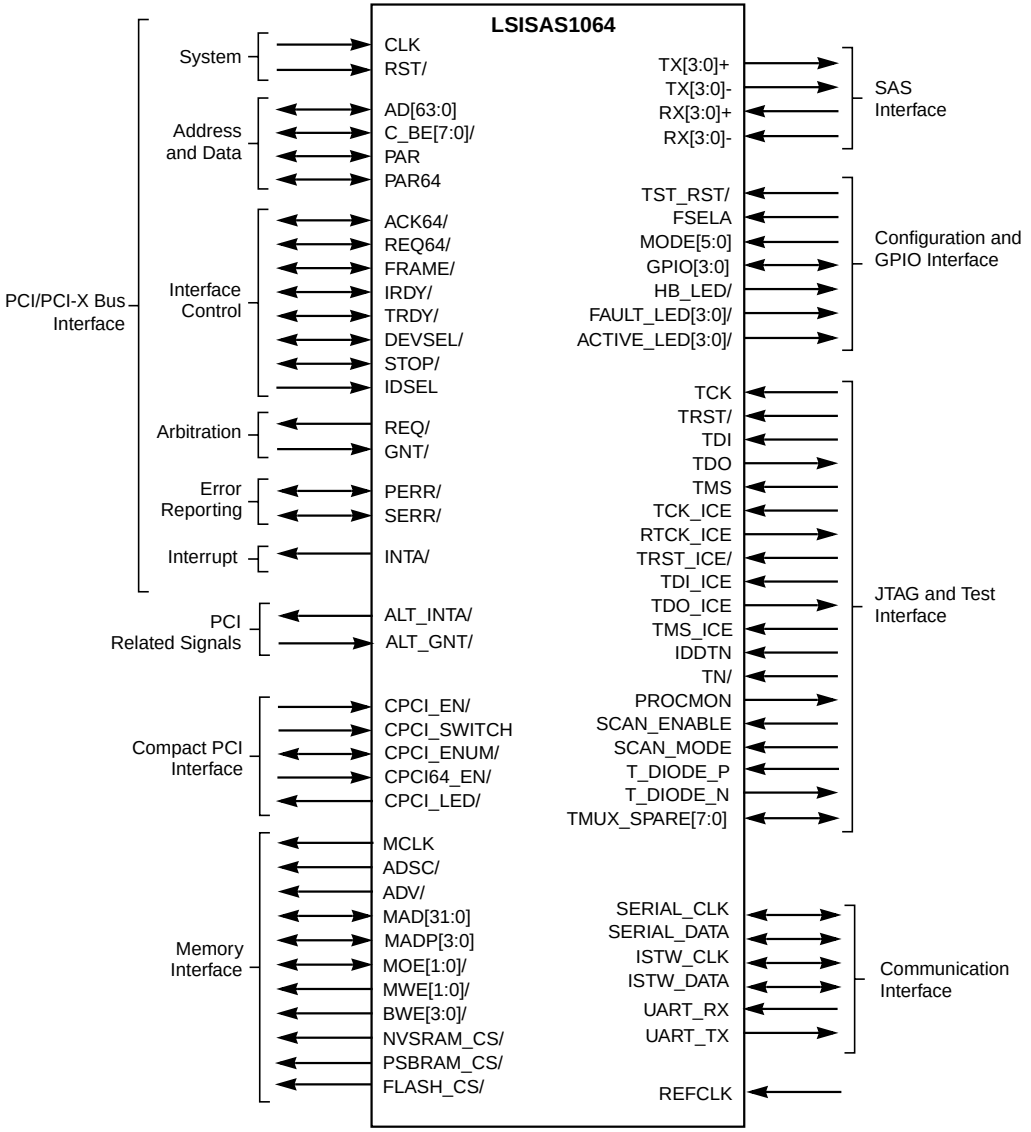
There are five signal types:

I	Input, a standard input-only signal
O	Output, a standard output driver (typically a Totem Pole output)
I/O	Input and output (bidirectional)
P	Power
G	Ground

Figure 3.1 contains the functional signal groupings of the LSISAS1064. Figure 5.8 on page 5-18 provides a diagram of the LSISAS1064 472 Ball Grid Array (BGA). Table 5.31 and Table 5.32 on page 5-13 and page 5-15 provide alphabetical and alphanumeric pin listings for the LSISAS1064.

The following subsections provide the signal descriptions for the LSISAS1064.

Figure 3.1 LSISAS1064 Functional Signal Grouping



3.2 PCI Signals

This section describes the PCI signals.

3.2.1 PCI System Signals

Table 3.1 describes the PCI system signals.

Table 3.1 PCI System Signals

Signal Name	BGA Position	Type	Description
CLK	Y4	I	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.
RST/	W5	I	

3.2.2 PCI Address and Data Signals

Table 3.1 describes the PCI address and data signals.

Table 3.2 PCI Address and Data Signals

Signal Name	BGA Position	Type	Description
AD[63:0]	AF19, AF20, AC19, AF21, AE23, AE22, AF23, AF22, AD23, AD22, AB19, AF24, AE24, AE25, AA19, AC23, AD25, AA20, AC20, AB21, AF25, AD24, Y20, AC24, AC25, AB25, W20, Y22, AA23, AD26, AC26, AB24, AD1, V5, AC1, AB2, AE1, AA4, AA5, Y7, AE3, AB3, Y8, Y6, AE4, AD4, AE5, AF4, AF5, AD10, AF9, AB10, AB12, AE9, AF11, AF10, AE11, AF12, AF16, AF13, AF15, AD14, AE17, AF14	I/O	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.
C_BE[7:0]/	AE19, AF17, AD19, AF18, AD2, AD6, AC8, AE10	I/O	
PAR	AD9	I/O	
PAR64	AB17	I/O	

3.2.3 PCI Interface Control Signals

Table 3.3 describes the PCI interface control signals.

Table 3.3 PCI Interface Control Signals

Signal Name	BGA Position	Type	Description
ACK64/	AE18	I/O	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.
REQ64/	AD18	I/O	
FRAME/	AB7	I/O	
IRDY/	AF6	I/O	
TRDY/	AA9	I/O	
DEVSEL/	AD5	I/O	
STOP/	AE6	I/O	
IDSEL	AD3	I	

3.2.4 PCI Arbitration Signals

Table 3.4 describes the PCI arbitration signals.

Table 3.4 PCI Arbitration Signals

Signal Name	BGA Position	Type	Description
REQ/	AB1	O	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.
GNT/	AA1	I	

3.2.5 PCI Error Reporting Signals

Table 3.5 describes the PCI error reporting signals.

Table 3.5 PCI Error Reporting Signals

Signal Name	BGA Position	Type	Description
PERR/	AF7	I/O	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.
SERR/	AF3	I/O	

3.2.6 PCI Interrupt Signals

Table 3.6 describes the PCI interrupt signals.

Table 3.6 PCI Interrupt Signals

Signal Name	BGA Position	Type	Description
INTA/	V3	O	Refer to the *PCI Local Bus Specification, Version 3.0,* and the *PCI-X Addendum to the PCI Local Bus Specification, Version 2.0*, for complete signal descriptions.

3.3 PCI-Related Signals

Table 3.7 describes the PCI-related signals.

Table 3.7 PCI-Related Signals

Signal Name	BGA Position	Type	Description
ALT_INTA/	U3	O	The PCI device asserts active LOW **Alternate Interrupt A** to request service from the host device driver. This signal is disabled when ZCR is disabled. ALT_INTA/ is an open drain signal. The interrupt request routing mode bits, bits [9:8] in the PCI Host Interrupt Mask register, control the routing of interrupt signals to INTA/ and/or ALT_INTA/.
ALT_GNT/	T5	I	Active LOW **Alternate Grant** signal provides a grant signal for ZCR implementations.
ZCR_EN/	T1	–	The active LOW **ZCR enable** input configures the LSISAS1064 for Zero Channel RAID operation. When this input is asserted, the standard PCI signals INTA/ and GNT/ are not used, and the alternate signals ALT_INTA/ and ALT_GNT/ are used. When this input is deasserted, the chip is configured for standard PCI operation.
BZR_SET	V21	–	This signal provides the reference resistor node for the PCI-X impedance controller.
BZVDD	AA24	–	This signal provides the reference resistor node for the PCI-X impedance controller.

3.4 Compact PCI Signals

Table 3.8 describes the CompactPCI signals.

Table 3.8 CompactPCI Signals

Signal Name	BGA Position	Type	Description
CPCI_EN/	R1	I	Asserting active LOW **CompactPCI Enable** configures the LSISAS1064 for the CompactPCI protocol.
CPCI_SWITCH	P1	I	The active HIGH **CompactPCI Switch** signal indicates to the LSISAS1064 that a change in the system configuration is imminent. The CompactPCI device insertion/removal mechanism controls the assertion of this signal.
CPCI_ENUM/	U1	I/O	This signal informs the system of a board removal or insertion. This signal remains asserted until the host driver services the hot-swapped board.
CPCI64_EN/	U2	I	The active LOW **Enable 64-bit Compact PCI** signal indicates the width of the CompactPCI bus.
CPCI_LED/	M5	O	The active LOW **CompactPCI Blue LED** signal provides the CompactPCI status LED. Asserting this signal drives the CompactPCI blue LED. This is a 3.3 V output.

3.5 SAS Signals

Table 3.9 describes the SAS interface signals.

Table 3.9 SAS Interface Signals

Signal Name	BGA Position	Type	Description
RX[3:0]+	A13, B16, B21, B24	I	These signals are the **Differential Receiver** signals for each phy.
RX[3:0]-	A14, C16, C21, B25		
TX[3:0]+	A10, B13, A20, A24	O	These signals are the **Differential Transmitter** signals for each phy.
TX[3:0]-	A9, C13, A19, A23		
REFCLK_P, REFCLK_N	F26, J22	I	The **Reference Clock** signals provide the serial differential clock. Connect a 75 MHz oscillator with an accuracy of at least 50ppm to these pins. To use a single-ended crystal, tie the crystal to REFCLK_P and tie REFCLK_N to a resistor termination.
RTRIM	C9	–	This pin provides the analog resistor reference for the GigaBlaze transceivers.

3.6 Memory Interface Signals

Table 3.10 describes the memory interface signals.

Table 3.10 Memory Interface Signals

Signal Name	BGA Position	Type	Description
MCLK	N26	O	All synchronous RAM control/data signals reference the rising edge of the **Memory Clock** signal. MOE[1:0]/ are asynchronous inputs and do not reference this clock.
ADSC/	P23	O	Asserting the active LOW **Address-Strobe-Controller** signal initiates read, write, or chip deselect cycles.
ADV/	U26	O	Asserting the active LOW **Advance** signal increments the burst address counter of the selected synchronous SRAM.
MAD[31:0]	AB26, AA25, R22, W26, V24, V25, AA26, U24, T22, Y26, R23, U25, R26, T24, T26, V26, H24, K24, H23, H21, D23, C26, E25, D25, D24, D26, E24, C24, C25, G23, F23, B26	I/O	The **Multiplexed Address/Data** bus signals provide the address and data bus to the PSBRAM, Flash ROM, and NVSRAM. These signals also provide Power-On Sense configuration functions to the LSISAS1064. Section 3.11, "Power-On Sense Pins Description," describe the Power-On sense configuration options. Provide both pull-down and pull-up resistors for these pins.
MADP[3:0]	W23, P26, J26, G21	I/O	The **Multiplexed Address/Data Parity** signals provide parity checking for MAD[31:0]. MADP[3] provides parity protection for the high-order byte (MAD[31:24]). while MADP[0] provides parity protection for low-order byte (MADP[7:0]).
MOE[1:0]/	E26, M22	O	Asserting the active LOW **Memory Output Enable** signals enable the selected PSBRAM, Flash ROM, or NVSRAM device to drive data. MOE[1]/ enables Flash ROM devices. MOE[0]/ enables NVSRAM devices. MOE[1:0]/ allow interleaved PSBRAM configurations.
MWE[1:0]/	H25, L26	O	The LSISAS1064 uses the active LOW **Memory Bank Write Enable** signals for interleaved PSBRAM configurations.
BWE[3:0]/	N25, J25, M26, N22	O	Asserting the active LOW **Byte-lane Write Enable** signals enable partial word writes to the PSBRAM. BWE[3]/ and BWE[2]/ enable partial word writes to the Flash ROM and/or the NVSRAM if FLASH_CS/ or NVSRAM_CS/ are asserted.
NVSRAM_CS/	G26	O	Asserting the active LOW **NVSRAM Chip Select** signal selects the NVSRAM.

Table 3.10 Memory Interface Signals (Cont.)

Signal Name	BGA Position	Type	Description
PSBRAM_CS/	J24	O	Asserting the active LOW **RAM Chip Select** signal selects the PSBRAMs. The LSISAS1064 supports up to four PSBRAMs in an interleaved and depth-expanded configuration.
FLASH_CS/	H26	O	Asserting the active LOW **Flash Chip Select** signal selects the Flash ROM. The LSISAS1064 maps the Flash ROM address space into system memory.

3.7 Communication Signals

Table 3.11 describes the UART and I^2C signals.

Table 3.11 UART and I^2C Signals

Signal Name	BGA Position	Type	Description
ISTWI_CLK	F22	I/O	The **I^2C Clock** pin provides the I^2C clock signal.
ISTWI_DATA	F21	I/O	The **I^2C Data** pin provides the I^2C data signal.
UART_RX	F8	I	This signal is the **UART Receive** signal.
UART_TX	A6	O	This signal is the **UART Transmit** signal.

3.8 Configuration and General Purpose Signals

Table 3.12 describes the configuration and general purpose signals.

Table 3.12 Configuration and General Purpose Signals

Signal Name	BGA Position	Type	Description
TST_RST/	G7	I	Asserting the **Test Reset** signal forces the chip into a Power-On-Reset state. The LSISAS1064 does not contain an internal power-on reset circuit. This signal must be supplied by a power-on reset circuit on the board.
REFCLK_B	D3	I	This pin provides the ARM reference clock.
MODE[5:0]	C2, F4, D1, E3, E2, F3	I	The **Mode Select** bus defines the operational and test modes for the chip. For normal operation, pull these signals to 0b000000.
GPIO[3:0]	K2, L3, K3, J2	I/O	These pins provide general purpose input/output signals. These pins have internal pull-ups and default to input mode upon device reset.
FAULT_LED[3:0]/	F1, J5, E1, F2	O	The active LOW **Fault LED** signals are nominally configured to indicate a SAS link fault for each respective phy.
ACTIVE_LED[3:0]/	L5, H1, G1, H4	O	The active LOW **Activity LED** signals are nominally configured to indicate SAS link activity.
HB_LED/	J3	O	The active LOW **Heart Beat LED** signal is nominally configured to intermittently assert, which indicates that the IOP is operational.
FSELA	G5	I	The **Frequency Select** signal supports clocking configuration options for internal clocks. This signal is reserved for diagnostic purposes.

3.9 JTAG and Test Signals

Table 3.13 describes the test and JTAG signals.

Table 3.13 Test and JTAG Signals

Signal Name	BGA Position	Type	Description
TCK	L2	I	JTAG Debug Clock.
TRST/	L1	I	JTAG Debug Reset.
TDI	J1	I	JTAG Debug Test Data In.
TDO	K1	O	JTAG Debug Test Data Out.
TMS	P2	I	JTAG Debug Test Mode Select.
TCK_ICE	B5	I	Multi-ICE Debug Clock.
RTCK_ICE	A5	O	Multi-ICE Debug Return Clock.
TRST_ICE/	C5	I	Multi-ICE Debug Reset.
TDI_ICE	F7	I	Multi-ICE Debug Test Data In.
TDO_ICE	B4	O	Multi-ICE Debug Test Data Out.
TMS_ICE	A4	I	Multi-ICE Debug Test Mode Select.
IDDTN	N1	I	Reserved for LSI Logic factory test.
TN/	P5	I	Reserved for LSI Logic factory test.
PROCMON	M1	O	Process Monitor Test output driver.
TDIODE_P	M23	I	Anode connection of the thermal diode.
TDIODE_N	K26	O	Cathode connection of the thermal diode.
SCAN_ENABLE	B2	I	Reserved for LSI Logic factory test.
SCAN_MODE	H7	I	Reserved for LSI Logic factory test.
TMUX_SPARE[7:0]	F6, C3, B3, D4, C4, E6, A2, A3	I/O	Reserved for LSI Logic factory test.
RESERVED	V4, W3	O	Reserved for LSI Logic factory test. These signals must be left unconnected.

3.10 Power Signals

Table 3.14 describes the power and ground signals.

Table 3.14 Power and Ground Signals

Signal Name	BGA Position	Type	Description
REFPLL_VDD	D2	P	These signals provide 1.2 V power.
REFPLL_VSS	C1	G	These signals provide ground.
PLL_VDD	AC4	P	These signals provide 1.2 V power.
PLL_VSS	AC3	G	These signals provide ground.
VDD2	C11, C12, D10, M13, M15, N12, N14, P13, P15, R12, R14	P	These signals provide 1.2 V core power.
VDDIO33	C6, C7, E4, E5, E22, F24, G3, G24, H3, K23, L4, L24, M3, M24, N3, P24, R3, R24, T3, T23, U4	P	These signals provide 3.3 V I/O power.
VDDIO33PCIX	W24, Y3, Y24, AA3, AB5, AB22, AB23, AC5, AC11, AC17, AD7, AD8, AD12, AD13, AD15, AD16, AD20, AD21	P	These signals provide 3.3 V PCI I/O power.
VDDIO5PCIX	V1, W1, Y23, AA6, AA21, AB14, AB18, AB20, AC2, AC6, AC12, AD17, AF8	P	These signals provide the bias reference for PCI pads. Connect this signal to 3.3 V. The LSISAS1064 does not support 5 V PCI.
VSS2	A25, B1, B6, B7, B11, B12, B14, B15, B19, B20, D5, D11, D17, E21, E23, F5, F25, G2, G8, G25, H2, H20, K4, L23, L25, M2, M12, M14, M25, N2, N13, N15, P12, P14, P25, R2, R13, R15, R25, T2, T4, U23, W7, W25, Y2, Y19, Y25, AA2, AA22, AB4, AB6, AC10, AC16, AC22, AE7, AE8, AE12, AE13, AE15, AE16, AE20, AE21, AE26, AF2	G	These signals provide ground.
RX_VSS[3:0]	E12, B17, F18, F20	G	These signals provide ground for the GigaBlaze core of each respective phy.
RXB_VSS[3:0]	D13, B18, E20, G20	G	
TX_VSS[3:0]	E11, A15, D18, D20	G	
TXB_VSS[3:0]	C10, A17, D19, D21	G	

Table 3.14 Power and Ground Signals (Cont.)

Signal Name	BGA Position	Type	Description
RX_VDD[3:0]	A12, E14, A22, C23	P	These signals provide 1.2 V power for the GigaBlaze core.
RXB_VDD[3:0]	D12, C17, E19, G19	P	
TX_VDD[3:0]	B9, E13, C18, C22	P	
TXB_VDD[3:0]	B10, A18, E18, F19	P	
NC	A11, A16, A21, B8, B22, B23, C8, C14, C15, C19, C20, D6, D7, D8, D9, D14, D15, D16, D22, E7, E8, E9, E10, E15, E16, E17, F9, G4, G6, G22, H5, H6, H22, J4, J6, J21, J23, K5, K22, K25, L22, M4, M23, N4, N5, N23, N24, P3, P4, P22, R4, R5, T25, U5, U22, V2, V6, V22, V23, W2, W4, W6, W21, W22, Y1, Y5, Y21, AA7, AA8, AA18, AB8, AB9, AB11, AB13, AB15, AB16, AC7, AC9, AC13, AC14, AC15, AC18, AC21, AD11, AE2, AE14		No connect.

3.11 Power-On Sense Pins Description

This section discusses the power-on sense pin configuration options. For setting global operating conditions, the LSISAS1064 uses power-on sense register bits that source their data from the state of the memory address/data bus (MAD[31:0]) during the device boot up sequence. The MAD signals are 3-stated and read continuously during PCI reset, and are latched upon removal of the PCI reset signal. Each of these pins contains an internal pull-down resistor and senses the presence of an external 4.7 kΩ pull-up resistor that is tied to 3.3 V Vdd power.

Provide both pull-up and pull-down options for all MAD[31:0] bus signals. Pull all reserved MAD bus signals LOW. Table 3.15 describes the power-on sense options.

Table 3.15 Power-On Sense Pin Definitions

Signal	Ball	Function	Pulled LOW (Default)	Pulled HIGH
MAD[31]	AB26	NVSRAM/SRAM Installed	No NVSRAM/SRAM installed	NVSRAM/SRAM installed
MAD[30]	AA25	NVSRAM or SRAM Select	SRAM Installed	NVSRAM installed
MAD[29]	R22	SGPIO CPLD	SGPIO CPLD not installed	SGPIO CPLD installed
MAD[28:17]	–	Reserved		
MAD[16]	V26	PCI-X Mode	Enables PCI-X mode support	Disables PCI-X mode support
MAD[15]	H24	133 MHz PCI-X	Enables 133 MHz PCI-X bus	Disables 133 MHz PCI-X bus
MAD[14]	K24	64-bit PCI	Configures a 64-bit PCI bus	Configures a 32-bit PCI bus
MAD[13]	H23	66 MHz PCI	Enables 66 MHz PCI bus	Disables 66 MHz PCI bus
MAD[12:11]	–	Reserved		
MAD[10]	C26	MSI-X	Enables MSI-X operation	Disables MSI-X operation
MAD[9]	–	Reserved		
MAD[8]	D25	PCI Hot Swap	Disables PCI Hot Swap	Enables PCI Hot Swap
MAD[7]	D24	IOP Boot Enable	Enables the IOP at power-up	Disables the IOP at power-up
MAD[6]	–	Reserved		
MAD[5]	E24	Subsystem ID	Subsystem ID bit [15] = 0b0	Subsystem ID bit [15] = 0b1
MAD[4]	–	Reserved		
MAD[3]	C25	Device ID	Device ID bit [0] = 0b0	Device ID bit [0] = 0b1
MAD[2:1]	G23; F23	Flash ROM Size	0b00 = 1 Mbyte 0b01 = 2 Mbytes 0b10 = 4 Mbytes 0b11 = No Flash ROM present	
MAD[0]	–	Reserved		

- **MAD[31] NVSRAM or SRAM Installed –** Pulling this signal HIGH indicates that an NVSRAM or an SRAM is installed. Pulling this signal LOW indicates that neither an NVSRAM nor an SRAM is installed.
- **MAD[30] NVSRAM or SRAM Select –** Pulling this signal LOW when MAD[31] is pulled HIGH indicates that an SRAM is installed. Pulling this signal HIGH when MAD[31] is pulled HIGH indicates that an NVSRAM is installed.
- **MAD[29] SGPIO CPLD Installed –** Pulling this signal LOW indicates that an SGPIO CPLD is not installed. Pulling this signal HIGH indicates that an SGPIO CPLD is installed.

- **MAD[28:17]**, Reserved.
- **MAD[16], PCI-X Operation –** Pulling this signal LOW enables the PCI-X operation. Pulling this signal HIGH disables PCI-X operation.
- **MAD[15], 133 MHz PCI-X Operation –** Pulling this signal LOW enables 133 MHz PCI-X operation. Pulling this signal HIGH disables 133 MHz PCI-X operation.
- **MAD[14], 64-bit PCI Operation –** Pulling this signal LOW enables 64-bit PCI operation. Pulling this signal HIGH disables 64-bit PCI operation.
- **MAD[13], 66 MHz PCI Operation –** Pulling this signal LOW enables 66 MHz PCI operation. Pulling this signal HIGH disables the 66 MHz PCI operation.
- **MAD[12:11]**, Reserved.
- **MAD[10], MSI-X –** Pulling this signal LOW enables MSI-X operation. Pulling this signal HIGH disables MSI-X operation.
- **MAD[9]**, Reserved.
- **MAD[8], PCI Hot Swap –** Pulling this signal LOW indicates that PCI Hot Swap is not implemented on the board. Pulling this signal HIGH indicates that PCI Hot Swap is implemented on the board.
- **MAD[7], IOP Boot Sequence –** Pulling downs to pull this signal LOW enables the IOP boot sequence following a reset. Pulling this signal HIGH disables the IOP boot sequence.
- **MAD[6]**, Reserved.
- **MAD[5], Subsystem Device ID Control –** Pulling this signal LOW programs bit 15 of the Subsystem Device ID register to 0b0. Pulling this signal HIGH programs bit 15 of the Subsystem Device ID register to 0b1. Refer to Subsystem ID register description on page 4-13 for more information.
- **MAD[4]**, Reserved.
- **MAD[3], Device ID Control –** Pulling this signal LOW programs bit 0 of the Device ID register to 0b0. Pulling this signal HIGH programs bit 0 of the Device ID register to 0b1.
- **MAD[2:1], Flash ROM Size –** These pins configure the Flash ROM size.

3.12 Internal Pull-Ups and Pull-Downs

Table 3.16 describes the pull-up and pull-down signals for the LSISAS1064.

Table 3.16 Pull-Up and Pull-Down Conditions

Signal Name	BGA Position	Pull Type
MODE[5:0]	C2, F4, D1, E3, E2, F3	Internal Pull-down.
MAD[31:0]	AB26, AA25, R22, W26, V24, V25, AA26, U24, T22, Y26, R23, U25, R26, T24, T26, V26, H24, K24, H23, H21, D23, C26, E25, D25, D24, D26, E24, C24, C25, G23, F23, B26	Internal Pull-down.
MADP[3:0]	W23, P26, J26, G21	Internal Pull-up.
SERIAL_DATA, SERIAL_CLK	A7, A8	Internal Pull-up.
GPIO[3:0]	K2, L3, K3, J2	Internal Pull-up.
TRST/	L1	Internal Pull-up.
TCK, TDI, TMS	L2, J1, P2	Internal Pull-up.
TRST_ICE/, TCK_ICE, TDI_ICE, TMS_ICE	C5, B5, F7, A4	Internal Pull-up.
SCAN_ENABLE, SCAN_MODE, IDDTN	B2, H7, N1	Internal Pull-down.
TN/	P5	Internal Pull-up.
ZCR_EN/	T1	Internal Pull-up.
CPCI_EN/	R1	Internal Pull-up.
CPCI_SWITCH	P1	Internal Pull-down.
ISTWI_CLK, ISTWI_DATA	F22, F21	Internal Pull-up.
REFCLK_B	D3	Internal Pull-down.
FSELA	G5	Internal Pull-down.
TST_RST/	G7	Internal Pull-up.

Chapter 4
PCI Host Register Description

This chapter describes the PCI host register space. This chapter consists of the following sections:

- Section 4.1, “PCI Configuration Space Register Description”
- Section 4.2, “PCI I/O Space and Memory Space Register Description”

The register map at the beginning of each register description provides the default bit settings for the register. Shading indicates a reserved bit or register. Do not access the reserved address areas.

The PCI System Address space consists of three regions: Configuration Space, Memory Space, and I/O Space. PCI Configuration Space supports the identification, configuration, initialization and error management functions for the LSISAS1064 PCI function.

PCI Memory Space [0] and Memory Space [1] form the PCI Memory Space. PCI Memory Space [0] provides normal system accesses to memory and PCI Memory Space [1] provides diagnostic memory accesses. PCI I/O Space provides normal system access to memory.

4.1 PCI Configuration Space Register Description

This section provides bit level descriptions of the PCI Configuration Space registers. Table 4.1 defines the PCI Configuration Space registers.

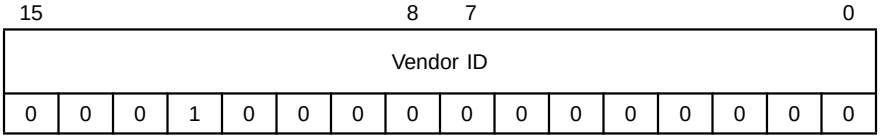
The LSISAS1064 enables, orders, and locates the PCI extended capability register structures (Power Management, Messaged Signaled Interrupts, MSI-X, and PCI-X) to optimize device performance. The LSISAS1064 does not hard code the location and order of the PCI extended capability structures. The address and location of the PCI extended capability structures are subject to change. To access a PCI extended capability structure, follow the pointers held in the Capability

Pointer registers and identify the extended capability structure with the Capability ID register for the given structure.

Table 4.1 LSISAS1064 PCI Configuration Space Address Map

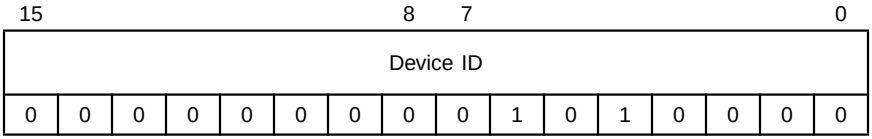
31	24	23	16	15	8	7	0	Offset	Page
Device ID				Vendor ID				0x00	4-3
Status				Command				0x04	4-3
Class Code						Revision ID		0x08	4-7
Reserved		Header Type		Latency Timer		Cache Line Size		0x0C	4-8
I/O Base Address								0x10	4-9
Memory [0] Low								0x14	4-10
Memory [0] High								0x18	4-10
Memory [1] Low								0x1C	4-11
Memory [1] High								0x20	4-11
Reserved								0x24	–
								0x28	–
Subsystem ID				Subsystem Vendor ID				0x2C	4-12
Expansion ROM Base Address								0x30	4-13
Reserved						Capabilities Pointer		0x34	4-14
								0x38	–
Maximum Latency		Minimum Grant		Interrupt Pin		Interrupt Line		0x3C	4-15
Reserved								0x40–0xFF	–
Power Management Capabilities				PM Next Pointer		PM Capability ID			4-17
PM Data		PM BSE		Power Management Control/Status					4-18
Reserved									–
MSI Message Control				MSI Next Pointer		MSI Capability ID			4-20
MSI Message Lower Address									4-22
MSI Message Upper Address									4-23
Reserved				MSI Message Data					4-23
MSI Mask Bits									4-24
MSI Pending Bits									4-24
Reserved									–
MSI-X Message Control				MSI-X Next Pointer		MSI-X Capability ID			4-24
MSI-X Table Offset									4-26
MSI-X PBA Offset									4-27
Reserved									–
PCI-X Command				PCI-X Next Pointer		PCI-X Capability ID			4-28
PCI-X Status									4-30
Reserved									–

Register: 0x00–0x01
Vendor ID
Read Only



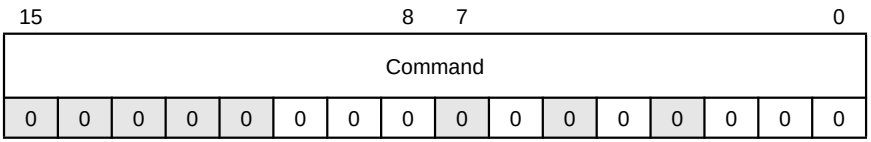
Vendor ID **[15:0]**
This 16-bit register identifies the manufacturer of the device. The Vendor ID is 0x1000.

Register: 0x02–0x03
Device ID
Read Only



Device ID **[15:0]**
This 16-bit register identifies the particular device. The default Device ID for the LSISAS1064 is 0x0050.

Register: 0x04–0x05
Command
Read/Write



The Command register provides coarse control over the PCI function's ability to generate and respond to PCI cycles. Writing a zero to this register logically disconnects the LSISAS1064 PCI function from the PCI bus for all accesses except configuration accesses.

Reserved **[15:11]**
This field is reserved.

Interrupt Disable **10**
Clearing this bit enables the PCI function to assert its interrupt signal (INTA/). Setting this bit disables the PCI function from asserting its interrupt signal.

Fast Back-to-Back Enable **9**
This bit determines if the master can perform fast back-to-back transactions to different devices. Clearing this bit indicates that fast back-to-back transactions are permitted to only the same device. Setting this bit indicates that the master can perform fast back-to-back transactions to different devices. To set this bit, all devices on the PCI bus must support fast back-to-back transactions.

SERR/ Enable **8**
Setting this bit enables the LSISAS1064 to activate the SERR/ driver. Clearing this bit disables the SERR/ driver.

Reserved **7**
This bit is reserved.

Enable Parity Error Response **6**
Setting this bit enables the LSISAS1064 PCI function to detect parity errors on the PCI bus and report these errors to the system. Clearing this bit causes the LSISAS1064 PCI function to set the Detected Parity Error bit, bit 15 in the PCI Status register, but not assert PERR/ when the PCI function detects a parity error. This bit only affects parity checking. The PCI function always generates parity for the PCI bus.

Reserved **5**
This bit is reserved.

Write and Invalidate Enable **4**
Setting this bit enables the PCI function to generate write and invalidate commands on the PCI bus when operating in the conventional PCI mode.

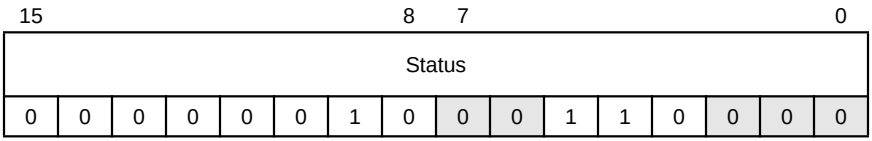
Reserved **3**
This bit is reserved.

Enable Bus Mastering **2**
Setting this bit allows the PCI function to behave as a PCI bus master. Clearing this bit disables the PCI function from generating PCI bus master accesses.

Enable Memory Space **1**
This bit controls the ability of the PCI function to respond to Memory Space accesses. Setting this bit allows the LSISAS1064 to respond to Memory Space accesses at the address range specified by the Memory [0] Low, Memory [0] High, Memory [1] Low, Memory [1] High, and the Expansion ROM Base Address registers. Clearing this bit disables the PCI function's response to PCI Memory Space accesses.

Enable I/O Space **0**
This bit controls the LSISAS1064 PCI function's response to I/O Space accesses. Setting this bit enables the PCI function to respond to I/O Space accesses at the address range the PCI Configuration Space I/O Base Address register specifies. Clearing this bit disables the PCI function's response to I/O Space accesses.

Register: 0x06–0x07
Status
Read/Write



Reads to this register behave normally. To clear a bit location that is currently set, write the bit to one (1). For example, to clear bit 15 when it is set and not affect any other bits, write 0x8000 to the register.

Detected Parity Error (from Slave) **15**
This bit is set per the *PCI Local Bus Specification, Version 3.0*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0*.

Signaled System Error **14**
The LSISAS1064 PCI function sets this bit when asserting the SERR/ signal.

Received Master Abort (from Master) **13**
A master device sets this bit when a Master Abort command terminates its transaction (except for Special Cycle).

Received Target Abort (from Master) **12**
A master device sets this bit when a Target Abort command terminates its transaction.

Signaled Target Abort **11**
The target device must set this bit when it terminates a transaction with a target abort command.

DEVSEL/ Timing **[10:9]**
These two read only bits encode the timing of DEVSEL/ and indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. The LSISAS1064 only supports medium DEVSEL/ timing. The possible timing values are:

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved

Data Parity Error Reported **8**
This bit is set per the *PCI Local Bus Specification, Revision 3.0*, and *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0*. Refer to bit 0 of the PCI-X Command register for more information.

Reserved **[7:6]**
This field is reserved.

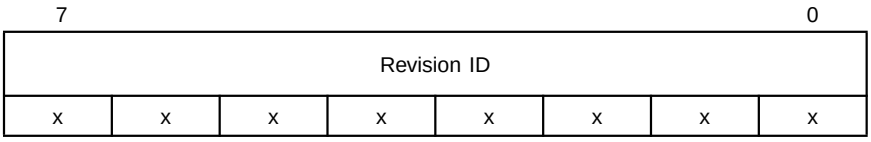
66 MHz Capable **5**
The MAD[13] Power-On Sense pin controls this bit. Allowing the internal pull-down to pull MAD[13] LOW sets this bit and indicates to the host system that the LSISAS1064 PCI function is capable of operating at 66 MHz. Pulling MAD[13] HIGH clears this bit and indicates to the host system that the LSISAS1064 PCI function is not configured to operate at 66 MHz. Refer to Section 3.11, “Power-On Sense Pins Description,” for more information.

New Capabilities **4**
The LSISAS1064 PCI function sets this read only bit to indicate a list of PCI extended capabilities such as PCI Power Management, MSI, MSI-X, and PCI-X support.

Interrupt Status **3**
This bit reflects the status of the INTA/ (or ALT_INTA/) signal.

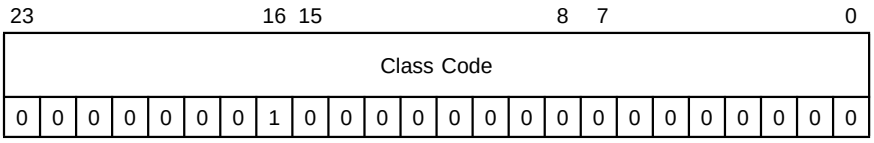
Reserved **[2:0]**
This field is reserved.

Register: 0x08
Revision ID
Read/Write



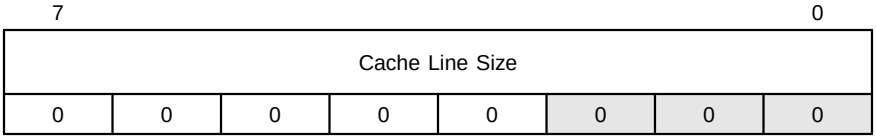
Revision ID **[7:0]**
This register indicates the current revision level of the device.

Register: 0x09–0x0B
Class Code
Read Only



Class Code **[23:0]**
This 24-bit register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 0x010000, which identifies a SCSI controller.

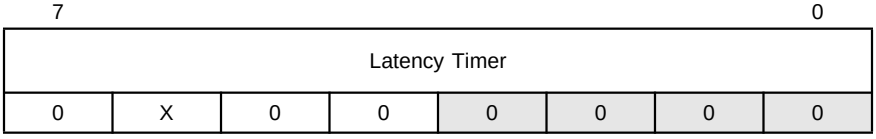
Register: 0x0C
Cache Line Size
Read/Write



Cache Line Size **[7:3]**
This register specifies the system cache line size in units of 32-bit words. In the conventional PCI mode, the LSISAS1064 PCI function uses this register to determine whether to use Write and Invalidate or Write commands for performing write cycles. Programming this register to a number other than a nonzero power of two disables the the use of the PCI performance commands to execute data transfers. The PCI function ignores this register when operating in the PCI-X mode.

Reserved **[2:0]**
This field is reserved.

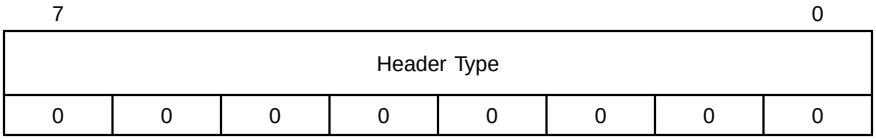
Register: 0x0D
Latency Timer
Read/Write



Latency Timer **[7:4]**
The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. If the LSISAS1064 initializes in the PCI mode, the default value of this register is 0x00. If the LSISAS1064 initializes in the PCI-X mode, the default value of this register is 0x40.

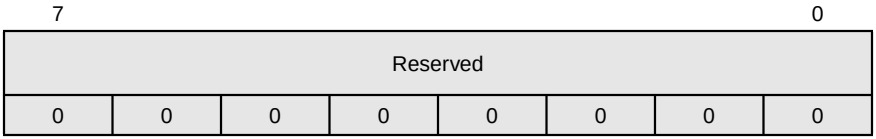
Reserved **[3:0]**
This field is reserved.

Register: 0x0E
Header Type
Read Only



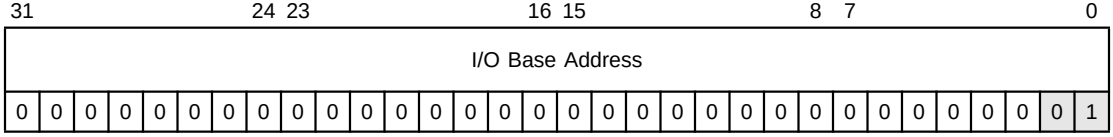
Header Type **[7:0]**
This 8-bit register identifies the layout of bytes 0x10 through 0x3F in configuration space and also indicates if the device is a single function or multifunction PCI device. Since the LSISAS1064 is a single function PCI device, bit 7 is cleared.

Register: 0x0F
Reserved



Reserved **[7:0]**
This register is reserved.

Register: 0x10–0x13
I/O Base Address
Read/Write

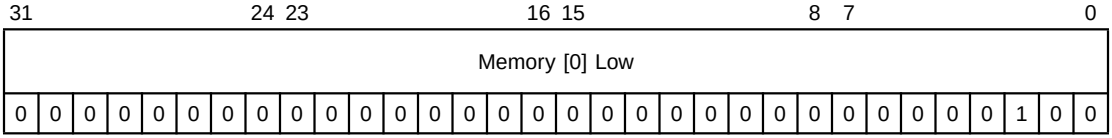


This base address register maps the operating register set into I/O Space. The LSISAS1064 requires 256 bytes of I/O Space for this base address register. Hardware sets bit 0 to 0b1. Bit 1 is reserved and returns 0b0 on all reads.

I/O Base Address **[31:2]**
This field contains the I/O Base address.

Reserved **[1:0]**
This field is reserved.

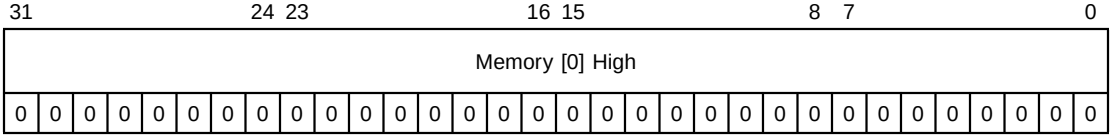
Register: 0x14–0x17
Memory [0] Low
Read/Write



The Memory [0] Low register and the Memory [0] High register map SCSI operating registers into Memory Space [0]. This register contains the lower 32 bits of the Memory Space [0] base address. Hardware programs bits [9:0] to 0b0000000100, which indicates that the Memory Space [0] base address is 64 bits wide and that the memory data is not prefetchable. The LSISAS1064 requires 1024 bytes of memory space.

Memory [0] Low **[31:0]**
This field contains the Memory [0] Low address.

Register: 0x18–0x1B
Memory [0] High
Read/Write

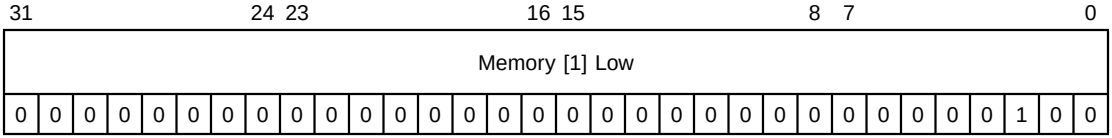


The Memory [0] High register and the Memory [0] Low register map SCSI operating registers into Memory Space [0]. This register contains the upper 32 bits of the Memory Space [0] base address. The LSISAS1064 requires 1024 bytes of memory space.

Memory [0] High **[31:0]**
This field contains the Memory [0] High address.

Register: 0x1C–0x1F

Memory [1] Low
Read/Write

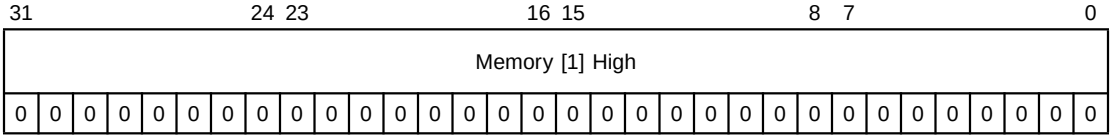


The Memory [1] Low register and the Memory [1] High register map the RAM into Memory Space [1]. This register contains the lower 32 bits of the Memory Space [1] base address. Hardware programs bits [12:0] to 0b0000000000100, which indicates that the Memory Space [1] base address is 64 bits wide and that the memory data is not prefetchable. The LSISAS1064 requires 64 Kbytes of memory for Memory Space [1].

Memory [1] Low **[31:0]**
This field contains the Memory [1] Low address.

Register: 0x20–0x23

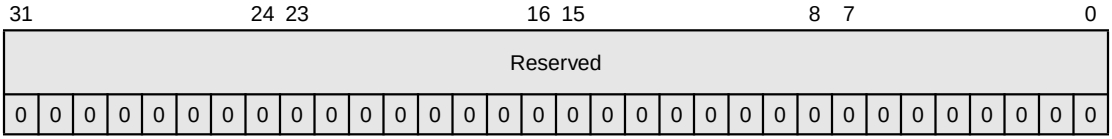
Memory [1] High
Read/Write



The Memory [1] High register and the Memory [1] Low register map the RAM into Memory Space [1]. This register contains the upper 32 bits of the Memory Space [1] base address. The LSISAS1064 requires 64 Kbytes of memory for Memory Space [1].

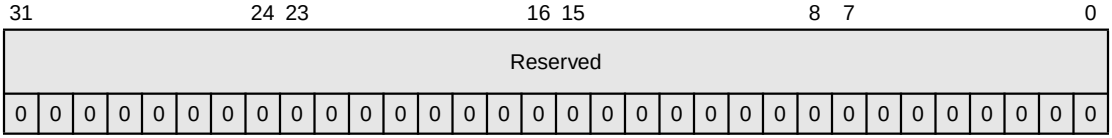
Memory [1] High **[31:0]**
This field contains the Memory [1] High address.

Register: 0x24–0x27
Reserved



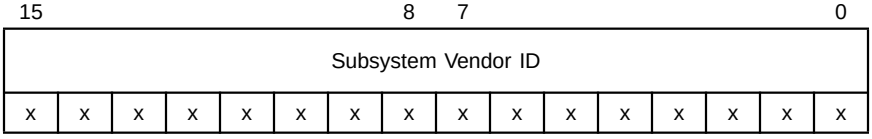
Reserved **[31:0]**
This register is reserved.

Register: 0x28–0x2B
Reserved



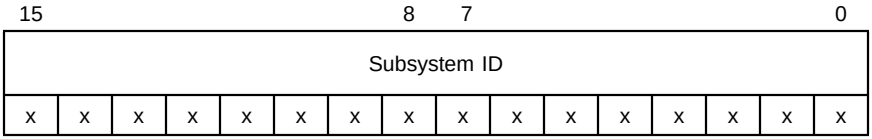
Reserved **[31:0]**
This register is reserved.

Register: 0x2C–0x2D
Subsystem Vendor ID
Read Only



Subsystem Vendor ID **[15:0]**
This 16-bit register uniquely identifies the vendor that manufactures the add-in board or subsystem where the LSISAS1064 resides. This register provides a mechanism for an add-in card vendor to distinguish their cards from another vendor's cards, even if the cards use the same PCI controller (and have the same Vendor ID and Device ID).

Register: 0x2E–0x2F
Subsystem ID
Read Only



Subsystem ID **[15:0]**

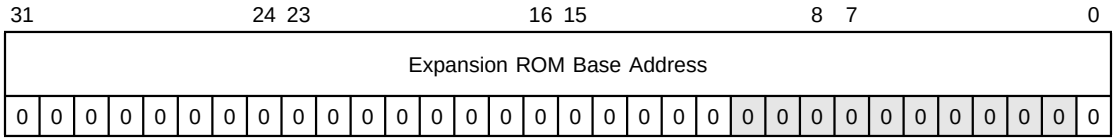
This 16-bit register uniquely identifies the add-in board or subsystem where this PCI device resides. This register provides a mechanism for an add-in card vendor to distinguish their cards from one another even if the cards use the same PCI controller (and have the same Vendor ID and Device ID). The board designer can store a vendor specific, 16-bit value in the NVData image. By default, the LSISAS1064 loads this register from the NVData image at power up.

The Subsystem Device ID Control Power-On Sense pin (MAD[5]) can control the value of bit [15] of this register. Allowing the Subsystem Device ID Control pin to remain internally pulled LOW has no effect on this register. Pulling this pin HIGH sets bit [15] of this register. Pulling the ID Control pin HIGH takes precedence over all other settings for bit [15].

- If the ID Control pin is pulled LOW, this register contains 0x1000.
- If the ID Control pin is pulled HIGH, this register contains 0x9000.

Refer to Section 3.11, “Power-On Sense Pins Description,” for additional information.

Register: 0x30–0x33
Expansion ROM Base Address
Read/Write



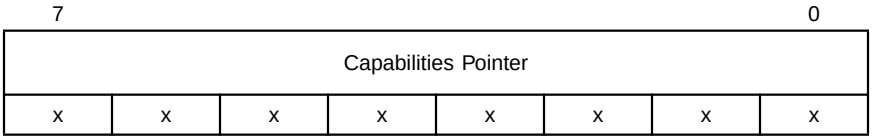
This four-byte register contains the base address and size information for the expansion ROM.

Expansion ROM Base Address **[31:11]**
These bits correspond to the upper 21 bits of the expansion ROM base address. The host system detects the size of the external memory by first writing 0xFFFFFFFF to this register and then reading the register back. The LSISAS1064 responds with zeros in all don't care locations. The least significant one (1) that remains represents the binary version of the external memory size. For example, to indicate an external memory size of 32 Kbytes, this register returns ones in the upper 17 bits when written with 0xFFFFFFFF and read back.

Reserved **[10:1]**
This field is reserved.

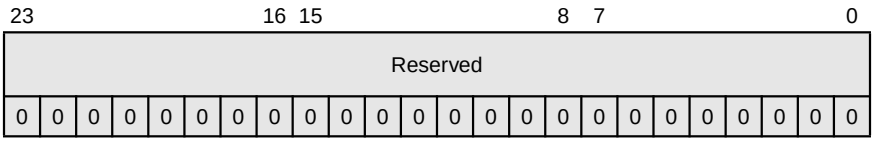
Expansion ROM Enable **0**
This bit controls if the device accepts accesses to its expansion ROM. Setting this bit enables address decoding. Depending on the system configuration, the device can optionally use an expansion ROM. Note that to access the expansion ROM, the user must also set bit 1 in the PCI Command register.

Register: 0x34
Capabilities Pointer
Read Only



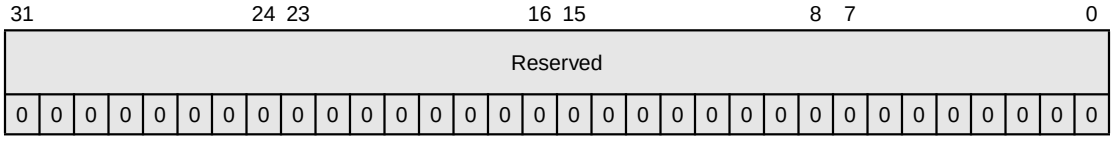
Capabilities Pointer **[7:0]**
This register indicates the location of the first extended capabilities register in PCI Configuration Space. The value of this register varies according to system configuration.

Register: 0x35–0x37
Reserved



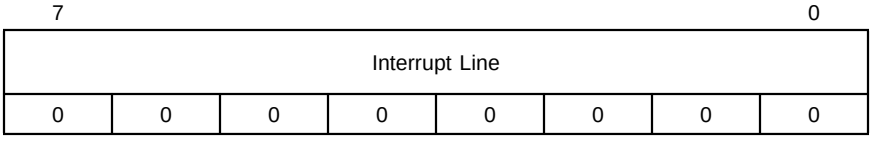
Reserved **[23:0]**
This register is reserved.

Register: 0x38–0x3B
Reserved



Reserved **[31:0]**
This register is reserved.

Register: 0x3C
Interrupt Line
Read/Write



Interrupt Line **[7:0]**
This register communicates interrupt line routing information. Power-On-Self-Test (POST) software writes the routing information into this register as it configures the system. This register indicates the system interrupt controller input to which this PCI function's interrupt pin connects. System architecture determines the values in this register.

Register: 0x3D
Interrupt Pin
Read Only

7							0
Interrupt Pin							
0	0	0	0	0	0	0	1

Interrupt Pin **[7:0]**
This read only register indicates which interrupt pin the PCI function uses. This register is set to 0x01, which indicates that PCI function presents interrupts on the INTA/ or ALT_INTA/ pins. The Interrupt Request Routing Mode bits, bits [9:8] in the Host Interrupt Mask register, determine if the function presents interrupts on INTA/, ALT_INTA/, or both.

Register: 0x3E
Minimum Grant
Read Only

7							0
Minimum Grant							
0	1	0	0	0	0	0	0

Min_Gnt **[7:0]**
This register specifies the desired settings for the latency timer values in units of 0.25 µs. Min_Gnt specifies how long of a burst period the device needs. The LSISAS1064 sets this register to 0x40 indicating a burst period of 16.0 µs.

Register: 0x3F
Maximum Latency
Read Only

7							0
Maximum Latency							
0	0	0	0	1	0	1	0

Max_Lat **[7:0]**

This register specifies the desired settings for the latency timer values in units of 0.25 µs. Max_Lat specifies how often the device needs to gain access to the PCI bus. The LSISAS1064 sets this register to 0x0A since it requires the PCI bus every 2.5 µs.

Register: 0xXX

Power Management Capability ID

Read Only

7							0
Power Management Capability ID							
0	0	0	0	0	0	0	1

Power Management Capability ID **[7:0]**

This register indicates the type of the current data structure. It is set to 0x01 to indicate the Power Management Data Structure.

Register: 0xXX

Power Management Next Pointer

Read Only

7							0
Power Management Next Pointer							
x	x	x	x	x	x	x	x

Power Management Next Pointer **[7:0]**

This register contains the pointer to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX

Power Management Capabilities

Read Only

15								8	7						0
Power Management Capabilities															
0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0

PME_Support **[15:11]**
These bits define the power management states in which the device asserts the Power Management Event (PME) pin. The LSISAS1064 clears these bits since the LSISAS1064 does not provide a PME signal.

D2_Support **10**
The PCI function sets this bit since the LSISAS1064 supports power management state D2.

D1_Support **9**
The PCI function sets this bit since the LSISAS1064 supports power management state D1.

Aux_Current **[8:6]**
The PCI function clears this field since the LSISAS1064 does not support Aux_Current.

Device Specific Initialization **5**
The PCI function clears this bit since no special initialization is required before a generic class device driver can use it.

Reserved **4**
This bit is reserved.

PME Clock **3**
The LSISAS1064 clears this bit since the chip does not provide a PME pin.

Version **[2:0]**
The PCI function programs these bits to 0b010 to indicate that the LSISAS1064 complies with the *PCI Power Management Interface Specification, Revision 1.2*.

Register: 0xXX
Power Management Control/Status
Read/Write

15							8	7							0
Power Management Control/Status															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PME_Status **15**
The PCI function clears this bit since the LSISAS1064 does not support PME signal generation from $D3_{cold}$.

Data_Scale **[14:13]**
The PCI function clears these bits since the LSISAS1064 does not support the Power Management Data register.

Data_Select **[12:9]**
The PCI function clears these bits since the LSISAS1064 does not support the Power Management Data register.

PME_Enable **8**
The PCI function clears this bit since the LSISAS1064 does not provide a PME signal and disables PME assertion.

Reserved **[7:2]**
This field is reserved.

Power State **[1:0]**
These bits determine the current power state of the LSISAS1064. Power states are:

0b00	D0
0b01	D1
0b10	D2
0b11	$D3_{hot}$

Register: 0xXX
Power Management Bridge Support Extensions
Read Only

7							0
Power Management Bridge Support Extensions							
0	0	0	0	0	0	0	0

Power Management Bridge Support Extensions [7:0]
This register indicates PCI Bridge specific functionality. The LSISAS1064 always returns 0x00 in this register.

Register: 0xXX

Power Management Data
Read Only

7							0
Power Management Data							
0	0	0	0	0	0	0	0

Power Management Data **[7:0]**
This register provides an optional mechanism for the PCI function to report state-dependent operating data. The LSISAS1064 always returns 0x00 in this register.

Register: 0xXX

MSI Capability ID
Read Only

7							0
MSI Capability ID							
0	0	0	0	0	1	0	1

MSI Capability ID **[7:0]**
This register indicates the type of the current data structure. This register always returns 0x05, indicating Message Signaled Interrupts (MSI).

Register: 0xXX

MSI Next Pointer
Read Only

7							0
MSI Next Pointer							
x	x	x	x	x	x	x	x

MSI Next Pointer **[7:0]**
This register points to the next item in the PCI function's extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
MSI Message Control
Read/Write

15							8	7							0
MSI Message Control															
0	0	0	0	0	0	0	X	1	0	0	0	0	0	0	0

Reserved **[15:9]**
This field is reserved.

Per-Vector Masking Capable **8**
If this bit is set, the device supports MSI per-vector masking. If this bit is cleared, the function does not support MSI per-vector masking. This bit is read only.

64-Bit Address Capable **7**
The PCI function sets this read only bit to indicate support of a 64-bit message address.

Multiple Message Enable **[6:4]**
These read/write bits indicate the number of messages that the host allocates to the LSISAS1064. The host system software allocates all or a subset of the requested messages by writing to this field. The number of allocated request messages must align to a power of two. Table 4.2 provides the bit encoding of this field.

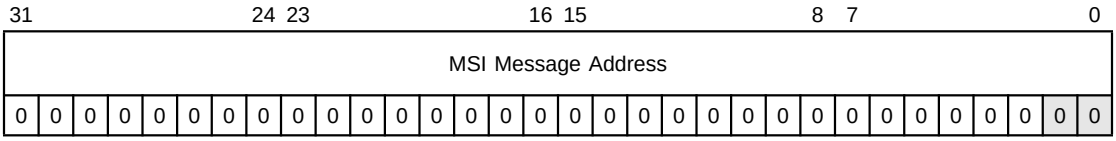
Table 4.2 Multiple Message Enable Field Bit Encoding

Bits [6:4] Encoding	Number of Allocated Messages
0b000	1
0b001	2
0b010	4
0b011	8
0b100	16
0b101	32
0b110	Reserved
0b111	Reserved

Multiple Message Capable **[3:1]**
These read only bits indicate the number of messages that the LSISAS1064 requests from the host. The host system software reads this field to determine the number of requested messages. The number of requested messages must align to a power of two. The LSISAS1064 sets this field to 0b000 to request one message. All other encodings of this field are reserved.

MSI Enable **0**
System software sets this bit to enable MSI. To enable MSI, the MSI-X bit in the MSI-X Message Control register must also be cleared (‘0’). Setting this bit enables the device to use MSI to interrupt the host and request service. Setting this bit prohibits the LSISAS1064 from using the INTA/ or ALT_INTA/ pins to request service from the host. Setting this bit to mask interrupts on the INTA/ or ALT_INTA/ pins is a violation of the PCI specification.

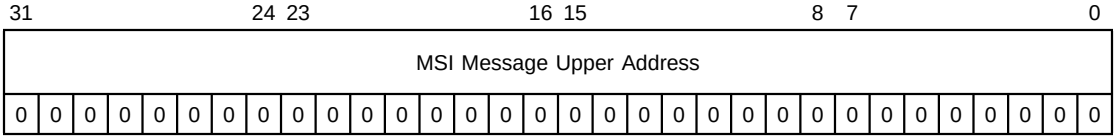
Register: 0xXX
MSI Message Lower Address
Read/Write



MSI Message Address **[31:2]**
This register contains message address bits [31:2] for the MSI memory write transaction. The host system specifies and Dword aligns the message address. During the address phase, the LSISAS1064 drives Message Address[1:0] to 0b00.

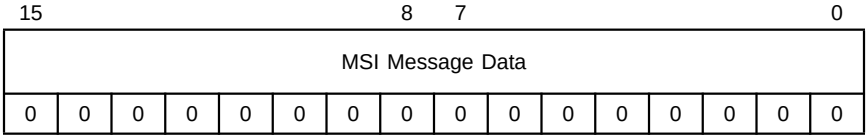
Reserved **[1:0]**
This field is reserved.

Register: 0xXX
MSI Message Upper Address
Read/Write



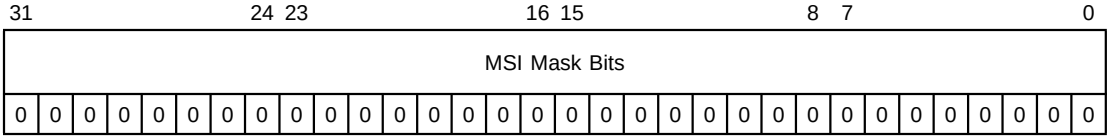
MSI Message Upper Address **[31:0]**
The LSISAS1064 supports 64-bit MSI message. This register contains the upper 32 bits of the 64-bit message address, which the system specifies. The host system software can program this register to 0x0000 to force the PCI function to generate 32-bit message addresses.

Register: 0xXX
MSI Message Data
Read/Write



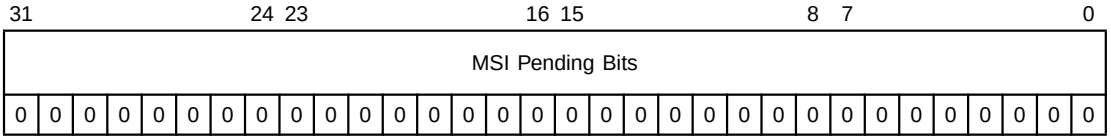
MSI Message Data **[15:0]**
System software initializes this register by writing to it. The LSISAS1064 sends an interrupt message by writing a Dword to the address held in the MSI Message Lower Address and MSI Message Upper Address registers. This register forms bits [15:0] of the Dword message that the PCI function passes to the host. The PCI function drives bits [31:16] of this message to 0x0000.

Register: 0xXX
MSI Mask Bits
Read/Write



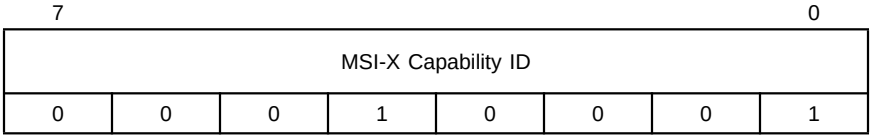
MSI Mask Bits **[31:0]**
For each mask bit that is set, the device is prohibited from sending an associated message. Refer to the PCI specification for a complete description of this register.

Register: 0xXX
MSI Pending Bits
Read Only



MSI Pending Bits **[31:0]**
For each Pending bit that is set, the function has a pending associated message. Refer to the PCI specification for a complete description of this register.

Register: 0xXX
MSI-X Capability ID
Read Only



MSI-X Capability ID **[7:0]**
This register indicates the type of the current data structure. This register always returns 0x11, indicating MSI-X.

Register: 0xXX
MSI-X Next Pointer
Read Only

7							0
MSI-X Next Pointer							
x	x	x	x	x	x	x	x

MSI-X Next Pointer **[7:0]**
This register points to the next item in the extended capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
MSI-X Message Control
Read/Write

15								8	7						0
MSI-X Message Control															
0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x

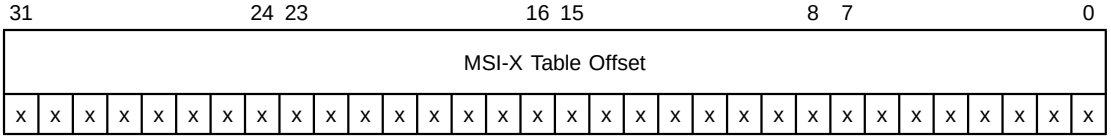
MSI-X Enable **15**
Setting this bit enables the device to use MSI-X to request service from the host. To enable MSI-X, the MSI Enable bit in the MSI Message Control register must be cleared (‘0’). Setting this bit also prohibits the device from using the INTA/ or ALT_INTA/ pins to request service from the host. Setting this bit to mask interrupts on the INTA/ or ALT_INTA/ pins is a violation of the PCI specification.

Function Mask **14**
Setting this bit masks all of the reset vectors that are associated with the function. This bit overrides the per-vector mask bit settings. Clearing this bit enables the per-vector mask bit to determine if a vector is masked.

Reserved **[13:11]**
This field is reserved.

Table Size **[10:0]**
Host software reads this field to determine the MSI-X table size.

Register: 0xXX
MSI-X Table Offset
Read Only



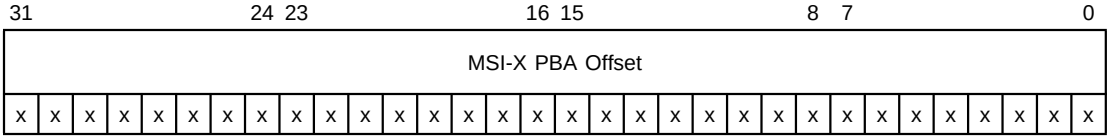
MSI-X Table Offset **[31:3]**
This field provides an offset from the address held in the base address registers of the device to the base of the MSI-X table.

Table BIR **[2:0]**
This field indicates which of the base address registers of the device, which are located at 0x10 in PCI Configuration Space, maps the MSI-X table into memory. Table 4.3 provides the BIR field definitions.

Table 4.3 BIR Field Definitions

BIR Value	Base Address Register
0	0x10
1	0x14
2	0x18
3	0x1C
4	0x20
5	0x24
6	Reserved
7	Reserved

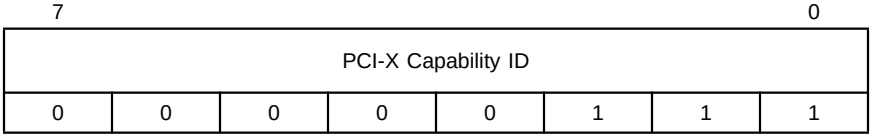
Register: 0xXX
MSI-X PBA Offset
Read Only



MSI-X PBA Offset **[31:3]**
This field contains an offset from one of the base address registers of the device that points to the MSI-X PBA. The lower 3 bits of this register are cleared (‘0’) for a 32-bit aligned offset.

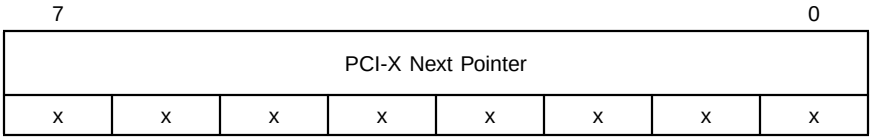
PBA BIR **[2:0]**
This field indicates which of the base address registers of the device, which are located at 0x10 in PCI Configuration Space, maps the MSI-X PBA into memory. Table 4.3 provides the BIR field definitions.

Register: 0xXX
PCI-X Capability ID
Read Only



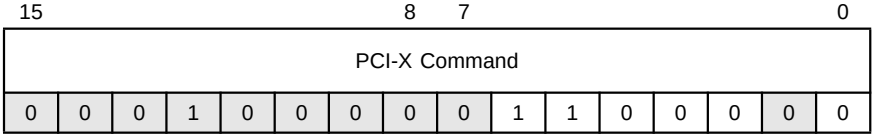
PCI-X Capability ID **[7:0]**
This register indicates the type of the current data structure. This register returns 0x07, indicating the PCI-X Data Structure.

Register: 0xXX
PCI-X Next Pointer
Read Only



PCI-X Next Capabilities Pointer **[7:0]**
This register points to the next item in the device's capabilities list. The value of this register varies according to system configuration.

Register: 0xXX
PCI-X Command
Read/Write



Reserved **[15:7]**
This field is reserved.

Maximum Outstanding Split Transactions **[6:4]**
These bits indicate the maximum number of split transactions the LSISAS1064 can have outstanding at one time. The LSISAS1064 uses the most recent value of this register each time it prepares a new sequence. Note that if the LSISAS1064 prepares a sequence before the setting of this field changes, the PCI function initiates the prepared sequence with the previous setting. Table 4.4 provides the bit encodings for this field.

Table 4.4 Maximum Outstanding Split Transactions

Bits [6:4] Encoding	Maximum Outstanding Split Transactions
0b000	1
0b001	2
0b010	3

Table 4.4 Maximum Outstanding Split Transactions (Cont.)

Bits [6:4] Encoding	Maximum Outstanding Split Transactions
0b011	4
0b100	8
0b101	12
0b110	16
0b111	Reserved

Maximum Memory Read Byte Count **[3:2]**
These bits indicate the maximum byte count the LSISAS1064 uses when initiating a sequence with one of the burst memory read commands. Table 4.5 provides the bit encodings for this field.

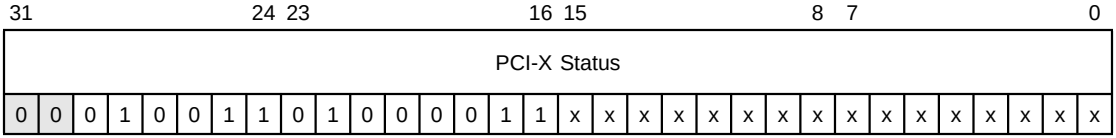
Table 4.5 Maximum Memory Read Count

Bits [3:2] Encoding	Maximum Memory Read Byte Count
0b00	512
0b01	1024
0b10	2048
0b11	Reserved

Reserved **1**
This bit is reserved.

Data Parity Error Recovery Enable **0**
The host device driver sets this bit to allow the LSISAS1064 to attempt to recover from data parity errors. If the user clears this bit and the LSISAS1064 is operating in the PCI-X mode, the LSISAS1064 asserts SERR/ whenever the Master Data Parity Error bit in the PCI Status register is set.

Register: 0xXX
PCI-X Status
Read/Write



Reserved **[31:30]**
This field is reserved.

Received Split Completion Error Message **29**
The LSISAS1064 sets this bit upon receipt of a split completion message if the split completion error attribute bit is set. Write a one (1) to this bit to clear it.

Designed Maximum Cumulative Read Size **[28:26]**
These read only bits indicate a number greater than or equal to the maximum cumulative size of all outstanding burst memory read transactions for the LSISAS1064 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSISAS1064 reports 0b100 in this field to indicate a designed maximum cumulative read size of 16 Kbytes.

Designed Maximum Outstanding Split Transactions **[25:23]**
These read only bits indicate a number greater than or equal to the maximum number of all outstanding split transactions for the LSISAS1064 PCI device. The PCI function must report the smallest value that correctly indicates its capability. The LSISAS1064 reports 0b110 in this field to indicate that the designed maximum number of outstanding split transactions is sixteen.

Designed Maximum Memory Read Byte Count **[22:21]**
These read only bits indicate a number greater than or equal to the maximum byte count for the LSISAS1064 device. The PCI function uses this count to initiate a sequence with one of the burst memory read commands. The PCI function must report the smallest value that correctly indicates its capability. The LSISAS1064 reports

0b10 in this field to indicate that the designed maximum memory read bytes count is 2048.

Device Complexity **20**
The PCI function clears this read only bit to indicate that the LSISAS1064 is a simple device.

Unexpected Split Completion **19**
The PCI function sets this read only bit when it receives an unexpected split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

Split Completion Discarded **18**
The PCI function sets this read only bit when it discards a split completion. Once set, this bit remains set until software clears it. Write a one (1) to this bit to clear it.

133 MHz Capable **17**
The MAD[15] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[15] LOW sets this bit and enables 133 MHz operation of the PCI bus. Pulling MAD[15] HIGH clears this bit and disables 133 MHz operation of the PCI bus. Refer to Section 3.11, "Power-On Sense Pins Description," for more information concerning the Power-On Sense pins.

64-Bit Device **16**
The MAD[14] Power-On Sense pin controls this read only bit. Allowing the internal pull-downs to pull MAD[14] LOW sets this bit and indicates a 64-bit PCI Address/Data bus. Pulling MAD[14] HIGH clears this bit and indicates a 32-bit PCI Address/Data bus. If using the LSISAS1064 on an add-in card, this bit must indicate the size of the card's PCI Address/Data bus. Refer to Section 3.11, "Power-On Sense Pins Description," for more information concerning the Power-On Sense pins.

Bus Number **[15:8]**
These read only bits indicate the number of the LSISAS1064 bus segment. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Device Number **[7:3]**
These read only bits indicate the device number of the LSISAS1064. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

Function Number **[2:0]**
These read only bits indicate the number in the Function Number field (AD[10:8]) of a Type 0 PCI configuration transaction. The PCI function uses this number as part of its Requester ID and Completer ID. This field is read for diagnostic purposes only.

4.2 PCI I/O Space and Memory Space Register Description

This section describes the host interface registers in the PCI I/O Space and PCI Memory Space. These address spaces contain the Fusion-MPT interface register set. PCI Memory Space [0] and PCI Memory Space [1] form the PCI Memory Space. PCI Memory [0] supports normal memory accesses while PCI Memory Space [1] supports diagnostic memory accesses. For all registers except the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers, access the address offset through either PCI I/O Space or PCI Memory Space [0]. Access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers is only through PCI I/O Space. Table 4.6 defines the PCI I/O Space address map.

Table 4.6 PCI I/O Space Address Map

31 16 15 0	Offset	Page
System Doorbell	0x0000	4-34
Write Sequence	0x0004	4-34
Host Diagnostic	0x0008	4-35
Test Base Address	0x000C	4-37
Diagnostic Read/Write Data	0x0010	4-37
Diagnostic Read/Write Address	0x0014	4-38
Reserved	0x0018–0x002F	–
Host Interrupt Status	0x0030	4-38
Host Interrupt Mask	0x0034	4-39
Reserved	0x0038–0x003F	–
Request Queue	0x0040	4-40
Reply Queue	0x0044	4-41
High Priority Request MFA Queue	0x0048	4-41
Reserved	0x004C–0x007F	–

Table 4.7 defines the PCI Memory Space [0] address map.

Table 4.7 PCI Memory [0] Address Map

31 16 15 0	Offset	Page
System Doorbell	0x0000	4-34
Write Sequence	0x0004	4-34
Host Diagnostic	0x0008	4-35
Test Base Address	0x000C	4-37
Reserved	0x0010–0x002F	–
Host Interrupt Status	0x0030	4-38
Host Interrupt Mask	0x0034	4-39
Reserved	0x0038–0x003F	–
Request Queue	0x0040	4-40
Reply Queue	0x0044	4-41
High Priority Request MFA Queue	0x0048	4-41
Reserved	0x004C–0x007F	–
Shared Memory	0x0080– 0x(Sizeof(Mem0)–1)	–

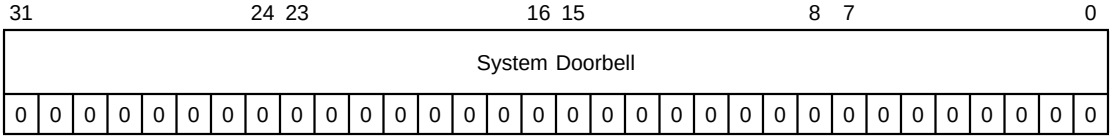
Table 4.8 defines the PCI Memory Space [1] address map.

Table 4.8 PCI Memory [1] Address Map

31 16 15 0	
Diagnostic Memory	0x0000– 0x(Sizeof(Mem1)–1)

A bit level description of the PCI Memory and PCI I/O Spaces follows.

Register: 0x00
System Doorbell
Read/Write



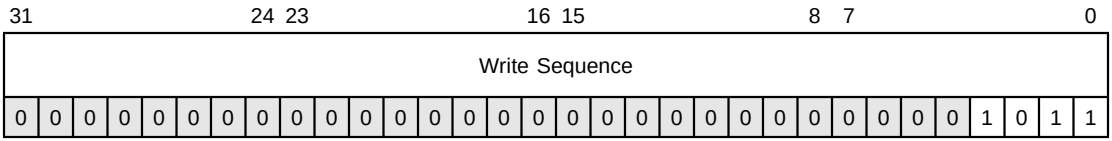
The System Doorbell register is a simple message passing mechanism that allows the system to pass single word messages to the embedded IOP processor and vice versa.

When a host system PCI master writes to the Host Registers->Doorbell register, the LSISAS1064 generates a maskable interrupt to the IOP. The value written by the host system is available for the IOP to read in the System Interface Registers->Doorbell register. The IOP clears the interrupt status after reading the value.

Conversely, when the IOP processor writes to the System Interface Registers->Doorbell register, the LSISAS1064 generates a maskable interrupt to the PCI system. The host system can read the value written by the IOP in the Host Registers->Doorbell register. The host system clears the interrupt status bit and interrupt pin by writing any value to the Host Registers->Interrupt Status register.

Host Doorbell Value **[31:0]**
During a write, this register contains the doorbell value that the host system passes to the IOP. During a read, this register contains the doorbell value that the IOP passes to the host system.

Register: 0x04
Write Sequence
Read/Write

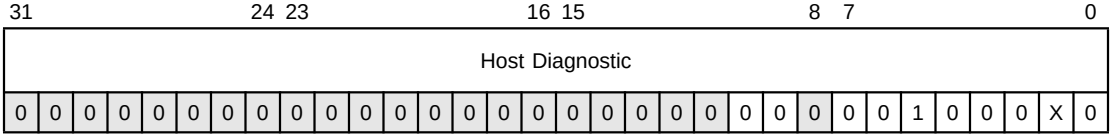


The Write Sequence register provides a protection mechanism against inadvertent writes to the Host Diagnostic register.

Reserved **[31:4]**
This field is reserved.

Write I/O Key **[3:0]**
To enable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic register, perform five data-specific writes to the Write I/O Key. Writing an incorrect value to the Write I/O Key invalidates the key sequence and the host must rewrite the entire sequence. The Write I/O Key sequence is: 0x00FF, 0x0004, 0x000B, 0x0002, 0x0007, and 0x000D. To disable write access to the Diagnostic Read/Write Data, Diagnostic Read/Write Address, and Host Diagnostic registers, perform a write of any value, except the Write I/O Key sequence, to the Write Sequence register. The Diagnostic Write Enable bit, bit 7 in the Host Diagnostic register, indicates the write access status.

Register: 0x08
Host Diagnostic
Read/Write



The Host Diagnostic register contains diagnostic controls and status information. This register can only be written when bit 7 of this register is set. This bit is set by writing the correct key sequence to the Write Sequence register.

Reserved **[31:11]**
This field is reserved.

Clear Flash Bad Signature **10**
Writing a one (1) to this bit clears the Flash Bad Signature setting within the LSISAS1064. This bit is self-clearing.

Prevent IOC Boot **9**
Setting this bit prevents the IOP from rebooting after a reset.

Reserved **8**
This field is reserved.

Diagnostic Write Enable **7**
The LSISAS1064 sets this read only bit when the host writes the correct Write I/O Key to the Write Sequence register. The LSISAS1064 clears this bit when the host writes a value other than the Write I/O Key to the Write Sequence register.

Flash Bad Signature **6**
The LSISAS1064 sets this bit if the IOP ARM966E-S™ processor encounters a bad Flash signature when booting from Flash ROM. The LSISAS1064 also sets the DisARM bit (bit 1 in this register) to hold the IOP ARM processor in a reset state. The LSISAS1064 maintains this state until the PCI host clears both the Flash Bad Signature and DisARM bits.

Reset History **5**
The LSISAS1064 sets this bit if it experiences a Power On Reset (POR), PCI Reset, or TestReset/.

Diagnostic Read/Write Enable **4**
Setting this bit enables access to the Diagnostic Read/Write Data and Diagnostic Read/Write Address registers.

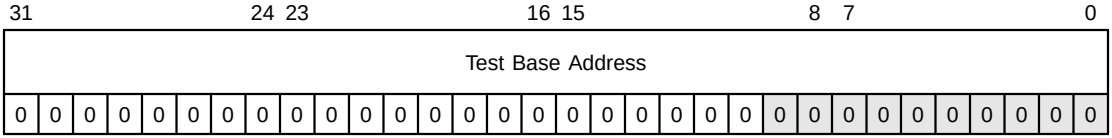
TTL Interrupt **3**
Setting this bit configures PCI INTA/ as a TTL output. Clearing this bit configures PCI INTA/ as an open-drain output. Use this bit for test purposes only.

Reset Adapter **2**
Setting this write only bit causes a hard reset within the LSISAS1064. The bit self-clears after eight PCI clock periods. After deasserting this bit, the IOP ARM processor executes from its default reset vector.

DisARM **1**
Setting this bit disables the ARM processor.

Diagnostic Memory Enable **0**
Setting this bit enables diagnostic memory accesses through PCI Memory Space [1]. Clearing this bit disables diagnostic memory accesses to PCI Memory Space [1] and returns 0xFFFF on reads.

Register: 0x0C
Test Base Address
Read/Write

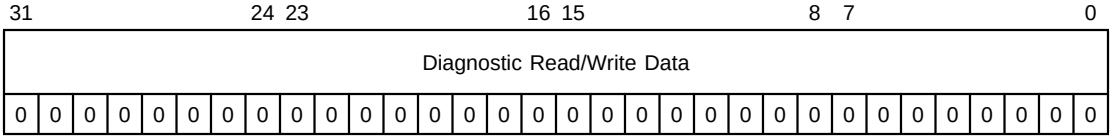


The Test Base Address register specifies the base address for Memory Space [1] accesses.

Test Base Address **[31:10]**
The number of significant bits is determined by the size of the PCI Memory Space [1] in the NVData image.

Reserved **[9:0]**
This field is reserved.

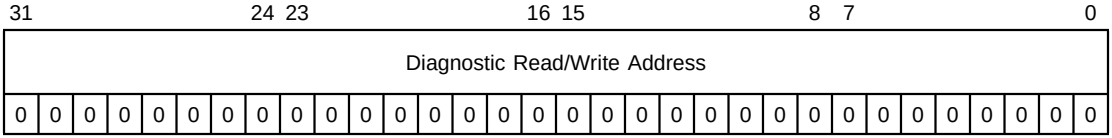
Register: 0x10
Diagnostic Read/Write Data
Read/Write



This register reads or writes Dword locations on the LSISAS1064 internal bus. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write I/O Key to the Write Sequence register and setting bit 4, the Diagnostic Write Enable bit, of the Host Diagnostic register. A write of any value other than the correct Write I/O Key to the Write Sequence register disables write access to this register.

Diagnostic Read/Write Data **[31:0]**
Using this register, the LSISAS1064 reads/writes data at the address that the Diagnostic Read/Write Address register specifies.

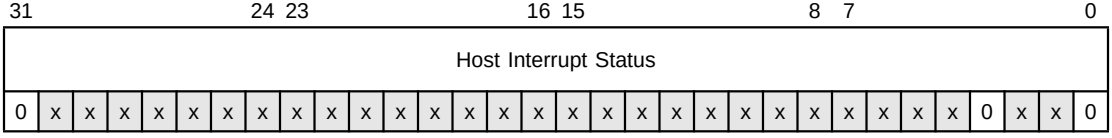
Register: 0x14
Diagnostic Read/Write Address
Read/Write



The Diagnostic Read/Write Address register specifies a Dword location on the internal bus. The address increments by a Dword whenever the host system accesses the Diagnostic Read/Write Address register. This register is only accessible through PCI I/O Space and returns 0xFFFFFFFF if read through PCI Memory Space. The host can enable write access to this register by writing the correct Write I/O Key to the Write Sequence register and setting bit 4, the Diagnostic Write Enable bit, of the Host Diagnostic register. A write of any value other than the correct Write I/O Key to the Write Sequence register disables write access to this register.

Diagnostic Read/Write Address **[31:0]**
This register holds the address that the Diagnostic Read/Write Data register writes data to or reads data from.

Register: 0x30
Host Interrupt Status
Read/Write



The Host Interrupt Status register provides read only interrupt status information to the PCI Host. A write to this register of any value clears the associated System Doorbell interrupt.

IOP Doorbell Status **31**
The LSISAS1064 sets this bit when the IOP receives a message from the system doorbell but has yet to process it. The IOP processes the System Doorbell message then clears the corresponding system request interrupt.

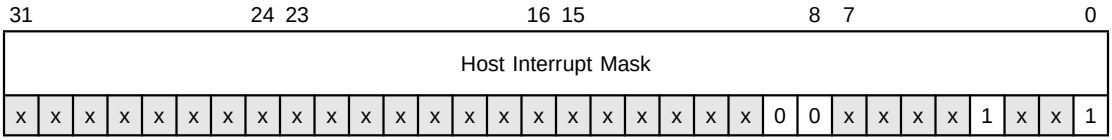
Reserved **[30:4]**
This field is reserved.

Reply Interrupt **3**
The LSISAS1064 sets this bit when the Reply Post FIFO is not empty. The LSISAS1064 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

Reserved **[2:1]**
This field is reserved.

System Doorbell Interrupt **0**
The LSISAS1064 sets this bit when the IOP writes a value to the System Doorbell. The host can clear this bit by writing any value to this register. The LSISAS1064 generates a PCI interrupt when this bit is set and the corresponding mask bit in the Host Interrupt Mask register is cleared.

Register: 0x34
Host Interrupt Mask
Read/Write



The Host Interrupt Mask register masks and/or routes the interrupt conditions that the Host Interrupt Status register reports.

Reserved **[31:10]**
This field is reserved.

Interrupt Request Routing Mode **[9:8]**
This field routes PCI interrupts to the INTA/ or ALT_INTA/ pins according to the bit encodings in Table 4.9. If the host system enables MSI or MSI-X, the LSISAS1064 does not signal PCI interrupts on the INTA/ or ALT_INTA/ pins.

Table 4.9 Interrupt Signal Routing

Bits [9:8] Encodings	Interrupt Signal Routing
0b00	INTA/ and ALT_INTA/
0b01	INTA/ Only
0b10	ALT_INTA/ Only
0b11	INTA/ and ALT_INTA/

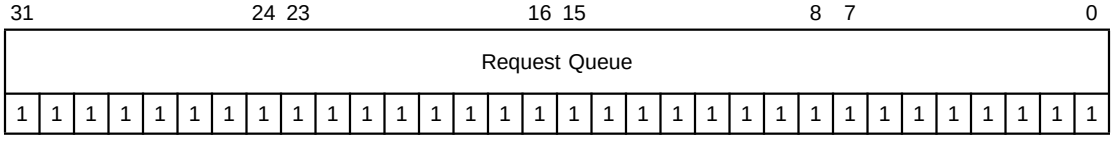
Reserved **[7:4]**
This field is reserved.

Reply Interrupt Mask **3**
Setting this bit masks reply interrupts and prevents the assertion of a PCI interrupt for all reply interrupt conditions.

Reserved **[2:1]**
This field is reserved.

Doorbell Interrupt Mask **0**
Setting this bit masks System Doorbell interrupts and prevents the assertion of a PCI interrupt for all System Doorbell interrupt conditions.

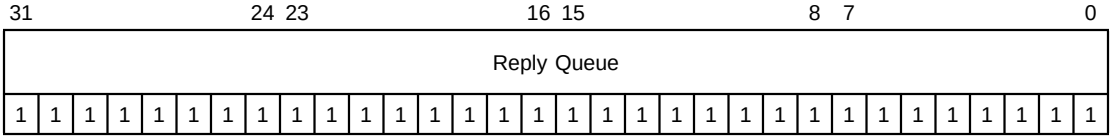
Register: 0x40
Request Queue
Read/Write



The Request Queue accepts Request Post MFAs from the host system on writes.

Request Queue **[31:0]**
For reads, this register contains 0xFFFFFFFF. For writes, the register contains the Request Post MFA.

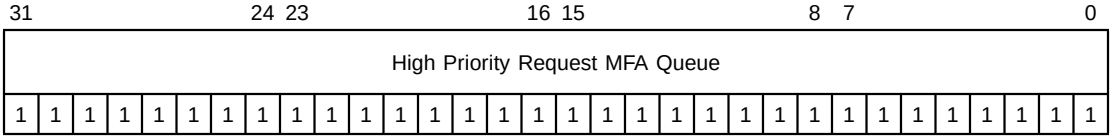
Register: 0x44
Reply Queue
Read/Write



The Reply Queue provides Reply Post MFAs to the host system on reads and accepts Reply Free MFAs from the host system on writes.

Reply FIFO **[31:0]**
For reads, this register contains the Reply Post MFA. For writes, the register contains the Reply Free MFA.

Register: 0x48
High Priority Request MFA Queue
Read/Write



The High Priority Request Queue accepts High Priority Request Post MFAs from the host on writes. The High Priority Request Post Queue is similar to the Request Post Queue, except that the LSISAS1064 processes requests from the High Priority Request Post FIFO before processing requests from the Request Post Queue.

High Priority Request MFA **[31:0]**
For reads, this register contains 0xFFFFFFFF. For writes, the register contains the High Priority Request Post MFA.

Chapter 5
Specifications

This chapter specifies the LSISAS1064 electrical and mechanical characteristics. It is divided into the following sections:

- Section 5.1, “DC Characteristics”
- Section 5.2, “AC Characteristics”
- Section 5.3, “External Memory Timing Diagrams”
- Section 5.4, “Pinout”
- Section 5.5, “Package Drawings”

Please refer to the *PCI Local Bus Specification*, the *PCI-X Addendum to the PCI Local Bus Specification*, and the *Serial Attached SCSI Standard* for timing information. The LSISAS1064 timings conform to the information that these specifications provide.

5.1 DC Characteristics

This section of the manual describes the LSISAS1064 DC characteristics. Tables 5.1 through 5.23 give current and voltage specifications.

Table 5.1 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage Temperature	–65	150	°C	–
$V_{DD\text{-}Core}$	Supply Voltage	-0.3	2.0	V	–
$V_{DD\text{-}IO}$	I/O Supply Voltage	-0.3	3.96	V	–
I_{LP}	Latch-up Current	150	–	mA	EIA/JESD78
ESD_{HBM}	Electrostatic Discharge -Human Body Model (HBM)	–	2 kV	V	JESD-A114-B

1. Stresses beyond those listed above can damage the device. These are stress ratings only; functional operation of the device at or beyond these values is not implied.

Table 5.2 Operating Conditions[1]

Symbol	Parameter	Min	Nominal	Max	Unit	Test Conditions
$V_{DD\text{-}Core}$	Core and Analog Supply Voltage	1.14	1.2	1.26	V	–
$V_{DD\text{-}IO}$	I/O Supply Voltage	2.97	3.3	3.63	V	–
$I_{DD\text{-}Core}$	Core and Analog Supply Current (dynamic)[2]	–	–	1.3	A	–
$I_{DD\text{-}I/O}$	I/O Supply Current (dynamic)[3]	–	–	1.0	A	–
T_j	Junction Temperature	–	–	115	°C	–
T_A	Operating Free Air	–	–	70	°C	–
θ_{JA}	Thermal Resistance (junction to ambient air)	–	17.5	–	°C/W	0 Linear Feet/Minute

1. Conditions that exceed the operating limits can cause the device to function incorrectly.
2. Core and analog supply only.
3. These numbers are specified for the design of the I/O power network. Not all of the $I_{DD\text{-}I/O}$ supplied to the LSISAS1064 dissipates on-chip.

For more information concerning the SAS/SATA transceivers, please refer to the Serial Attached SCSI specification.

Table 5.3 GigaBlaze Transmitter Voltage Characteristics – TX[3:0]

Speed and Technology	Parameter	Min $V_{p\text{-}p}$ Inside EYE	Max $V_{p\text{-}p}$ Outside EYE	Unit
SAS - 1.5 Gbit/s	Peak-to-Peak Voltage ($V_{p\text{-}p}$)	1050	1180	mV
SAS - 3.0 Gbit/s	$V_{p\text{-}p}$	1658	1780	mV
SATA - 1.5 Gbit/s	$V_{p\text{-}p}$	476	620	mV
SATA - 3.0 Gbit/s	$V_{p\text{-}p}$	505	694	mV

Table 5.4 GigaBlaze Receiver Voltage Characteristics – RX[3:0]

Parameter	Min	Max	Unit	Condition
V_{p-p} – OOB	150	–	mV	inside the EYE
V_{p-p} – normal operation	275	–	mV	inside the EYE

Table 5.5 GigaBlaze Transceiver Rise/Fall Characteristics – TX[3:0], RX[3:0]

Speed and Technology	Nominal Rise Time	Nominal Fall Time	Specified Range	Unit
SAS - 1.5 Gbit/s	141	153	67 - 273	psec
SAS - 3.0 Gbit/s	129	125	67 - 137	psec
SATA - 1.5 Gbit/s	141	141	100 - 273	psec
SATA - 3.0 Gbit/s	112	112	66.6 - 136.6	psec

Table 5.6 PCI-X Input Signals – CLK, RST/, GNT/, IDSEL, ALT_GNT/, CPCI64_EN/

Parameter	Min	Max	Unit
V_{il}	-0.5	0.35 × VDDIO	V
V_{ih}	0.5 × VDDIO	VDDIO + 0.5	V
I_{in}	-10	10	µA

Table 5.7 PCI-X Output Signals – REQ/, INTA/, ALT_INTA/

Parameter	Min	Max	Unit	Condition
V_{ol}	–	0.1 × VDDIO	V	I_{out} = 1500 µA
V_{oh}	0.9 × VDDIO	–	V	I_{out} = -500 µA
I_{oz}	-10	10	µA	–

Table 5.8 PCI-X Bidirectional Signals – AD[63:0], C_BE[7:0]/, CPCI_ENUM/, PAR, PAR64, ACK64/, REQ64/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, SERR/

Parameter	Min	Max	Unit	Condition
V_{il}	-0.5	0.35 × VDDIO	V	–
V_{ih}	0.5 × VDDIO	VDDIO + 0.5	V	–

Table 5.8 PCI-X Bidirectional Signals – AD[63:0], C_BE[7:0]/, CPCI_ENUM/, PAR, PAR64, ACK64/, REQ64/, FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, SERR/ (Cont.)

Parameter	Min	Max	Unit	Condition
V_{ol}	–	0.1 × VDDIO	V	I_{out} = 1500 µA
V_{oh}	0.9 × VDDIO	–	V	I_{out} = -500 µA
I_{oz}	-10	10	µA	–

Table 5.9 Inputs – ZCR_EN/, CPCI_EN/, TN/, UART_RX

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
I_{in}	-10	10	µA
$I_{pull\text{-}up}$	70	200	µA

Table 5.10 Inputs – CPCI_SWITCH, MODE[5:0], SCAN_ENABLE, SCAN_MODE

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
I_{in}	-10	10	µA
$I_{pull\text{-}down}$	70	350	µA

Table 5.11 Schmitt Trigger Inputs – TST_RST/, TCK, TRST/, TDI, TMS, TCK_ICE, TRST_ICE/, TDI_ICE, TMS_ICE

Parameter	Min	Nom	Max	Unit
VT+	–	1.6	2	V
VT-	1	1.2	–	V
Hysteresis	0.3	0.4	–	V
I_{in}	-10	–	10	µA
$I_{pull\text{-}up}$	70	105	200	µA

Table 5.12 Schmitt Trigger Inputs – REFCLK_B, FSELA

Parameter	Min	Nom	Max	Units
VT+	–	1.6	2	V
VT-	1	1.2	–	V
Hysteresis	0.3	0.4	–	V
I_{in}	-10	–	10	µA
$I_{pull\text{-}down}$	70	140	350	µA

Table 5.13 10 mA, 3-State Outputs – CPCI_LED/, HB_LED/, FAULT_LED[3:0]/, ACTIVE_LED[3:0]/

Parameter	Min	Max	Unit
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.14 5 mA, 3-State Outputs – TDO, TDO_ICE, RTCK_ICE

Parameter	Min	Max	Unit
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.15 8 mA Outputs – MCLK, ADSC/, ADV/

Parameter	Min	Max	Unit
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.16 5 mA Outputs – UART_TX

Parameter	Min	Max	Unit
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.17 4 mA Outputs – PROCMON

Parameter	Min	Max	Unit
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.18 8 mA Bidirectional Signals – MAD[31:0]

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA
$I_{pull\text{-}down}$	70	350	µA

Table 5.19 8 mA Bidirectional Signals – MADP[3:0]

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA
$I_{pull\text{-}up}$	70	200	µA

Table 5.20 8 mA Bidirectional Signals – MOE[1:0]/, MWE[1:0]/, BWE[3:0]/, NVSRAM_CS/, PSBRAM_CS/, FLASH_CS/

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA

Table 5.21 5 mA Bidirectional Signals – SERIAL_CLK, SERIAL_DATA, ISTWI_CLK, ISTWI_DATA, GPIO[3:0], TMUX_SPARE[7:0]

Parameter	Min	Max	Unit
V_{il}	VSS - 0.5	0.8	V
V_{ih}	2	VDD + 0.3	V
V_{ol}	–	0.4	V
V_{oh}	2.4	–	V
I_{oz}	-10	10	µA
$I_{pull\text{-}up}$	70	200	µA

Table 5.22 PECL Buffer Signals – REFCLK_P, REFCLK_N

Parameter	Min	Nominal	Max	Unit
V_{in_cm}	1.6	2.0	2.4	V
$V_{in\_diff\_pp}$	0.6	–	2.0	V
V_{il}	0.6	–	2.1	V
V_{ih}	1.9	–	3.4	V
I_{in}	-10	–	10	µA

Table 5.23 Capacitance[1]

Capacitance	Value
C_{in}	3.5 pF
Co_{ut}	3.5 pF
C_{io} (PCI-X pads)	5 pF

1. Capacitance values do not include package capacitance.

5.2 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to Section 5.1, “DC Characteristics.”) Chip timing is based on simulation at worst case voltage, temperature, and processing. Timing was developed with a load capacitance of 50 pF, which does not include the PCI/PCI-X pads. The PCI/PCI-X pads are specified as 10 pF loads. Figure 5.1 and Table 5.24 provide external clock timing data.

Figure 5.1 External Clock

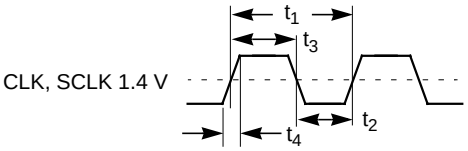


Table 5.24 External Clock

Symbol	Parameter	133 MHz PCI-X		66 MHz PCI-X		66 MHz PCI		33 MHz PCI		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_1	PCI Bus clock period[1]	7.5	20	15	20	15	30	30	250	ns
t_2	PCI CLK LOW time[2]	3	–	6	–	6	–	11	–	ns
t_3	PCI CLK HIGH time	3	–	6	–	6	–	11	–	ns
t_4	PCI CLK slew rate	1.5	4	1.5	4	1.5	4	1	4	V/ns

1. For frequencies above 33 MHz, the clock frequency can not be changed beyond the spread spectrum limits except while RST/ is asserted.
2. Duty cycle not to exceed 60/40.

Figure 5.2 and Table 5.25 provide reset input timing data.

Figure 5.2 Reset Input

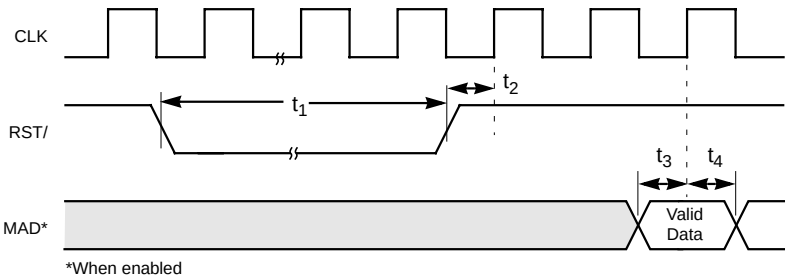


Table 5.25 Reset Input

Symbol	Parameter	Min	Max	Unit
t_1	Reset pulse width	10	–	ns
t_2	Reset deasserted setup to CLK HIGH	0	–	ns
t_3	MAD setup time to CLK HIGH (for configuring the MAD bus only)	20	–	ns
t_4	MAD hold time from CLK HIGH (for configuring the MAD bus only)	20	–	ns

Figure 5.3 and Table 5.26 provide Interrupt Output timing data.

Figure 5.3 Interrupt Output

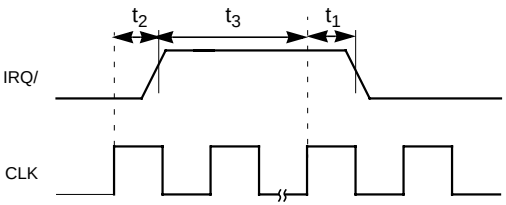


Table 5.26 Interrupt Output

Symbol	Parameter	Min	Max	Unit
t_1	CLK HIGH to IRQ/ LOW	2	11	ns
t_2	CLK HIGH to IRQ/ HIGH	2	11	ns
t_3	IRQ/ deassertion time	3	–	CLK

5.3 External Memory Timing Diagrams

This section provides timing information and examples for the external memory options available for use with the LSISAS1064.

Table 5.27 Flash Write Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_4	Flash Address Setup to FLASH_CS/ (Write)	20	–	ns
t_5	Flash Address Setup to BWE/ (Write Enables)	10	–	ns
t_6	FLASH_CS/ Width (Write)	60	400	ns
t_7	Flash Write Recover	40	–	ns
–	Flash ROM Write Cycle Time	120	460	ns

Figure 5.4 Flash Write

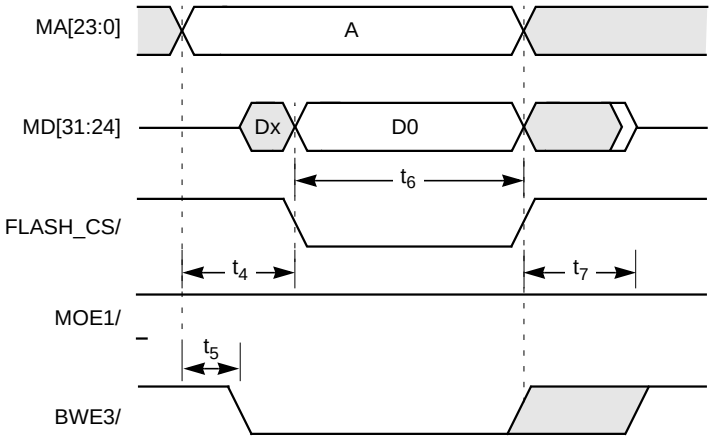


Table 5.28 Flash Read Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_1	Flash Address Setup to FLASH_CS/ (Read)	10	–	ns
t_2	FLASH_CS/ Width (Read)	60	400	ns
t_3	Flash Read Recover (back-to-back access)	10	–	ns
–	Flash ROM Read Cycle Time	70	420	ns

Figure 5.5 Flash Read

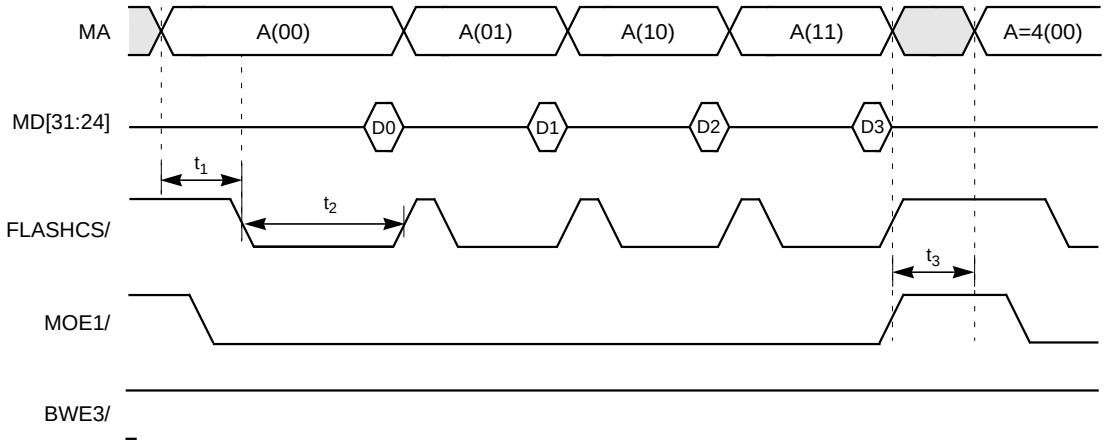


Table 5.29 NVRAM Read Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_1	NVRAM Address Setup to NVRAM_CS/ (Read)	10	–	ns
t_2	NVRAM_CS/ Width (Read)	15	400	ns
t_3	NVRAM Read Recover (back-to-back access)	10	–	ns
–	NVRAM Read Cycle Time	25	420	ns

Figure 5.6 NV Read

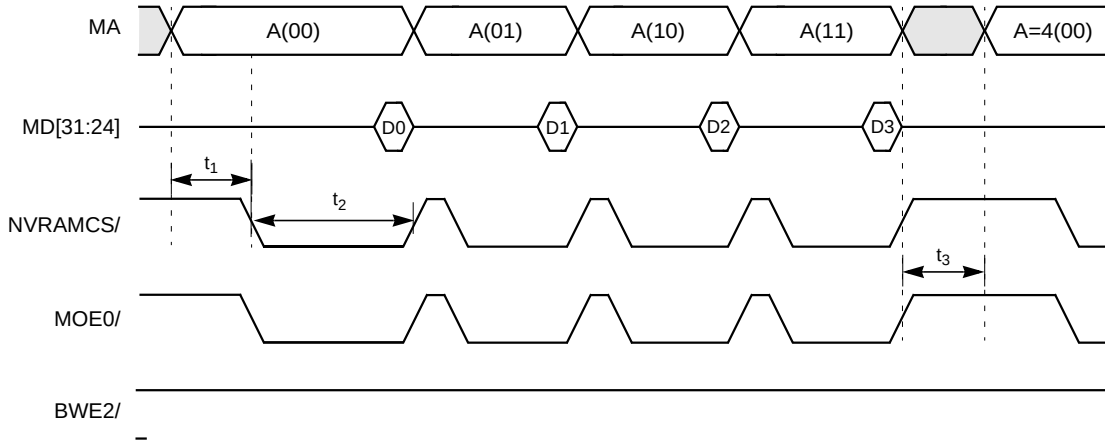
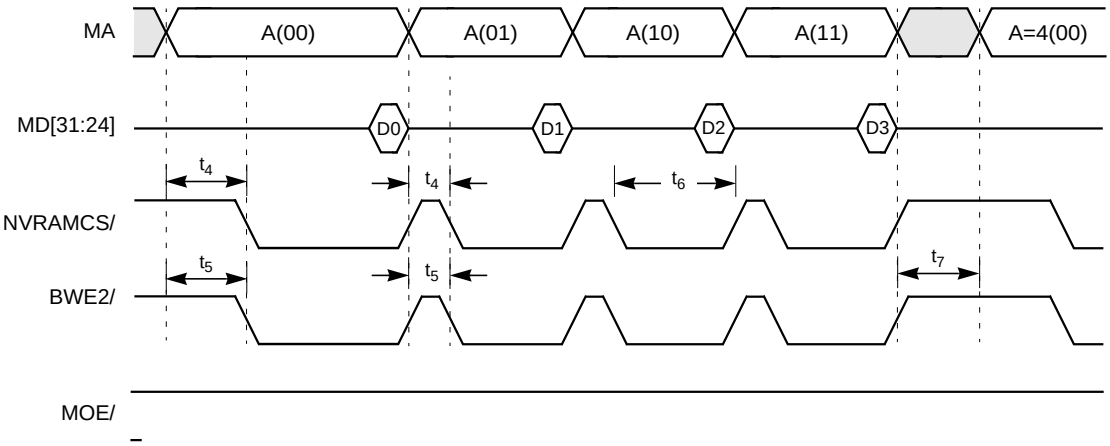


Table 5.30 NVRAM Write Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_4	NVRAM Address Setup to NVRAM_CS/ (Write)	10	–	ns
t_5	NVRAM Address Setup to BWE/ (Write Enables)	10	–	ns
t_6	NVRAM_CS/ Width (Write)	15	400	ns
t_7	NVRAM Write Recover	0	40	ns
–	NVRAM Write Cycle Time	25	460	ns

Figure 5.7 NV Write



5.4 Pinout

Table 5.31 provides the signal listing by signal name. Table 5.32 provides the BGA pin listing. Figure 5.8 provides a BGA diagram.

Table 5.31 Listing by Signal Name

SignalPin		SignalPin		SignalPin		SignalPin	
ACK64/	AE18	AD[55]	AD23	MAD[7]	D24	N/C	E8
ACTIVE_LED[0]/	H4	AD[56]	AF22	MAD[8]	D25	N/C	E9
ACTIVE_LED[1]/	G1	AD[57]	AF23	MAD[9]	E25	N/C	E10
ACTIVE_LED[2]/	H1	AD[58]	AE22	MAD[10]	C26	N/C	E15
ACTIVE_LED[3]/	L5	AD[59]	AE23	MAD[11]	D23	N/C	E16
AD[0]	AF14	AD[60]	AF21	MAD[12]	H21	N/C	E17
AD[1]	AE17	AD[61]	AC19	MAD[13]	H23	N/C	F9
AD[2]	AD14	AD[62]	AF20	MAD[14]	K24	N/C	G4
AD[3]	AF15	AD[63]	AF19	MAD[15]	H24	N/C	G6
AD[4]	AF13	ADSC/	P23	MAD[16]	V26	N/C	G22
AD[5]	AF16	ADV/	U26	MAD[17]	T26	N/C	H5
AD[6]	AF12	ALT_GNT/	T5	MAD[18]	T24	N/C	H6
AD[7]	AE11	ALT_INTA/	U3	MAD[19]	R26	N/C	H22
AD[8]	AF10	BWE[0]/	N22	MAD[20]	U25	N/C	J4
AD[9]	AF11	BWE[1]/	M26	MAD[21]	R23	N/C	J6
AD[10]	AE9	BWE[2]/	J25	MAD[22]	Y26	N/C	J21
AD[11]	AB12	BWE[3]/	N25	MAD[23]	T22	N/C	J23
AD[12]	AB10	BZR_SET	V21	MAD[24]	U24	N/C	K5
AD[13]	AF9	BZVDD	AA24	MAD[25]	AA26	N/C	K22
AD[14]	AD10	C_BE[0]/	AE10	MAD[26]	V25	N/C	K25
AD[15]	AF5	C_BE[1]/	AC8	MAD[27]	V24	N/C	L22
AD[16]	AF4	C_BE[2]/	AD6	MAD[28]	W26	N/C	M4
AD[17]	AE5	C_BE[3]/	AD2	MAD[29]	R22	N/C	N4
AD[18]	AD4	C_BE[4]/	AF18	MAD[30]	AA25	N/C	N5
AD[19]	AE4	C_BE[5]/	AD19	MAD[31]	AB26	N/C	N23
AD[20]	Y6	C_BE[6]/	AF17	MADP[0]	G21	N/C	N24
AD[21]	Y8	C_BE[7]/	AE19	MADP[1]	J26	N/C	P3
AD[22]	AB3	CLK	Y4	MADP[2]	P26	N/C	P4
AD[23]	AE3	CPCI64_EN/	U2	MADP[3]	W23	N/C	P22
AD[24]	Y7	CPCI_LED/	M5	MCLK	N26	N/C	R4
AD[25]	AA5	CPCI_EN/	R1	MODE[0]	F3	N/C	R5
AD[26]	AA4	CPCI_ENUM/	U1	MODE[1]	E2	N/C	T25
AD[27]	AE1	CPCI_SWITCH	P1	MODE[2]	E3	N/C	U5
AD[28]	AB2	DEVSEL/	AD5	MODE[3]	D1	N/C	U22
AD[29]	AC1	FAULT_LED[0]/	F2	MODE[4]	F4	N/C	V2
AD[30]	V5	FAULT_LED[1]/	E1	MODE[5]	C2	N/C	V4
AD[31]	AD1	FAULT_LED[2]/	J5	MOE[0]/	M22	N/C	V6
AD[32]	AB24	FAULT_LED[3]/	F1	MOE[1]/	E26	N/C	V22
AD[33]	AC26	FLASH_CS/	H26	MWE[0]/	L26	N/C	V23
AD[34]	AD26	FRAME/	AB7	MWE[1]/	H25	N/C	W2
AD[35]	AA23	FSELA	G5	N/C	A11	N/C	W3
AD[36]	Y22	GNT/	AA1	N/C	A16	N/C	W4
AD[37]	W20	GPIO[0]	J2	N/C	A21	N/C	W6
AD[38]	AB25	GPIO[1]	K3	N/C	B8	N/C	W21
AD[39]	AC25	GPIO[2]	L3	N/C	B22	N/C	W22
AD[40]	AC24	GPIO[3]	K2	N/C	B23	N/C	Y1
AD[41]	Y20	HB_LED/	J3	N/C	C8	N/C	Y5
AD[42]	AD24	IDDTN	N1	N/C	C14	N/C	Y21
AD[43]	AF25	IDSEL	AD3	N/C	C15	N/C	AA7
AD[44]	AB21	INTA/	V3	N/C	C19	N/C	AA8
AD[45]	AC20	IRDY/	AF6	N/C	C20	N/C	AA18
AD[46]	AA20	ISTW_CLK	F22	N/C	D6	N/C	AB8
AD[47]	AD25	ISTW_DATA	F21	N/C	D7	N/C	AB9
AD[48]	AC23	MAD[0]	B26	N/C	D8	N/C	AB11
AD[49]	AA19	MAD[1]	F23	N/C	D9	N/C	AB13
AD[50]	AE25	MAD[2]	G23	N/C	D14	N/C	AB15
AD[51]	AE24	MAD[3]	C25	N/C	D15	N/C	AB16
AD[52]	AF24	MAD[4]	C24	N/C	D16	N/C	AC7
AD[53]	AB19	MAD[5]	E24	N/C	D22	N/C	AC9
AD[54]	AD22	MAD[6]	D26	N/C	E7		

Note: *NC* pins are not connected.

Table 5.31 Listing by Signal Name (Cont.)

SignalPin		SignalPin		SignalPin		SignalPin	
N/C	AC13	TDI	J1	VDDIO33	C6	VSS2	B14
N/C	AC14	TDI_ICE	F7	VDDIO33	C7	VSS2	B15
N/C	AC15	TDIODE_P	M23	VDDIO33	E4	VSS2	B19
N/C	AC18	TDIODE_N	K26	VDDIO33	E5	VSS2	B20
N/C	AC21	TDO	K1	VDDIO33	E22	VSS2	D5
N/C	AD11	TDO_ICE	B4	VDDIO33	F24	VSS2	D11
N/C	AE2	TMS	P2	VDDIO33	G3	VSS2	D17
N/C	AE14	TMS_ICE	A4	VDDIO33	G24	VSS2	E21
NVSRAM_CS/	G26	TMUX_SPARE[0]	A3	VDDIO33	H3	VSS2	E23
PAR	AD9	TMUX_SPARE[1]	A2	VDDIO33	K23	VSS2	F5
PAR64	AB17	TMUX_SPARE[2]	E6	VDDIO33	L4	VSS2	F25
PERR/	AF7	TMUX_SPARE[3]	C4	VDDIO33	L24	VSS2	G2
PLL_VDD	AC4	TMUX_SPARE[4]	D4	VDDIO33	M3	VSS2	G8
PLL_VSS	AC3	TMUX_SPARE[5]	B3	VDDIO33	M24	VSS2	G25
PROCMON	M1	TMUX_SPARE[6]	C3	VDDIO33	N3	VSS2	H2
PSBRAM_CS/	J24	TMUX_SPARE[7]	F6	VDDIO33	P24	VSS2	H20
REFCLK_B	D3	TN/	P5	VDDIO33	R3	VSS2	K4
REFCLK_N	J22	TRDY/	AA9	VDDIO33	R24	VSS2	L23
REFCLK_P	F26	TRST_ICE/	C5	VDDIO33	T3	VSS2	L25
REFPLL_VDD	D2	TRST/	L1	VDDIO33	T23	VSS2	M2
REFPLL_VSS	C1	TST_RST/	G7	VDDIO33	U4	VSS2	M12
REQ/	AB1	TXB_VDD0	F19	VDDIO33PCIX	W24	VSS2	M14
REQ64/	AD18	TXB_VDD1	E18	VDDIO33PCIX	Y3	VSS2	M25
RST/	W5	TXB_VDD2	A18	VDDIO33PCIX	Y24	VSS2	N2
RTCK_ICE	A5	TXB_VDD3	B10	VDDIO33PCIX	AA3	VSS2	N13
RTRIM	C9	TXB_VSS0	D21	VDDIO33PCIX	AB5	VSS2	N15
RXB_VDD0	G19	TXB_VSS1	D19	VDDIO33PCIX	AB22	VSS2	P12
RXB_VDD1	E19	TXB_VSS2	A17	VDDIO33PCIX	AB23	VSS2	P14
RXB_VDD2	C17	TXB_VSS3	C10	VDDIO33PCIX	AC5	VSS2	P25
RXB_VDD3	D12	TX0–	A23	VDDIO33PCIX	AC11	VSS2	R2
RXB_VSS0	G20	TX1–	A19	VDDIO33PCIX	AC17	VSS2	R13
RXB_VSS1	E20	TX2–	C13	VDDIO33PCIX	AD7	VSS2	R15
RXB_VSS2	B18	TX3–	A9	VDDIO33PCIX	AD8	VSS2	R25
RXB_VSS3	D13	TX0+	A24	VDDIO33PCIX	AD12	VSS2	T2
RX0–	B25	TX1+	A20	VDDIO33PCIX	AD13	VSS2	T4
RX1–	C21	TX2+	B13	VDDIO33PCIX	AD15	VSS2	U23
RX2–	C16	TX3+	A10	VDDIO33PCIX	AD16	VSS2	W7
RX3–	A14	TX_VDD0	C22	VDDIO33PCIX	AD20	VSS2	W25
RX0+	B24	TX_VDD1	C18	VDDIO33PCIX	AD21	VSS2	Y2
RX1+	B21	TX_VDD2	E13	VDDIO5PCIX	V1	VSS2	Y19
RX2+	B16	TX_VDD3	B9	VDDIO5PCIX	W1	VSS2	Y25
RX3+	A13	TX_VSS0	D20	VDDIO5PCIX	Y23	VSS2	AA2
RX_VDD0	C23	TX_VSS1	D18	VDDIO5PCIX	AA6	VSS2	AA22
RX_VDD1	A22	TX_VSS2	A15	VDDIO5PCIX	AA21	VSS2	AB4
RX_VDD2	E14	TX_VSS3	E11	VDDIO5PCIX	AB14	VSS2	AB6
RX_VDD3	A12	UART_RX	F8	VDDIO5PCIX	AB18	VSS2	AC10
RX_VSS0	F20	UART_TX	A6	VDDIO5PCIX	AB20	VSS2	AC16
RX_VSS1	F18	VDD2	C11	VDDIO5PCIX	AC2	VSS2	AC22
RX_VSS2	B17	VDD2	C12	VDDIO5PCIX	AC6	VSS2	AE7
RX_VSS3	E12	VDD2	D10	VDDIO5PCIX	AC12	VSS2	AE8
SCAN_ENABLE	B2	VDD2	M13	VDDIO5PCIX	AD17	VSS2	AE12
SCAN_MODE	H7	VDD2	M15	VDDIO5PCIX	AF8	VSS2	AE13
SERIAL_CLK	A8	VDD2	N12	VSS2	A25	VSS2	AE15
SERIAL_DATA	A7	VDD2	N14	VSS2	B1	VSS2	AE16
SERR/	AF3	VDD2	P13	VSS2	B6	VSS2	AE20
STOP/	AE6	VDD2	P15	VSS2	B7	VSS2	AE21
TCK	L2	VDD2	R12	VSS2	B11	VSS2	AE26
TCK_ICE	B5	VDD2	R14	VSS2	B12	VSS2	AF2
						ZCR_EN/	T1

Note:*NC* pins are not connected.

Table 5.32 Listing by Pin Number

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
TMUX_SPARE[1]	A2	VDD2	C12	VSS2	E21	REFCLK_N	J22
TMUX_SPARE[0]	A3	TX2–	C13	VDDIO33	E22	N/C	J23
TMS_ICE	A4	N/C	C14	VSS2	E23	PSBRAM_CS/	J24
RTCK_ICE	A5	N/C	C15	MAD[5]	E24	BWE[2]/	J25
UART_TX	A6	RX2–	C16	MAD[9]	E25	MADP[1]	J26
SERIAL_DATA	A7	RXB_VDD2	C17	MOE[1]/	E26	TDO	K1
SERIAL_CLK	A8	TX_VDD1	C18	FAULT_LED[3]/	F1	GPIO[3]	K2
TX3–	A9	N/C	C19	FAULT_LED[0]/	F2	GPIO[1]	K3
TX3+	A10	N/C	C20	MODE[0]	F3	VSS2	K4
N/C	A11	RX1–	C21	MODE[4]	F4	N/C	K5
RX_VDD3	A12	TX_VDD0	C22	VSS2	F5	N/C	K22
RX3+	A13	RX_VDD0	C23	TMUX_SPARE[7]	F6	VDDIO33	K23
RX3–	A14	MAD[4]	C24	TDI_ICE	F7	MAD[14]	K24
TX_VSS2	A15	MAD[3]	C25	UART_RX	F8	N/C	K25
N/C	A16	MAD[10]	C26	N/C	F9	TDIODE_N	K26
TXB_VSS2	A17	MODE[3]	D1	RX_VSS1	F18	TRST/	L1
TXB_VDD2	A18	REFPLL_VDD	D2	TXB_VDD0	F19	TCK	L2
TX1–	A19	REFCLK_B	D3	RX_VSS0	F20	GPIO[2]	L3
TX1+	A20	TMUX_SPARE[4]	D4	ISTW_DATA	F21	VDDIO33	L4
N/C	A21	VSS2	D5	ISTW_CLK	F22	ACTIVE_LED[3]/	L5
RX_VDD1	A22	N/C	D6	MAD[1]	F23	N/C	L22
TX0–	A23	N/C	D7	VDDIO33	F24	VSS2	L23
TX0+	A24	N/C	D8	VSS2	F25	VDDIO33	L24
VSS2	A25	N/C	D9	REFCLK_P	F26	VSS2	L25
VSS2	B1	VDD2	D10	ACTIVE_LED[1]/	G1	MWE[0]/	L26
SCAN_ENABLE	B2	VSS2	D11	VSS2	G2	PROCMON	M1
TMUX_SPARE[5]	B3	RXB_VDD3	D12	VDDIO33	G3	VSS2	M2
TDO_ICE	B4	RXB_VSS3	D13	N/C	G4	VDDIO33	M3
TCK_ICE	B5	N/C	D14	FSELA	G5	N/C	M4
VSS2	B6	N/C	D15	N/C	G6	CPCI_LED/	M5
VSS2	B7	N/C	D16	TST_RST/	G7	VSS2	M12
N/C	B8	VSS2	D17	VSS2	G8	VDD2	M13
TX_VDD3	B9	TX_VSS1	D18	RXB_VDD0	G19	VSS2	M14
TXB_VDD3	B10	TXB_VSS1	D19	RXB_VSS0	G20	VDD2	M15
VSS2	B11	TX_VSS0	D20	MADP[0]	G21	MOE[0]/	M22
VSS2	B12	TXB_VSS0	D21	N/C	G22	TDIODE_P	M23
TX2+	B13	N/C	D22	MAD[2]	G23	VDDIO33	M24
VSS2	B14	MAD[11]	D23	VDDIO33	G24	VSS2	M25
VSS2	B15	MAD[7]	D24	VSS2	G25	BWE[1]/	M26
RX2+	B16	MAD[8]	D25	NVSRAM_CS/	G26	IDDTN	N1
RX_VSS2	B17	MAD[6]	D26	ACTIVE_LED[2]/	H1	VSS2	N2
RXB_VSS2	B18	FAULT_LED[1]/	E1	VSS2	H2	VDDIO33	N3
VSS2	B19	MODE[1]	E2	VDDIO33	H3	N/C	N4
VSS2	B20	MODE[2]	E3	ACTIVE_LED[0]/	H4	N/C	N5
RX1+	B21	VDDIO33	E4	N/C	H5	VDD2	N12
N/C	B22	VDDIO33	E5	N/C	H6	VSS2	N13
N/C	B23	TMUX_SPARE[2]	E6	SCAN_MODE	H7	VDD2	N14
RX0+	B24	N/C	E7	VSS2	H20	VSS2	N15
RX0–	B25	N/C	E8	MAD[12]	H21	BWE[0]/	N22
MAD[0]	B26	N/C	E9	N/C	H22	N/C	N23
REFPLL_VSS	C1	N/C	E10	MAD[13]	H23	N/C	N24
MODE[5]	C2	TX_VSS3	E11	MAD[15]	H24	BWE[3]/	N25
TMUX_SPARE[6]	C3	RX_VSS3	E12	MWE[1]/	H25	MCLK	N26
TMUX_SPARE[3]	C4	TX_VDD2	E13	FLASH_CS/	H26	CPCI_SWITCH	P1
TRST_ICE/	C5	RX_VDD2	E14	TDI	J1	TMS	P2
VDDIO33	C6	N/C	E15	GPIO[0]	J2	N/C	P3
VDDIO33	C7	N/C	E16	HB_LED/	J3	N/C	P4
N/C	C8	N/C	E17	N/C	J4	TN/	P5
RTRIM	C9	TXB_VDD1	E18	FAULT_LED[2]/	J5	VSS2	P12
TXB_VSS3	C10	RXB_VDD1	E19	N/C	J6	VDD2	P13
VDD2	C11	RXB_VSS1	E20	N/C	J21	VSS2	P14

Note: *NC* pins are not connected.

Table 5.32 Listing by Pin Number (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
P15	VDD2	W6	N/C	AB15	N/C	AD20	VDDIO33PCIX
P22	N/C	W7	VSS2	AB16	N/C	AD21	VDDIO33PCIX
P23	ADSC/	W20	AD[37]	AB17	PAR64	AD22	AD[54]
P24	VDDIO33	W21	N/C	AB18	VDDIO5PCIX	AD23	AD[55]
P25	VSS2	W22	N/C	AB19	AD[53]	AD24	AD[42]
P26	MADP[2]	W23	MADP[3]	AB20	VDDIO5PCIX	AD25	AD[47]
R1	CPCI_EN/	W24	VDDIO33PCIX	AB21	AD[44]	AD26	AD[34]
R2	VSS2	W25	VSS2	AB22	VDDIO33PCIX	AE1	AD[27]
R3	VDDIO33	W26	MAD[28]	AB23	VDDIO33PCIX	AE2	N/C
R4	N/C	Y1	N/C	AB24	AD[32]	AE3	AD[23]
R5	N/C	Y2	VSS2	AB25	AD[38]	AE4	AD[19]
R12	VDD2	Y3	VDDIO33PCIX	AB26	MAD[31]	AE5	AD[17]
R13	VSS2	Y4	CLK	AC1	AD[29]	AE6	STOP/
R14	VDD2	Y5	N/C	AC2	VDDIO5PCIX	AE7	VSS2
R15	VSS2	Y6	AD[20]	AC3	PLL_VSS	AE8	VSS2
R22	MAD[29]	Y7	AD[24]	AC4	PLL_VDD	AE9	AD[10]
R23	MAD[21]	Y8	AD[21]	AC5	VDDIO33PCIX	AE10	C_BE[0]/
R24	VDDIO33	Y19	VSS2	AC6	VDDIO5PCIX	AE11	AD[7]
R25	VSS2	Y20	AD[41]	AC7	N/C	AE12	VSS2
R26	MAD[19]	Y21	N/C	AC8	C_BE[1]/	AE13	VSS2
T1	ZCR_EN/	Y22	AD[36]	AC9	N/C	AE14	N/C
T2	VSS2	Y23	VDDIO5PCIX	AC10	VSS2	AE15	VSS2
T3	VDDIO33	Y24	VDDIO33PCIX	AC11	VDDIO33PCIX	AE16	VSS2
T4	VSS2	Y25	VSS2	AC12	VDDIO5PCIX	AE17	AD[1]
T5	ALT_GNT/	Y26	MAD[22]	AC13	N/C	AE18	ACK64/
T22	MAD[23]	AA1	GNT/	AC14	N/C	AE19	C_BE[7]/
T23	VDDIO33	AA2	VSS2	AC15	N/C	AE20	VSS2
T24	MAD[18]	AA3	VDDIO33PCIX	AC16	VSS2	AE21	VSS2
T25	N/C	AA4	AD[26]	AC17	VDDIO33PCIX	AE22	AD[58]
T26	MAD[17]	AA5	AD[25]	AC18	N/C	AE23	AD[59]
U1	CPCI_ENUM/	AA6	VDDIO5PCIX	AC19	AD[61]	AE24	AD[51]
U2	CPCI64_EN/	AA7	N/C	AC20	AD[45]	AE25	AD[50]
U3	ALT_INTA/	AA8	N/C	AC21	N/C	AE26	VSS2
U4	VDDIO33	AA9	TRDY/	AC22	VSS2	AF2	VSS2
U5	N/C	AA18	N/C	AC23	AD[48]	AF3	SERR/
U22	N/C	AA19	AD[49]	AC24	AD[40]	AF4	AD[16]
U23	VSS2	AA20	AD[46]	AC25	AD[39]	AF5	AD[15]
U24	MAD[24]	AA21	VDDIO5PCIX	AC26	AD[33]	AF6	IRDY/
U25	MAD[20]	AA22	VSS2	AD1	AD[31]	AF7	PERR/
U26	ADV/	AA23	AD[35]	AD2	C_BE[3]/	AF8	VDDIO5PCIX
V1	VDDIO5PCIX	AA24	BZVDD	AD3	IDSEL	AF9	AD[13]
V2	N/C	AA25	MAD[30]	AD4	AD[18]	AF10	AD[8]
V3	INTA/	AA26	MAD[25]	AD5	DEVSEL/	AF11	AD[9]
V4	N/C	AB1	REQ/	AD6	C_BE[2]/	AF12	AD[6]
V5	AD[30]	AB2	AD[28]	AD7	VDDIO33PCIX	AF13	AD[4]
V6	N/C	AB3	AD[22]	AD8	VDDIO33PCIX	AF14	AD[0]
V21	BZR_SET	AB4	VSS2	AD9	PAR	AF15	AD[3]
V22	N/C	AB5	VDDIO33PCIX	AD10	AD[14]	AF16	AD[5]
V23	N/C	AB6	VSS2	AD11	N/C	AF17	C_BE[6]/
V24	MAD[27]	AB7	FRAME/	AD12	VDDIO33PCIX	AF18	C_BE[4]/
V25	MAD[26]	AB8	N/C	AD13	VDDIO33PCIX	AF19	AD[63]
V26	MAD[16]	AB9	N/C	AD14	AD[2]	AF20	AD[62]
W1	VDDIO5PCIX	AB10	AD[12]	AD15	VDDIO33PCIX	AF21	AD[60]
W2	N/C	AB11	N/C	AD16	VDDIO33PCIX	AF22	AD[56]
W3	N/C	AB12	AD[11]	AD17	VDDIO5PCIX	AF23	AD[57]
W4	N/C	AB13	N/C	AD18	REQ64/	AF24	AD[52]
W5	RST/	AB14	VDDIO5PCIX	AD19	C_BE[5]/	AF25	AD[43]

Note: *NC* pins are not connected.

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Figure 5.8 LSISAS1064 472-Pin BGA Top View

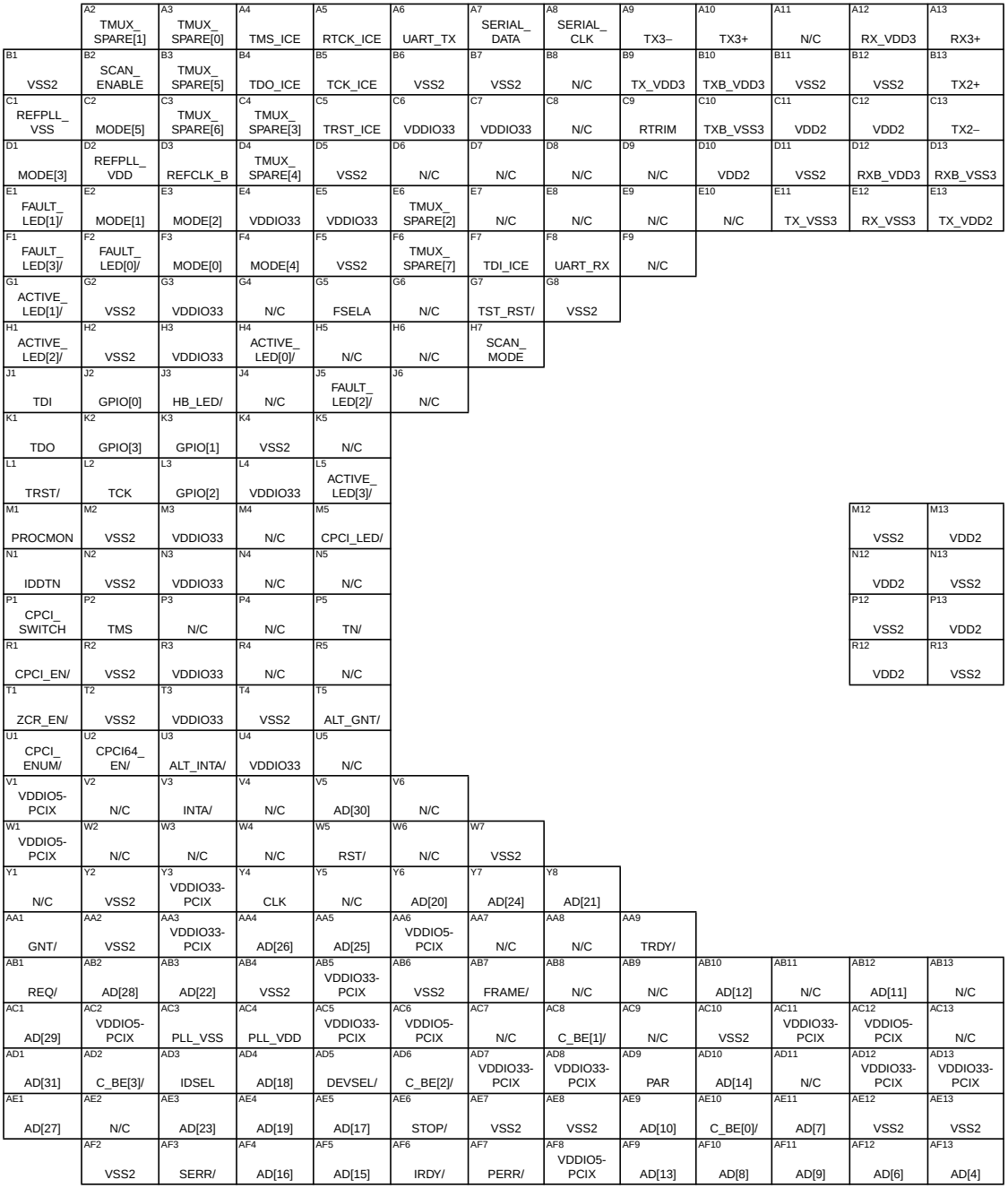
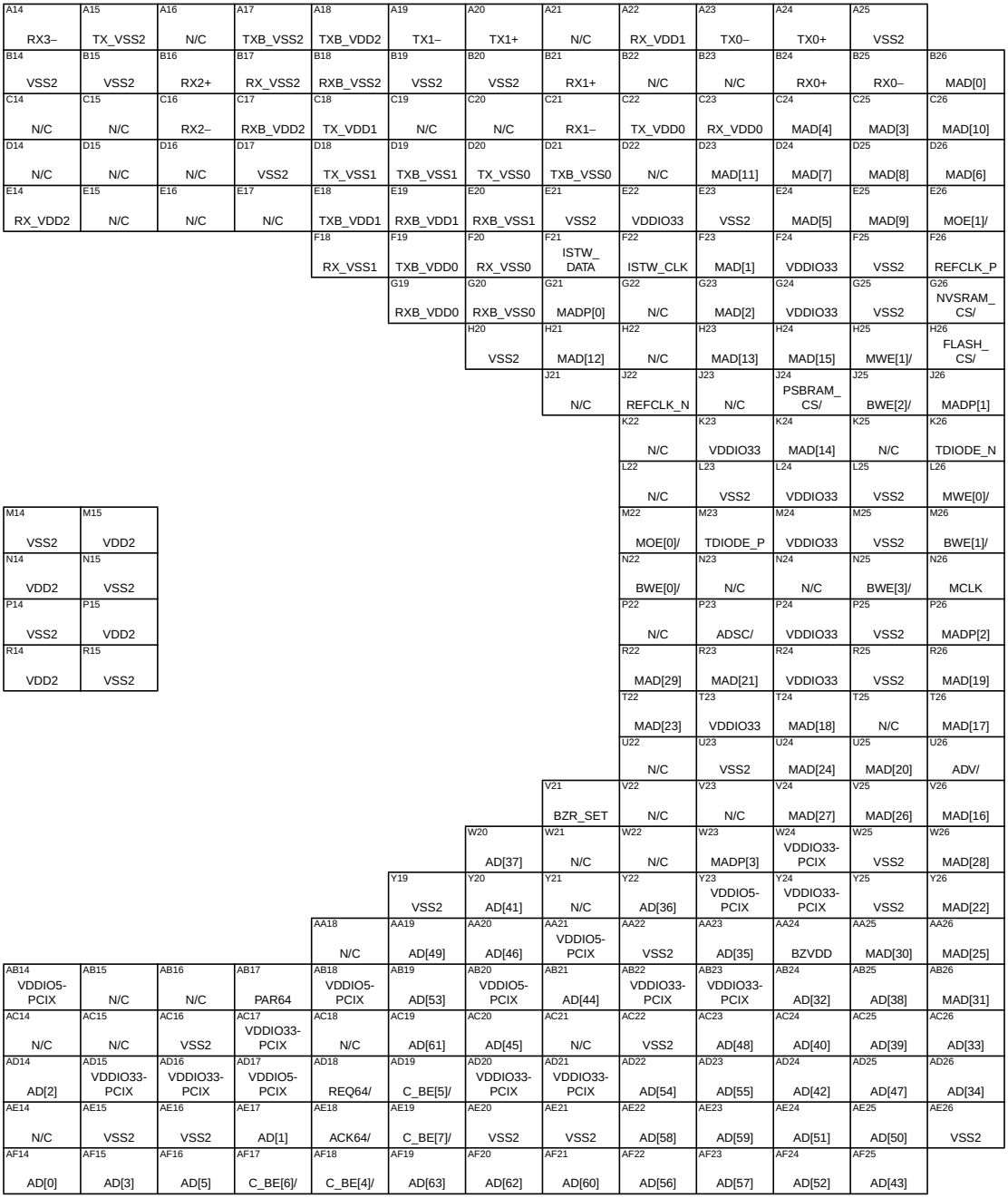


Figure 5.8 LSISAS1064 472-Pin BGA Top View (Cont.)



A14 RX3–	A15 TX_VSS2	A16 N/C	A17 TXB_VSS2	A18 TXB_VDD2	A19 TX1–	A20 TX1+	A21 N/C	A22 RX_VDD1	A23 TX0–	A24 TX0+	A25 VSS2	
B14 VSS2	B15 VSS2	B16 RX2+	B17 RX_VSS2	B18 RXB_VSS2	B19 VSS2	B20 VSS2	B21 RX1+	B22 N/C	B23 N/C	B24 RX0+	B25 RX0–	B26 MAD[0]
C14 N/C	C15 N/C	C16 RX2–	C17 RXB_VDD2	C18 TX_VDD1	C19 N/C	C20 N/C	C21 RX1–	C22 TX_VDD0	C23 RX_VDD0	C24 MAD[4]	C25 MAD[3]	C26 MAD[10]
D14 N/C	D15 N/C	D16 N/C	D17 VSS2	D18 TX_VSS1	D19 TXB_VSS1	D20 TX_VSS0	D21 TXB_VSS0	D22 N/C	D23 MAD[11]	D24 MAD[7]	D25 MAD[8]	D26 MAD[6]
E14 RX_VDD2	E15 N/C	E16 N/C	E17 N/C	E18 TXB_VDD1	E19 RXB_VDD1	E20 RXB_VSS1	E21 VSS2	E22 VDDIO33	E23 VSS2	E24 MAD[5]	E25 MAD[9]	E26 MOE[1]/
				F18 RX_VSS1	F19 TXB_VDD0	F20 RX_VSS0	F21 ISTW_ DATA	F22 ISTW_CLK	F23 MAD[1]	F24 VDDIO33	F25 VSS2	F26 REFCLK_P
					G19 RXB_VDD0	G20 RXB_VSS0	G21 MADP[0]	G22 N/C	G23 MAD[2]	G24 VDDIO33	G25 VSS2	G26 NVSRAM_ CS/
						H20 VSS2	H21 MAD[12]	H22 N/C	H23 MAD[13]	H24 MAD[15]	H25 MWE[1]/	H26 FLASH_ CS/
							J21 N/C	J22 REFCLK_N	J23 N/C	J24 PSBRAM_ CS/	J25 BWE[2]/	J26 MADP[1]
								K22 N/C	K23 VDDIO33	K24 MAD[14]	K25 N/C	K26 TDIODE_N
								L22 N/C	L23 VSS2	L24 VDDIO33	L25 VSS2	L26 MWE[0]/
M14 VSS2	M15 VDD2							M22 MOE[0]/	M23 TDIODE_P	M24 VDDIO33	M25 VSS2	M26 BWE[1]/
N14 VDD2	N15 VSS2							N22 BWE[0]/	N23 N/C	N24 N/C	N25 BWE[3]/	N26 MCLK
P14 VSS2	P15 VDD2							P22 N/C	P23 ADSC/	P24 VDDIO33	P25 VSS2	P26 MADP[2]
R14 VDD2	R15 VSS2							R22 MAD[29]	R23 MAD[21]	R24 VDDIO33	R25 VSS2	R26 MAD[19]
								T22 MAD[23]	T23 VDDIO33	T24 MAD[18]	T25 N/C	T26 MAD[17]
								U22 N/C	U23 VSS2	U24 MAD[24]	U25 MAD[20]	U26 ADV/
							V21 BZR_SET	V22 N/C	V23 N/C	V24 MAD[27]	V25 MAD[26]	V26 MAD[16]
						W20 AD[37]	W21 N/C	W22 N/C	W23 MADP[3]	W24 VDDIO33- PCIX	W25 VSS2	W26 MAD[28]
					Y19 VSS2	Y20 AD[41]	Y21 N/C	Y22 AD[36]	Y23 VDDIO5- PCIX	Y24 VDDIO33- PCIX	Y25 VSS2	Y26 MAD[22]
				AA18 N/C	AA19 AD[49]	AA20 AD[46]	AA21 VDDIO5- PCIX	AA22 VSS2	AA23 AD[35]	AA24 BZVDD	AA25 MAD[30]	AA26 MAD[25]
AB14 VDDIO5- PCIX	AB15 N/C	AB16 N/C	AB17 PAR64	AB18 VDDIO5- PCIX	AB19 AD[53]	AB20 VDDIO5- PCIX	AB21 AD[44]	AB22 VDDIO33- PCIX	AB23 VDDIO33- PCIX	AB24 AD[32]	AB25 AD[38]	AB26 MAD[31]
AC14 N/C	AC15 N/C	AC16 VSS2	AC17 VDDIO33- PCIX	AC18 N/C	AC19 AD[61]	AC20 AD[45]	AC21 N/C	AC22 VSS2	AC23 AD[48]	AC24 AD[40]	AC25 AD[39]	AC26 AD[33]
AD14 AD[2]	AD15 VDDIO33- PCIX	AD16 VDDIO33- PCIX	AD17 VDDIO5- PCIX	AD18 REQ64/	AD19 C_BE[5]/	AD20 VDDIO33- PCIX	AD21 VDDIO33- PCIX	AD22 AD[54]	AD23 AD[55]	AD24 AD[42]	AD25 AD[47]	AD26 AD[34]
AE14 N/C	AE15 VSS2	AE16 VSS2	AE17 AD[1]	AE18 ACK64/	AE19 C_BE[7]/	AE20 VSS2	AE21 VSS2	AE22 AD[58]	AE23 AD[59]	AE24 AD[51]	AE25 AD[50]	AE26 VSS2
AF14 AD[0]	AF15 AD[3]	AF16 AD[5]	AF17 C_BE[6]/	AF18 C_BE[4]/	AF19 AD[63]	AF20 AD[62]	AF21 AD[60]	AF22 AD[56]	AF23 AD[57]	AF24 AD[52]	AF25 AD[43]	

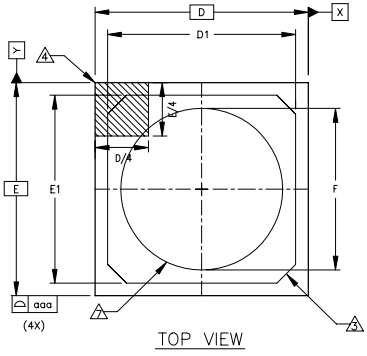
5.5 Package Drawings

The LSISAS1064 is packaged in a 472-EPBGA-T package with a 27 mm x 27 mm footprint and 1.0 mm ball pitch. The package code is UO. The package drawing number is JZ02-000015-00. Figure 5.9 provides the package diagram for the LSISAS1064.

Figure 5.9 472-Pin EPBGA-T (UO) Mechanical Drawing (Sheet 1 of 3)

REVISIONS

APPROVAL	DATE	DESCRIPTION	REV
C.FISHLEY	01–24–02	INITIAL RELEASE	0
C.FISHLEY	03–20–02	REVISE DIMENSION (ddd)	1
R.MENDOZA	01–29–03	ADD PACKAGE (4E)	2
C.FISHLEY	06–04–03	ADD PACKAGE (6I)	3
C.FISHLEY	06–25–03	ADD PACKAGE (61)	4
WK Liew	10–06–03	ADD PACKAGE (4X) (5E) (HT)	5
L. MORA	03–24–04	ADD PACKAGE (5Y)	6
WK Liew	07–02–04	ADD PACKAGE (8C)	7
C. Fishley	08–13–04	ADD PACKAGE (uo, 3w, ow, 82)	8



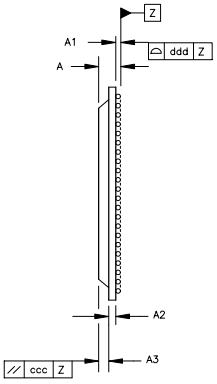


TABLE 1: COMMON DIMENSIONS			
SYM	MIN	NOM	MAX
A	–	–	2.50
A1	0.40	–	–
A2	0.25	–	0.70
A3	–	–	1.25
b	0.50	–	0.70
D		27.00 BSC	
D1	23.00	–	25.00
E		27.00 BSC	
E1	23.00	–	25.00
e		1.00 BSC	
F	19.50	–	21.50

TABLE 2: TOLERANCES OF FORM AND POSITION	
DIMENSION	e = 1.00
aaa	0.20
ccc	0.35
ddd	0.15
eee	0.25
fff	0.10

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

2 ALL DIMENSIONS IN MM.

3 CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.

4 DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

5 JEDEC CODE MS–034.

6 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

7 HEAT SPREADER OUTLINE.

LSI LOGIC CORPORATION
1551 McCARTHY BLVD. MILPITAS, CA. 95035

TITLE: 27x27mm EPBGA–T, EPBGA–HP
1.00 BALL PITCH

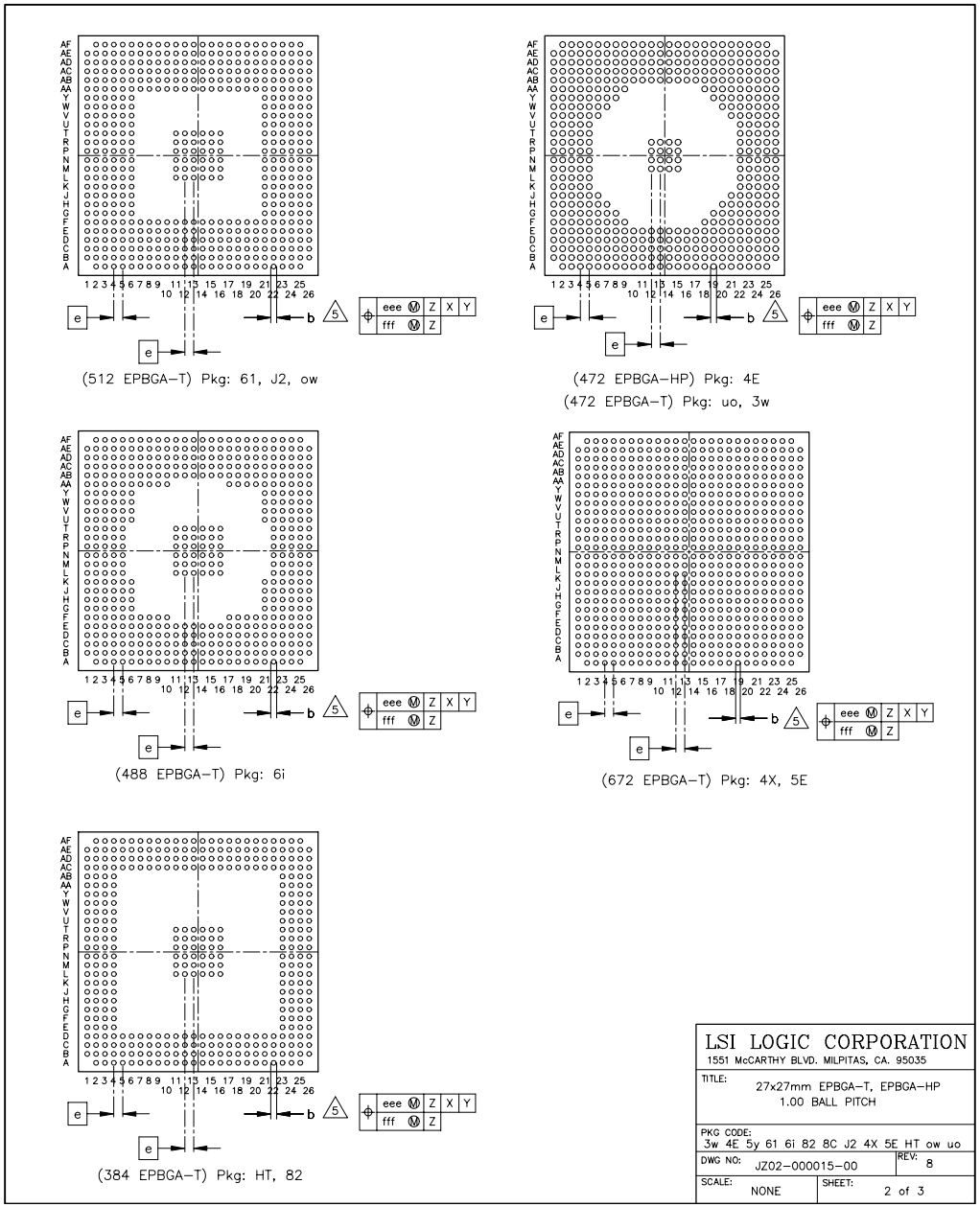
PKG CODE: 3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo

DWG NO: JZ02–000015–00 REV: 8

SCALE: NONE SHEET: 1 of 3

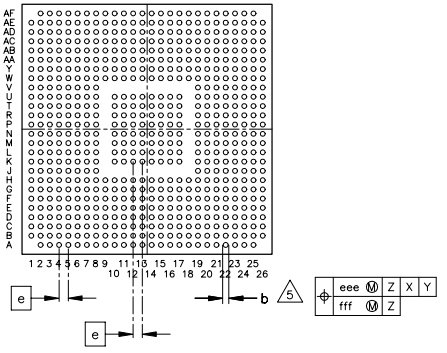
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

Figure 5.9 472-Pin EPBGA-T (UO) Mechanical Drawing (Sheet 2 of 3) (Cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

Figure 5.9 472-Pin EPBGA-T (UO) Mechanical Drawing (Sheet 3 of 3) (Cont.)



LSI LOGIC CORPORATION 1551 McCARTHY BLVD. MILPITAS, CA. 95035	
TITLE: 27x27mm EPBGA–T, EPBGA–HP 1.00 BALL PITCH	
PKG CODE: 3w 4E 5y 61 6i 82 8C J2 4X 5E HT ow uo	
DWG NO: JZ02–000015–00	REV: 8
SCALE: NONE	SHEET: 3 of 3

Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code UO.**

Appendix A
Register Summary

Tables A.1, A.2, and A.3 provide a register summary.

Table A.1 LSISAS1064 PCI Configuration Space Registers

Register Name	Offset[1]	Read/Write	Page
Vendor ID	0x00–0x01	Read Only	4-3
Device ID	0x02–0x03	Read Only	4-3
Command	0x04–0x05	Read/Write	4-3
Status	0x06–0x07	Read/Write	4-5
Revision ID	0x08	Read/Write	4-7
Class Code	0x09–0x0B	Read Only	4-7
Cache Line Size	0x0C	Read/Write	4-8
Latency Timer	0x0D	Read/Write	4-8
Header Type	0x0E	Read Only	4-9
Reserved	0x0F	Reserved	4-9
I/O Base Address	0x10–0x13	Read/Write	4-9
Memory [0] Low	0x14–0x17	Read/Write	4-10
Memory [0] High	0x18–0x1B	Read/Write	4-10
Memory [1] Low	0x1C–0x1F	Read/Write	4-11
Memory [1] High	0x20–0x23	Read/Write	4-11
Reserved	0x24–0x27; 0x28–0x2B	Reserved	4-12
Subsystem Vendor ID	0x2C–0x2D	Read Only	4-12
Subsystem ID	0x2E–0x2F	Read Only	4-13

Table A.1 LSISAS1064 PCI Configuration Space Registers (Cont.)

Register Name	Offset[1]	Read/Write	Page
Expansion ROM Base Address	0x30–0x33	Read/Write	4-13
Capabilities Pointer	0x34	Read Only	4-14
Reserved	0x35–0x37; 0x38–0x3B	Reserved	4-15
Interrupt Line	0x3C	Read/Write	4-15
Interrupt Pin	0x3D	Read Only	4-16
Minimum Grant	0x3E	Read Only	4-16
Maximum Latency	0x3F	Read Only	4-16
Power Management Capability ID	–	Read Only	4-17
Power Management Next Pointer	–	Read Only	4-17
Power Management Capabilities	–	Read Only	4-17
Power Management Control/Status	–	Read/Write	4-18
Power Management Bridge Support Extensions	–	Read Only	4-19
Power Management Data	–	Read Only	4-20
MSI Capability ID	–	Read Only	4-20
MSI Next Pointer	–	Read Only	4-20
MSI Message Control	–	Read/Write	4-21
MSI Message Lower Address	–	Read/Write	4-22
MSI Message Upper Address	–	Read/Write	4-23
MSI Message Data	–	Read/Write	4-23
MSI Mask Bits	–	Read/Write	4-24
MSI Pending Bits	–	Read Only	4-24
MSI-X Capability ID	–	Read Only	4-24
MSI-X Next Pointer	–	Read Only	4-25
MSI-X Message Control	–	Read/Write	4-25

Table A.1 LSISAS1064 PCI Configuration Space Registers (Cont.)

Register Name	Offset[1]	Read/Write	Page
MSI-X Table Offset	–	Read Only	4-26
MSI-X PBA Offset	–	Read Only	4-27
PCI-X Capability ID	–	Read Only	4-27
PCI-X Next Pointer	–	Read Only	4-28
PCI-X Command	–	Read/Write	4-28
PCI-X Status	–	Read/Write	4-30

1. The offset of the PCI extended capabilities registers can vary. Access these registers through the Next Pointer and Capability ID registers.

Table A.2 LSISAS1064 PCI I/O Space Registers

Register Name	Offset	Read/Write	Page
System Doorbell	0x00	Read/Write	4-34
Write Sequence	0x04	Read/Write	4-34
Host Diagnostic	0x08	Read/Write	4-35
Test Base Address	0x0C	Read/Write	4-37
Diagnostic Read/Write Data	0x10	Read/Write	4-37
Diagnostic Read/Write Address	0x14	Read/Write	4-38
Reserved	0x18–0x2F	Reserved	–
Host Interrupt Status	0x30	Read/Write	4-38
Host Interrupt Mask	0x34	Read/Write	4-39
Reserved	0x38–0x3F	Reserved	–
Request Queue	0x40	Read/Write	4-40
Reply Queue	0x44	Read/Write	4-41
High Priority Request MFA Queue	0x48	Read/Write	4-41

Table A.3 LSISAS1064 PCI Memory [0] Space Registers

Register Name	Offset	Read/Write	Page
System Doorbell	0x00	Read/Write	4-34
Write Sequence	0x04	Read/Write	4-34
Host Diagnostic	0x08	Read/Write	4-35
Test Base Address	0x0C	Read/Write	4-37
Reserved	0x10–0x2F	Reserved	–
Host Interrupt Status	0x30	Read/Write	4-38
Host Interrupt Mask	0x34	Read/Write	4-39
Reserved	0x38–0x3F	Reserved	–
Request Queue	0x40	Read/Write	4-40
Reply Queue	0x44	Read/Write	4-41
High Priority Request MFA Queue	0x48	Read/Write	4-41

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