LSISAS1064E PCI Express to 4-Port Serial Attached SCSI Controller

Datasheet

Version 2.0

The LSISAS1064E is a four-port, 3.0 Gbit/s SAS/SATA controller that is compliant with the Fusion-MPT™ (Message Passing Technology) architecture, provides an eight-lane PCI Express interface, and supports Integrated RAID™ technology. The PCI Express software is backward compatible with previous revisions of the PCI bus and PCI-X bus. The LSISAS1064E supports the *PCI Express Base Specification, Revision 1.0a,* and the ANSI *Serial Attached SCSI Standard, Revision 1.1*. Figure 1 and Figure 2 provide examples of LSISAS1064E applications.

The point-to-point interconnect feature of the PCI Express bus limits the electrical load on links, allowing increased transmission and reception frequencies. The PCI Express transmission and reception data rates for each full-duplex interconnect is 2.5 Gbits/s. The LSISAS1064E has eight PCI Express phys, which provide host-side possible maximum transmission and reception rates of 4.0 Gbytes/s. The LSISAS1064E supports x8, x4, and x1 PCI Express link widths, and automatically downshifts if plugged into either a x4 connector or into a x8 connector that is wired as a x4 connector. The serial PCI Express interconnect between devices lowers the number of pins per device, which reduces both the PCI Express board design costs and the overall board design complexity. The serial connection also makes the PCI Express performance highly scalable.

Figure 1 LSISAS1064E Direct-Connect Example

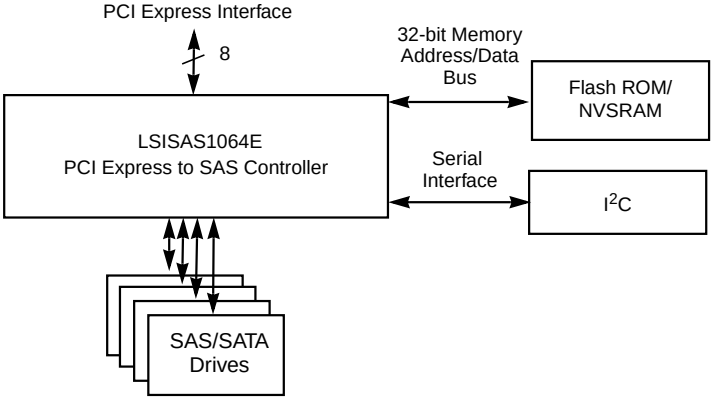
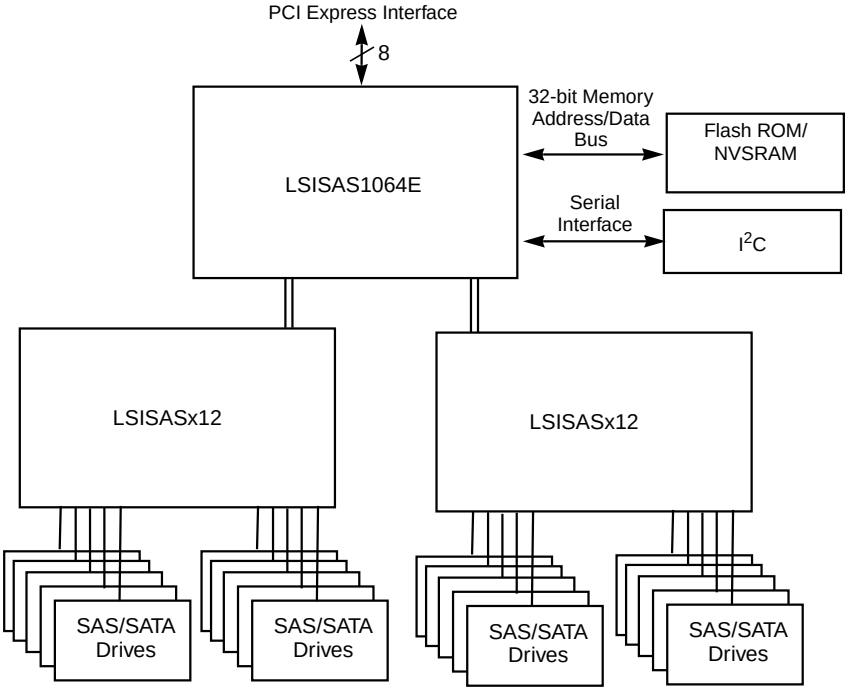


Figure 2 LSISAS1064E Controller and LSISASx12 Expander Example



PCI Express implements a switch-based technology to interconnect a large number of devices. Communication over the serial interconnect is accomplished using packet-based communication protocol. Quality of Service (QOS) features provide differentiated transmission performance for different applications. Hot Plug/Hot Swap support enables “always-on” systems. Enhanced error handling features, such as end-to-end CRC (ECRC) and Advanced Error Reporting, make PCI Express suitable for robust, high-end server applications. Hot Plug, power management, error handling, and interrupt signaling are accomplished using packet-based messaging rather than sideband signals. This keeps the device pin count low and reduces the system cost.

Each of the four SAS phys on the LSISAS1064E is capable of SAS/SATA link rates of 3.0 Gbits/s and 1.5 Gbits/s. The user can configure ports as wide or narrow. Narrow ports have one phy per port. Wide ports have two, three, or four phys per port. Each port supports the SSP, SMP, STP, and SATA protocols.

The SAS interface uses the proven SCSI command set to ensure reliable data transfers, while providing the connectivity and flexibility of point-to-point serial data transfers. The SAS interface provides improved performance, simplified cabling, smaller connectors, lower pin count, and lower power requirements when compared to parallel SCSI. SAS controllers leverage an electrical and physical connection interface that is compatible with SATA technology.

The LSISAS1064E supports the Integrated RAID solution, which is a highly integrated, low cost RAID implementation. It is designed for systems requiring redundancy and high availability, but not needing a full-featured RAID implementation. Integrated RAID technology supports up to two volumes and ten drives. Each volume can contain up to eight drives. The Integrated RAID solution includes Integrated Mirroring™ (IM) technology, Integrated Mirroring Enhanced (IME), and Integrated Striping™ (IS) technology. IM provides physical mirroring of two physical drives, plus a hot spare drive. IME supports 3–8 drives plus a hot spare drive. IM and IME require an NVSRAM to support write journaling. IS enables data striping across up to eight physical drives. The Integrated RAID solution is OS independent, easy to install and configure, supports up to eight drives at RAID Level 0, and does not require a special driver. The run-time operation of the Integrated RAID solution is transparent to the operating system. A single firmware build supports all Integrated RAID capabilities.

The LSISAS1064E uses the Fusion-MPT architecture, which features a performance based message passing protocol that offloads the host CPU by completely managing all I/Os and minimizes system bus overhead by coalescing interrupts. The proven Fusion-MPT architecture requires only thin, easy-to-develop device drivers that are independent of the I/O bus. LSI Logic provides these device drivers.

To meet its flexibility and data transfer requirements, the LSISAS1064E uses an ARM966 processor that operates at 225 MHz. LSI manufactures the LSISAS1064E using Gflx™ technology.

Features

This section lists the features of the LSISAS1064E.

SSP and SAS Features

This section describes the SSP and SAS features.

- Each phy supports 3.0 Gbit/s and 1.5 Gbit/s SAS data transfers
- Provides a serial, point-to-point, enterprise-level storage interface
- Supports wide transfers consisting of two, three, or four phys
- Supports narrow ports consisting of a single phy
- Transfers data using SCSI information units
- Is compatible with SATA target devices

SATA and STP Features

This section describes the SATA and STP features.

- Each phy supports 3.0 Gbit/s and 1.5 Gbit/s SATA data transfers
- Each phy supports 3.0 Gbit/s and 1.5 Gbit/s STP data transfers
- Allows addressing of multiple SATA targets through an expander
- Allows multiple initiators to address a single target (in a fail-over configuration) through an expander

PCI Express Features

The LSISAS1064E supports these PCI Express features.

- Provides eight PCI Express phys
- Supports a single-phy (1 lane) link transfer rate up to 2.5 Gbits/s in each direction
- Supports x8, x4, and x1 link widths
- Automatically downshifts to a x4 link width if plugged into a x4 connector or into a x8 connector that is wired as a x4 connector

- Provides a scalable interface
  - Single-lane aggregate bandwidth of up to 0.5 Gbytes/s (500 Mbytes/s)
  - Quad-lane aggregate bandwidth of up to 2.0 Gbytes/s (2000 Mbytes/s)
  - 8-lane aggregate bandwidth of up to 4.0 Gbytes/s (4000 Mbytes/s)
- Offers a maximum payload of 2 Kbytes
- Supports serial, point-to-point interconnections between devices
  - Reduces the electrical load of the connection
  - Enables higher transmission and reception frequencies
- Supports lane reversal and polarity inversion
- Supports PCI Express Hot Plug
- Supports Power Management
  - Supports the PCI Power Management 1.2 specification
  - Supports Active State Power Management, including the L0, L0s, and L1 states, by placing links in a power-savings mode during times of no link activity
- Uses a packetized and layered architecture
- Achieves a high bandwidth per pin with low overhead and low latency
- PCI Express is software compatible with PCI and PCI-X software
  - Leverages existing PCI device drivers
  - Supports the Memory, I/O, and Configuration address spaces
  - Supports memory read/write transactions, I/O read/write transactions, and configuration read/write transactions
- Provides 4 Kbytes of PCI Configuration address space per device
- Supports posted and nonposted transactions
- Provides quality of service (QOS) link configuration and arbitration policies
- Supports Traffic Class 0 and one virtual channel
- Supports Message Signaled Interrupts (both MSI and MSI-X) as well as INTx interrupt signaling for legacy PCI support
- Supports end-to-end CRC (ECRC) and Advanced Error Reporting

Integration

These features make the LSISAS1064E easy to integrate:

- Leverages the proven Fusion-MPT technology
- PCI Express device can use PCI-based device drivers, which reduces integration challenges and risks
- Provides unequaled performance through the Fusion-MPT architecture
- Reduces time to market with the Fusion-MPT architecture
  - Single driver binary for SAS/SATA, Ultra320 SCSI, and Fibre Channel products
  - One firmware build supports all Integrated RAID capabilities
  - Thin, easy to develop drivers
  - Reduced integration and certification effort

Usability

These usability features are incorporated into the design:

- Simplifies cabling with point-to-point, serial architecture
- Provides drive spin-up sequencing control
- Provides up to two LED signals for each SAS/SATA phy to indicate drive activity and faults
- Provides a serialized general purpose I/O (SGPIO) interface

Flexibility

These features increase the flexibility of the LSISAS1064E:

- Supports an 8-bit flash ROM interface and an 8-bit nonvolatile RAM (NVSRAM) interface
- Offers a flexible programming interface to tune I/O performance
- Allows mixed connections to SAS or SATA targets
- Allows a grouping of up to four phys in a wide port
- Leverages compatible connectors for SAS and SATA connections

- Supports Integrated RAID technology, which provides for Integrated Mirroring technology and/or Integrated Striping technology
- Provides 17 LED signals
- Provides four independent GPIO signals

Reliability

These features enhance the reliability of the LSISAS1064E:

- Uses proven GigaBlaze® transceivers on both the SAS/SATA phys and the PCI Express phys
- Isolates the power and ground of I/O pads and internal chip logic
- Provides ESD protection
- Provides latch-up protection
- Has a high proportion of power and ground pins
- Integrated Mirroring technology provides physical mirroring of the boot volume

Testability

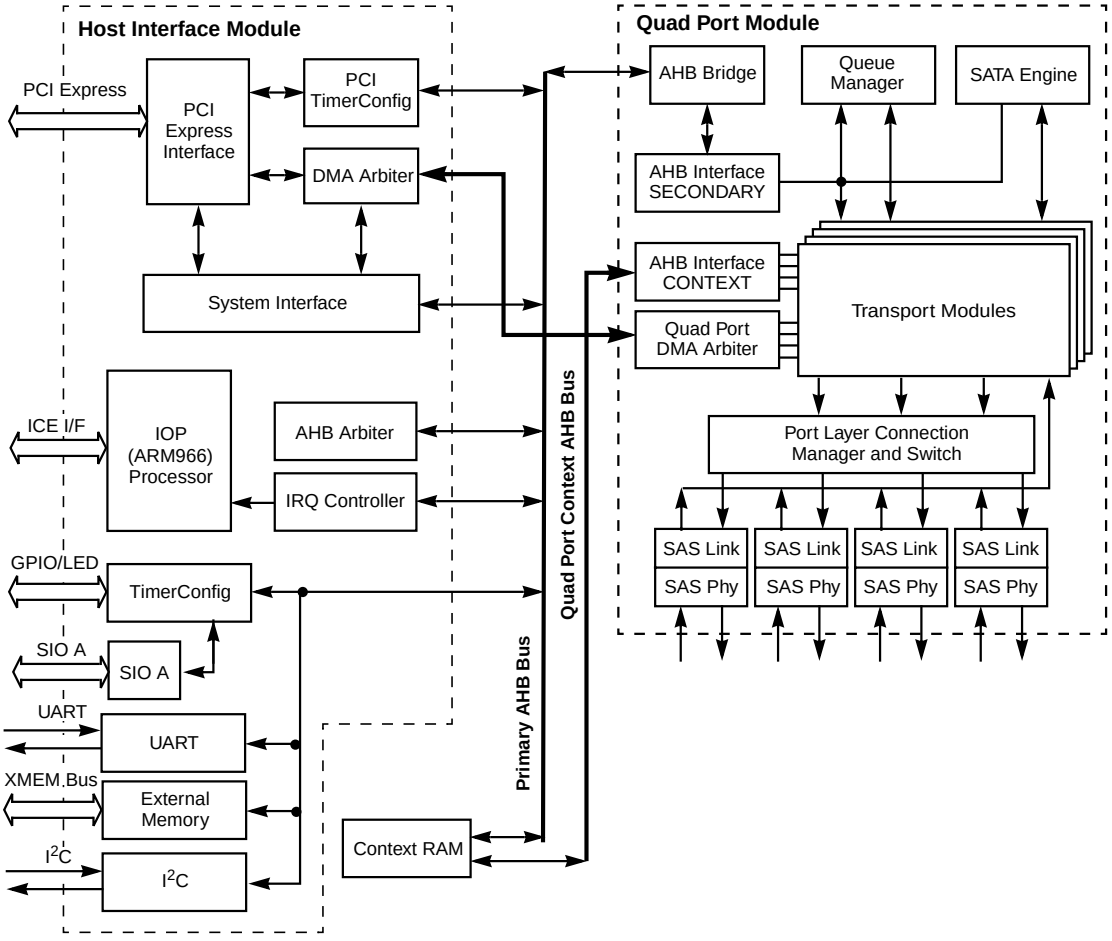
These features enhance the testability of the LSISAS1064E:

- Offers JTAG boundary scan
- Offers ARM® Multi-ICE® technology for debugging the ARM966 processor

Block Diagram Description

Figure 3 provides the block diagram for the LSISAS1064E. The following subsections discuss the block diagram. There is a single Host Interface module and a Quad Port module. The Host Interface module supports the 8-lane PCI Express interface. The Quad Port module supports four SAS phys.

Figure 3 LSISAS1064E Block Diagram



Host Interface Module

The LSISAS1064E interfaces with the host through the host interface module. The host interface module contains the PCI Express interface, system interface, IOP (ARM966) processor, timer and configuration, DMA arbiter, PCI timer and configuration, SIO, external memory, I^2C, and UART blocks.

PCI Express Interface

The PCI Express interface block supports an 8-lane PCI Express interface. This is a high bandwidth, serial interface that features point-to-point interconnects between devices and an advanced packetized and layered protocol architecture. The PCI Express software is backward compatible with previous implementations of the PCI specification.

System Interface

In combination with the IOP, the system interface supports the Fusion-MPT architecture. The system interface efficiently passes messages between the LSISAS1064E and the host interface using a high-performance, packetized mailbox architecture. The LSISAS1064E system interface takes advantage of PCI Express point-to-point connections, thereby allowing a dedicated connection to each device with no sharing.

IOP (ARM966) Processor

The LSISAS1064E I/O processor (IOP) controls the system interface and manages the host side of the Fusion-MPT architecture without host processor intervention, which frees the host processor for other tasks.

Timer and Configuration

This block supports the LSISAS1064E LED and GPIO interfaces. There are nine LED signals. The GPIO interface contains four independent GPIO signals. This block also supports internal timing adjustments and power-on sense configuration options.

DMA Arbiter

The LSISAS1064E provides the ability to transfer system memory blocks to and from local memory through the descriptor-based DMA arbiter and router. The DMA channel includes a system DMA FIFO and the internal bus interface logic.

PCI Timer and Configuration

This PCI timer and configuration module supports the PCI configuration register space and a power-on reset (POR).

SIO

The LSISAS1064E provides an SGPIO interface that is compliant with the SFF-8485 specification. A typical use of the serial I/O (SIO) module is to provide control of LEDs. The SIO module is SFF-8485 compliant.

External Memory

The external memory controller block provides an interface for flash ROM and NVSRAM devices. The external memory bus provides a 32-bit memory bus, parity checking, and chip select signals for NVSRAM and flash ROM. The flash ROM and NVSRAM are capable of 8-bit accesses.

Typical system configurations require a flash ROM to store firmware, configuration information, and persistent data information.

I^2C

The LSISAS1064E contains an Inter-IC (I^2C) block that communicates with peripherals. The I^2C block operates as either a master or a slave on the bus and sustains data rates up to 400 Kbits/s. The I^2C block accomplishes byte-wise bidirectional data transfers by using either an interrupt or a polling handshake at the completion of each byte. The I^2C block controls all bus timing and performs bus-specific sequences.

UART

The UART provides test and debug access to the LSISAS1064E.

Quad Port Module

The Quad Port module in the LSISAS1064E implements the SSP, SMP, and STP/SATA protocols, and manages the SAS/SATA phys. The Quad Port module supports four phys. The following subsections describe the Quad Port module.

Transport Modules

The transport modules transmit frames to and from the port layer and implement the STP, SSP, and SMP protocols. The Quad Port module has four instances of the transport module, one for each SAS/SATA phy on the LSISAS1064E. The transport modules also manage DMA transfers.

Queue Manager

The queue manager is responsible for managing various queue structures that support the SSP, SMP, and SATA/STP protocols. The queue structures are the primary means for the IOP to initiate I/Os to the hardware, and for the hardware to notify the IOP of I/O status.

SATA Engine

The SATA engine provides information to the transport modules to enable handling of SATA commands. The SATA engine tracks queued commands per device and provides these tags to the SATA transport layer blocks.

Port Layer Connection Manager and Switch

The port layer connection manager and switch handles transmission requests from the transport modules and originates connection requests to the SAS links. It is also responsible for handling SAS wide port configurations.

SAS Link

The SAS link layer manages SAS connections between initiator and target ports, data clocking, and CRC checking on transmitted data. The SAS link is also responsible for starting a link reset sequence.

SAS Phys

The SAS phys interface to the physical layer, perform serial-to-parallel conversion of received data and parallel-to-serial conversion of transmit data, manage phy reset sequences, and perform 8b/10b encoding.

Quad Port DMA Arbiter

The quad port arbiter interfaces with the host interface DMA arbiter and determines bus priority between the quad port phys for DMA transfers.

Context RAM

The context RAM is a memory that is shared between the host interface module and the quad port module. The context RAM holds a portion of the firmware.

Signal Descriptions

The following subsections provide the signal descriptions for the LSISAS1064E. A '/' following the signal indicates an active LOW signal.

PCI Express Signals

This section describes the PCI Express signals. Refer to the PCI Express specification for detailed signal descriptions.

PCI Express System Signals

This section describes the PCI Express system signals.

P_REFCLK_P PCI Express Differential Clock **Input**
This signal provides half of the PCI Express differential clock input signal.

P_REFCLK_N PCI Express Differential Clock **Input**
This signal provides half of the PCI Express differential clock input signal.

RST/ Reset **Input**
Asserting the RST/ signal causes a reset.

PCI Express Data Signals

This section describes the PCI Express transmit and receive signals.

P_RX[7:0]+ PCI Express Receive Differential Data **Input**
P_RX[x]+ provides the positive differential data receiver for PCI Express phy[x].

P_RX[7:0]– PCI Express Receive Differential Data **Input**
P_RX[x]– provides the negative differential data receiver for PCI Express phy[x].

P_TX[7:0]+ PCI Express Transmit Differential Data **Output**
P_TX[x]+ provides the positive differential data transmitter for PCI Express phy[x].

P_TX[7:0]– PCI Express Transmit Differential Data **Output**
P_TX[x]– provides the negative differential data transmitter for PCI Express phy[x].

SAS Signals

This section describes the SAS interface signals.

REFCLK_P, REFCLK_N **Input**
These pins provide the serial differential clock. Connect a 75 MHz oscillator with an accuracy of at least 50ppm to these pins. To use a single-ended crystal, tie the crystal to REFCLK_P and tie REFCLK_N to a resistor termination.

RTRIM **Resistor Reference** **Analog**
This pin provides the analog resistor reference for the GigaBlaze transceivers. The resistor provides a reference to calibrate the 50 Ω termination.

RX[3:0]– **Receive Negative Differential Data** **Input**
RX[x]– provides the negative differential data receiver for SAS/SATA phy[x].

RX[3:0]+ **Receive Positive Differential Data** **Input**
RX[x]+ provides the positive differential data receiver for SAS/SATA phy[x].

TX[3:0]– **Transmit Negative Differential Data** **Output**
TX[x]– provides the negative differential data transmit signal for SAS/SATA phy[x].

TX[3:0]+ **Transmit Positive Differential Data** **Output**
TX[x]+ provides the positive differential data transmit signal for SAS/SATA phy[x].

I^2C and UART Signals

This section describes the I^2C and UART signals.

ISTWI_CLK **I^2C Clock** **Input/Output**
This signal provides the I^2C clock signal.

ISTWI_DATA **I^2C Data** **Input/Output**
This signal provides the I^2C data signal.

UART_RX **UART Receive** **Input**
This signal provides the UART receive signal.

UART_TX	**UART Transmit**	**Output**
	This signal provides the UART transmit signal.	

Memory Interface Signals

This section describes the memory interface signals.

MCLK	**Memory Clock**	**Output**
	All synchronous RAM control/data signals reference the rising edge of this clock.	
ADSC/	**Address-Strobe-Controller**	**Output**
	Asserting this active LOW signal initiates read, write, or chip deselect cycles.	
ADV/	**Advance**	**Output**
	Asserting this active LOW signal increments the burst address counter of the selected synchronous SRAM.	
MAD[31:0]	**Multiplexed Address/Data**	**Input/Output**
	These signals provide the address and data bus for the flash ROM and NVSRAM. These signals also provide Power-On Sense configuration functions to the LSISAS1064E. These signals are internally pulled LOW.	
MADP[3:0]	**Memory Parity**	**Input/Output**
	These signals provide parity checking for MAD[31:0]. These signals are internally pulled HIGH.	
MOE[1:0]/	**Memory Output Enables**	**Output**
	Asserting these active LOW signals enable the selected flash ROM or NVSRAM device to drive data. MOE1/ enables flash ROM devices. MOE0/ enables NVSRAM devices.	
MWE[1:0]/	**Memory Write Enables**	**Output**
	The MWE[1:0]/ signals provide memory enable signals.	
BWE[3:0]/	**Memory Byte Write Enables**	**Output**
	BWE[3]/ and BWE[2]/ enable partial word writes to the flash ROM and the NVSRAM if FLASH_CS/ or NVSRAM_CS/ is asserted.	

NVSRAM_CS/
NVSRAM Chip Select **Output**
Asserting this active LOW signal selects the NVSRAM device.

FLASH_CS/ **Flash Chip Select** **Output**
Asserting this active LOW signal selects the flash ROM. The LSISAS1064E maps flash ROM address space into system memory space.

SIO Signals

This section describes the SIO signals.

SIO_CLK_A **SIO Clock** **Input/Output**
This signal provides the clock signal for SIO A.

SIO_DIN_A **SIO Data In A** **Input**
This signal provides the data input signal to SIO A.

SIO_DOUT_A **SIO Data Out A** **Output**
This signal provides the data output signal to SIO A and can control the Quad Port LED drives.

SIO_END_A **SIO End Control** **Input/Output**
The SIO module drives this output to end control of the SIO bus.

Configuration and General Purpose Signals

This section describes the configuration and general purpose pins.

TST_RST/ **Test Reset** **Input**
Asserting this signal forces the chip into a Power-On-Reset (POR) state. This signal has an internal pull-up. The LSISAS1064E does *not* have an internal POR.

REFCLK_B **ARM Reference Clock** **Input**
This pin provides the ARM reference clock.

MODE[7:0] **Mode Select** **Input**
This 8-bit bus defines operational and test modes for the chip. These pins have internal pull-downs.

FAULT_LED[3:0]/
Fault LED **Input/Output**
These output signals indicate a SAS link fault.

ACTIVE_LED[3:0]/
Activity LED **Input/Output**
These output signals indicate SAS link activity.

GPIO[3:0] **General Purpose I/O** **Input/Output**
These signals provide general purpose input/output signals. These signals have internal pull-ups.

HB_LED/ **Heartbeat LED** **Output**
Firmware intermittently asserts this signal to indicate that the IOP is operational.

JTAG and Test Signals

This section describes the JTAG and test signals.

FSELA	**Clock Select**	**Input**
	This is a test signal. Pull this signal LOW.	
SCAN_ENABLE	**Scan Enable**	**Input**
SCAN_MODE	**Scan Mode**	**Input**
TCK	**JTAG Debug Clock**	**Input**
TRST/	**JTAG Debug Reset**	**Input**
TDI	**JTAG Debug Test Data In**	**Input**
TDO	**JTAG Debug Test Data Out**	**Output**
TMS	**JTAG Debug Test Mode Select**	**Input**
TCK_ICE	**Multi-ICE Debug Clock**	**Input**
RTCK_ICE	**Multi-ICE Debug Return Clock**	**Output**
TRST_ICE/	**Multi-ICE Debug Reset**	**Input**
TDI_ICE	**Multi-ICE Debug Test Data In**	**Input**
TDO_ICE	**Multi-ICE Debug Test Data Out**	**Output**

TMS_ICE	**Multi-ICE Debug Test Mode Select**	**Input**
IDDT	**IDDQ Test Mode Enable** This signal is active HIGH.	**Input**
TN/	**3-State Output Enable Control** This signal is active LOW.	**Input**
PROCMON	**Process Monitor Test Output Driver**	**Output**
TDIODE_P	**Anode Connection of the Thermal Diode**	**Input**
TDIODE_VSS	**Cathode Connection of the Thermal Diode**	**Output**

Power and Ground Signals

This section describes the power and ground signals.

REFPLL_VDD **Power**
These signals provide 1.2 V power.

REFPLL_VSS **Ground**
These signals provide ground.

VDD2 **Power**
These signals provide 1.2 V core power.

VDDIO33 **Power**
These signals provide 3.3 V I/O power.

VSS **Ground**
These signals provide ground.

RX_VSS[3:0], RXB_VSS[3:0], TX_VSS[3:0], TXB_VSS[3:0] **Ground**
These signals provide ground for the SAS GigaBlaze core.

RX_VDD[3:0], RXB_VDD[3:0], TX_VDD[3:0], TXB_VDD[3:0] **Power**
These signals provide 1.2 V power for the SAS GigaBlaze core.

P_RX_VDD[7:0], P_RXB_VDD[7:0], P_TX_VDD[7:0], P_TXB_VDD[7:0] **Power**
These signals provide 1.2 V power for the PCI Express GigaBlaze core.

P_RX_VSS[7:0], P_RXB_VSS[7:0], P_TX_VSS[7:0], P_TXB_VSS[7:0] **Ground**

These signals provide ground for the PCI Express GigaBlaze core.

Pin Listing

Table 1 provides the signal listing by signal name. Table 2 provides the signal listing by pin name. Figure 4 provides a BGA diagram.

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Table 1 LSISAS1064E Pin Assignments Listed by Signal Name[1]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACTIVE_LED[0]/	H1	N/C	E1	N/C	AC24	P_TX2-	AF5	RX_VSS3	F15
ACTIVE_LED[1]/	H2	N/C	E3	N/C	AD1	P_TX2+	AF6	RX0-	B25
ACTIVE_LED[2]/	G1	N/C	E13	N/C	AD3	P_TX3-	AE9	RX0+	B24
ACTIVE_LED[3]/	H3	N/C	E22	N/C	AD13	P_TX3+	AF9	RX1-	B21
ADSC/	V22	N/C	E23	N/C	AE3	P_TX4-	AF15	RX1+	B20
ADV/	V23	N/C	E24	N/C	AE13	P_TX4+	AF16	RX2-	A20
BWE[0]/	T21	N/C	F1	N/C	AF13	P_TX5-	AF18	RX2+	A19
BWE[1]/	U24	N/C	F6	NVSRAM_CS/	N26	P_TX5+	AE18	RX3-	B17
BWE[2]/	R23	N/C	F22	P_REFCLK_N	AD14	P_TX6-	AF21	RX3+	A17
BWE[3]/	W25	N/C	F23	P_REFCLK_P	AE14	P_TX6+	AF22	RXB_VDD0	C23
FAULT_LED[0]/	N1	N/C	G20	P_RX_VDD0	AB6	P_TX7-	AE23	RXB_VDD1	C19
FAULT_LED[1]/	N3	N/C	G21	P_RX_VDD1	AC7	P_TX7+	AE22	RXB_VDD2	F17
FAULT_LED[2]/	M1	N/C	H5	P_RX_VDD2	AC9	P_TXB_VDD0	Y7	RXB_VDD3	E15
FAULT_LED[3]/	L1	N/C	H6	P_RX_VDD3	AE10	P_TXB_VDD1	AD8	RXB_VSS0	F21
FLASH_CS/	P25	N/C	H21	P_RX_VDD4	AC15	P_TXB_VDD2	AB10	RXB_VSS1	F19
FSELA	E2	N/C	H23	P_RX_VDD5	AD18	P_TXB_VDD3	AA12	RXB_VSS2	E17
GPIO[0]	V4	N/C	H25	P_RX_VDD6	AC19	P_TXB_VDD4	AF14	RXB_VSS3	G16
GPIO[1]	Y1	N/C	J1	P_RX_VDD7	AB21	P_TXB_VDD5	AA16	SCAN_ENABLE	E4
GPIO[2]	W3	N/C	J2	P_RX_VSS0	AB7	P_TXB_VDD6	AB18	SCAN_MODE	F5
GPIO[3]	AB1	N/C	J3	P_RX_VSS1	AA9	P_TXB_VDD7	AA20	SIO_CLK_A	H22
HB_LED/	P4	N/C	J4	P_RX_VSS2	AD9	P_TXB_VSS0	AC4	SIO_DIN_A	J21
IDDT	AB4	N/C	J5	P_RX_VSS3	AB12	P_TXB_VSS1	AB8	SIO_DOUT_A	D25
ISTWI_CLK	G26	N/C	J22	P_RX_VSS4	AA15	P_TXB_VSS2	AA10	SIO_END_A	E25
ISTWI_DATA	K21	N/C	K1	P_RX_VSS5	AC17	P_TXB_VSS3	AC11	TCK	AB2
MAD[0]	J26	N/C	K5	P_RX_VSS6	AA18	P_TXB_VSS4	AA14	TCK_ICE	U3
MAD[1]	H26	N/C	K6	P_RX_VSS7	AC22	P_TXB_VSS5	AB16	TDI	AC1
MAD[2]	K24	N/C	L4	P_RX0-	AF4	P_TXB_VSS6	AE19	TDI_ICE	T5
MAD[3]	J24	N/C	L5	P_RX0+	AF3	P_TXB_VSS7	AB20	TDIODE_P	V26
MAD[4]	J23	N/C	L6	P_RX1-	AE7	PROCMON	AA4	TDIODE_VSS	T22
MAD[5]	M26	N/C	L22	P_RX1+	AE6	REFCLK_B	B13	TDO	AC2
MAD[6]	M23	N/C	M5	P_RX2-	AF8	REFCLK_N	D12	TDO_ICE	V3
MAD[7]	J25	N/C	M6	P_RX2+	AE8	REFCLK_P	C13	TMS	AC3
MAD[8]	K25	N/C	M21	P_RX3-	AF11	REFPLL_VDD	D13	TMS_ICE	U4
MAD[9]	L26	N/C	M22	P_RX3+	AF10	REFPLL_VSS	A13	TN/	AD2
MAD[10]	L23	N/C	N6	P_RX4-	AE17	RESERVED	A3	TRST_ICE/	W1
MAD[11]	K23	N/C	N21	P_RX4+	AF17	RESERVED	A4	TRST/	Y4
MAD[12]	K26	N/C	N22	P_RX5-	AF20	RESERVED	A5	TST_RST/	C2
MAD[13]	N23	N/C	N25	P_RX5+	AF19	RESERVED	A6	TX_VDD0	A23
MAD[14]	R26	N/C	P2	P_RX6-	AE21	RESERVED	A8	TX_VDD1	D18
MAD[15]	P23	N/C	P6	P_RX6+	AE20	RESERVED	A9	TX_VDD2	C17
MAD[16]	V21	N/C	P21	P_RX7-	AE25	RESERVED	A10	TX_VDD3	D14
MAD[17]	Y26	N/C	P22	P_RX7+	AE24	RESERVED	A11	TX_VSS0	E19
MAD[18]	W24	N/C	P26	P_RXB_VDD0	Y8	RESERVED	B3	TX_VSS1	G18
MAD[19]	U21	N/C	R1	P_RXB_VDD1	AB9	RESERVED	B4	TX_VSS2	D16
MAD[20]	AA26	N/C	R4	P_RXB_VDD2	AD10	RESERVED	B5	TX_VSS3	E14
MAD[21]	W23	N/C	R5	P_RXB_VDD3	AF12	RESERVED	B6	TX0-	B23
MAD[22]	AA23	N/C	R6	P_RXB_VDD4	AB15	RESERVED	B7	TX0+	B22
MAD[23]	Y23	N/C	R22	P_RXB_VDD5	AA17	RESERVED	B8	TX1-	A21
MAD[24]	AB25	N/C	T6	P_RXB_VDD6	AD19	RESERVED	B9	TX1+	A22
MAD[25]	AB23	N/C	T26	P_RXB_VDD7	AD23	RESERVED	C3	TX2-	A18
MAD[26]	AB24	N/C	U1	P_RXB_VSS0	AD7	RESERVED	D24	TX2+	B18
MAD[27]	Y21	N/C	U2	P_RXB_VSS1	Y10	RESERVED	D26	TX3-	A15
MAD[28]	AC25	N/C	U5	P_RXB_VSS2	AA11	RESERVED	H24	TX3+	A16
MAD[29]	AC26	N/C	U6	P_RXB_VSS3	AA13	RESERVED	K2	TXB_VDD0	F20
MAD[30]	AB22	N/C	U22	P_RXB_VSS4	Y16	RESERVED	K3	TXB_VDD1	E18
MAD[31]	AD25	N/C	V1	P_RXB_VSS5	AB17	RESERVED	K4	TXB_VDD2	F16
MADP[0]	L21	N/C	V2	P_RXB_VSS6	AA19	RESERVED	K22	TXB_VDD3	A14
MADP[1]	U26	N/C	V5	P_RXB_VSS7	AA21	RESERVED	G22	TXB_VSS0	E20
MADP[2]	W26	N/C	V6	P_TX_VDD0	AB5	RESERVED	G23	TXB_VSS1	B19
MADP[3]	AA22	N/C	V24	P_TX_VDD1	AD4	RESERVED	M4	TXB_VSS2	E16
MCLK	U23	N/C	V25	P_TX_VDD2	AC8	RESERVED	N2	TXB_VSS3	F14
MODE[0]	J6	N/C	W2	P_TX_VDD3	AC10	RESERVED	N4	UART_RX	E26
MODE[1]	H4	N/C	W4	P_TX_VDD4	AC14	RESERVED	N5	UART_TX	F26
MODE[2]	D1	N/C	W5	P_TX_VDD5	AD17	RESERVED	P1	VDD2	A12
MODE[3]	G4	N/C	W6	P_TX_VDD6	AC18	RESERVED	P3	VDD2	B10
MODE[4]	G5	N/C	W7	P_TX_VDD7	AF23	RESERVED	P5	VDD2	C4
MODE[5]	D2	N/C	W21	P_TX_VSS0	AA7	RESERVED	R21	VDD2	C8
MODE[6]	F4	N/C	W22	P_TX_VSS1	AA8	RESERVED	T1	VDD2	C10
MODE[7]	G6	N/C	Y5	P_TX_VSS2	AF7	RST/	AB3	VDD2	D7
MOE0/	U25	N/C	Y6	P_TX_VSS3	AB11	RTCK_ICE	T4	VDD2	D8
MOE1/	N24	N/C	Y22	P_TX_VSS4	AB14	RTRIM	C14	VDD2	D9
MWE0/	T23	N/C	AA1	P_TX_VSS5	AC16	RX_VDD0	E21	VDD2	D10
MWE1/	P24	N/C	AA5	P_TX_VSS6	Y18	RX_VDD1	D19	VDD2	E5
N/C	B14	N/C	AA6	P_TX_VSS7	AB19	RX_VDD2	C18	VDD2	E6
N/C	C24	N/C	AB13	P_TX0-	AE2	RX_VDD3	D15	VDD2	E9
N/C	C25	N/C	AB26	P_TX0+	AF2	RX_VSS0	D22	VDD2	E10
N/C	D3	N/C	AC12	P_TX1-	AE5	RX_VSS1	F18	VDD2	F12
N/C	D23	N/C	AC13	P_TX1+	AE4	RX_VSS2	D17		

1. N/C pins are not connected.

Table 1 LSISAS1064E Pin Assignments Listed by Signal Name[1] (Cont.)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
VDD2	G7	VDDIO33	G11	VDDIO33	AA2	VSS	H11	VSS	R17
VDD2	G8	VDDIO33	G12	VDDIO33	AA25	VSS	H12	VSS	R19
VDD2	K11	VDDIO33	G13	VDDIO33	AC23	VSS	H13	VSS	R24
VDD2	K13	VDDIO33	G14	VDDIO33	AD5	VSS	H14	VSS	T3
VDD2	K15	VDDIO33	G15	VDDIO33	AD6	VSS	H15	VSS	T8
VDD2	K17	VDDIO33	G17	VDDIO33	AD20	VSS	H16	VSS	T10
VDD2	L10	VDDIO33	G19	VDDIO33	AD21	VSS	H17	VSS	T12
VDD2	L12	VDDIO33	G25	VDDIO33	AD24	VSS	H18	VSS	T14
VDD2	L14	VDDIO33	H7	VDDIO33	AD26	VSS	H19	VSS	T16
VDD2	L16	VDDIO33	H20	VDDIO33	AE11	VSS	J8	VSS	T19
VDD2	M11	VDDIO33	J7	VDDIO33	AE12	VSS	J19	VSS	T24
VDD2	M13	VDDIO33	J20	VDDIO33	AE15	VSS	K8	VSS	U8
VDD2	M15	VDDIO33	K7	VDDIO33	AE16	VSS	K10	VSS	U11
VDD2	M17	VDDIO33	K20	VDDIO33	AF24	VSS	K12	VSS	U13
VDD2	N10	VDDIO33	L2	VSS	A2	VSS	K14	VSS	U15
VDD2	N12	VDDIO33	L7	VSS	A7	VSS	K16	VSS	U17
VDD2	N14	VDDIO33	L20	VSS	A25	VSS	K19	VSS	U19
VDD2	N16	VDDIO33	L25	VSS	B1	VSS	L3	VSS	V8
VDD2	P11	VDDIO33	M2	VSS	B26	VSS	L8	VSS	V19
VDD2	P13	VDDIO33	M7	VSS	C7	VSS	L11	VSS	W8
VDD2	P15	VDDIO33	M20	VSS	C9	VSS	L13	VSS	W9
VDD2	P17	VDDIO33	M25	VSS	C11	VSS	L15	VSS	W10
VDD2	R10	VDDIO33	N7	VSS	C12	VSS	L17	VSS	W11
VDD2	R12	VDDIO33	N20	VSS	C15	VSS	L19	VSS	W12
VDD2	R14	VDDIO33	P7	VSS	C16	VSS	L24	VSS	W13
VDD2	R16	VDDIO33	P20	VSS	C22	VSS	M3	VSS	W14
VDD2	T11	VDDIO33	R2	VSS	D4	VSS	M8	VSS	W15
VDD2	T13	VDDIO33	R7	VSS	D5	VSS	M10	VSS	W16
VDD2	T15	VDDIO33	R20	VSS	D6	VSS	M12	VSS	W17
VDD2	T17	VDDIO33	R25	VSS	D11	VSS	M14	VSS	W18
VDD2	U10	VDDIO33	T2	VSS	D20	VSS	M16	VSS	W19
VDD2	U12	VDDIO33	T7	VSS	D21	VSS	M19	VSS	Y3
VDD2	U14	VDDIO33	T20	VSS	E7	VSS	M24	VSS	Y24
VDD2	U16	VDDIO33	T25	VSS	E8	VSS	N8	VSS	AA3
VDDIO33	A24	VDDIO33	U7	VSS	E11	VSS	N11	VSS	AA24
VDDIO33	B2	VDDIO33	U20	VSS	E12	VSS	N13	VSS	AC5
VDDIO33	B11	VDDIO33	V7	VSS	F3	VSS	N15	VSS	AC6
VDDIO33	B12	VDDIO33	V20	VSS	F7	VSS	N17	VSS	AC20
VDDIO33	B15	VDDIO33	W20	VSS	F8	VSS	N19	VSS	AC21
VDDIO33	B16	VDDIO33	Y2	VSS	F9	VSS	P8	VSS	AD11
VDDIO33	C1	VDDIO33	Y9	VSS	F10	VSS	P10	VSS	AD12
VDDIO33	C5	VDDIO33	Y11	VSS	F11	VSS	P12	VSS	AD15
VDDIO33	C6	VDDIO33	Y12	VSS	F13	VSS	P14	VSS	AD16
VDDIO33	C20	VDDIO33	Y13	VSS	F24	VSS	P16	VSS	AD22
VDDIO33	C21	VDDIO33	Y14	VSS	G3	VSS	P19	VSS	AE1
VDDIO33	C26	VDDIO33	Y15	VSS	G10	VSS	R3	VSS	AE26
VDDIO33	F2	VDDIO33	Y17	VSS	G24	VSS	R8	VSS	AF25
VDDIO33	F25	VDDIO33	Y19	VSS	H8	VSS	R11		
VDDIO33	G2	VDDIO33	Y20	VSS	H9	VSS	R13		
VDDIO33	G9	VDDIO33	Y25	VSS	H10	VSS	R15		

1. N/C pins are not connected.

Table 2 LSISAS1064E Pin Assignments Listed by Pin Number[1]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VSS	D3	N/C	G3	VSS	K14	VSS	N21	N/C
A3	RESERVED	D4	VSS	G4	MODE[3]	K15	VDD2	N22	N/C
A4	RESERVED	D5	VSS	G5	MODE[4]	K16	VSS	N23	MAD[13]
A5	RESERVED	D6	VSS	G6	MODE[7]	K17	VDD2	N24	MOE1/
A6	RESERVED	D7	VDD2	G7	VDD2	K19	VSS	N25	N/C
A7	VSS	D8	VDD2	G8	VDD2	K20	VDDIO33	N26	NVSRAM_CS/
A8	RESERVED	D9	VDD2	G9	VDDIO33	K21	ISTWI_DATA	P1	RESERVED
A9	RESERVED	D10	VDD2	G10	VSS	K22	RESERVED	P2	N/C
A10	RESERVED	D11	VSS	G11	VDDIO33	K23	MAD[11]	P3	RESERVED
A11	RESERVED	D12	REFCLK_N	G12	VDDIO33	K24	MAD[2]	P4	HB_LED/
A12	VDD2	D13	REFPLL_VDD	G13	VDDIO33	K25	MAD[8]	P5	RESERVED
A13	REFPLL_VSS	D14	TX_VDD3	G14	VDDIO33	K26	MAD[12]	P6	N/C
A14	TXB_VDD3	D15	RX_VDD3	G15	VDDIO33	L1	FAULT_LED[3]/	P7	VDDIO33
A15	TX3-	D16	TX_VSS2	G16	RXB_VSS3	L2	VDDIO33	P8	VSS
A16	TX3+	D17	RX_VSS2	G17	VDDIO33	L3	VSS	P10	VSS
A17	RX3+	D18	TX_VDD1	G18	TX_VSS1	L4	N/C	P11	VDD2
A18	TX2-	D19	RX_VDD1	G19	VDDIO33	L5	N/C	P12	VSS
A19	RX2+	D20	VSS	G20	N/C	L6	N/C	P13	VDD2
A20	RX2-	D21	VSS	G21	N/C	L7	VDDIO33	P14	VSS
A21	TX1-	D22	RX_VSS0	G22	RESERVED	L8	VSS	P15	VDD2
A22	TX1+	D23	N/C	G23	RESERVED	L10	VDD2	P16	VSS
A23	TX_VDD0	D24	RESERVED	G24	VSS	L11	VSS	P17	VDD2
A24	VDDIO33	D25	SIO_DOUT_A	G25	VDDIO33	L12	VDD2	P19	VSS
A25	VSS	D26	RESERVED	G26	ISTWI_CLK	L13	VSS	P20	VDDIO33
B1	VSS	E1	N/C	H1	ACTIVE_LED[0]/	L14	VDD2	P21	N/C
B2	VDDIO33	E2	FSELA	H2	ACTIVE_LED[1]/	L15	VSS	P22	N/C
B3	RESERVED	E3	N/C	H3	ACTIVE_LED[3]/	L16	VDD2	P23	MAD[15]
B4	RESERVED	E4	SCAN_ENABLE	H4	MODE[1]	L17	VSS	P24	MWE1/
B5	RESERVED	E5	VDD2	H5	N/C	L19	VSS	P25	FLASH_CS/
B6	RESERVED	E6	VDD2	H6	N/C	L20	VDDIO33	P26	N/C
B7	RESERVED	E7	VSS	H7	VDDIO33	L21	MADP[0]	R1	N/C
B8	RESERVED	E8	VSS	H8	VSS	L22	N/C	R2	VDDIO33
B9	RESERVED	E9	VDD2	H9	VSS	L23	MAD[10]	R3	VSS
B10	VDD2	E10	VDD2	H10	VSS	L24	VSS	R4	N/C
B11	VDDIO33	E11	VSS	H11	VSS	L25	VDDIO33	R5	N/C
B12	VDDIO33	E12	VSS	H12	VSS	L26	MAD[9]	R6	N/C
B13	REFCLK_B	E13	N/C	H13	VSS	M1	FAULT_LED[2]/	R7	VDDIO33
B14	N/C	E14	TX_VSS3	H14	VSS	M2	VDDIO33	R8	VSS
B15	VDDIO33	E15	RXB_VDD3	H15	VSS	M3	VSS	R10	VDD2
B16	VDDIO33	E16	TXB_VSS2	H16	VSS	M4	RESERVED	R11	VSS
B17	RX3-	E17	RXB_VSS2	H17	VSS	M5	N/C	R12	VDD2
B18	TX2+	E18	TXB_VDD1	H18	VSS	M6	N/C	R13	VSS
B19	TXB_VSS1	E19	TX_VSS0	H19	VSS	M7	VDDIO33	R14	VDD2
B20	RX1+	E20	TXB_VSS0	H20	VDDIO33	M8	VSS	R15	VSS
B21	RX1-	E21	RX_VDD0	H21	N/C	M10	VSS	R16	VDD2
B22	TX0+	E22	N/C	H22	SIO_CLK_A	M11	VDD2	R17	VSS
B23	TX0-	E23	N/C	H23	N/C	M12	VSS	R19	VSS
B24	RX0+	E24	N/C	H24	RESERVED	M13	VDD2	R20	VDDIO33
B25	RX0-	E25	SIO_END_A	H25	N/C	M14	VSS	R21	RESERVED
B26	VSS	E26	UART_RX	H26	MAD[1]	M15	VDD2	R22	N/C
C1	VDDIO33	F1	N/C	J1	N/C	M16	VSS	R23	BWE[2]/
C2	TST_RST/	F2	VDDIO33	J2	N/C	M17	VDD2	R24	VSS
C3	RESERVED	F3	VSS	J3	N/C	M19	VSS	R25	VDDIO33
C4	VDD2	F4	MODE[6]	J4	N/C	M20	VDDIO33	R26	MAD[14]
C5	VDDIO33	F5	SCAN_MODE	J5	N/C	M21	N/C	T1	RESERVED
C6	VDDIO33	F6	N/C	J6	MODE[0]	M22	N/C	T2	VDDIO33
C7	VSS	F7	VSS	J7	VDDIO33	M23	MAD[6]	T3	VSS
C8	VDD2	F8	VSS	J8	VSS	M24	VSS	T4	RTCK_ICE
C9	VSS	F9	VSS	J19	VSS	M25	VDDIO33	T5	TDI_ICE
C10	VDD2	F10	VSS	J20	VDDIO33	M26	MAD[5]	T6	N/C
C11	VSS	F11	VSS	J21	SIO_DIN_A	N1	FAULT_LED[0]/	T7	VDDIO33
C12	VSS	F12	VDD2	J22	N/C	N2	RESERVED	T8	VSS
C13	REFCLK_P	F13	VSS	J23	MAD[4]	N3	FAULT_LED[1]/	T10	VSS
C14	RTRIM	F14	TXB_VSS3	J24	MAD[3]	N4	RESERVED	T11	VDD2
C15	VSS	F15	RX_VSS3	J25	MAD[7]	N5	RESERVED	T12	VSS
C16	VSS	F16	TXB_VDD2	J26	MAD[0]	N6	N/C	T13	VDD2
C17	TX_VDD2	F17	RXB_VDD2	K1	N/C	N7	VDDIO33	T14	VSS
C18	RX_VDD2	F18	RX_VSS1	K2	RESERVED	N8	VSS	T15	VDD2
C19	RXB_VDD1	F19	RXB_VSS1	K3	RESERVED	N10	VDD2	T16	VSS
C20	VDDIO33	F20	TXB_VDD0	K4	RESERVED	N11	VSS	T17	VDD2
C21	VDDIO33	F21	RXB_VSS0	K5	N/C	N12	VDD2	T19	VSS
C22	VSS	F22	N/C	K6	N/C	N13	VSS	T20	VDDIO33
C23	RXB_VDD0	F23	N/C	K7	VDDIO33	N14	VDD2	T21	BWE[0]/
C24	N/C	F24	VSS	K8	VSS	N15	VSS	T22	TDIODE_VSS
C25	N/C	F25	VDDIO33	K10	VSS	N16	VDD2	T23	MWE0/
C26	VDDIO33	F26	UART_TX	K11	VDD2	N17	VSS	T24	VSS
D1	MODE[2]	G1	ACTIVE_LED[2]/	K12	VSS	N19	VSS	T25	VDDIO33
D2	MODE[5]	G2	VDDIO33	K13	VDD2	N20	VDDIO33	T26	N/C

1. N/C pins are not connected.

Table 2 LSISAS1064E Pin Assignments Listed by Pin Number[1] (Cont.)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
U1	N/C	W11	VSS	AA9	P_RX_VSS1	AC7	P_RX_VDD1	AE5	P_TX1-
U2	N/C	W12	VSS	AA10	P_TXB_VSS2	AC8	P_TX_VDD2	AE6	P_RX1+
U3	TCK_ICE	W13	VSS	AA11	P_RXB_VSS2	AC9	P_RX_VDD2	AE7	P_RX1-
U4	TMS_ICE	W14	VSS	AA12	P_TXB_VDD3	AC10	P_TX_VDD3	AE8	P_RX2+
U5	N/C	W15	VSS	AA13	P_RXB_VSS3	AC11	P_TXB_VSS3	AE9	P_TX3-
U6	N/C	W16	VSS	AA14	P_TXB_VSS4	AC12	N/C	AE10	P_RX_VDD3
U7	VDDIO33	W17	VSS	AA15	P_RX_VSS4	AC13	N/C	AE11	VDDIO33
U8	VSS	W18	VSS	AA16	P_TXB_VDD5	AC14	P_TX_VDD4	AE12	VDDIO33
U10	VDD2	W19	VSS	AA17	P_RXB_VDD5	AC15	P_RX_VDD4	AE13	N/C
U11	VSS	W20	VDDIO33	AA18	P_RX_VSS6	AC16	P_TX_VSS5	AE14	P_REFCLK_P
U12	VDD2	W21	N/C	AA19	P_RXB_VSS6	AC17	P_RX_VSS5	AE15	VDDIO33
U13	VSS	W22	N/C	AA20	P_TXB_VDD7	AC18	P_TX_VDD6	AE16	VDDIO33
U14	VDD2	W23	MAD[21]	AA21	P_RXB_VSS7	AC19	P_RX_VDD6	AE17	P_RX4-
U15	VSS	W24	MAD[18]	AA22	MADP[3]	AC20	VSS	AE18	P_TX5+
U16	VDD2	W25	BWE[3]/	AA23	MAD[22]	AC21	VSS	AE19	P_TXB_VSS6
U17	VSS	W26	MADP[2]	AA24	VSS	AC22	P_RX_VSS7	AE20	P_RX6+
U19	VSS	Y1	GPIO[1]	AA25	VDDIO33	AC23	VDDIO33	AE21	P_RX6-
U20	VDDIO33	Y2	VDDIO33	AA26	MAD[20]	AC24	N/C	AE22	P_TX7+
U21	MAD[19]	Y3	VSS	AB1	GPIO[3]	AC25	MAD[28]	AE23	P_TX7-
U22	N/C	Y4	TRST/	AB2	TCK	AC26	MAD[29]	AE24	P_RX7+
U23	MCLK	Y5	N/C	AB3	RST/	AD1	N/C	AE25	P_RX7-
U24	BWE[1]/	Y6	N/C	AB4	IDDT	AD2	TN/	AE26	VSS
U25	MOE0/	Y7	P_TXB_VDD0	AB5	P_TX_VDD0	AD3	N/C	AF2	P_TX0+
U26	MADP[1]	Y8	P_RXB_VDD0	AB6	P_RX_VDD0	AD4	P_TX_VDD1	AF3	P_RX0+
V1	N/C	Y9	VDDIO33	AB7	P_RX_VSS0	AD5	VDDIO33	AF4	P_RX0-
V2	N/C	Y10	P_RXB_VSS1	AB8	P_TXB_VSS1	AD6	VDDIO33	AF5	P_TX2-
V3	TDO_ICE	Y11	VDDIO33	AB9	P_RXB_VDD1	AD7	P_RXB_VSS0	AF6	P_TX2+
V4	GPIO[0]	Y12	VDDIO33	AB10	P_TXB_VDD2	AD8	P_TXB_VDD1	AF7	P_TX_VSS2
V5	N/C	Y13	VDDIO33	AB11	P_TX_VSS3	AD9	P_RX_VSS2	AF8	P_RX2-
V6	N/C	Y14	VDDIO33	AB12	P_RX_VSS3	AD10	P_RXB_VDD2	AF9	P_TX3+
V7	VDDIO33	Y15	VDDIO33	AB13	N/C	AD11	VSS	AF10	P_RX3+
V8	VSS	Y16	P_RXB_VSS4	AB14	P_TX_VSS4	AD12	VSS	AF11	P_RX3-
V19	VSS	Y17	VDDIO33	AB15	P_RXB_VDD4	AD13	N/C	AF12	P_RXB_VDD3
V20	VDDIO33	Y18	P_TX_VSS6	AB16	P_TXB_VSS5	AD14	P_REFCLK_N	AF13	N/C
V21	MAD[16]	Y19	VDDIO33	AB17	P_RXB_VSS5	AD15	VSS	AF14	P_TXB_VDD4
V22	ADSC/	Y20	VDDIO33	AB18	P_TXB_VDD6	AD16	VSS	AF15	P_TX4-
V23	ADV/	Y21	MAD[27]	AB19	P_TX_VSS7	AD17	P_TX_VDD5	AF16	P_TX4+
V24	N/C	Y22	N/C	AB20	P_TXB_VSS7	AD18	P_RX_VDD5	AF17	P_RX4+
V25	N/C	Y23	MAD[23]	AB21	P_RX_VDD7	AD19	P_RXB_VDD6	AF18	P_TX5-
V26	TDIODE_P	Y24	VSS	AB22	MAD[30]	AD20	VDDIO33	AF19	P_RX5+
W1	TRST_ICE/	Y25	VDDIO33	AB23	MAD[25]	AD21	VDDIO33	AF20	P_RX5-
W2	N/C	Y26	MAD[17]	AB24	MAD[26]	AD22	VSS	AF21	P_TX6-
W3	GPIO[2]	AA1	N/C	AB25	MAD[24]	AD23	P_RXB_VDD7	AF22	P_TX6+
W4	N/C	AA2	VDDIO33	AB26	N/C	AD24	VDDIO33	AF23	P_TX_VDD7
W5	N/C	AA3	VSS	AC1	TDI	AD25	MAD[31]	AF24	VDDIO33
W6	N/C	AA4	PROCMON	AC2	TDO	AD26	VDDIO33	AF25	VSS
W7	N/C	AA5	N/C	AC3	TMS	AE1	VSS		
W8	VSS	AA6	N/C	AC4	P_TXB_VSS0	AE2	P_TX0-		
W9	VSS	AA7	P_TX_VSS0	AC5	VSS	AE3	N/C		
W10	VSS	AA8	P_TX_VSS1	AC6	VSS	AE4	P_TX1+		

1. N/C pins are not connected.

Figure 4 LSISAS1064E 636 EPBGA-T – Top View (Sheet 1 of 2)

*	1	2	3	4	5	6	7	8	9	10	11	12	13
A		VSS	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	VSS	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	VDD2	REFPLL_VSS
B	VSS	VDDIO33	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	RE-SERVED	VDD2	VDDIO33	VDDIO33	REFCLK_B
C	VDDIO33	TST_RST/	RE-SERVED	VDD2	VDDIO33	VDDIO33	VSS	VDD2	VSS	VDD2	VSS	VSS	REFCLK_P
D	MODE[2]	MODE[5]	N/C	VSS	VSS	VSS	VDD2	VDD2	VDD2	VDD2	VSS	REFCLK_N	REFPLL_VDD
E	N/C	FSELA	N/C	SCAN_ENABLE	VDD2	VDD2	VSS	VSS	VDD2	VDD2	VSS	VSS	N/C
F	N/C	VDDIO33	VSS	MODE[6]	SCAN_MODE	N/C	VSS	VSS	VSS	VSS	VSS	VDD2	VSS
G	ACTIVE_LED[2]/	VDDIO33	VSS	MODE[3]	MODE[4]	MODE[7]	VDD2	VDD2	VDDIO33	VSS	VDDIO33	VDDIO33	VDDIO33
H	ACTIVE_LED[0]/	ACTIVE_LED[1]/	ACTIVE_LED[3]/	MODE[1]	N/C	N/C	VDDIO33	VSS	VSS	VSS	VSS	VSS	VSS
J	N/C	N/C	N/C	N/C	N/C	MODE[0]	VDDIO33	VSS					
K	N/C	RE-SERVED	RE-SERVED	RE-SERVED	N/C	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2
L	FAULT_LED[3]/	VDDIO33	VSS	N/C	N/C	N/C	VDDIO33	VSS		VDD2	VSS	VDD2	VSS
M	FAULT_LED[2]/	VDDIO33	VSS	RE-SERVED	N/C	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2
N	FAULT_LED[0]/	RE-SERVED	FAULT_LED[1]/	RE-SERVED	RE-SERVED	N/C	VDDIO33	VSS		VDD2	VSS	VDD2	VSS
P	RE-SERVED	N/C	RE-SERVED	HB_LED/	RE-SERVED	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2
R	N/C	VDDIO33	VSS	N/C	N/C	N/C	VDDIO33	VSS		VDD2	VSS	VDD2	VSS
T	RE-SERVED	VDDIO33	VSS	RTCK_ICE	TDI_ICE	N/C	VDDIO33	VSS		VSS	VDD2	VSS	VDD2
U	N/C	N/C	TCK_ICE	TMS_ICE	N/C	N/C	VDDIO33	VSS		VDD2	VSS	VDD2	VSS
V	N/C	N/C	TDO_ICE	GPIO[0]	N/C	N/C	VDDIO33	VSS					
W	TRST_ICE/	N/C	GPIO[2]	N/C	N/C	N/C	N/C	VSS	VSS	VSS	VSS	VSS	VSS
Y	GPIO[1]	VDDIO33	VSS	TRST/	N/C	N/C	P_TXB_VDD0	P_RXB_VDD0	VDDIO33	P_RXB_VSS1	VDDIO33	VDDIO33	VDDIO33
AA	N/C	VDDIO33	VSS	PROC-MON	N/C	N/C	P_TX_VSS0	P_TX_VSS1	P_RX_VSS1	P_TXB_VSS2	P_RXB_VSS2	P_TXB_VDD3	P_RXB_VSS3
AB	GPIO[3]	TCK	RST/	IDDT	P_TX_VDD0	P_RX_VDD0	P_RX_VSS0	P_TXB_VSS1	P_RXB_VDD1	P_TXB_VDD2	P_TX_VSS3	P_RX_VSS3	N/C
AC	TDI	TDO	TMS	P_TXB_VSS0	VSS	VSS	P_RX_VDD1	P_TX_VDD2	P_RX_VDD2	P_TX_VDD3	P_TXB_VSS3	N/C	N/C
AD	N/C	TN/	N/C	P_TX_VDD1	VDDIO33	VDDIO33	P_RXB_VSS0	P_TXB_VDD1	P_RX_VSS2	P_RXB_VDD2	VSS	VSS	N/C
AE	VSS	P_TX0-	N/C	P_TX1+	P_TX1-	P_RX1+	P_RX1-	P_RX2+	P_TX3-	P_RX_VDD3	VDDIO33	VDDIO33	N/C
AF		P_TX0+	P_RX0+	P_RX0-	P_TX2-	P_TX2+	P_TX_VSS2	P_RX2-	P_TX3+	P_RX3+	P_RX3-	P_RXB_VDD3	N/C

Figure 4 LSISAS1064E 636 EPBGA-T – Top View (Sheet 2 of 2)

14	15	16	17	18	19	20	21	22	23	24	25	26	*
TXB_ VDD3	TX3-	TX3+	RX3+	TX2-	RX2+	RX2-	TX1-	TX1+	TX_ VDD0	VDDIO33	VSS		A
N/C	VDDIO33	VDDIO33	RX3-	TX2+	TXB_ VSS1	RX1+	RX1-	TX0+	TX0-	RX0+	RX0-	VSS	B
RTRIM	VSS	VSS	TX_ VDD2	RX_ VDD2	RXB_ VDD1	VDDIO33	VDDIO33	VSS	RXB_ VDD0	N/C	N/C	VDDIO33	C
TX_ VDD3	RX_ VDD3	TX_ VSS2	RX_ VSS2	TX_ VDD1	RX_ VDD1	VSS	VSS	RX_ VSS0	N/C	RE-SERVED	SIO_ DOUT_A	RE-SERVED	D
TX_ VSS3	RXB_ VDD3	TXB_ VSS2	RXB_ VSS2	TXB_ VDD1	TX_ VSS0	TXB_ VSS0	RX_ VDD0	N/C	N/C	N/C	SIO_ END_A	UART _RX	E
TXB_ VSS3	RX_ VSS3	TXB_ VDD2	RXB_ VDD2	RX_ VSS1	RXB_ VSS1	TXB_ VDD0	RXB_ VSS0	N/C	N/C	VSS	VDDIO33	UART _TX	F
VDDIO33	VDDIO33	RXB_ VSS3	VDDIO33	TX_ VSS1	VDDIO33	N/C	N/C	RE-SERVED	RE-SERVED	VSS	VDDIO33	ISTWI_ CLK	G
VSS	VSS	VSS	VSS	VSS	VSS	VDDIO33	N/C	SIO_ CLK_A	N/C	RE-SERVED	N/C	MAD[1]	H
					VSS	VDDIO33	SIO_ DIN_A	N/C	MAD[4]	MAD[3]	MAD[7]	MAD[0]	J
VSS	VDD2	VSS	VDD2		VSS	VDDIO33	ISTWI_ DATA	RE-SERVED	MAD[11]	MAD[2]	MAD[8]	MAD[12]	K
VDD2	VSS	VDD2	VSS		VSS	VDDIO33	MADP[0]	N/C	MAD[10]	VSS	VDDIO33	MAD[9]	L
VSS	VDD2	VSS	VDD2		VSS	VDDIO33	N/C	N/C	MAD[6]	VSS	VDDIO33	MAD[5]	M
VDD2	VSS	VDD2	VSS		VSS	VDDIO33	N/C	N/C	MAD[13]	MOE1/	N/C	NVSRAM _CS/	N
VSS	VDD2	VSS	VDD2		VSS	VDDIO33	N/C	N/C	MAD[15]	MWE1/	FLASH _CS/	N/C	P
VDD2	VSS	VDD2	VSS		VSS	VDDIO33	RE-SERVED	N/C	BWE[2]/	VSS	VDDIO33	MAD[14]	R
VSS	VDD2	VSS	VDD2		VSS	VDDIO33	BWE[0]/	TDIODE_ VSS	MWE0/	VSS	VDDIO33	N/C	T
VDD2	VSS	VDD2	VSS		VSS	VDDIO33	MAD[19]	N/C	MCLK	BWE[1]/	MOE0/	MADP[1]	U
					VSS	VDDIO33	MAD[16]	ADSC/	ADV/	N/C	N/C	TDIODE _P	V
VSS	VSS	VSS	VSS	VSS	VSS	VDDIO33	N/C	N/C	MAD[21]	MAD[18]	BWE[3]/	MADP[2]	W
VDDIO33	VDDIO33	P_RXB_ VSS4	VDDIO33	P_TX_ VSS6	VDDIO33	VDDIO33	MAD[27]	N/C	MAD[23]	VSS	VDDIO33	MAD[17]	Y
P_TXB_ VSS4	P_RX_ VSS4	P_TXB_ VDD5	P_RXB_ VDD5	P_RX_ VSS6	P_RXB_ VSS6	P_TXB_ VDD7	P_RXB_ VSS7	MADP[3]	MAD[22]	VSS	VDDIO33	MAD[20]	AA
P_TX_ VSS4	P_RXB_ VDD4	P_TXB_ VSS5	P_RXB_ VSS5	P_TXB_ VDD6	P_TX_ VSS7	P_TXB_ VSS7	P_RX_ VDD7	MAD[30]	MAD[25]	MAD[26]	MAD[24]	N/C	AB
P_TX_ VDD4	P_RX_ VDD4	P_TX_ VSS5	P_RX_ VSS5	P_TX_ VDD6	P_RX_ VDD6	VSS	VSS	P_RX_ VSS7	VDDIO33	N/C	MAD[28]	MAD[29]	AC
P_REF-CLK_N	VSS	VSS	P_TX_ VDD5	P_RX_ VDD5	P_RXB_ VDD6	VDDIO33	VDDIO33	VSS	P_RXB_ VDD7	VDDIO33	MAD[31]	VDDIO33	AD
P_REF-CLK_P	VDDIO33	VDDIO33	P_RX4-	P_TX5+	P_TXB_ VSS6	P_RX6+	P_RX6-	P_TX7+	P_TX7-	P_RX7+	P_RX7-	VSS	AE
P_TXB_ VDD4	P_TX4-	P_TX4+	P_RX4+	P_TX5-	P_RX5+	P_RX5-	P_TX6-	P_TX6+	P_TX_ VDD7	VDDIO33	VSS		AF

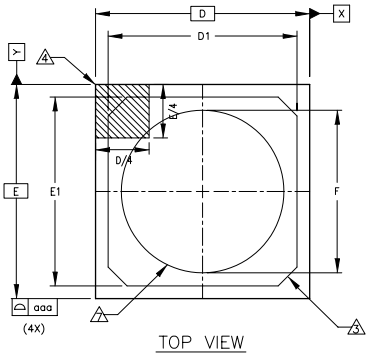
Package Drawing

The LSISAS1064E uses a 636 EPBGA-T package. The package code is 8C. Figure 5 provides the package drawing.

Figure 5 636-Ball EPBGA-T (8C) Mechanical Drawing (Sheet 1 of 3)

REVISIONS

APPROVAL	DATE	DESCRIPTION	REV
C. Fishley	08–13–04	ADD PACKAGE (uo, 3w, ow, 82)	8
L. Mora	01–24–05	ADD PACKAGE (gz)	9
L. Mora	05–26–05	Changed "F" min from 19.5 to 17.5.	10
L. Mora	08–22–05	Add Package (aa2au)	11
M.Othieno	10–21–05	Add Package (aa2a3)	12
C. Fishley	10–26–05	Add Package (7o, uy)	13
A. Lim	02–22–06	Add Package (1N)	14



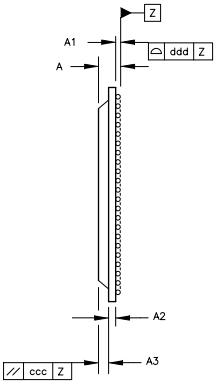


TABLE 1: COMMON DIMENSIONS			
SYM	MIN	NOM	MAX
A	–	–	2.50
A1	0.40	–	–
A2	0.25	–	0.70
A3	–	–	1.25
b	0.50	–	0.70
D		27.00 BSC	
D1	23.00	–	25.00
E		27.00 BSC	
E1	23.00	–	25.00
e		1.00 BSC	
F	17.5	–	21.50

TABLE 2: TOLERANCES OF FORM AND POSITION	
DIMENSION	e = 1.00
aaa	0.20
ccc	0.35
ddd	0.15
eee	0.25
fff	0.10

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS IN MM.
3. CORNER DETAIL IS LSI LOGIC CORPORATION OPTION.
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, AND MAY CONSIST OF INK, LASER MARK OR METALLIZED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
5. JEDEC CODE MS–034.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. HEAT SPREADER OUTLINE.

LSI LOGIC CORPORATION
1551 McCARTHY BLVD. MILPITAS, CA. 95035

TITLE: 27x27mm EPBGA–T, EPBGA–HP, PBGA–T 1.00 BALL PITCH

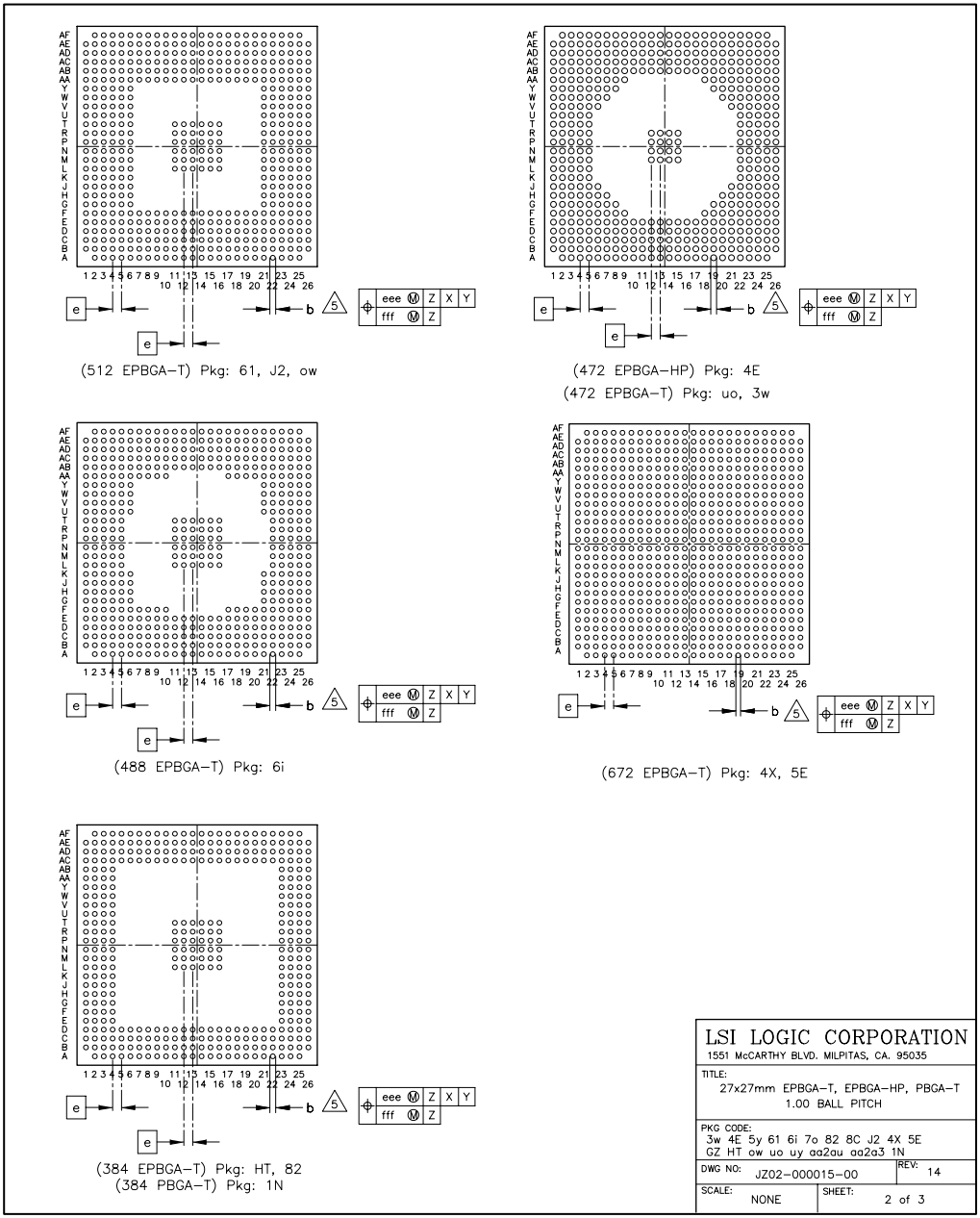
PKG CODE: 3w 4E 5y 61 6i 7o 82 8C J2 4X 5E GZ HT ow uo uy aa2au aa2a3 1N

DWG NO: JZ02–000015–00 REV: 14

SCALE: NONE SHEET: 1 of 3

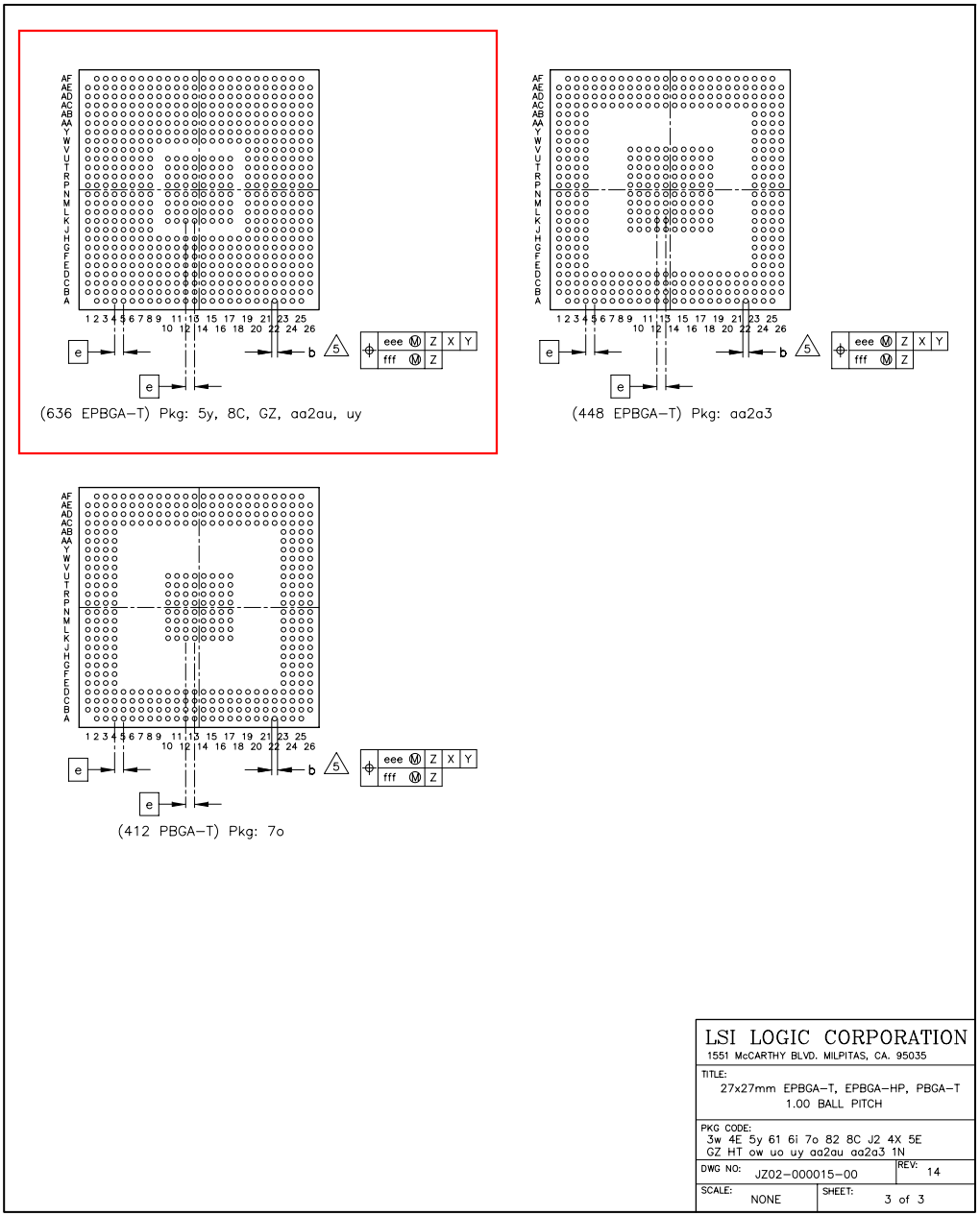
Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI marketing representative by requesting the outline drawing for package code 8C.**

Figure 5 636-Ball EPBGA-T (8C) Mechanical (Sheet 2 of 3); Bottom View (Cont.)



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI marketing representative by requesting the outline drawing for package code 8C.**

Figure 5 636-Ball EPBGA-T (8C) Mechanical (Sheet 3 of 3); Bottom View (Cont.)



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