LSI53C1010R
ULTRA160 SCSI CONTROLLER

PCI-DUAL CHANNEL ULTRA160 SCSI CONTROLLER OVERVIEW

The LSI53C1010R PCI-Dual Channel Ultra160 SCSI Controller provides a low-risk upgrade path to Ultra320 SCSI and to PCI-X. Because the LSI53C1010R is packaged in the same BGA as the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Controller, a motherboard can be designed now to accept either part without the need for redesign. The LSI53C1010R is identical in function to the proven LSI53C1010 PCI-Dual Channel Ultra160 SCSI Controller.

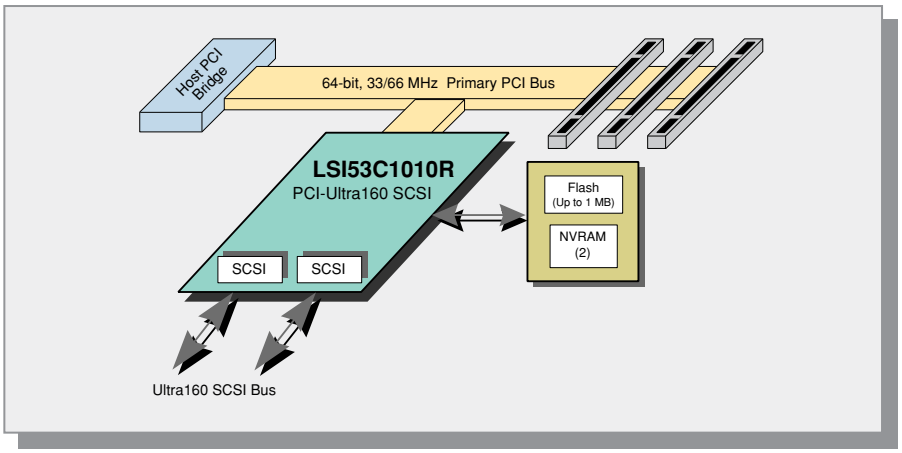

Figure 1. SCSI on the motherboard

KEY APPLICATIONS

- *Servers* – Internet/Intranet network, video, e-mail, printing, database management, and financial applications
- *Workstations* – CAD/CAM, industrial simulation, etc.
- *Host attach for RAID and JBOD mass storage subsystems* – Anywhere data access is the bottleneck

BENEFITS

- Provides a low-risk upgrade path to next level of performance
- Paves the way to Ultra320 SCSI by being pin compatible with the LSI53C1030 PCI-X to Dual Channel Ultra320 SCSI Controller
- Allows you to design one board for present and future technologies
- Preserves SCSI investment
- Reduces time to market
- Provides complete end-to-end protection of the SCSI I/O with Cyclic Redundancy Check (CRC) and Asynchronous Information Protection (AIP)
- Provides robust performance with SureLINK™ domain validation
- Supports all major operating systems

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FEATURES

- Pin compatible with LSI53C1030 Ultra320 controller
  - Functionally identical to LSI53C1010 Ultra160 controller
- No external memory required
- 64-bit, 33/66 MHz PCI interface
  - Theoretical 528 MBps (on 66 MHz part) zero wait state transfer rate
  - 64-bit addressing supported through Dual Address Cycle (DAC)
  - Compliant with PCI 2.2, PCI Power Management 1.1 and PC99
- Supports Ultra160 SCSI
  - Double transition clocking for 160 MBps throughput on each channel
  - CRC
  - Domain validation
- AIP
  - Covers all non-data, including command, status and messages
- High-performance PCI multifunction device
  - Presents one electrical load to PCI bus
  - Two independent wide Ultra160 SCSI channels
- SCSI Interrupt Steering Logic (SISL) alternate interrupt routing for RAID applications

ULTRA160 SCSI FEATURES

Double transition clocking enables throughput of up to 160 MBps on each channel for a total of 320 MBps, without increasing the interface clock rate.

Cyclic Redundancy Check (CRC) improves the reliability of SCSI data transmission through enhanced detection of communication errors. CRC provides extra data protection for marginal cable plants and external devices. CRC is the best way to ensure data protection during hot plugging. It uses the same proven CRC algorithm used by FDDI, Ethernet, and Fibre Channel, and detects all single bit errors, all double bit errors, all odd number of errors, and all burst errors up to 32 bits long. To provide complete end-to-end protection of the SCSI I/O, AIP protects all non-data phases, augmenting the CRC feature of Ultra160.

SureLINK domain validation technology detects the configuration of the SCSI bus and automatically tests and adjusts the SCSI transfer rate to optimize interoperability. The LSI53C1010R exceeds Ultra160 by providing not only Basic (Level 1) and Enhanced (Level 2) domain validation, but adds Margined (Level 3) domain validation. This enhancement margins LVD drive strength and clock signal timing characteristics to identify marginal Ultra160 systems.

HARDWARE/SOFTWARE OVERVIEW

PCI Interface

The host PCI interface complies with PCI Local Bus Specification Revision 2.2, and implements a 64-bit/66 MHz PCI bus. It is backward compatible with 32-bit/33 MHz buses. Additionally, support for DAC is provided.

The LSI53C1010R is a true PCI multifunction device in that it presents one electrical load to the PCI bus. It uses one REQ/-GNT/pair to arbitrate for PCI bus mastership, and separate interrupt signals are generated for SCSI Function A and SCSI Function B for maximum performance.

The LSI53C1010R complies with PCI Power Management Interface Specification Revision 1.1 and PC 99, supporting power states D0, D1, D2, D3hot and D3cold, power management capabilities registers, and programmable values for PCI Subsystem Vendor ID and Subsystem ID. Extended access cycles (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) are also supported.

SCSI Processors

The LSI53C1010R provides two independent Ultra160 SCSI controllers on a single chip. Each controller supports wide Ultra160 SCSI synchronous transfer rates up to 160 MBps on a LVD SCSI bus. Integrated LVDlink™ transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI, and Ultra160 SCSI are all supported by the LSI53C1010R.

An on-chip SCSI clock quadrupler allows the chip to achieve Ultra160 SCSI transfer rates with an input frequency of 40 MHz. The 8 KB of internal RAM per channel for SCRIPTS™ instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the device to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

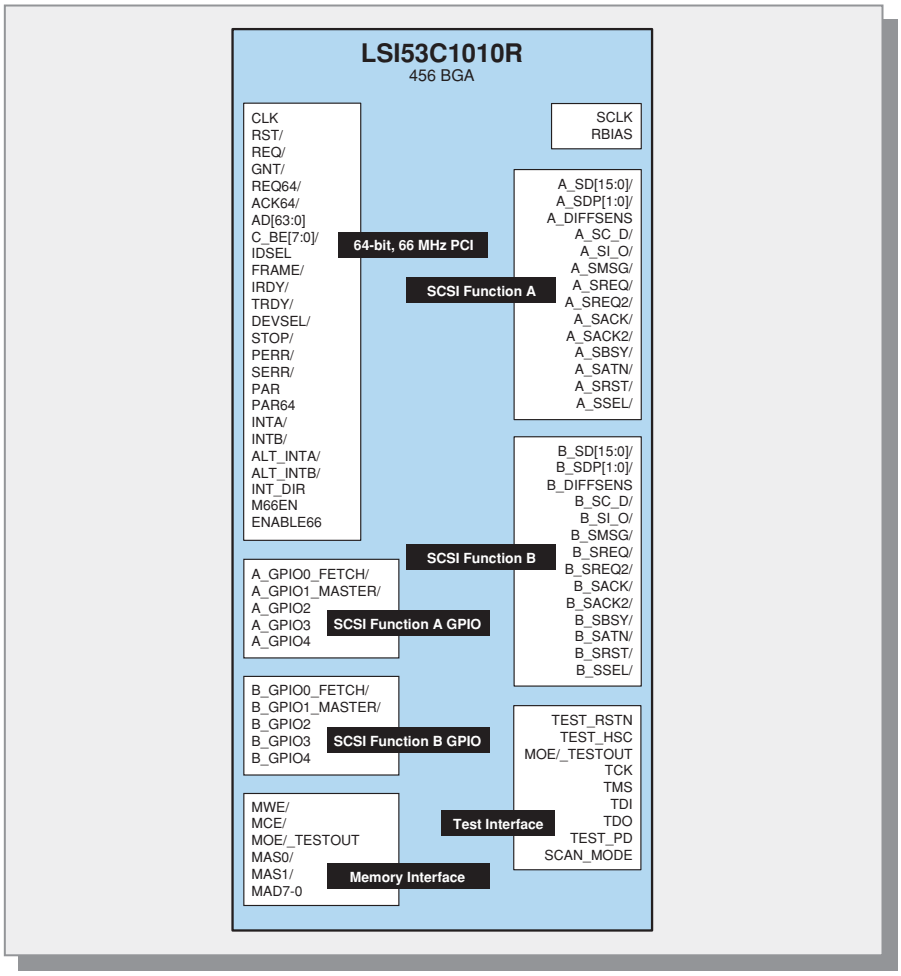

Figure 2. LSI53C1010R functional signal grouping

FEATURES (Continued)

- Proven integrated LVDlink transceivers for direct attach to either Low Voltage Differential (LVD) or single-ended (SE) SCSI buses
- Comprehensive SureLINK domain validation
  - Basic (Level 1) with inquiry command
  - Enhanced (Level 2) with read/write buffer
  - Margined (Level 3) with margining of LVD drive strength and programmable skew test
- IEEE 1149.1 JTAG boundary scan
- Flash and local memory interface
- Packaged in a 456 BGA
- Supported in Storage Device Management System (SDMS™) software release 4.6
  - Full operating system support:
    - Windows® NT® 4.0, 95/98 and 2000
    - Linux™
    - Solaris™
    - UnixWare™
    - Novell® NetWare®
    - OS/2
  - Server Management CI (component instrumentation)

MEMORY INTERFACES

The LSI53C1010R supports up to 1 MB of external expansion ROM through a parallel interface, for add-in card designs. For ease of software development and field upgrades of the ROM, the interface supports local programming of FLASH memory. A serial 2-wire interface on each SCSI channel provides a connection to an external serial EEPROM for storing Subsystem Vendor ID and Subsystem ID.

SOFTWARE

The LSI53C1010R is supported with the proven SDMS software. SDMS software enables the performance enhancements of Ultra160 data transfer speed increases and improved PCI bus utilization capabilities included in the LSI53C1010R. The LSI53C1010R reliability capabilities of AIP and CRC are enabled and managed by the SDMS software. SDMS software implements the manageability improvements of the LSI Logic SureLINK domain validation technology. SureLINK technology extends standard domain validation with the addition of full cable plant margining. The cable plant margining capability, exclusive to LSI Logic's Ultra160 solution, includes end-to-end margining from the LSI53C1010R through LSI Logic's LSI53C180 SCSI bus expander to the target device. The domain validation capability of SDMS software is available as an independent application as well as integrated in the DMI 2.0 based system management solution for enterprise class implementations. SDMS software includes BIOS and OSV certified drivers for all major operating systems including DOS with ASPI support, Windows 95/98, Windows NT/2000, UnixWare, OS/2, NetWare, Solaris and Linux. A complete set of SCSI utilities rounds out the software solution, which includes a DMI 2.0 based system management software for Windows NT, NetWare, UnixWare, Solaris and Linux, and a stand-alone or snap-in DMI browser applet and SureLINK applet.

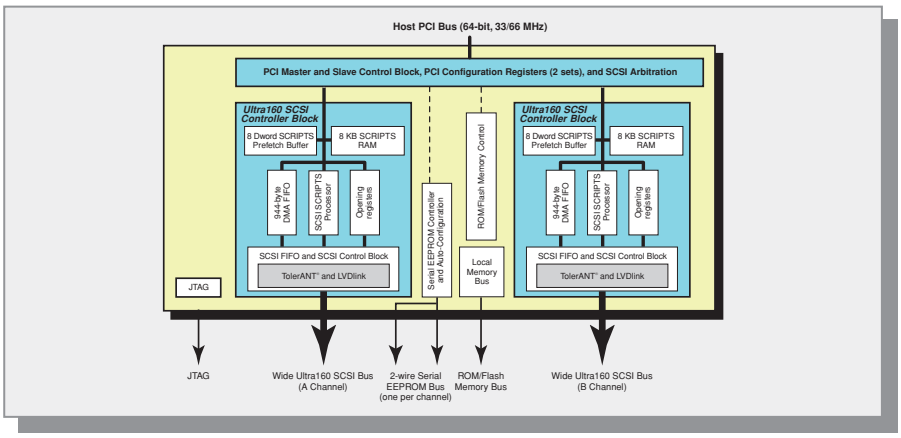

Figure 3. LSI53C1010R functional block diagram

For more information please visit the LSI Logic web site at:
http://storageio.lsilogic.com

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