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Intel® 852GME / 852PM Chipset Graphics and Memory Controller Hub (GMCH)

Specification Update

November 2004

Notice: The Intel® 852GME/852PM chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 253562-003

Contents

Intel® 852GME/852PM Specification Update

Revision History

Revision	Description	Date
- 001	Initial Release	June 2003
- 002	Added specification update on support for Mobile Intel® Pentium® 4 Processors with Hyper-Threading Technology.	Sept 2003
- 003	• Added Errata A7/B7 • Added Specification Change #2 • Added Documentation Changes #1 & 2	November 2004

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Preface

This document is an update to the specifications contained in the *Intel® 852GME/852PM Chipset GMCH/MCH Datasheet*. It is intended for hardware system manufacturers. It contains Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

This NDA document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document will contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 852GME/852PM Chipset GMCH Datasheet: Intel® 82852GME/82852PM Graphics and Memory Controller Hub (GMCH)	253027

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 852GME/852PM Chipset GMCH/MCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 852GME and Intel 852PM chipset GMCH/MCH may be identified by the following register contents.

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	3580h	02h

NOTES:
1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 852GME and Intel 852PM chipset GMCH/MCH may be identified by the following component markings.

Stepping	S-Spec	QDF	Top Marking	Notes
A2	SL72K	QE29	RG82852GME	82852GME GMCH
A2	SL72J	QE50	RG82852PM	82852PM MCH

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Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 852GME/852PM chipset GMCH/MCH steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Note: Each Specification Update item is prefaced with a capital letter to distinguish the product. The key below details the letters that are used in this Intel® 852GME/852PM Chipset Specification Update.

A = Intel® 82852GME Graphics and Memory Controller Hub (GMCH)

B = Intel® 82852PM Memory Controller Hub (MCH)

Errata

NO.	Stepping A2	PLANS	ERRATA
A1,B1	X	No Fix	VGA Panning Test Issue
A2,B2	X	No Fix	VGA Timing issue
A3,B3	X	No Fix	Intermittent System hangs during power cycle test.
A4,B4	X	No Fix	AGP PCI Write to memory may be corrupted
A5,B5	X	No Fix	AGP write failure with ECC memory enabled

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NO.	Stepping A2	PLANS	ERRATA
A6,B6	X	No Fix	Display may flicker when integrated graphics and ECC support are enabled
A7,B7	X	No Fix	Anomalous System Behavior May Occur When AGP GART Size Is 64MB and APBASE bit 27 Is Set

Specification Changes

NO.	Stepping A2	PLANS	SPECIFICATION CHANGES
1	X		Added support for Mobile Intel® Pentium® 4 Processors with Hyper-Threading Technology.
2	X		24-Bit LVDS Will Not Be Supported On 852GME Platforms

Specification Clarifications

NO.	Stepping A2	PLANS	SPECIFICATION CLARIFICATIONS
1	X	No Fix	Strapping Option Clarification

Documentation Changes

NO.	Stepping A2	PLANS	DOCUMENTATION CHANGES
1	X	No Fix	Ball Definition For RSTIN# Incorrectly Shown In Table 49
2	X	No Fix	Sections 6.3 and 8 Incorrectly Show Some Signal Pins as Reserved

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Errata

1.   **A1,B1 - VGA Panning**

Problem: VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. This issue is seen in two test configurations.

    1. Test applications using a single VGA font table with a 32KB font buffer range could fail. The failure can occur using 64MB technology products that use 2KB and 4KB page sizes. This failure was seen in a diagnostic utility.

    2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

Implication: Entire scan lines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end user applications fail for this erratum.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon..

2.   **A2,B2 - VGA Timings**

Problem: Some VGA applications, running in 40-column modes that use a non-black border color may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists.

Status: There are no plans to fix this erratum in silicon

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3. **A3,B3 - Intermittent system hangs during BIOS memory testing when power cycle testing**

Problem: Systems may intermittently hang during BIOS memory testing as a result of the internal RCOMP state machine colliding with BIOS induced RCOMP cycle.

Implication: System hang may occur during boot-up or resume from S3. No other failures have been identified or reported. Issues are resolved with a BIOS workaround.

Workaround: Please refer to your Intel representative for BIOS workaround details.

Status: There are no plans to fix this erratum in silicon.

4. **A4,B4 - AGP PCI Write to system memory may be corrupted**

Problem: Display corruption or a system hang may result if an upstream AGP FRAME#-based PCI write crosses a 32-byte aligned boundary. Note that upstream AGP FRAME#-based PCI writes which cross a 32-byte aligned boundary are expected to be rare.

Implication: The issue may cause display corruption or a system hang. With the workaround implemented, Intel has done extensive validation and expects less than 3% impact on system performance.

Workaround: A BIOS workaround is available which disconnects upstream AGP FRAME#-based PCI writes to system memory at 32-byte aligned boundaries. Please refer to your Intel representative for BIOS workaround details.

Status: There are no plans to fix this erratum in silicon.

5. **A5,B5 - AGP write failure when ECC memory is enabled.**

Problem: Memory corruption or system hang may result if an AGP semantic write cycle targets a cache line in the AGP aperture window at the same time a PCI semantic write cycle from another PCI device is targeting the same cache line if ECC memory is enabled.

Implication: If ECC memory is enabled, data corruption or system hang may result.

Workaround: No workaround available. ECC memory will not be supported when using an AGP graphics device.

Status: There are no plans to fix this erratum in silicon.

6. **A6,B6 - Display may flicker when integrated graphics and ECC support are enabled.**

Problem: Display flicker and flashing may occur when integrated graphics and ECC support are enabled under certain graphics resolution modes.

Implication: A potentially undesirable amount of display flicker may occur.

Workaround: No workaround available.

Status: There are no plans to fix this erratum in silicon.

7. **A7, B7 - Anomalous system behavior may occur when AGP GART size is 64MB and APBASE bit 27 Is set**

Problem: Incorrect address decoded when AGP aperture size is set to 64MB and the aperture base has bit 27 set (e.g. APBASE=0xD8000000 causes failures, but 0xD0000000 is fine).

Implication: Problem may result in anomalous system behavior which can cause a system hang.

Workaround: Use an aperture base size of 128MB or 256MB. If using a 64MB aperture size, set APBASE such that bit 27 is cleared (e.g. use 0xD0000000 instead of 0xD8000000).

Status: There are no plans to fix this erratum in silicon.

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Specification Changes

1.   **Mobile Intel® Pentium® 4 processors with Hyper-Threading Technology is supported by the Intel® 852GME GMCH and the Intel® 852PM MCH.**

The following text should be added to the section titled "Intel 852PM Chipset MCH Features" under bullet "Processor/Host Bus Support" (p 12).

- Mobile Intel® Pentium® 4 processor with Hyper-Threading Technology

2.   **24-bit LVDS will not be supported on 852GME platforms**

Due to no availability of 24-Bit LVDS panels for validation, 24-Bit LVDS support is dropped from 852GME platforms. This change affects Section 5.5.2.1 paragraph 4. Any text stating support for 24-Bit LVDS should be ignored.

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Specification Clarifications

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1.   **Strapping Option Clarification**

Notes 1, 2, and 3 have been added to Table 53, "Strapping Configuration Table" in Section 7.1, pg 227 of the 852GME/852PM datasheet.

GST[2] **Note**: Intel 852GME GMCH Only	§Clock Config: Bit_2 PSB 400 = 0 PSB 533 = 1	See notes 1, 2, 3	DVO	Hi-Z

NOTES:
1. External pull-ups/downs will be required on the board to enable the non-default state of the straps.
2. Only GST[2] is used to strap the PSB frequency to either 400MHz or 533MHz, GST0 and GST1 must be left un-strapped.
3. DDR and GFX frequencies are set by BIOS programming of the HPLLCC register (D0,F3, reg C0-C1h).

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Documentation Changes

1.	**Ball definition for RSTIN# incorrectly shown in Table 49**

Section 6.2 Table 49, "XOR Chains Exclusion List" incorrectly shows the ball definition for RSTIN# to be D28. Actual ball definition is AD28. D28 is a VSS ball. This is the only reference where RSTIN# is incorrectly defined. Ballout and Package Information in Section 8 are correct.

2.	**Sections 6.3 and 8 incorrectly show some signal pins as reserved**

Section 6.3 Table 50 and Section 8 Table 55 show balls D2, D3, B3, F2, F3, L4 , & B2 as reserved. Balls should be defined as follows for Intel® 852GME and Intel® 852PM chipsets:

Ball	Signal Name
D2	GWBF#
D3	GRBF#
B3	GREQ#
F2	GSBSTB
F3	GSBSTB#
L4	GCBE2#
B2	GGNT#

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