November 2002
Revision 2.3

Geode™ CS1301/CS1311 Multimedia Companion: Media Coprocessor

General Description

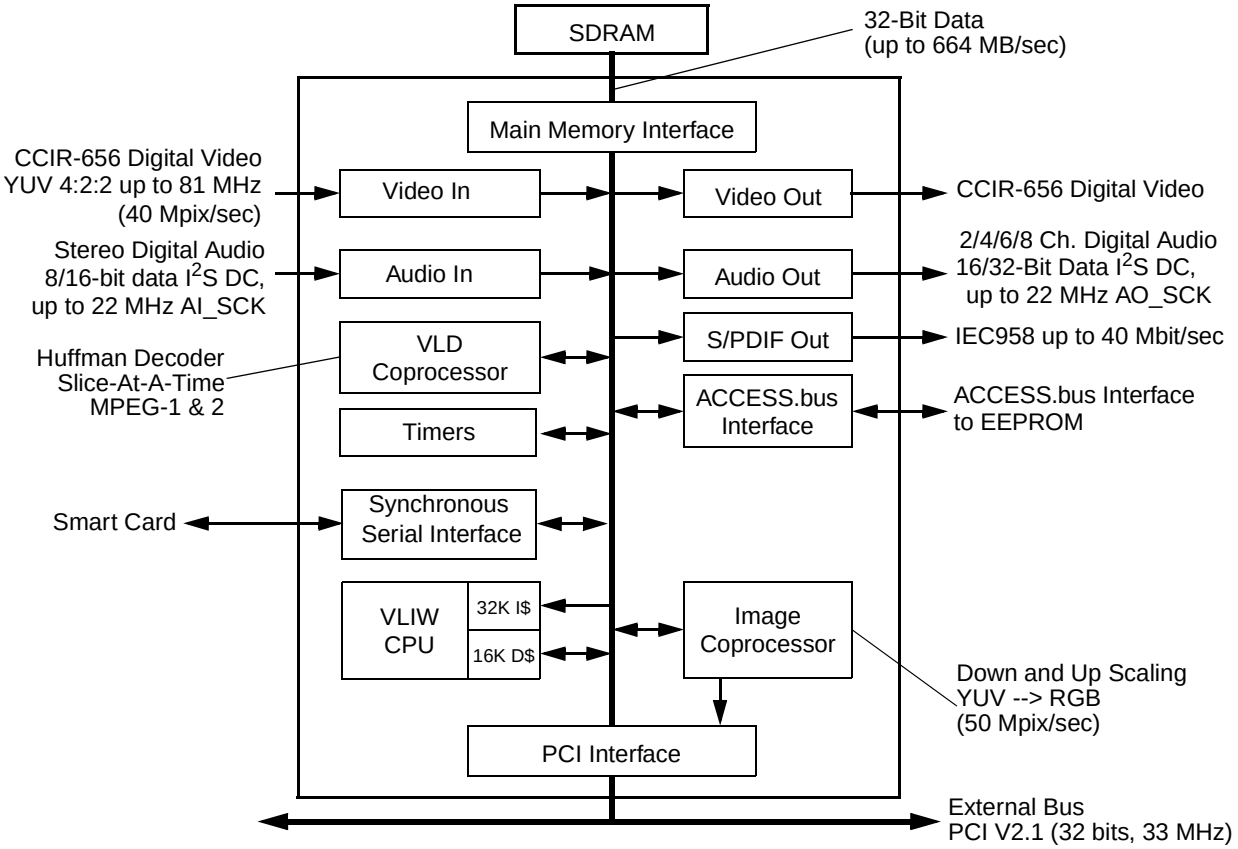
The National Semiconductor® Geode™ CS1301 and CS1311 multimedia companions act as coprocessors to decode multimedia in National's Geode single chip processor-based systems (i.e., SC1200/SC1201, SC2200, and SC3200, hereafter referred to as SCx200). They provide a multimedia experience for an Information Appliance (IA) user that cannot typically be achieved on a PC.

By implementing a dedicated coprocessor to perform multimedia tasks, a high quality video viewing experience can be achieved. This high quality is achieved by having a coprocessor architecture that is ideally suited for decoding digital media. In addition, since the decoding is not occurring on the SCx200, system events cannot interrupt the coprocessor's task of decoding media that can cause stuttering of sound or interruptions in the video.

Lower power consumption can also be achieved using the SCx200/CS1301 or SCx200/CS1311 solution. The CS1301/CS1311 has an architecture specifically designed for decoding media. The architecture is such that while decoding media, power is not consumed by portions of the system that are not used to decode media. Since the SCx200 is not decoding the media locally, it is able to go into a lower power state. When the CS1301/CS1311 is not decoding media, it uses almost no power.

Additionally, since the architecture is designed for decoding media, fewer CS1301/CS1311 cycles are required.

Internal Block Diagram



Features

General Features

- Physical
  - Process 0.25-micron CMOS
  - Packaged in a 292-terminal TEPBGA (Thermally Enhanced Plastic Ball Grid Array)
- Power supply:
  - CS1301: 2.5V Core; 3.3V I/O (5V tolerant)
  - CS1311: 2.2V Core; 3.3V I/O (5V tolerant)
- Consumption 1300 mA; 3.5W
- Power-down 300 mA
- Case Temperature 0° to 85°C

Central Processing Unit

- Clock speed:
  - CS1301: 180 MHz
  - CS1311: 166 MHz
- Instruction length variable (2 to 23 bytes)
- Instruction set arithmetic and logical operations, load/store operations, special multimedia and DSP operations, IEEE compliant floating point operations
- 27 pipelined functional units

Caches

- Data 16 KB, instructions 32 KB

Memory System

- Speed 166 MHz SDRAM
- CPU/memory programmable; 1:1, 5:4, 4:3, 3:2, and 2:1 speed ratios
- Memory size 512 KB to 64 MB (up to four banks)
- Recommended configurations:
  - 16 MB: Two 4M x 16 or two 2M x 32
  - 32 MB: Four 2M x 32 or four 4M x 16
- Width 32-bit bus
- Max. bandwidth 664 MB/sec (at 166 MHz)

Image Coprocessor

- Scaling programmable scale factor (0.2X to 10X) using 5-tap filters:
  - Horizontal or vertical scaling and filtering of individual Y, U, or V
  - Horizontal scaling and filtering with color conversion and overlay
  - YUV to RGB, RGB overlay and alpha blending, bit mask blanking

VLD Coprocessor

- Parses MPEG-1 and MPEG-2 elementary bit streams generating run-level pairs and filling macroblock headers

Timers

- Four 32-bit wide timers

Input/Output Support

- PCI Interface:
  - PCI 2.1 compliant
  - Speed 33 MHz
  - Bus width 32 bits
  - Voltage drive and receive at 3.3V
- Audio In (AI):
  - Two I^2S compliant channels
  - Sample size 8 or 16-bit samples per channel
- Audio Out (AO):
  - Eight I^2S compliant channels
  - Sample size 16- or 32-bit samples per channel
- Video In (VI):
  - Supported signals CCIR-601/656:
    - 8-bit video (up to 40 Mpix/sec)
  - Image sizes all sizes, subject to sample rate
  - Provides programmable on-the-fly 2X horizontal resolution subsampling
- Video Out (VO):
  - Image sizes flexible, including CCIR-601; max. 4K x 4K pixels (subject to 80 MB/sec data rate)
  - Outputs CCIR-601/656 8-bit video, PAL or NTSC
  - Clock rates programmable (4-80 MHz), typical 27 MB/sec (13.5 Mpix/sec for NTSC and PAL or 40 Mpix/sec in YUV 4:2:2 mode)
  - Features full 129-level alpha blending, GenLock mode, frame synchronization chroma key, programmable YUV color clipping
- S/PDIF Out:
  - Number of channels up to 6
  - Sample size 16 or 24 bits per channel
  - IEC-958, output up to 40 Mbits/sec
- ACCESS.bus Interface:
  - Supported modes single master only
  - Addressing 7-bit
  - Rates up to 400 Kbps
- SYNCHRONOUS SERIAL INTERFACE
  - Flexible bit serial connection
  - Full duplex

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1.0 System Architecture

The CS1301/CS1311 multimedia companion acts as a coprocessor to decode multimedia in National's Geode SC1200/SC1201, SC2200, and SC3200 (SCx200 unless otherwise specified). Figure 1-1 provides a typical system block diagram.

Media decoding is one of the most demanding system applications. If media is decoded on the main processor, a much higher performance processor is required to achieve even comparable levels of media decoding quality. Such a system would be significantly over-designed for other tasks, such as browsing the Internet. Using a low-cost processor that is ideally suited for all tasks, and adding the coprocessor for the high performance media decoding requirement, results in a cost-effective solution.

Another advantage of an processor/coprocessor solution is that an OEM (Original Equipment Manufacturer) can provide a scalable solution. A single board can be designed that supports the coprocessor. If it is desired to support a low-end product that does not support the high quality media decoding capabilities, the coprocessor and its supporting components can be excluded from the system, which results in additional savings in an already cost-effective design.

1.1 IMPORTANT DESIGN NOTE

The CS1301/CS1311 was designed to be a general purpose media data processor. As such, the CS1301/CS1311 is capable of far more than the current National CS1301/CS1311 solution. National is providing the device as part of a complete solution and supporting these target solutions only. Refer to the document titled "*CS1301/CS1311 MultiMedia Companion: System Architecture and Software Solution*" for the National Semiconductor supported solution.

1.2 SOFTWARE

The CS1301/CS1311 software and reference schematic is provided for a system that decodes media quickly with no original software development needed. As part of the CS1301/CS1311 purchase (see Section A.1 "Ordering Information" on page 21 for purchase details), National will license for the use of the operating system drivers and media decoder codecs in object form, which include:

- Communications manager driver.
- Video filter: Takes the video from the VIP (Video Input Port) of the Geode SCx200 and plays it back through the operating system media player.
- Various multimedia codecs.

1.2.1 Software Support

National provides a reference schematic and the associated software for a processor/coprocessor solution using the Geode SCx200 and the CS1301/CS1311. This implementation is currently supplied as a multimedia decoder for CE player under Microsoft Windows CE.net or Linux. Future support for Microsoft Windows XP is planned. Since this is a software-based DSP (Digital Signal Processor) coprocessor rather than strictly a silicon-based coprocessor, the software can be upgraded to support evolving media standards without a redesign of the hardware.

1.2.2 Software Features Support

For the currently supported system architectures and a complete list of supported MultiMedia codecs see the "*CS1301/CS1311 MultiMedia Companion: System Architecture and Software Solution*" document.

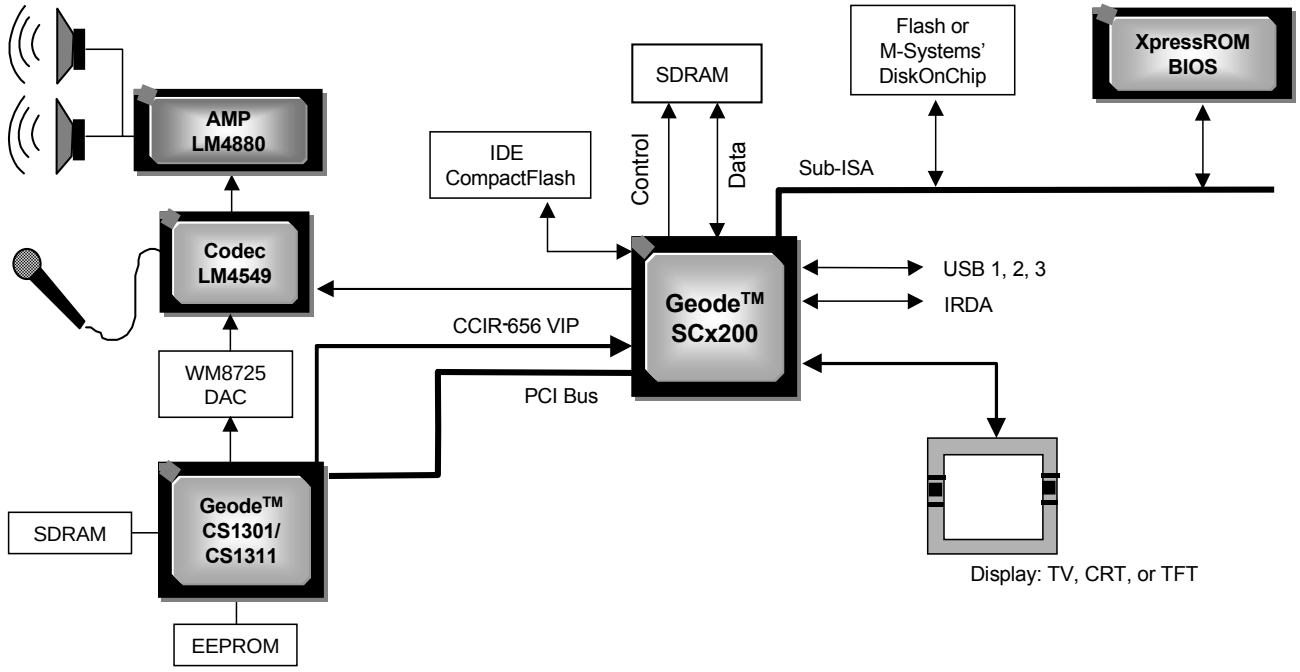


Figure 1-1. System Block Diagram

2.0 Signal Definitions

This section defines the signals and describes the external interface of the CS1301/CS1311 media companion. Figure 2-1 shows the signals organized by their functional groups.

The remaining subsections of this chapter describe:

- Section 2.1 "Ball Assignments": Provides a ball assignment diagram and tables listing the signals sorted according to ball number and alphabetically by signal name.
- Section 2.2 "Signal Descriptions": Detailed descriptions of each signal according to functional group.
- Section 2.3 "Reference Voltages": Discussion on ball reference voltages.

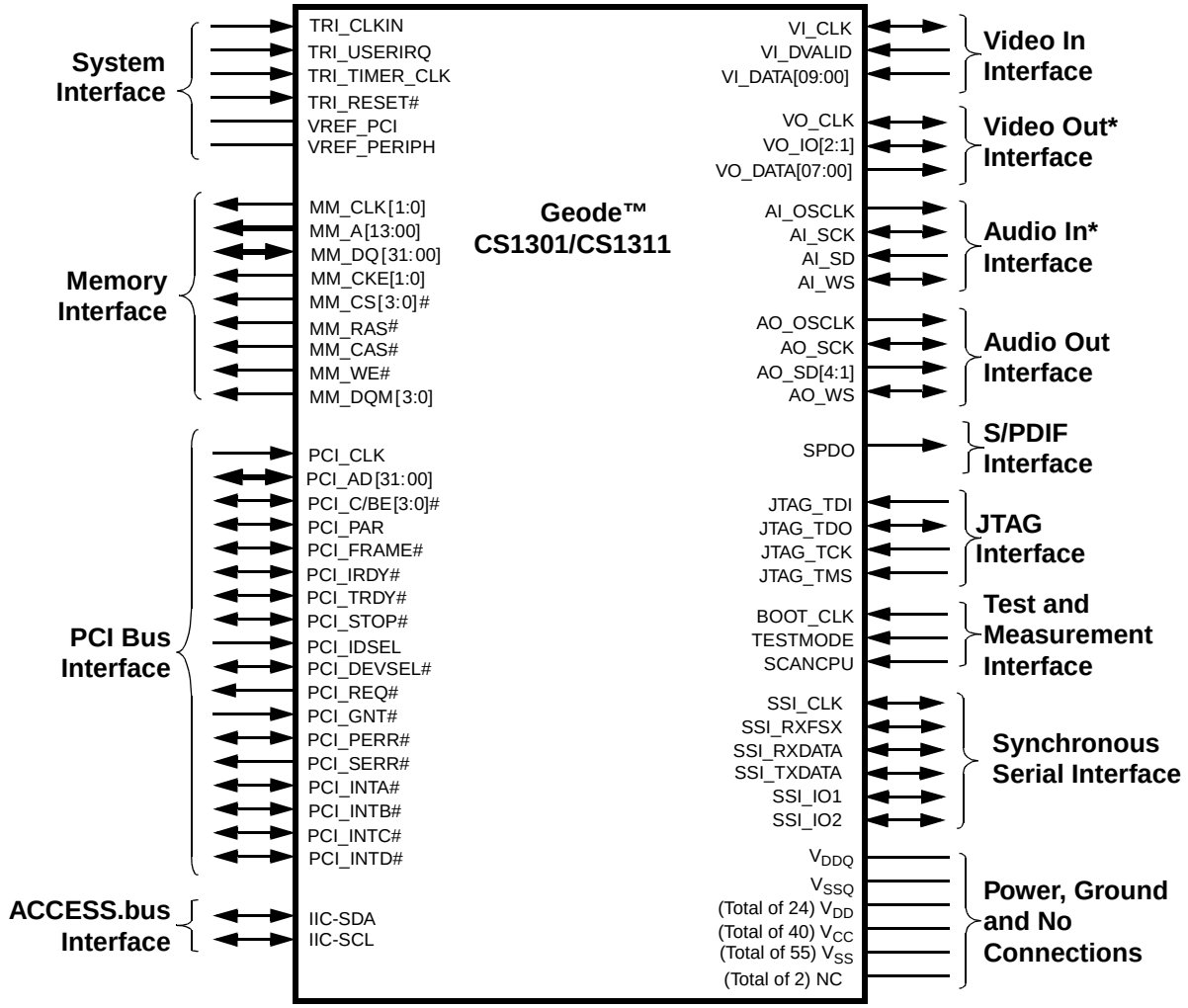
2.1 BALL ASSIGNMENTS

The CS1301/CS1311 has a total of 169 functional pins, excluding V_{DDQ}, V_{SSQ}, VREF_PCI, VREF_PERIPH, and digital power/ground. For pins with 5.0V input capability, the VREF_PCI or VREF_PERIPH determines 3.3V or 5.0V input tolerance. Unused pins can remain floating/unconnected; all pins that drive a clock should drive a series resistor.

Table 2-1 shows the types of I/O circuits used by the CS1301/CS1311 devices. Note that the # symbol in a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. Otherwise, the signal is asserted when at a high voltage level.

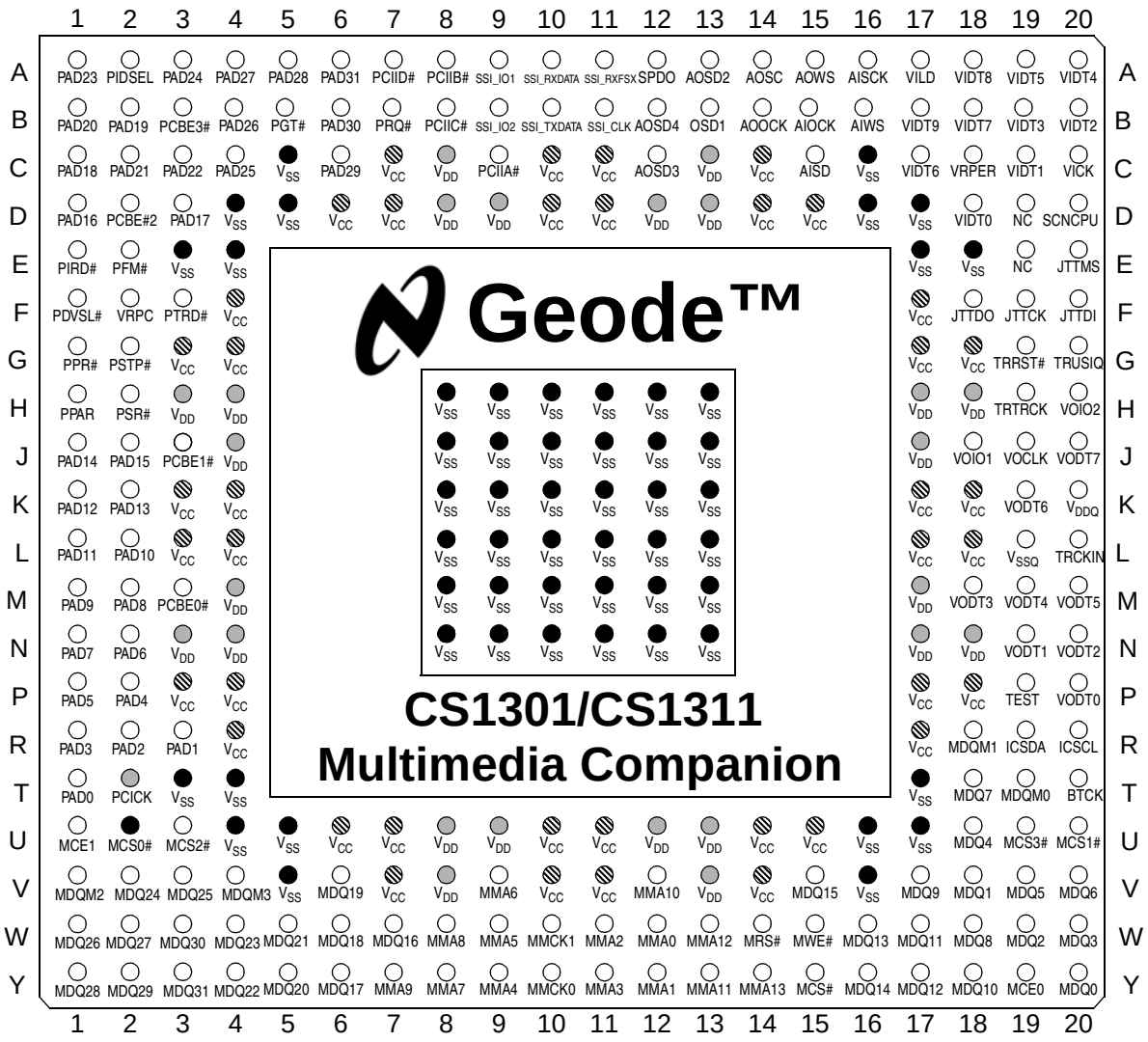
Table 2-1. Ball Type Descriptions

Modes	Description
I	Input only, except during boundary scan.
O	Output only, except during boundary scan.
OD	Open Drain output, active pull low, no active drive high, requires external pull-up.
I/O	Input or Output.
I/OD	Input with Open Drain output, active pull low, no active drive high, requires external pull-up.



*Video In and Audio In are supported by third party software solutions, not by the National Semiconductor solution.

Figure 2-1. Functional Block Diagram



Note: Signal names have been abbreviated in this figure due to space constraints.
- ● = GND Connection
- ◌ = CS1301 2.5V Core Power Connection; CS1311 2.2V Core Power Connection
- ▨ = 3.3V I/O Power Connection

Figure 2-2. 292-TEPBGA Ball Assignment Diagram

Table 2-2. Ball Assignment Sorted by Ball Number

Ball No.	Signal Name	Type
A1	PCI_AD23	I/O
A2	PCI_IDSEL	I
A3	PCI_AD24	I/O
A4	PCI_AD27	I/O
A5	PCI_AD28	I/O
A6	PCI_AD31	I/O
A7	PCI_INTD#	I/OD
A8	PCI_INTB#	I/O/OD
A9	SSI_IO1	I
A10	SSI_RXDATA	I
A11	SSI_RXFSX	I
A12	SPDO	O
A13	AO_SD2	O
A14	AO_SCK	I/O
A15	AO_WS	I/O
A16	AI_SCK	I/O
A17	VI_DVALID	I
A18	VI_DATA8	I
A19	VI_DATA5	I
A20	VI_DATA4	I
B1	PCI_AD20	I/O
B2	PCI_AD19	I/O
B3	PCI_C/BE3#	I/O
B4	PCI_AD26	I/O
B5	PCI_GNT#	I
B6	PCI_AD30	I/O
B7	PCI_REQ#	O
B8	PCI_INTC#	I/OD
B9	SSI_IO2	I/O
B10	SSI_TXDATA	O
B11	SSI_CLK	I
B12	AO_SD4	O
B13	AO_SD1	O
B14	AO_OSCLK	O
B15	AI_OSCLK	O
B16	AI_WS	I/O
B17	VI_DATA9	I
B18	VI_DATA7	I
B19	VI_DATA3	I
B20	VI_DATA2	I
C1	PCI_AD18	I/O
C2	PCI_AD21	I/O
C3	PCI_AD22	I/O
C4	PCI_AD25	I/O
C5	V_{SS}	GND
C6	PCI_AD29	I/O
C7	V_{CC}	PWR
C8	V_{DD}	PWR
C9	PCI_INTA#	I/OD
C10	V_{CC}	PWR
C11	V_{CC}	PWR
C12	AO_SD3	O

Ball No.	Signal Name	Type
C13	V_{DD}	PWR
C14	V_{CC}	PWR
C15	AI_SD	I
C16	V_{SS}	GND
C17	VI_DATA6	I
C18	VREF_PERIPH	PWR
C19	VI_DATA1	I
C20	VI_CLK	I/O
D1	PCI_AD16	I/O
D2	PCI_C/BE#2	I/O
D3	PCI_AD17	I/O
D4	V_{SS}	GND
D5	V_{SS}	GND
D6	V_{CC}	PWR
D7	V_{CC}	PWR
D8	V_{DD}	PWR
D9	V_{DD}	PWR
D10	V_{CC}	PWR
D11	V_{CC}	PWR
D12	V_{DD}	PWR
D13	V_{DD}	PWR
D14	V_{CC}	PWR
D15	V_{CC}	PWR
D16	V_{SS}	GND
D17	V_{SS}	GND
D18	VI_DATA0	I
D19	NC	---
D20	SCANCPU	I
E1	PCI_IRDY#	I/O
E2	PCI_FRAME#	I/O
E3	V_{SS}	GND
E4	V_{SS}	GND
E17	V_{SS}	GND
E18	V_{SS}	GND
E19	NC	---
E20	JTAG_TMS	I
F1	PCI_DEVSEL#	I/O
F2	VREF_PCI	PWR
F3	PCI_TRDY#	I/O
F4	V_{CC}	PWR
F17	V_{CC}	PWR
F18	JTAG_TDO	I/O
F19	JTAG_TCK	I
F20	JTAG_TDI	I
G1	PCI_PERR#	I/O
G2	PCI_STOP#	I/O
G3	V_{CC}	PWR
G4	V_{CC}	PWR
G17	V_{CC}	PWR
G18	V_{CC}	PWR

Ball No.	Signal Name	Type
G19	TRI_RESET#	I
G20	TRI_USERIRQ	I
H1	PCI_PAR	I/O
H2	PCI_SERR#	OD
H3	V_{DD}	PWR
H4	V_{DD}	PWR
H8	V_{SS}	GND
H9	V_{SS}	GND
H10	V_{SS}	GND
H11	V_{SS}	GND
H12	V_{SS}	GND
H13	V_{SS}	GND
H17	V_{DD}	PWR
H18	V_{DD}	PWR
H19	TRI_TIMER_CLK	I
H20	VO_IO2	I/O
J1	PCI_AD14	I/O
J2	PCI_AD15	I/O
J3	PCI_C/BE1#	I/O
J4	V_{DD}	PWR
J8	V_{SS}	GND
J9	V_{SS}	GND
J10	V_{SS}	GND
J11	V_{SS}	GND
J12	V_{SS}	GND
J13	V_{SS}	GND
J17	V_{DD}	PWR
J18	VO_IO1	I/O
J19	VO_CLK	I/O
J20	VO_DATA7	O
K1	PCI_AD12	I/O
K2	PCI_AD13	I/O
K3	V_{CC}	PWR
K4	V_{CC}	PWR
K8	V_{SS}	GND
K9	V_{SS}	GND
K10	V_{SS}	GND
K11	V_{SS}	GND
K12	V_{SS}	GND
K13	V_{SS}	GND
K17	V_{CC}	PWR
K18	V_{CC}	PWR
K19	VO_DATA6	O
K20	V_{DDQ}	PWR
L1	PCI_AD11	I/O
L2	PCI_AD10	I/O
L3	V_{CC}	PWR
L4	V_{CC}	PWR
L8	V_{SS}	GND

Table 2-2. Ball Assignment Sorted by Ball Number (Continued)

Ball No.	Signal Name	Type
L9	V_{SS}	GND
L10	V_{SS}	GND
L11	V_{SS}	GND
L12	V_{SS}	GND
L13	V_{SS}	GND
L17	V_{CC}	PWR
L18	V_{CC}	PWR
L19	V_{SSQ}	GND
L20	TRI_CLKIN	I
M1	PCI_AD09	I/O
M2	PCI_AD08	I/O
M3	PCI_C/BE0#	I/O
M4	V_{DD}	PWR
M8	V_{SS}	GND
M9	V_{SS}	GND
M10	V_{SS}	GND
M11	V_{SS}	GND
M12	V_{SS}	GND
M13	V_{SS}	GND
M17	V_{DD}	PWR
M18	VO_DATA3	O
M19	VO_DATA4	O
M20	VO_DATA5	O
N1	PCI_AD07	I/O
N2	PCI_AD06	I/O
N3	V_{DD}	PWR
N4	V_{DD}	PWR
N8	V_{SS}	GND
N9	V_{SS}	GND
N10	V_{SS}	GND
N11	V_{SS}	GND
N12	V_{SS}	GND
N13	V_{SS}	GND
N17	V_{DD}	PWR
N18	V_{DD}	PWR
N19	VO_DATA1	O
N20	VO_DATA2	O
P1	PCI_AD05	I/O
P2	PCI_AD04	I/O
P3	V_{CC}	PWR
P4	V_{CC}	PWR
P17	V_{CC}	PWR
P18	V_{CC}	PWR
P19	TESTMODE	I
P20	VO_DATA0	O
R1	PCI_AD03	I/O
R2	PCI_AD02	I/O
R3	PCI_AD01	I/O
R4	V_{CC}	PWR
R17	V_{CC}	PWR
R18	MM_DQM1	O
R19	IIC_SDA	I/OD
R20	IIC_SCL	I/OD
T1	PCI_AD00	I/O
T2	PCI_CLK	I
T3	V_{SS}	GND
T4	V_{SS}	GND
T17	V_{SS}	GND
T18	MM_DQ07	I/O
T19	MM_DQM0	O
T20	BOOT_CLK	I
U1	MM_CKE1	O
U2	MM_CS0#	O
U3	MM_CS2#	O
U4	V_{SS}	GND
U5	V_{SS}	GND
U6	V_{CC}	PWR
U7	V_{CC}	PWR
U8	V_{DD}	PWR
U9	V_{DD}	PWR
U10	V_{CC}	PWR
U11	V_{CC}	PWR
U12	V_{DD}	PWR
U13	V_{DD}	PWR
U14	V_{CC}	PWR
U15	V_{CC}	PWR
U16	V_{SS}	GND
U17	V_{SS}	GND
U18	MM_DQ04	I/O
U19	MM_CS3#	O
U20	MM_CS1#	O
V1	MM_DQM2	O
V2	MM_DQ24	I/O
V3	MM_DQ25	I/O
V4	MM_DQM3	O
V5	V_{SS}	GND
V6	MM_DQ19	I/O
V7	V_{CC}	PWR
V8	V_{DD}	PWR
V9	MM_A06	O
V10	V_{CC}	PWR
V11	V_{CC}	PWR
V12	MM_A10	O
V13	V_{DD}	PWR
V14	V_{CC}	PWR
V15	MM_DQ15	I/O
V16	V_{SS}	GND
V17	MM_DQ09	I/O
V18	MM_DQ01	I/O
V19	MM_DQ05	I/O
V20	MM_DQ06	I/O
W1	MM_DQ26	I/O
W2	MM_DQ27	I/O
W3	MM_DQ30	I/O
W4	MM_DQ23	I/O
W5	MM_DQ21	I/O
W6	MM_DQ18	I/O
W7	MM_DQ16	I/O
W8	MM_A08	O
W9	MM_A05	O
W10	MM_CLK1	O
W11	MM_A02	O
W12	MM_A00	O
W13	MM_A12	O
W14	MM_RAS#	O
W15	MM_WE#	O
W16	MM_DQ13	I/O
W17	MM_DQ11	I/O
W18	MM_DQ08	I/O
W19	MM_DQ02	I/O
W20	MM_DQ03	I/O
Y1	MM_DQ28	I/O
Y2	MM_DQ29	I/O
Y3	MM_DQ31	I/O
Y4	MM_DQ22	I/O
Y5	MM_DQ20	I/O
Y6	MM_DQ17	I/O
Y7	MM_A09	O
Y8	MM_A07	O
Y9	MM_A04	O
Y10	MM_CLK0	O
Y11	MM_A03	O
Y12	MM_A01	O
Y13	MM_A11	O
Y14	MM_A13	O
Y15	MM_CAS#	O
Y16	MM_DQ14	I/O
Y17	MM_DQ12	I/O
Y18	MM_DQ10	I/O
Y19	MM_CKE0	O
Y20	MM_DQ00	I/O

Table 2-3. Ball Assignment Sorted Alphabetically by Signal Name

Signal Name	Ball No.
AI_OSCLK	B15
AI_SCK	A16
AI_SD	C15
AI_WS	B16
AO_OSCLK	B14
AO_SCK	A14
AO_SD1	B13
AO_SD2	A13
AO_SD3	C12
AO_SD4	B12
AO_WS	A15
BOOT_CLK	T20
IIC_SCL	R20
IIC_SDA	R19
JTAG_TCK	F19
JTAG_TDI	F20
JTAG_TDO	F18
JTAG_TMS	E20
MM_A00	W12
MM_A01	Y12
MM_A02	W11
MM_A03	Y11
MM_A04	Y9
MM_A05	W9
MM_A06	V9
MM_A07	Y8
MM_A08	W8
MM_A09	Y7
MM_A10	V12
MM_A11	Y13
MM_A12	W13
MM_A13	Y14
MM_CAS#	Y15
MM_CKE0	Y19
MM_CKE1	U1
MM_CLK0	Y10
MM_CLK1	W10
MM_CS0#	U2
MM_CS1#	U20
MM_CS2#	U3
MM_CS3#	U19
MM_DQ00	Y20
MM_DQ01	V18
MM_DQ02	W19
MM_DQ03	W20
MM_DQ04	U18
MM_DQ05	V19
MM_DQ06	V20
MM_DQ07	T18
MM_DQ08	W18
MM_DQ09	V17
MM_DQ10	Y18

Signal Name	Ball No.
MM_DQ11	W17
MM_DQ12	Y17
MM_DQ13	W16
MM_DQ14	Y16
MM_DQ15	V15
MM_DQ16	W7
MM_DQ17	Y6
MM_DQ18	W6
MM_DQ19	V6
MM_DQ20	Y5
MM_DQ21	W5
MM_DQ22	Y4
MM_DQ23	W4
MM_DQ24	V2
MM_DQ25	V3
MM_DQ26	W1
MM_DQ27	W2
MM_DQ28	Y1
MM_DQ29	Y2
MM_DQ30	W3
MM_DQ31	Y3
MM_DQM0	T19
MM_DQM1	R18
MM_DQM2	V1
MM_DQM3	V4
MM_RAS#	W14
MM_WE#	W15
NC (Total of 2)	E19, D19
PCI_AD00	T1
PCI_AD01	R3
PCI_AD02	R2
PCI_AD03	R1
PCI_AD04	P2
PCI_AD05	P1
PCI_AD06	N2
PCI_AD07	N1
PCI_AD08	M2
PCI_AD09	M1
PCI_AD10	L2
PCI_AD11	L1
PCI_AD12	K1
PCI_AD13	K2
PCI_AD14	J1
PCI_AD15	J2
PCI_AD16	D1
PCI_AD17	D3
PCI_AD18	C1
PCI_AD19	B2
PCI_AD20	B1
PCI_AD21	C2
PCI_AD22	C3
PCI_AD23	A1

Signal Name	Ball No.
PCI_AD24	A3
PCI_AD25	C4
PCI_AD26	B4
PCI_AD27	A4
PCI_AD28	A5
PCI_AD29	C6
PCI_AD30	B6
PCI_AD31	A6
PCI_C/BE0#	M3
PCI_C/BE1#	J3
PCI_C/BE2#	D2
PCI_C/BE3#	B3
PCI_CLK	T2
PCI_DEVSEL#	F1
PCI_FRAME#	E2
PCI_GNT#	B5
PCI_IDSEL	A2
PCI_INTA#	C9
PCI_INTB#	A8
PCI_INTC#	B8
PCI_INTD#	A7
PCI_IRDY#	E1
PCI_PAR	H1
PCI_PERR#	G1
PCI_REQ#	B7
PCI_SERR#	H2
PCI_STOP#	G2
PCI_TRDY#	F3
SCANCPU	D20
SPDO	A12
SSI_CLK	B11
SSI_IO1	A9
SSI_IO2	B9
SSI_RXDATA	A10
SSI_RXFSX	A11
SSI_TXDATA	B10
TESTMODE	P19
TRI_CLKIN	L20
TRI_RESET#	G19
TRI_TIMER_CLK	H19
TRI_USERIRQ	G20
V_{CC} (3.3V I/O Power Supply, Total of 40)	C7, C10, C11, C14, D6, D7, D10, D11, D14, D15, F4, F17, G3, G4, G17, G18, K3, K4, K17, K18, L3, L4, L17, L18, P3, P4, P17, P18, R4, R17, U6, U7, U10, U11, U14, U15, V7, V10, V11, V14

Signal Name	Ball No.
V_{DD} (2.5V Core Power Supply, Total of 24)	C8, C13, D8, D9, D12, D13, H3, H4, H17, H18, J4, J17, M4, M17, N3, N4, N17, N18, U8, U9, U12, U13, V8, V13
V_{DDQ}	K20
VI_CLK	C20
VI_DATA0	D18
VI_DATA1	C19
VI_DATA2	B20
VI_DATA3	B19
VI_DATA4	A20
VI_DATA5	A19
VI_DATA6	C17
VI_DATA7	B18
VI_DATA8	A18
VI_DATA9	B17
VI_DVALID	A17
VO_CLK	J19
VO_DATA0	P20
VO_DATA1	N19
VO_DATA2	N20
VO_DATA3	M18
VO_DATA4	M19
VO_DATA5	M20
VO_DATA6	K19
VO_DATA7	J20
VO_IO1	J18
VO_IO2	H20
VREF_PCI	F2
VREF_PERIPH	C18
V_{SS} (Ground Connection, Total of 55)	C5, C16, D4, D5, D16, D17, E3, E4, E17, E18, H8, H9, H10, H11, H12, H13, J8, J9, J10, J11, J12, J13, K8, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L13, M8, M9, M10, M11, M12, M13, N8, N9, N10, N11, N12, N13, T3, T4, T17, U4, U5, U16, U17, V5, V16,
V_{SSQ}	L19

2.2 SIGNAL DESCRIPTIONS

2.2.1 System Interface Signals

Signal Name	Ball No.	Type	Description
TRI_CLKIN	L20	I	**Main Input Clock.** The SDRAM clock outputs (MM_CLK0 and MM_CLK1) can be set to 2x or 3x this frequency. The on-chip DSPCPU clock (DSPCPU_CLK) can be set to 1x, 5/4, 4/3, 3/2, or 2x the SDRAM clock frequency. The maximum recommended ppm level is ±100 ppm or lower to improve jitter on generated clocks. The duty cycle should not exceed 30/70% asymmetry. The operating limits of the internal PLLs are: • 27 MHz < Output of the SDRAM PLL < 200 MHz • 33 MHz < Output of the CPU PLL < 266 MHz These are not the speed grades of the chips, just the PLL limits.
TRI_USERIRQ	G20	I	**General Purpose Level/Edge Interrupt Input.** Vectored interrupt source number 4.
TRI_TIMER_CLK	H19	I	**External General Purpose Clock Source for Timers**. Maximum 40 MHz.
TRI_RESET#	G19	I	**CS1301/CS1311 RESET Input.** This pin can be tied to the PCI_RST# signal in PCI bus systems. Upon releasing RESET, the CS1301/CS1311 initiates its boot protocol.
VREF_PCI	F2	PWR	**PCI Voltage Reference.** Determines the mode of operation of the PCI pins. VREF_PCI must be connected to V_{SS} (0V) for use in 3.3V PCI signaling environment, as is the case for a Geode SCx200 system. The supply to this pin should be AC bypassed and provide 40 mA of DC sink or source capability.
VREF_PERIPH	C18	PWR	**Peripheral Voltage Reference.** Determines the mode of operation of the I/O pins listed in Section 2.3 "Reference Voltages" on page 18. VREF_PERIPH must be connected to 5.0V if the designated I/O pins listed in Section 2.3 should be 5.0V input voltage capable. VREF_PERIPH must be connected to V_{SS} (0V) if the designated I/O pins listed in Section 2.3 are 3.3V only inputs. The supply to this pin should be AC bypassed and provide 40 mA of DC sink or source capability.

2.2.2 Memory Interface Signals

Signal Name	Ball No.	Type	Description
MM_CLK0	Y10	O	**SDRAM Output Clock (at 2x or 3x TRI_CLKIN frequency).** Two identical outputs are provided to reliably drive several small memory configurations without external glue. A series terminating resistor close to CS1301/CS1311 is required to reduce ringing. For driving a 50Ω trace, a resistor of 27 to 33Ω is recommended. The use of higher impedance traces in the SDRAM signals is not recommended.
MM_CLK1	W10		

2.2.2 Memory Interface Signals (Continued)

Signal Name	Ball No.	Type	Description
MM_A[13:00]	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	O	**Address Bus**. Used for row and column addresses. WARNING: Do not connect MM_A[13:11] directly to SDRAM A[13:11] pins. Refer to Chapter 12 of the SDRAM Memory System of the Philips Semiconductor *PNX1300 Series Media Processors Data Book* for accurate connection diagrams.
MM_DQ[31:00]	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	I/O	**32-Bit Data I/O Bus.** The Main Memory Interface module also supports a 16-bit I/O interface.
MM_CKE0	Y19	O	**Clock Enable Output to SDRAMs.** Two identical outputs are provided in order to reliably drive several small memory configurations without external glue.
MM_CKE1	U1		
MM_CS0#	U2	O	**Chip Select for DRAM rank n; active low.** The chip select pins may be used as address pins to support the 256-Mbit SDRAM device organized in x16.
MM_CS1#	U20		
MM_CS2#	U3		
MM_CS3#	U19		
MM_RAS#	W14	O	**Row Address Strobe; active low.**
MM_CAS#	Y15	O	**Column Address Strobe; active low.**
MM_WE#	W15	O	**Write Enable; active low**.
MM_DQM0	T19	O	**Data Mask Enable.** These are byte-enable signals for the 32-bit MM_DQ bus.
MM_DQM1	R18		
MM_DQM2	V1		
MM_DQM3	V4		

2.2.3 PCI Interface Signals

Signal Name	Ball No.	Type	Description
PCI_CLK	T2	I	**PCI Clock.** All PCI input signals are sampled with respect to the rising edge of this clock. All PCI outputs are generated based on this clock. This clock is required for normal operation of the PCI module.

2.2.3 PCI Interface Signals (Continued)

Signal Name	Ball No.	Type	Description
PCI_AD[31:00]	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	I/O	**Multiplexed Address and Data.**
PCI_C/BE0#	M3	I/O	**Multiplexed Bus Commands and Byte-Enables**. High for command, low for byte-enable.
PCI_C/BE1#	J3		
PCI_C/BE2#	D2		
PCI_C/BE3#	B3		
PCI_PAR	H1	I/O	**Parity.** Even parity across AD and C/BE# lines.
PCI_FRAME#	E2	I/O	**Frame Sustained TRI-STATE.** Frame is driven by a master to indicate the beginning and duration of an access.
PCI_IRDY#	E1	I/O	**Initiator Ready Sustained TRI-STATE.** Initiator Ready indicates that the bus master is ready to complete the current data phase.
PCI_TRDY#	F3	I/O	**Target Ready Sustained TRI-STATE.** Target Ready indicates that the bus target is ready to complete the current data phase.
PCI_STOP#	G2	I/O	**Stop Sustained TRI-STATE.** Indicates that the target is requesting that the master stop the current transaction.
PCI_IDSEL	A2	I	**ID Select.** Used as chip select during configuration read/write cycles.
PCI_DEVSEL#	F1	I/O	**Device Select Sustained TRI-STATE.** Indicates whether any device on the bus has been selected.
PCI_REQ#	B7	O	**Request.** Driven by the CS1301/CS1311 as a PCI bus master to request use of the PCI bus.
PCI_GNT#	B5	I	**Grant.** Indicates to the CS1301/CS1311 that access to the PCI bus has been granted.
PCI_PERR#	G1	I/O	**Parity Error Sustained TRI-STATE.** Parity error generated/received by CS1301/CS1311.
PCI_SERR#	H2	OD	**System Error.** This signal is asserted when operating as a target and detecting an address parity error.
PCI_INTA#	C9	I/OD	**PCI Interrupts A, B, C, and D.** Can operate as an input (power-up default) or output, as determined by direction control bits in PCI MMIO register INT_CTL. As an input, PCI_INT# can be used to receive PCI interrupt requests (normal PCI use is active low, level-sensitive mode, but the Vectored Interrupt Controller (VIC) can be set to treat these as a positive edge triggered mode). As an input, PCI_INT# can also be used as a general interrupt request if not needed for PCI. As an output, the value of a PCI_INT# can be programmed through PCI MMIO registers to generate interrupts for other PCI masters.
PCI_INTB#	A8	I/O/OD	
PCI_INTC#	B8	I/OD	
PCI_INTD#	A7	I/OD	
Note: Current buffer design allows drive/receive from either 3.3V or 5.0V PCI bus.			

2.2.4 Video In Interface Signals

Signal Name	Ball No.	Type	Description
VI_CLK	C20	I/O	**Clock.** This signal can be configured as either an input or an output. If configured as an input (power-up default): A positive transition on this incoming video clock pin samples VI_DATA[09:00] if VI_DVALID is high. If VI_DVALID is low, VI_DATA[09:00] is ignored. Clock and data rates of up to 81 MHz are supported. The CS1301/CS1311 supports an additional mode where VI_DATA[09:08] in message passing mode are not affected by the VI_DVALID signal. If configured as an output: VI_CLK performs as a programmable output clock to drive an external video A/D converter. It can be programmed to emit integral dividers of DSPCPU_CLK. If used as an output, a board level 27 to 33Ω series resistor is recommended to reduce ringing.
VI_DVALID	A17	I	**Data Valid.** VI_DVALID indicates that valid data is present on VI_DATA[09:00]. If high, VI_DATA will be accepted on the next VI_CLK positive edge. If low, VI_DATA[09:00] will not be sampled. However, the CS1301/CS1311 supports an additional mode where VI_DATA[9:8] in message passing mode are not affected by the VI_DVALID signal.
VI_DATA[07:00]	B18, C17, A19, A20, B19, B20, C19, D18	I	**Data Bus Lines [7:0].** CCIR-656 style YUV 4:2:2 data from a digital camera or general purpose high speed data input pins. Sampled on VI_CLK if VI_DVALID is high.
VI_DATA[09:08]	B17, A18		**Data Bus Lines [9:8].** Extension high speed data input bits to allow use of 10-bit video A/D converters in raw10 modes. VI_DATA[08] serves as START and VI_DATA[09] as END message input in message passing mode. Sampled on positive transitions of VI_CLK if VI_DVALID is high. The CS1301/CS1311 supports an additional mode where VI_DATA[09:08] in message passing mode are not affected by the VI_DVALID signal.
Note: Video In and Audio In are supported by third party software solutions, not by the National solution.			

2.2.5 Video Out Interface Signals

Signal Name	Ball No.	Type	Description
VO_CLK	J19	I/O	**Clock.** The VO module emits VO_DATA[07:00] on a positive edge of VO_CLK. VO_CLK can be configured as an input (reset default) or output. If configured as an input: VO_CLK is received from external display clock master circuitry. If configured as an output: The CS1301/CS1311 emits a programmable clock frequency. The emitted frequency can be set between approximately 4 and 81 MHz with a sub-Hertz resolution. The clock generated is frequency accurate and has low jitter properties due to a combination of an on-chip DDS (Direct Digital Synthesizer) and VCO/PLL. If used as an output, a board level 27 to 33Ω series resistor is recommended to reduce ringing.
VO_IO1	J18	I/O	**Input/Output 1.** This pin can function as HS (Horizontal Sync) output or as STMSG (Start Message) output. If set as HS output; VO_IO1 outputs the HS output signal. In message passing mode, VO_IO1 acts as the STMSG output signal.

2.2.5 Video Out Interface Signals (Continued)

Signal Name	Ball No.	Type	Description
VO_IO2	H20	I/O	**Input/Output 2.** This pin can function as FS (Frame Sync) input, FS output or as ENDMSG (End Message) output. If set as FS input, it can be set to respond to positive or negative edge transitions. If the VO module operates in external sync mode and the selected transition occurs, the VO module sends two fields of video data. Note: This works only once after a reset. In message passing mode, this pin acts as ENDMSG output signal.
VO_DATA[07:00]	K20, K12, M20, M19, M18, N20, N19, P20	O	**Data Bus.** CCIR-656 style YUV 4:2:2 digital output data, or general purpose high-speed data output channel. Output changes on the positive edge of VO_CLK.

2.2.6 Audio In Interface Signals

Signal Name	Ball No.	Type	Description
AI_OSCLK	B15	O	**Over-Sampling Clock.** This output can be programmed to emit any frequency up to 40 MHz with a sub-Hertz resolution. It is intended for use as the $256f_S$ or $384f_S$ over-sampling clock by the external A/D subsystem. A board level 27 to 33Ω series resistor is recommended to reduce ringing.
AI_SCK	A16	I/O	**Serial Clock.** When the AI module is programmed as a serial-interface timing slave (power-up default), AI_SCK is an input. AI_SCK receives the serial bit clock from the external A/D subsystem. This clock is treated as fully asynchronous to the CS1301/CS1311 main clock. When the AI module is programmed as the serial-interface timing master, AI_SCK is an output. AI_SCK drives the serial clock for the external A/D subsystem. The frequency is a programmable integral divisor of the AI_OSCLK frequency. AI_SCK is limited to 22 MHz. The sample rate of valid samples embedded within the serial stream is variable. If used as an output, a board level 27 to 33Ω series resistor is recommended to reduce ringing.
AI_SD	C15	I	**Serial Data**. Serial data from external A/D subsystem. Data on this pin is sampled on the positive or negative edges of AI_SCK as determined by the CLOCK_EDGE bit in the AI_SERIAL register.
AI_WS	B16	I/O	**Word-Select.** AI_WS is the word-select or frame-synchronization signal from/to the external A/D subsystem. When the AI module is programmed as the serial-interface timing slave (power-up default), AI_WS acts as an input. AI_WS is sampled on the same edge as selected for AI_SD. When the AI module is programmed as the serial-interface timing master, AI_WS acts as an output. It is asserted on the opposite edge of the AI_SD sampling edge.
Note: The AI module always acts as a receiver, but can be master or slave for A/D timing. Video In and Audio In are supported by third party software solutions, not by the National solution.			

2.2.7 Audio Out Interface Signals

Signal Name	Ball No.	Type	Description
AO_OSCLK	B14	O	**Over-Sampling Clock**. This output can be programmed to emit any frequency up to 40 MHz, with a sub-Hertz resolution. It is intended for use as the 256 or 384 f_S over-sampling clock by the external D/A conversion subsystem. A board-level 27 to 33Ω series resistor is recommended to reduce ringing.
AO_SCK	A14	I/O	**Serial Clock**. When the Audio Out (AO) module is programmed to act as the serial interface timing slave (power-up default), AO_SCK acts as an input. It receives the Serial Clock from the external audio D/A subsystem. The clock is treated as fully asynchronous to the CS1301/CS1311 main clock. When the AO module is programmed to act as the serial interface timing master, AO_SCK acts as an output. It drives the serial clock for the external audio D/A subsystem. The clock frequency is a programmable integral divisor of the AO_OSCLK frequency. AO_SCK is limited to 22 MHz. The sample rate of valid samples embedded within the serial stream is variable. If used as an output, a board-level 27 to 33Ω series resistor is recommended to reduce ringing.
AO_SD1	B13	O	**Serial Data Buses**. Serial data to external stereo audio D/A subsystem. The timing of transitions on this output is determined by the CLOCK_EDGE bit in the AO_SERIAL register, and can be on positive or negative AO_SCK edges.
AO_SD2	A13		
AO_SD3	C12		
AO_SD4	B12		
AO_WS	A15	I/O	**Word-Select or Frame synchronization**. Signal from/to the external D/A subsystem. Each audio channel receives one sample for every WS period. When the AO module is programmed as the serial interface timing slave (power-up default), AO_WS acts as an input. AO_WS is sampled on the opposite AO_SCK edge from which AO_SDx are asserted. When the AO module is programmed as serial interface timing master, AO_WS acts as an output. AO_WS is asserted on the same AO_SCK edge as AO_SDx.
Note: The AO module always acts as sender, but can be master or slave for D/A timing.			

2.2.8 S/PDIF Interface Signals

Signal Name	Ball No.	Type	Description
SPDO	A12	O	**S/PDIF Data Out.** Self-clocking serial data stream as per IEC958, with 1937 extensions. Note that the low impedance output buffer requires a 27 to 33Ω series terminator close to CS1301/CS1311 in order to match the board trace impedance. This series terminator must be part of the voltage divider needed to create the coaxial output through the AC isolation transformer.

2.2.9 ACCESS.bus Interface Signals

Signal Name	Ball No.	Type	Description
IIC_SDA	R19	I/OD	**ACCESS.bus Serial Data.**
IIC_SCL	R20	I/OD	**ACCESS.bus Serial Clock.**

2.2.10 JTAG Interface Signals

Signal Name	Ball No.	Type	Description
JTAG_TDI	F20	I	**JTAG Test Data Input.**
JTAG_TDO	F18	I/O	**JTAG Test Data Output.** This pin can either drive active low, high, or float.
JTAG_TCK	F19	I	**JTAG Test Clock Input.**
JTAG_TMS	E20	I	**JTAG Test Mode Select Input.**

2.2.11 Test and Measurement Interface Signals

Signal Name	Ball No.	Type	Description
BOOT_CLK	T20	I	**Boot Clock.** Used for testing purposes. Must be connected to TRI_CLKIN for normal operation.
TESTMODE	P19	I	**Test Mode.** Used for testing purposes. Must be connected to V_{SS} for normal operation.
SCANCPU	D20	I	**Scan CPU.** Used for testing purposes. Must be connected to V_{SS} for normal operation.

2.2.12 Synchronous Serial Interface (SSI)

Signal Name	Ball No.	Type	Description
SSI_CLK	B11	IN	**Clock.** Clock signal of the synchronous serial interface to an off-chip modem analog frontend or ISDN terminal adapter; provided by the receive channel of an external communication device.
SSI_RXFSX	A11	IN	**Receive Sync.** Receive frame sync reference of the synchronous serial interface. Provided by the receive channel of an external communication device.
SSI_RXDATA	A10	IN	**Receive Data.** Receive Serial Data Input; provided by the receive channel of an external communication device.
SSI_TXDATA	B10	OUT	**Transmit Data.** Transmit serial data output. Sent to the transmit channel of the external communication device.
SSI_IO1	A9	I/O	**I/O 1.** General Purpose Programmable I/O. Set to input on power up.
SSI_IO2	B9	I/O	**I/O 2.** General Purpose Programmable I/O. Set to input on power up. Can also be programmed to function as the transmit channel frame synchronization reference output.

2.2.13 Power, Ground, and No Connections

Signal Name	Ball No.	Type	Description
V_{DDQ}	K20	PWR	**Quiet V_{DD} for the PLL Subsystem.** Should be supplied from V_{DD} through a low-Q series inductor. It should be bypassed for AC to V_{SSQ}, using a dual capacitor bypass (high and low frequency AC bypass).

2.2.13 Power, Ground, and No Connections (Continued)

Signal Name	Ball No.	Type	Description
V_{SSQ}	L19	GND	**Quiet V_{SS} for the PLL Subsystem.** Should be AC bypassed to V_{DDQ}, otherwise left DC floating. It is connected on-chip to V_{SS}. No external coil or other connection to board ground is needed; such a connection would create a ground loop.
V_{DD}	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	PWR	**2.5V CS1301 Core Power Connection (Total of 24).** **2.2V CS1311 Core Power Connection (Total of 24).**
V_{CC}	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	PWR	**3.3V I/O Power Connection (Total of 24).**
V_{SS}	See Table 2-3 "Ball Assignment Sorted Alphabetically by Signal Name" on page 9	GND	**Ground Connection (Total of 50).**
NC	E19, D19	---	**No Connection.** For normal operation, leave unconnected.

2.3 REFERENCE VOLTAGES

Outputs always drive to a level determined by the 3.3V I/O voltage, with the exception of Open Drain mode outputs.

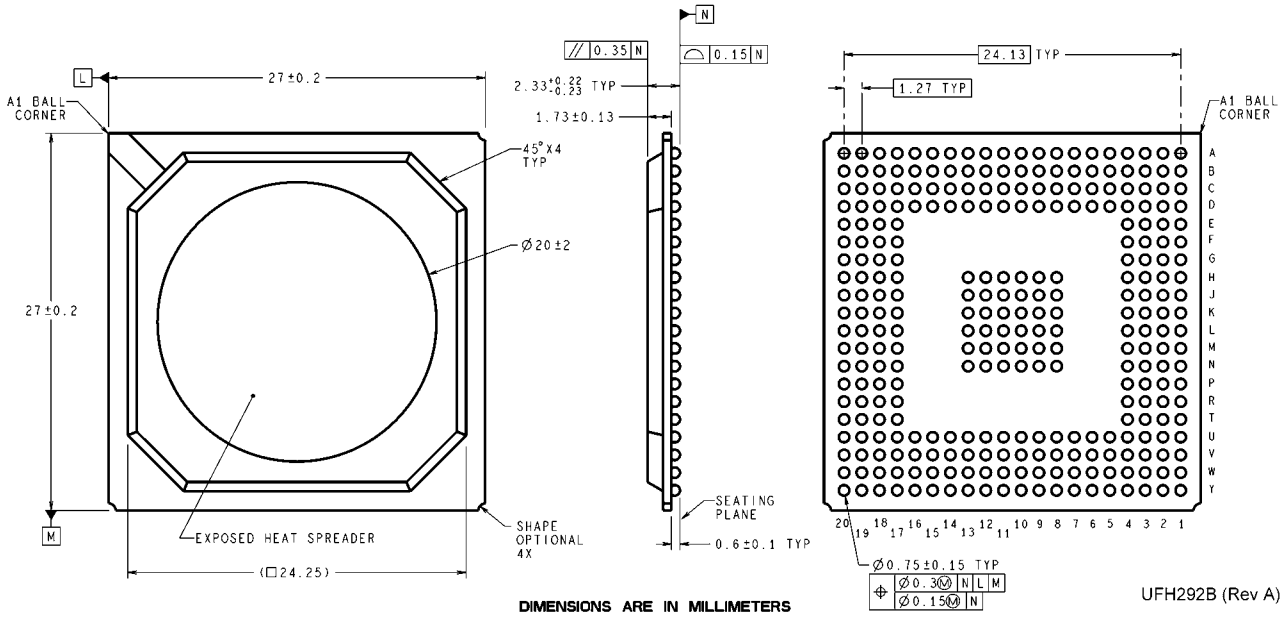
VREF_PERIPH and VREF_PCI determine input voltage clamping, not input signal thresholds or output levels. Table 2-4 shows the reference voltages.

Table 2-4. Reference Voltages

VREF_PCI Determined Mode		VREF_PERIPH Determined Mode	SDRAM Interface (3.3V Mode)		Inputs (3.3V Mode)	Output Only Pins
PCI_AD00	PCI_AD27	TRI_USERIRQ	MM_CLK0	MM_DQM2	TRI_CLKIN	VO_DATA0
PCI_AD01	PCI_AD28	TRI_TIMER_CLK	MM_CLK1	MM_DQM3	BOOT_CLK	VO_DATA1
PCI_AD02	PCI_AD29	JTAG_TDI	MM_A00	MM_DQ13	TESTMODE	VO_DATA2
PCI_AD03	PCI_AD30	JTAG_TDO	MM_A01	MM_DQ14	SCANCPU	VO_DATA3
PCI_AD04	PCI_AD31	JTAG_TCK	MM_A02	MM_DQ15		VO_DATA4
PCI_AD05	PCI_CLK	JTAG_TMS	MM_A03	MM_DQ16		VO_DATA5
PCI_AD06	PCI_C/BE#0	VI_CKL	MM_A04	MM_DQ17		VO_DATA6
PCI_AD07	PCI_C/BE#1	VI_DVALID	MM_A05	MM_DQ18		VO_DATA7
PCI_AD08	PCI_C/BE#2	VI_DATA0	MM_A06	MM_DQ19		AO_OSCLK
PCI_AD09	PCI_C/BE#3	VI_DATA1	MM_A07	MM_DQ20		AO_SCK
PCI_AD10	PCI_PAR	VI_DATA2	MM_A08	MM_DQ21		AO_SD1
PCI_AD11	PCI_FRAME#	VI_DATA3	MM_A09	MM_DQ22		AO_SD2
PCI_AD12	PCI_IRDY#	VI_DATA4	MM_A10	MM_DQ23		AO_SD3
PCI_AD13	PCI_TRDY#	VI_DATA5	MM_A11	MM_DQ24		AO_SD4
PCI_AD14	PCI_STOP#	VI_DATA6	MM_A12	MM_DQ25		SPDO
PCI_AD15	PCI_IDSEL	VI_DATA7	MM_A13	MM_DQ26		
PCI_AD16	PCI_DEVSEL#	VI_DATA8	MM_DQ00	MM_DQ27		
PCI_AD17	PCI_REQ#	VI_DATA9	MM_DQ01	MM_DQ28		
PCI_AD18	PCI_GNT#	IIC_SDA	MM_DQ02	MM_DQ29		
PCI_AD19	PCI_PERR#	IIC_SCL	MM_DQ03	MM_DQ30		
PCI_AD20	PCI_SERR#	VO_IO1	MM_DQ04	MM_DQ31		
PCI_AD21	PCI_INTA#	VO_IO2	MM_DQ05	MM_CKE0		
PCI_AD22	PCI_INTB#	VO_CLK	MM_DQ06	MM_CKE1		
PCI_AD23	PCI_INTC#	AI_SCK	MM_DQ07	MM_CS0#		
PCI_AD24	PCI_INTD#	AI_SD	MM_DQ08	MM_CS1#		
PCI_AD25	TRI_RESET#	AI_WS	MM_DQ09	MM_CS2#		
PCI_AD26		AO_SCK	MM_DQ10	MM_CS3#		
		AO_WS	MM_DQ11	MM_RAS#		
			MM_DQ12	MM_CAS#		
			MM_DQM0	MM_WE#		
			MM_DQM1			

3.0 Package Specifications

Figure 3-1 provides the mechanical package outline for the 292-Terminal TEPBGA (Thermally Enhanced Ball Grid Array) package.



NOTES: UNLESS OTHERWISE SPECIFIED.

1) SOLDER BALL COMPOSITION: SN 63%, PB 37%.
2) DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM N.
3) THE MOLD SURFACE AREA MAY INCLUDE DIMPLE FOR A1 BALL CORNER IDENTIFICATION.
4) REFERENCE JEDEC REGISTRATION MS-034, VARIATION BAL-1.

Figure 3-1. 292-Terminal TEPBGA (Body Size: 27x27x2.33 mm; Pitch: 1.27 mm)

Appendix A Support Documentation

A.1 ORDERING INFORMATION

Order Number (NSID)	Part Marking	Core Frequency (MHz)	Core Voltage (V)	Temperature (Degree C)	Package
CS1301	CS1301	180	2.5	0 - 85	TEPBGA
CS1311	CS1311	166	2.2	0 - 85	TEPBGA

Note: Due to licensing agreements, the CS1301/CS1311 can only be purchased by those customers using a Geode processor-based design.

A.2 PRODUCT BRIEF REVISION HISTORY

This section is a report of the revision/creation process of the product brief for the Geode Device Number. Any revisions (i.e., additions, deletions, parameter corrections, etc.) are recorded in the table below.

Note: This product brief must be used in conjunction with the Philips Semiconductor *PNX1300 Series Media Processors Data Book* for a complete understanding of the CS1301/CS1311 (posted on National's IA Developer's web site).

Table A-1. Revision History

Revision # (PDF Date)	Revisions / Comments
1.0 (November 2001)	First draft of product brief. (Confidential)
2.0 (April 2002)	Updated to include a list of supported software and software block diagram. (Confidential)
2.1 (July 2002)	Updated to include Signal Definitions and Package Specifications sections. (No longer confidential, to be posted on National external web site in the product folders.)
2.2 (August 2002)	Replaced "Product Brief" with "Preliminary". Updated package specifications to use National supplied drawing and changed HBGA to TEPBGA. (These changes were made to meet Corporate standard requirements, revision 2.1 was never posted on National external web site.)
2.3 (November 2002)	Removed the system and software architecture to a separate document. Added SSI balls.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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