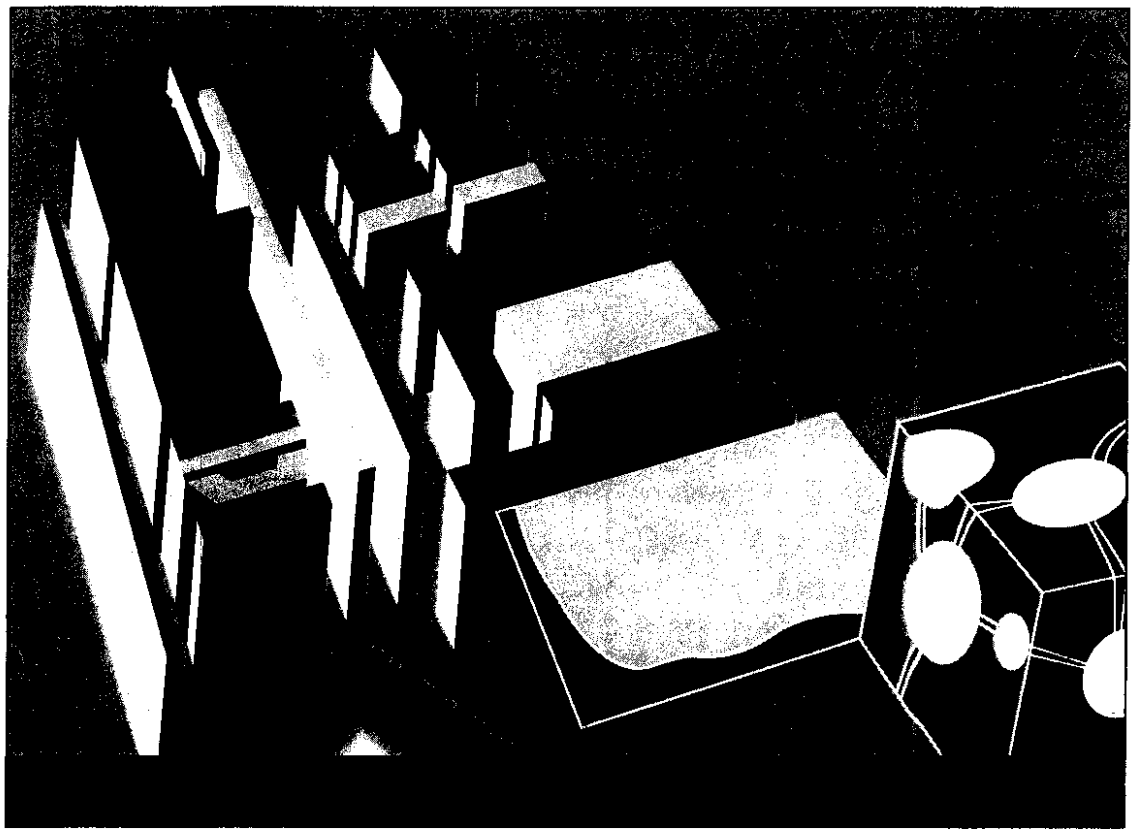
Data
Sheet



μPD71051

Serial Control Unit

January 1989

NEC

The uPD71051 serial control unit is designed for serial data communications in microcomputer systems.
On a system level, the uPD71051 is regarded as an ordinary peripheral device. Synchronous and asynchronous serial communications are possible using CPU programs. In the synchronous mode, operations in IBM's BSC system are also possible.
The uPD71051 was fabricated using CMOS technology and consumes low power. Its power consumption is even lower in the stand-by mode. In the stand-by mode, the operation mode in which uPD71051 has been set is released and the serial control unit waits for a mode word for mode setting, which is to be sent from the CPU. When the CPU has written the mode word to the uPD71051, the serial control unit is released from the stand-by mode, and enters in the specified operation mode.

Features:

- o Synchronous/asynchronous operation modes
  - ° Synchronous mode
    1 - 2 SYNC characters
    Internal/external synchronization
    Automatic SYNC character insertion
  - ° Asynchronous mode
    Clock rate: Baud rate x 1, 16, 64
    Send stop bits: 1, 1.5, 2 bits
    Break transmission
    Automatic break detection
    Error start bit detection

- o Directory connected to uPD70108-10 and uPD70116-10 with no wait state (uPD71051-10)

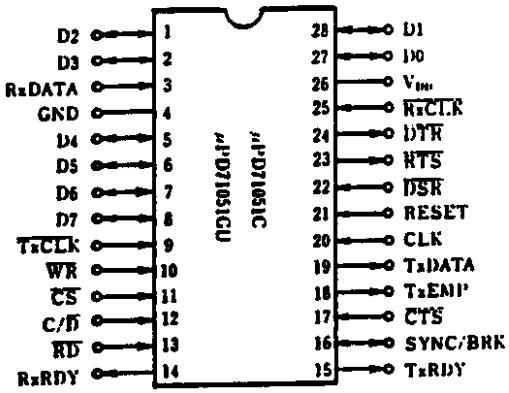
- o Baud rate
  uPD71051 : DC to 240K-bit/sec
  uPD71051-10: DC to 300K-bit/sec
- o Full duplex, double buffered transmitter/receiver

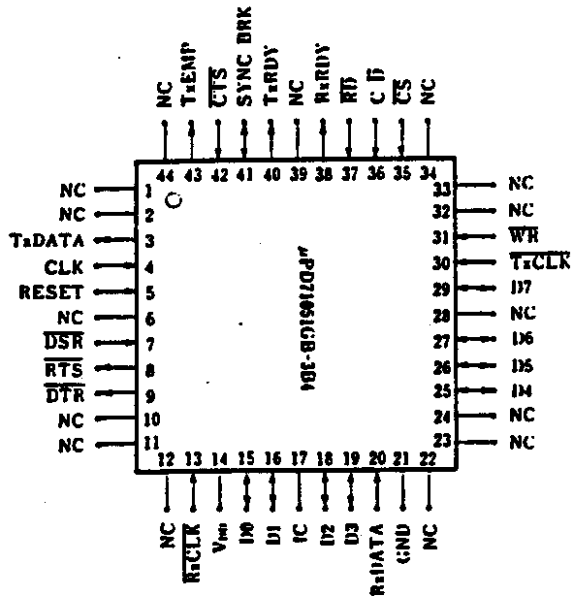
- o Parity generate/check
- o Error detection: Parity, overrun, framing
- o 5 - 8 bit characters
- o Stand-by mode
- o CMOS technology
- o Single power supply

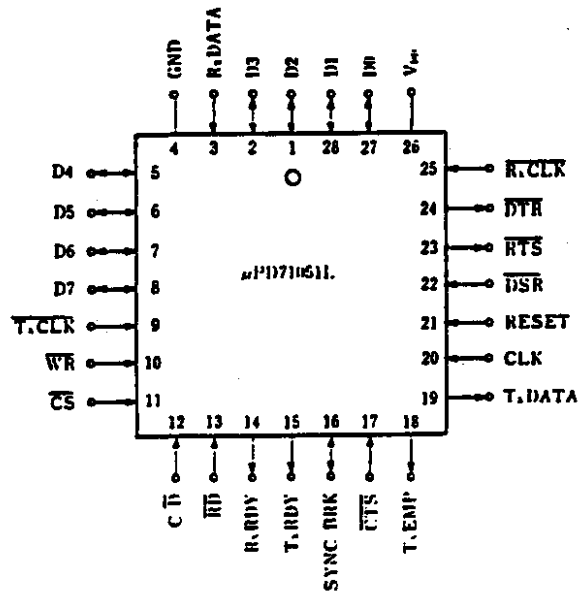
Ordering Information

Ordering Code	Package Type	Max. Frequency of Operation
uPD71051C	28-pin plastic DIP	8MHz
uPD71051C-10	28-pin plastic DIP	10MHz
uPD71051GB-3B4	44-pin plastic QFP(2.70mm thick)	8MHz
uPD71051GB-10-3B4	44-pin plastic QFP(2.70mm thick)	10MHz
uPD71051GU	28-pin plastic SOP	8MHz
uPD71051GU-10	28-pin plastic SOP	10MHz
uPD71051L	28-pin PLCC	8MHz
uPD71051L-10	28-pin PLCC	10MHz

Pin Configuration (Top View)

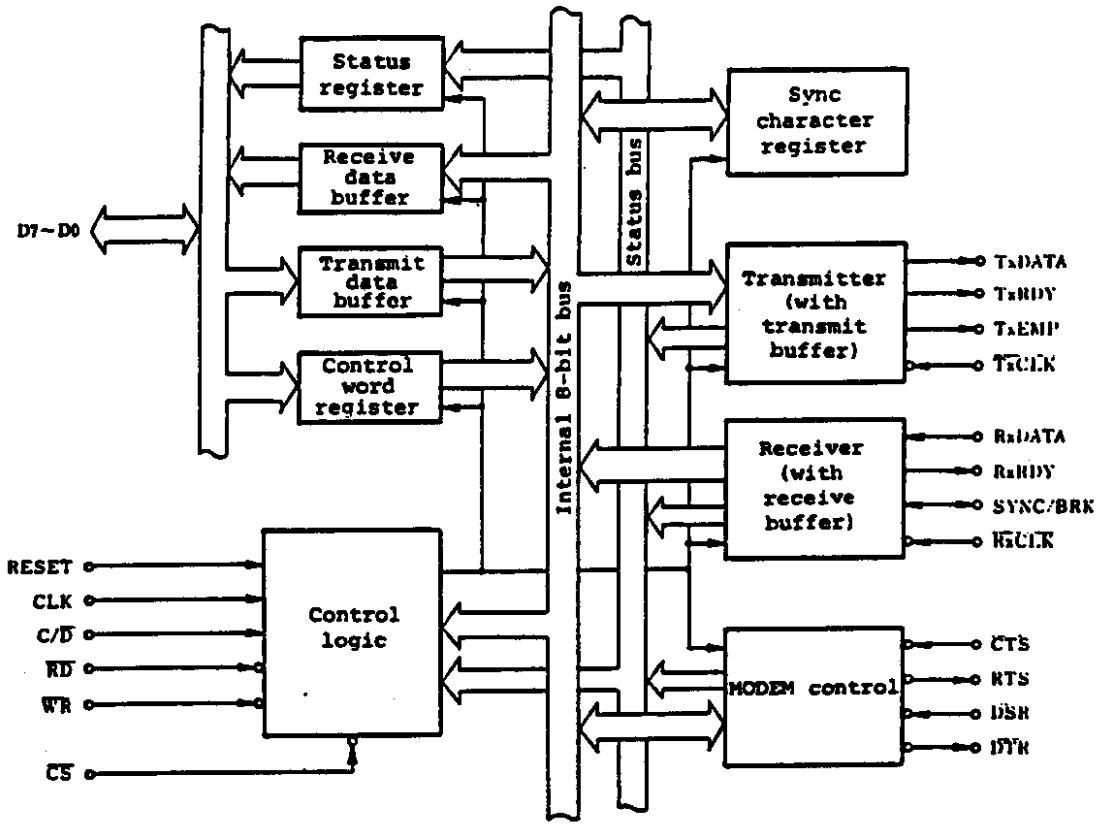






C4

uPD71051 Block Diagram



CONTENTS

1. BLOCK FUNCTION

1.1 Control Logic

The control logic sends control signals to the internal blocks and controls the operation of the uPD71051 in accordance with signals from the outside of the uPD71051 and internal status signals.

1.2 Status Register

This is an 8-bit register that stores the uPD71051 states. The status register contains an error, data buffer, and general-purpose input pin states. The CPU can read the contents of this register anytime.

1.3 Receive Data Buffer

The receive data buffer stores data which the receiver has received. The CPU receives receive data by reading the contents of this buffer.

1.4 Send Data Buffer

The send data buffer stores send data which the CPU has written. The written send data is transferred from this send data buffer to the send buffer inside the transmitter and is output from Pin TxDATA.

1.5 Control Word Register

A control word (a mode word, SYNC character after a mode word, and command word) to designate the operation is shifted inside the uPD71051 via this register.

1.6 Synchronous Character Register

This register stores one or two SYNC characters to be written in the control word register after the mode word in the SYNC mode. During transmitting the SYNC characters stored in this register are output from Pin TxDATA when data writing by the CPU is delayed and a TxEMP status is established. During receiving when the characters received and SYNC characters stored in this register coincide after a comparison is made, synchronization will be established.

1.7 Transmitter

The contents of the send data buffer are transferred to this transmitter and are output from Pin TxDATA after being parallel serial converted. The transmitter adds start, stop, and parity bits.

1.8 Receiver

The receiver converts serial data input from Pin RxDATA into parallel data and transfers parallel data to the receive data buffer to permit the CPU to read it.

Detection of SYNC characters and checking of parity bits in the SYNC mode, as well as detection of start and stop bits and checking of parity bits in the asynchronous mode, are performed inside this receiver.

In the asynchronous mode, receiving operation is not started unless one effective "1" (high level) is input to Pin RxDATA when the RECEIVE ENABLE (RxEN=1) status is first established after setting up the mode (start bit is not detected).

1.9 MODEM Control

This block controls MODEM interface. Pins $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, and $\overline{\text{DTR}}$ are controlled by this block. But three pins other than $\overline{\text{CTS}}$ can be used as general-purpose input/output pins.

2. PIN FUNCTIONS

2.1 D7 - D0 (Data Bus) ... 3 State Input/Output

This is an 8-bit, 3-state bi-directional data bus. The bus transfers data by connecting to the system data bus. It becomes active when $\overline{CS}$ = 0, and $\overline{RD}$ or $\overline{WR}$ is 0. Otherwise, it is in a high impedance state.

2.2 RESET (Reset) ... Input

Inputting a high level to this pin resets uPD71051 and sets it to an idle state. The uPD71051 operates nothing in this mode. It is set to the stand-by mode when the signal falls from a high to a low level. The stand-by mode is released when the CPU writes a mode word in the uPD71051.

At least 6 tcy is needed as the reset pulse width. (A clock must be input.)

2.3 CLK (Clock) ... Input

This pin is a clock input pin to produce timing inside the uPD71051. To assure stable operations, the clock frequency should be more than 30 times the transmitter or receiver clock input ($\overline{TxCLK}$, $\overline{RxCLK}$) frequency in the synchronous mode or in the asynchronous mode with X1 clock. The clock frequency should be more than 4.5 times in another asynchronous mode.

2.4 $\overline{CS}$ (Chip Select) ... Input

$\overline{CS}$ is a signal to select the uPD71051. The uPD71051 is selected by establishing $\overline{CS}$ = 0. Selection is not possible when $\overline{CS}$ = 1, and the data bus (D7 - D0) becomes high impedance. The $\overline{RD}$ and $\overline{WR}$ signals are neglected.

2.5 $\overline{RD}$ (Read Strobe) ... Input

$\overline{RD}$ = 0 is established when reading data or status information from the uPD71051.

2.6 $\overline{WR}$ (Write Strobe) ... Input

$\overline{WR}$ = 0 is established when writing data or a control word in the uPD71051.

2.7 C/$\overline{D}$ (Control or Data) ... Input

This signal regulates data type when accessing the uPD71051.

C/$\overline{D}$ = 1: Control word/status
C/$\overline{D}$ = 0: Character data

This pin is normally connected to the least significant bit A0 of the system address bus.

Table 2-1 Control Signals and Operations

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C/$\overline{D}$	uPD71051 operation	CPU operation
0	0	1	0	Receive data buffer ↓ Data bus	Read receive data
0	0	1	1	Status register ↓ Data bus	Read status
0	1	0	0	Data bus ↓ Transmit data buffer	Write transmit data
0	1	0	1	Data bus ↓ Control word register	Write transmit data
0	1	1	x	Data bus: High impedance	
1	x	x	x	Data bus: High impedance	

2.8 $\overline{DSR}$ (Data Set Ready) ... Input

This is a general-purpose input pin. The status of this pin can be known by reading the status (bit 7).

2.9 $\overline{DTR}$ (Data Terminal Ready) ... Output

This is a general-purpose output pin. The status of this pin can be controlled by Bit 1 of the command word.

bit 1 = 1 → $\overline{DTR}$ = 0 bit 1 = 0 → $\overline{DTR}$ = 1

2.10 $\overline{RTS}$ (Request to Send) ... Output

This is a general-purpose output pin. The status of this pin can be controlled by Bit 5 of the command word.

bit 5 = 1 $\overline{RTS}$ = 0 bit 5 = 0 $\overline{RTS}$ = 1

2.11 $\overline{CTS}$ (Clear to Send) ... Input

This is an input pin to control transmission. uPD71051 will be able to send when setting up $\overline{CTS}$ = 0 while TxEN = 1 is established by the command word. When setting $\overline{CTS}$ = 1 during transmission, the sending operation is disabled after sending all the data currently written, and the level of Pin TxDATA becomes high.

2.12 TxDATA (Transmit Data) ... Output

This pin sends serial data.

2.13 TxRDY (Transmitter Ready) ... Output

This signal notifies the CPU that the send data buffer in the uPD71051 is empty, that is, send data can be written. This pin signal is masked by the command word (TxEN bit) or $\overline{CTS}$ input. It can also be used as an interrupt signal of a data write request to the CPU. TxRDY can also be read by the status (Bit 0), and polling is also possible. Note that TxRDY of the status is not masked. TxRDY is automatically cleared to 0 by the falling edge of $\overline{WR}$ during writing of send data in the uPD71051 by the CPU when the CPU writes in the uPD71051.

Data in the send data buffer not yet sent is destroyed when send data is written in a TxRDY = 0 status.

2.14 TxEMP (Transmitter Empty) ... Output

The uPD71051 reduces the CPU overhead during the sending operation through a double buffer system using the send data buffer (second buffer) and send buffer (first buffer) in the transmitter. When the CPU writes send data in the send data buffer, which is the second buffer, the uPD71051 continues sending data by automatically transferring the contents of the second buffer to the first buffer after sending the contents of the first buffer in the transmitter.

Thus, the second buffer becomes empty, and TxRDY is set to 1. TxEMP becomes 1 after the contents of the first buffer is sent while the second buffer is empty, showing that TxEMP = 1 indicates that both the first and second buffers are empty. In half-duplex communications, the timing to change from a sending operation to receiving operation can be known by TxEMP = 1.

When TxEMP = 1 is established in the asynchronous mode, the level of Pin TxDATA becomes high. When the CPU writes send data thereafter, TxEMP is automatically set to 0, and data sending is resumed.

When TxEMP = 1 is set in the synchronous mode, the uPD71051 automatically loads SYNC characters from the SYNC character register and continues to send them through Pin TxDATA. TxEMP is set to 0 and resumes sending data after sending SYNC characters (one or two) sent when the CPU writes send data in this rate.

2.15 TxCLK (Transmitter Clock) ... Input

Reference clock input to decide a transmission rate. Transmission is performed at the same rate as that of $\overline{\text{TxCLK}}$ in the SYNC mode. In the asynchronous mode, the $\overline{\text{TxCLK}}$ frequency can be at three levels, 1, 16 and 64 times of the transmission rate.

Serial data from Pin TxDATA is performed by the falling edge of $\overline{\text{TxCLK}}$.

Examples)

19,000 baud in synchronous mode ... $\overline{\text{TxCLK}}$: 19.2 kHz

2,400 baud in asynchronous mode

x 1 clock ..... $\overline{\text{TxCLK}}$: 2.4 kHz

x 16 clock ..... $\overline{\text{TxCLK}}$: 38.4 kHz

x 64 clock ..... $\overline{\text{TxCLK}}$: 153.6 kHz

2.16 RxDATA (Receive Data) ... Input

Serial data is received through this pin.

2.17 RxRDY (Receiver Ready) ... Output

This signal becomes 1 when the uPD71051 receives data for one character and when that data is transferred to the receive data buffer, that is, when the receive data can be read. This signal can be used as an interrupt signal for a data read request to the CPU. The status of RxRDY can also be known by reading the status (Bit 1), and polling operation is also possible. RxRDY becomes 0 when the CPU reads receive data.

An overrun error occurs, and the bit OVE of the status is set unless the CPU completes reading receive data after RxRDY = 1 is set, and before the next one character is received and transferred to the receive data buffer. The data in the receive data buffer not read is substituted by newly transferred data at that time.

RxRDY is fixed to a 0 state by establishing a receive disable state by changing the RxEN bit to 0 through the command word. RxRDY becomes 1 after new characters are received and transferred to the receive data buffer when RxEN = 1 is set and receiving is possible.

2.18 SYNC/BRK (Synchronization/Break) ... Input/Output

• SYNC ... Input/Output

SYNC is used to detect synchronization in the SYNC mode. Selection between internal and external detection as a SYNC detection method is selected by the mode word of the SYNC mode. The SYNC pin becomes output when detecting internal synchronization and becomes input when detecting external synchronization.

The level becomes high when the uPD71051 detects a SYNC character in internal synchronization. When set to the double SYNC character, the level becomes high by the position of the last bit when bits for two characters are detected continuously. The SYNC signal can be known by reading the status (Bit 6), and both pin and status are cleared to 0 by the reading operation.

In external synchronization, a high level of more than one period of $\overline{\text{RxCLK}}$ is input to Pin SYNC when the external circuit detects synchronization. Upon detecting this high level, the uPD71051 starts receiving data beginning at the rising edge of the next $\overline{\text{RxCLK}}$. The high level input may be removed after synchronization is released.

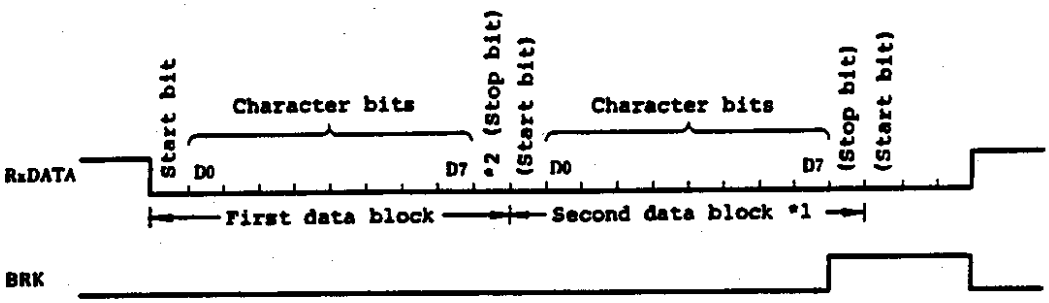
• BRK ... Output

BRK is a signal used only in the asynchronous mode and shows detection of a break state. The level of BRK becomes high when a low level signal is input to Pin RxDATA in more than two data blocks in a predetermined character bit length (including the start bit, parity bit, and a stop bit). As in the SYNC signal, the BRK signal can be checked by the status (Bit 6), but is not cleared by the read operation. The set BRK signal is cleared when the level of the RxDATA input returns to high, or when it is reset (hardware or software). Fig. 3-1 shows the break state and BRK signal.

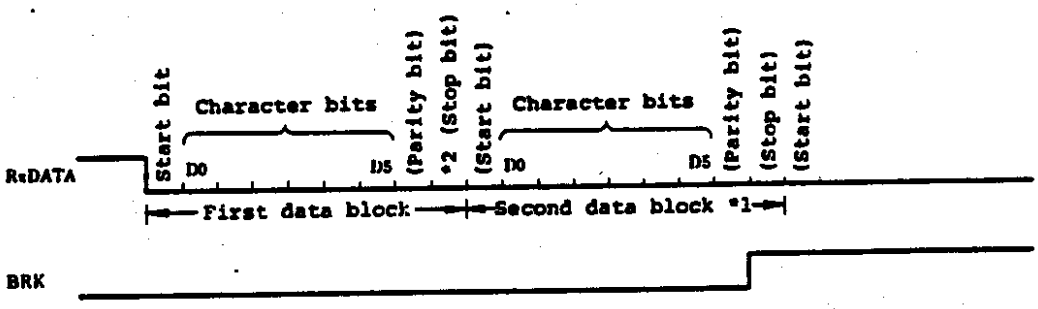
The level of the SYNC/BRK pin becomes low regardless of the mode when it is reset.

Fig. 2-1 Break Status and BRK Signal

° 8-bit character, no parity



° 6-bit character with parity



*1: When RxDATA bit goes high level in a stop bit of a second data block, the BRK signal may temporarily (one bit long at the most) become high or may not become high.

*2: Only one bit of the stop bit is checked.

2.19 $\overline{\text{RxCLK}}$ (Receiver Clock) ... Input

This is a reference clock input decide the receiving rate. The receiving rate in the SYNC mode will be the same as that of $\overline{\text{RxCLK}}$. In the asynchronous mode, $\overline{\text{RxCLK}}$ can be 1, 16 or 64 multiplication relative to the receiving rate.

Serial data from RxDATA is input by the rising edge of $\overline{\text{RxCLK}}$.

2.20 V_{DD} (Power)

Positive power supply.

2.21 GND (Ground)

Ground potential.

2.22 IC (Internally Connected)

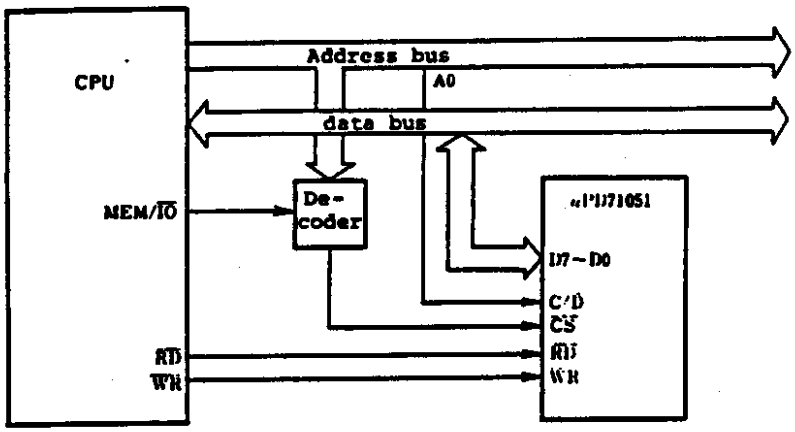
This pin must be left unconnected.

3. Connection with System

The CPU can handle the uPD71051 as a normal I/O device and uses it by allocating to two I/O addresses depending on the value of Pin C/$\overline{D}$. One is when the level of the C/$\overline{D}$ input is high and becomes a port to transfer send and receive data. The other is when the level of the C/$\overline{D}$ input is low and becomes a port to write control words and to read the status. Generally, the least significant bit A0 of the address bus is connected to Pin C/$\overline{D}$ to obtain a continuous I/O address.

Even though it is not shown in Fig. 4-1, Pins TxRDY and RxRDY are connected to the CPU or the interrupt pin of the interrupt controller when interrupt is utilized.

Fig. 3-1 System Configuration



4. Description of the uPD71051 Operations

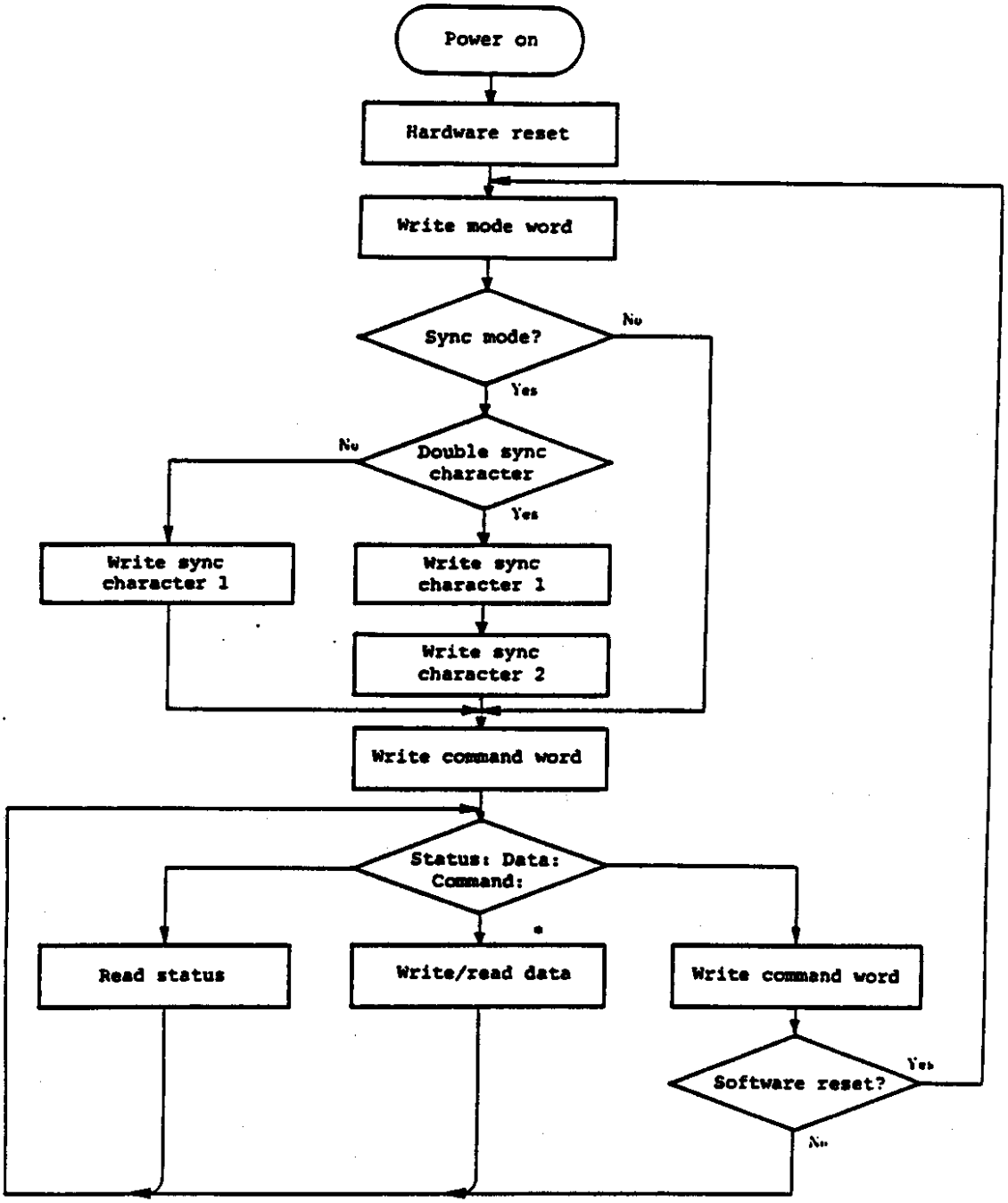
This chapter describes the basic operating procedure, detailed control method, operating modes, etc. to operate the uPD71051.

4.1 Operating Procedure

Start with hard resetting (set the level of Pin RESET to high) at all times as the status of the uPD71051 after switching ON the power. By doing this, the uPD71051 is set to the stand-by mode and queues for a mode word. By writing a mode word and setting a communication protocol mode in this state, the command word queue status is set when in the asynchronous mode. A queue state for writing one or two (determined by the mode word) SYNC characters is set in the SYNC mode. Note that $C/\overline{D} = 1$ should be set up in this case. After the SYNC characters are written, a command word queue status is established.

In both modes, writing of send data, reading of receive data, reading of status, and writing of command words will be possible after writing the command words. The uPD71051 performs a reset operation, shifts to the stand-by mode, then returns to the mode word queue mode when software resetting is performed by the command word.

Fig. 4-1 uPD71051 Operating Procedure

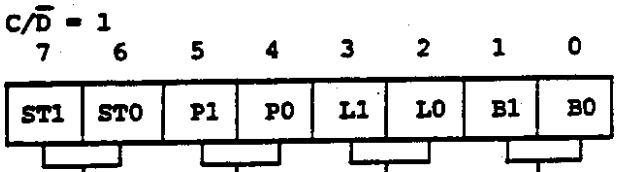


*: This is done with C/D = 0. Others are operated with C/D = 1.

4.2 Mode Designation

Mode words have to be written in the uPD71051, which is in the stand-by mode, by resetting (hardware or software) when designating a mode for the uPD71051. By doing this, the stand-by mode is released, and a mode is designated for the uPD71051. The mode word format is shown in Figs. 4-2 and 4-3. The SYNC mode is set when both Bits 1 and 0 are 0. In other cases, the asynchronous mode is set up.

Fig. 4-2 Mode Word for Setting Asynchronous Mode



B1	B0	Baud rate
0	1	x1 clock
1	0	x16 clock
1	1	x64 clock

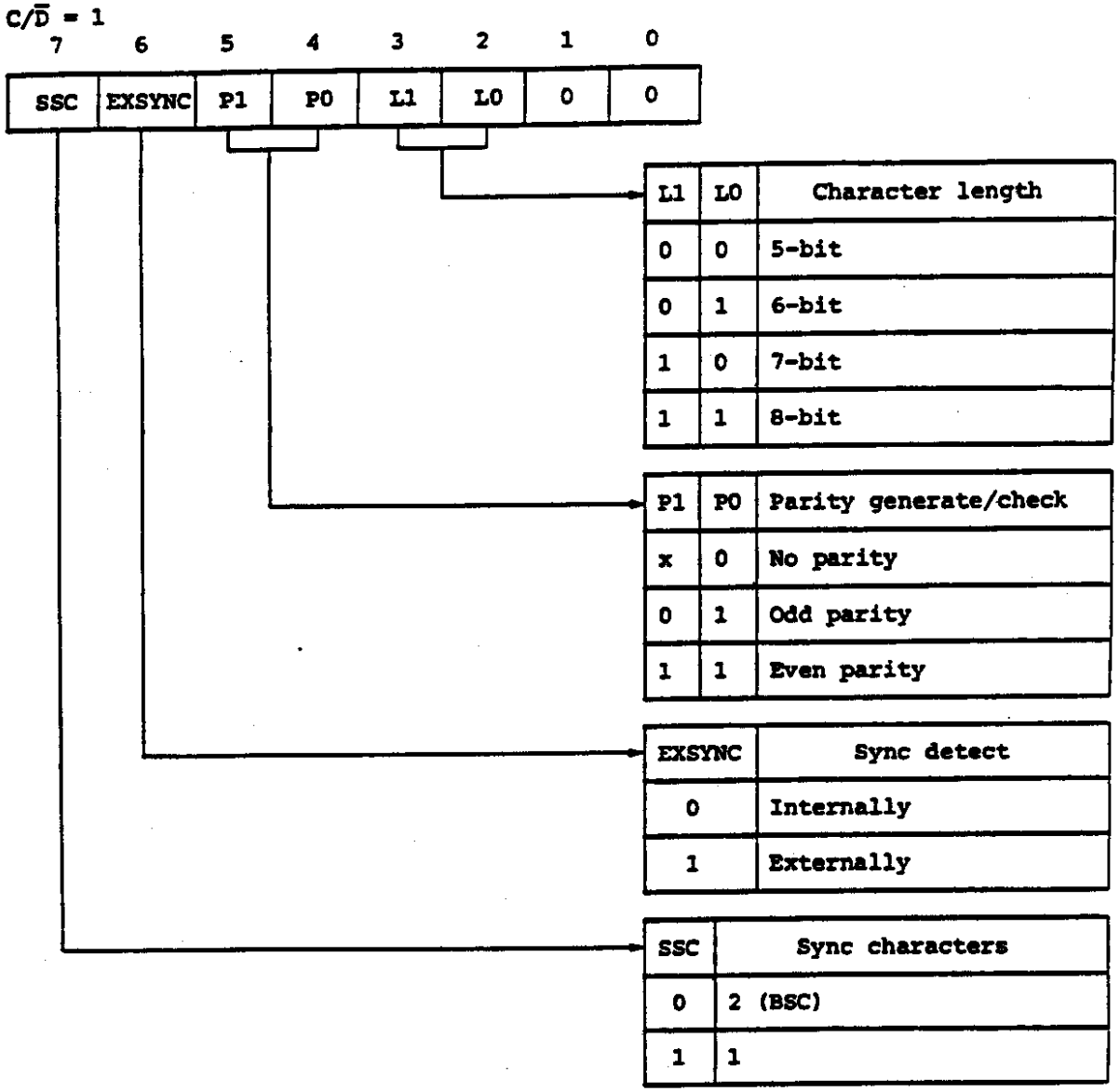
L1	L0	Character length
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

P1	P0	Parity generate/check
x	0	No parity
0	1	Odd parity
1	1	Even parity

ST1	ST0	Transmit stop bits
0	0	Use inhibited
0	1	1-bit
1	0	1 1/2 bit
1	1	2-bit

x: don't care

Fig. 4-3 Mode Word for Setting Synchronous Mode



L1	L0	Character length
0	0	5-bit
0	1	6-bit
1	0	7-bit
1	1	8-bit

P1	P0	Parity generate/check
x	0	No parity
0	1	Odd parity
1	1	Even parity

EXSYNC	Sync detect
0	Internally
1	Externally

SSC	Sync characters
0	2 (BSC)
1	1

x: don't care

First, the bits that are common in both modes are described. Bits P1 and P0 (parity) control parity bit generation (sending) and check (receiving) functions. The parity bit generation and check functions do not operate when P0 = 0. Generation and checking of odd parity are performed when both P1 and P0 are 01, and of even parity when both P1 and P0 are 11. Bits L1 and L0 (length) set the number of bits for one character. Additional bits such as a parity bit are not included in this number of bits. When set to n bits, the uPD71051 receives lower n bits of 8-bit data written by the CPU. Upper 8 minus n bits of data which the CPU reads from the uPD71051 become 0.

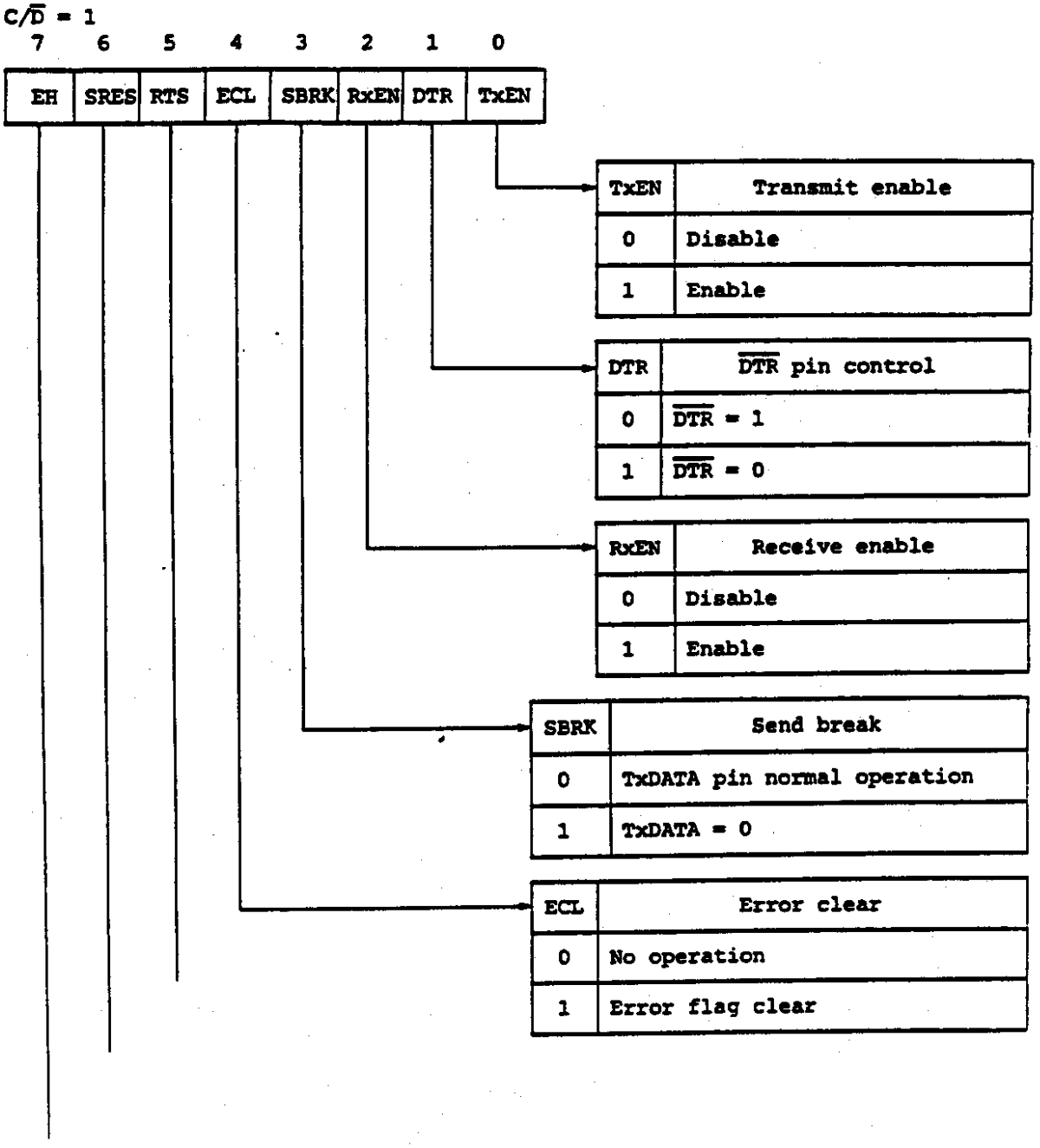
Special bits for the asynchronous mode are described next. Bits ST1 and ST0 (stop bits) designate the length of the stop bits (high level) which the uPD7051 adds during transmission. Bits B1 and B0 (baud rate) regulate the relationship between the baud rate for sending and receiving, and $\overline{\text{TxCLK}}$ and $\overline{\text{RxCLK}}$. A selection is made of a multiplication rate of 1, 16 or 64 for the frequency of the sending and receiving clock relative to the baud rate. Normally, the multiplication of 1 is not used in the asynchronous mode. Note that data and clock have to be synchronized on the sending and receiving sides when using multiplication 1.

Lastly, bits that are special to the SYNC mode are described. Bit SSC (single SYNC character) decides the number of SYNC characters. The number of characters is 1 if it is SSC = 1, two (BSC) if SSC = 0. After the mode word, SYNC characters in the number set by the SSC bit are written. Bit EXSYNC (external synchronization) decides whether SYNC detection during receiving should be internal or external detection. EXSYNC = 1 is for external detection, and EXCYNC = 0, for internal detection.

4.3 Commands and Operations

Commands are given by command words and control sending and receiving operations of the uPD71051. A command word is obtained by designating the mode by a mode word (after additionally writing SYNC characters in the SYNC mode) and writing $C/\overline{D}$ = 1.

Fig. 4-4 Command Word Format



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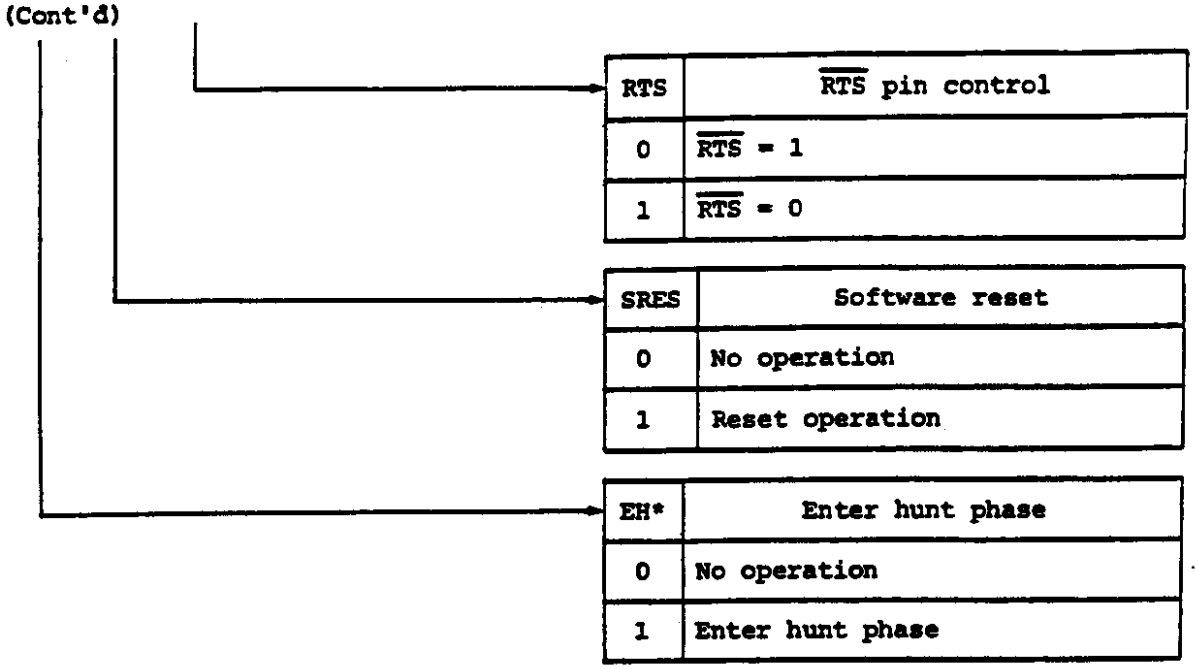


RTS	$\overline{RTS}$ pin control
0	$\overline{RTS}$ = 1
1	$\overline{RTS}$ = 0

SRES	Software reset
0	No operation
1	Reset operation

EH*	Enter hunt phase
0	No operation
1	Enter hunt phase

*: The EH bit is effective only in the sync mode. It will be not cared in the async mode.

Bit EH (enter hunt phase) is set to 1 when entering the hunt phase to synchronize in the SYNC mode. Bit RxEN for receiver enable should also be set to 1 at that time. Data receiving starts automatically after escaping from the hunt phase when SYNC characters are detected and synchronization is released.

Soft resetting is executed and SDA shifts to a stand-by mode, and is set to a mode word queue status, when Bit SRES (software reset) is set to 1.

Bit $\overline{\text{RTS}}$ (request to send) controls the general-purpose output pin $\overline{\text{RTS}}$. The level of RTS is low if RTS = 1, and becomes high if $\overline{\text{RTS}}$ = 0.

When Bit ECL (error clear) is set to 1, error flags (PE, OVE and EE) in the status are cleared. Establish ECL = 1 at the same time when entering the hunt phase (EH = 1) or receiver enable (RxEN = 1) to clear the error flags as well.

Bit SBRK (send break) sends a break. When SBRK = 1 is established, the data being currently sent is destroyed, and the level of Pin TxDATA becomes low. Set SBRK = 0 to release the break status. This function works in a send disable status as well.

Bit RxEN (receiver enable) instructs receiver enable/disable. Receiver enable is established when RxEN = 1. Receiver disable is established when RxEN = 0. Synchronization is lost when receiver disable is set during the SYNC mode.

Bit DTR (data terminal ready) controls general-purpose output Pin $\overline{\text{DTR}}$. The level of $\overline{\text{DTR}}$ becomes low when DTR = 1, and becomes high when DTR = 0.

Bit TxEN (transmitter enable) instructs sending enable/disable. The transmitter is enabled when TxEN = 1. When the transmitter is disabled by setting up TxEN = 0, sending is stopped and the level of Pin TxDATA becomes high (mark status) after all the data currently written is sent (when SBRK $\neq$ 1).

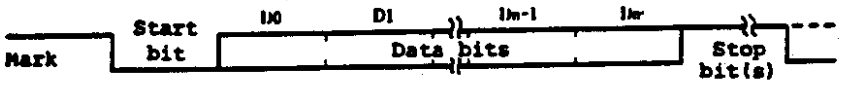
4.3.1 Asynchronous Mode Operation

(1) Sending

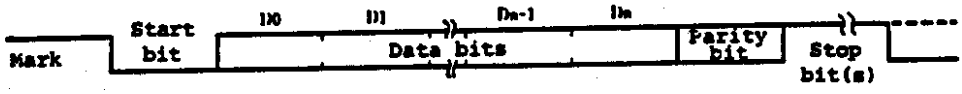
The level of Pin TxDATA is normally in a high state (marking) when data is not sent. When the CPU writes send data in the uPD71051, the uPD71051 transfers the send data from the send data buffer to the send buffer and sends the data from Pin TxDATA after automatically adding one start bit (low level) and programmed stop bit. When the parity is effective, a programmed even or odd parity bit is added between the character and stop bit. Serial data is sent by the falling edge of the signal which divided (1/1, 1/16, and 1/64 division) $\overline{\text{TxCLK}}$.

Fig. 4-5 Asynchronous Mode Data Format

• No parity



• With parity



n: 4, 5, 6, 7
Stop bit: 1 bit, 1.5 bit, 2 bit

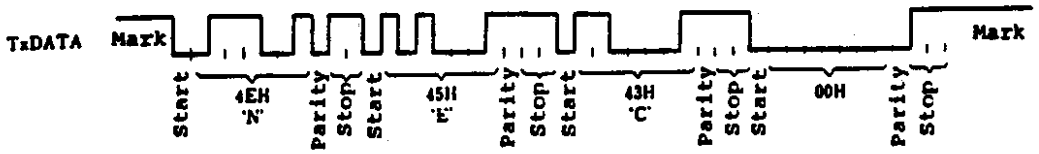
Upon issuing a command that sets Bit SBRK at 1, the level of Pin TxDATA becomes low (break status), regardless of whether or not data is being sent.

Fig. 4-6 shows an example of a program to send data in the asynchronous mode and output of Pin TxDATA.

Fig. 4-6 Asynchronous Mode Transmit Example

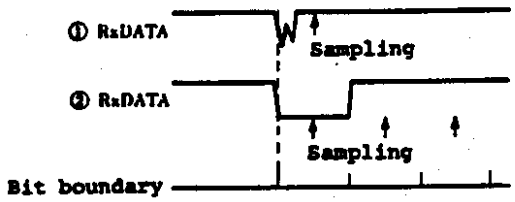
```
ASYNTX :  CALL  ASYNMOD                  Set async mode
          MOV   AL, 00010001B            Command
          OUT   PCTRL, AL                  • Error flag clear
                                           • Transmit enable
          MOV   BW, OFFSET TXDADR        Transmit data area
TXSTART:  IN    AL, PCTRL                Read status
          TEST1 AL, 0                      Wait until TxRDY = 1
          BZ    TXSTART
          MOV   AL, [BW]                 Write transmit data
          OUT   PDATA, AL
          INC   BW                       Set next data address
          CMP   AL, 0                    End if data = 0
          BNE   TXSTART
          RET
TXDADR    DB    'NEC'                    Transmit data
          DB    0                          4EH, 45H, 43H, 00H
ASYNMOD:  MOV   AL, 0                    Write control words 3
          OUT   PCTRL, AL                times with 00H to accept
          OUT   PCTRL, AL                the new command word
          OUT   PCTRL, AL                unconditionally
          MOV   AL, 01000000B            Software reset
          OUT   PCTRL, AL
          MOV   AL, 11111010B            Write mode word
          OUT   PCTRL, AL                  • Stop bit = 2-bit
                                           • Even parity
          RET                              • 7-bit/character
                                           • x16 clock
```

TxDATA Pin Output



(2) Receiving

Fig. 4-7 Start Bit Detection



In the case of ①, start bit is not recognized at the RxDATA is high at the sampling time.

In the case of ②, start bit is recognized as the RxDATA is low at the sampling time.

The level of Pin RxDATA is normally maintained high when data is not received. The uPD71051 detects the falling edge of a low level signal when a low level signal enters it. The uPD71051 samples the level of RxDATA input (only when x 16 and x 64 clocks are designated) in a position 1/2 bit behind the falling edge to check whether or not this low level is an effective start bit. The start bit is regarded effective when a low level is detected at that time. The bit is not regarded as a start bit when a high level is detected, and is returned to a low level input queue status again. When a start bit is detected, sampling points of the data bit, parity bit (when effective), and stop bit are decided by a bit counter, and data reading is started. The

sampling is performed by this rising edge of the signal that divided (1/1, 1/16, and 1/64 division) $\overline{\text{RxCLK}}$.

Data for one character entering the receive buffer is transferred to the receive data buffer and becomes RxRDY = 1, requesting the CPU to read the data. When the CPU reads the data the RxRDY automatically becomes 0.

Only one stop bit is detected. When a high level (the correct stop bit) is detected, a queue status for the start bit of the next data is established. A framing error flag is set when a low level is detected in the stop bit. However, the receiving operation continues as if a high level has been detected as a stop bit. A parity error flag is set when a parity error is occurred. An overrun error flag is set when the CPU is slow in reading, and the next receiving data is transferred to the receive data buffer. The sending and receiving operation of the uPD71051 is not affected regardless of which error is caused.

When a low level is input on Pin RxDATA for more than two data blocks in time duration in a receiving operation, the situation is judged as a break state, and SYNC/BRK (pin, status) becomes 1.

Start bit detection is not performed until a high level of more than one bit is input to Pin RxDATA when the asynchronous mode is set and receiving is enabled first after resetting.

Fig. 4-8 shows an example of a program to receive the data sent in Fig. 4-6.

Fig. 4-8 Asynchronous Mode Receive Program Example

```
ASYNRX :  CALL   ASYNMOD                 Set async mode
          MOV    AL, 00010100B           Command
          OUT    PCTRL, AL                 ° Error flag clear
                                           ° Receive
          MOV    BW, OFFSET RXDADR       Data store area
RXSTART:  IN     AL, PCTRL               Read status
          TEST1  AL, 1                     Wait until RxRDY = 1
          BZ     RXSTART
          IN     AL, PDATA               Read and store the
          MOV    [BW], AL                receive data
          INC    BW                      Set next store address
          CMP    AL, 0                   End if data = 0
          BNE    RXSTART
          RET
RXDADR    DB     256 DUP(?)              Reserve receive data area
```

Note: The frequencies of the $\overline{\text{TxCLK}}$ on the transmitter and the $\overline{\text{RxCLK}}$ on the receiver are the same.

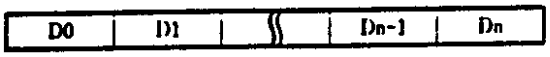
4.3.2 Synchronous Mode Operation

(1) Sending

Pin TxDATA continues to be in a high level status until the CPU writes the first data (normally, SYNC characters) after the transmitter is enabled following its setting in the SYNC mode. When data is written, Pin TxDATA sends one bit for each rising edge of $\overline{\text{TxCLK}}$ when the level of $\overline{\text{CTS}}$ is low. Unlike the asynchronous mode, neither a start bit nor a stop bit is added. A parity bit can be set.

Fig. 4-9 Synchronous Mode Data Format

• Character data without parity



• Character data with parity

n: 4, 5, 6, 7

Once sending is started, the CPU must write data in the uPD71051 at the same rate as that of $\overline{\text{TxCLK}}$. If TxEMP = 1 is established after data writing by the CPU is delayed, the uPD71051 continues to automatically send one or two SYNC characters until the CPU writes data. TxEMP = 0 is established when data is written, and written data is sent as soon as sending of the SYNC characters finishes. Automatic sending of the SYNC characters becomes effective after the CPU rewrites data, and the SYNC characters are not sent automatically merely by enabling the transmitter.

uPD71051 does not operate as specified when a command word is written while the uPD71051 is automatically sending SYNC characters. For this reason, when a command word has to be written during automatic sending (TxEMP = 1) of SYNC characters, the same data as that of the SYNC characters is written, and the command word is written while sending that data (See Fig. 4-11).

Fig. 4-12 shows a program example for sending in the SYNC mode.

Fig. 4-10 Sync Mode Transmit Timing

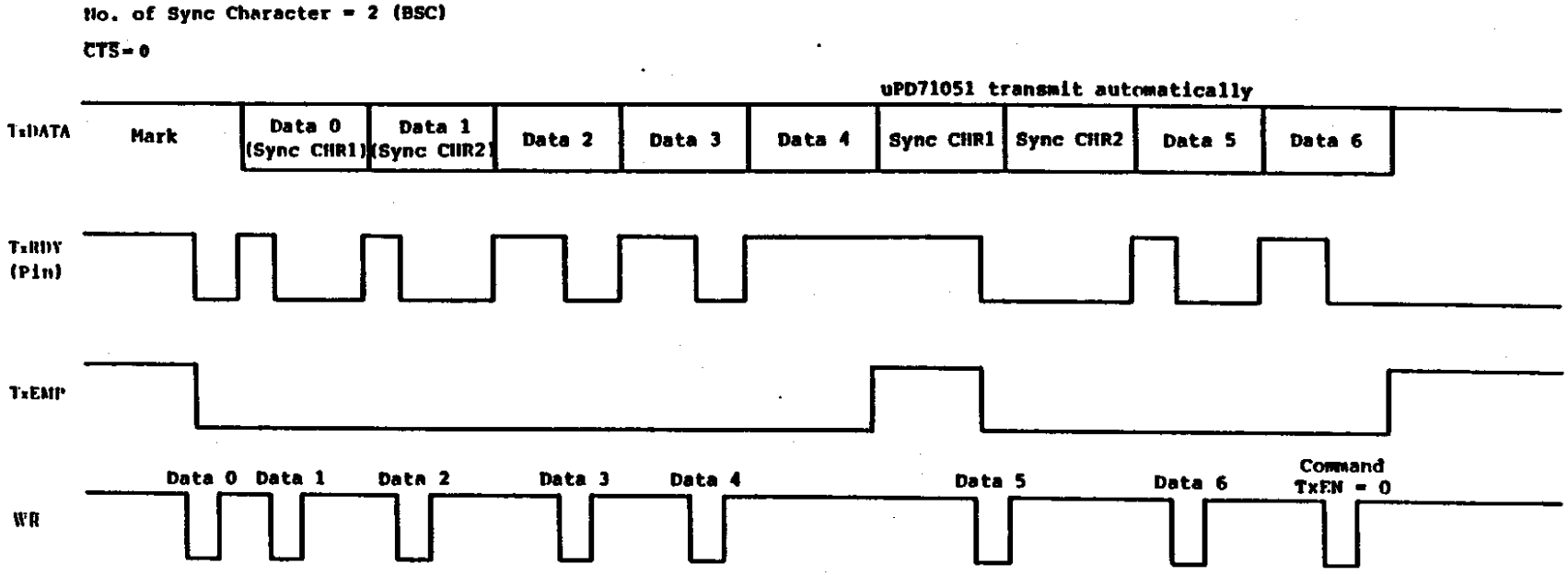
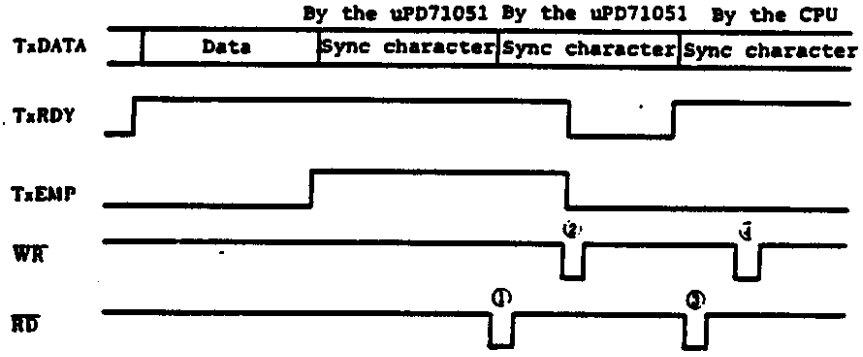


Fig. 4-11 Command Issue during Transmitting Sync Characters

No. of sync characters = 1



①: Confirm the auto-transmit of the sync character (TxEMP = 1) by status.

②: Write sync character data

③: Confirm the transmission start of the sync character written by the CPU by reading the status.

④: Write command word

Fig. 4-12 Synchronous Mode Transmit Program Example

```
SYNTX :  CALL SYNMOD                    Set sync mode
         MOV   AL, 00010001B            } Command
         OUT   PCTRL, AL                  • Error flag clear
                                          • Transmit enable
         MOV   BW, OFFSET TXDADR        Transmit data area
TXLEN :  IN    AL, PCTRL                }
         TEST1 AL,0                     }
         BZ    TXLEN                    } Transmit No. of
         MOV   AL, LDLEN                } transmit data
         OUT   PDATA, AL                }
         MOV   CL, AL                   } Set No. of transmit data to
         MOV   CH, 0                    } counter
TXDATA:  IN    AL, PCTRL                }
         TEST1 AL, 0                    }
         BZ    TXSTART                  }
         MOV   AL, [BW]                 } Transmit data as much No. of
         OUT   PDATA, AL                } set in the counter
         INC   BW                       }
         DBNZ  TXDATA                   }
         MOV   AL, 00010000B            } Command
         OUT   PCTRL, AL                }   • Error flag clear
                                        }   • Transmit disable
         RET
SYNC1    DB?                            Sync character 1
SYNC2    DB?                            Sync character 2
LDLEN    DB?                            Set No. of data to be
                                        transmitted (1 to 255)
TXDADR   DB 255 DUP (?)                 Data to be transmitted
```

```
SYNMOD:  MOV   AL,0
         OUT   PCTRL, AL
         OUT   PCTRL, AL
         OUT   PCTRL, AL
         MOV   AL, 01000000B
         OUT   PCTRL, AL
         MOV   AL, 00111100B
         OUT   PCTRL, AL
         MOV   AL, SYNC1
         OUT   PCTRL, AL
         MOV   AL, SYNC2
         OUT   PCTRL, AL
         RET
```

Write control words 3 times with 00H to accept the new command word unconditionally

Software reset

Write mode word
- Sync characters = 2
- Internal sync detect
- Even parity
- 8-bit/character

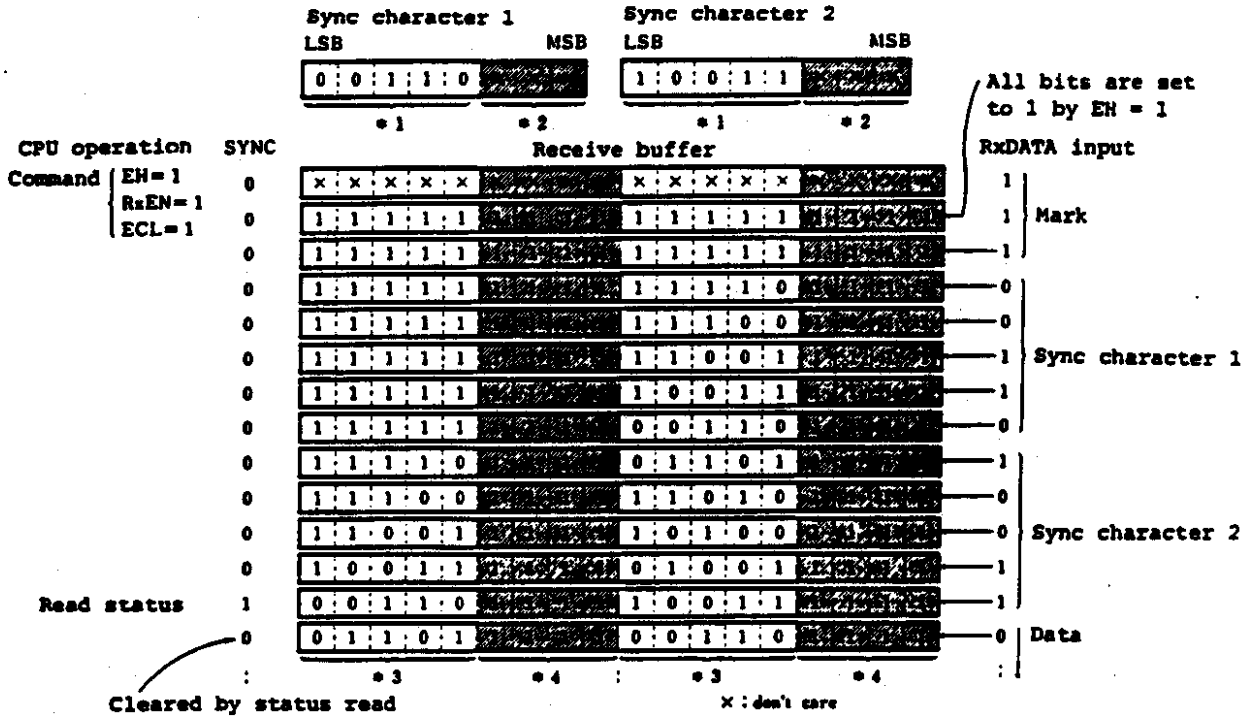
Write sync character

(2) Receiving

The first requirement for receiving in the SYNC mode is to synchronize with the sending side. For this reason, the first command after setting the SYNC mode and writing the SYNC character (C/$\overline{D}$ = 1) has to be EH = 1, ECL = 1, and RxEN = 1. When entering the hunt phase with this command, all the bits in the receive buffer are set to 1. In internal synchronization, data on Pin RxDATA is input to the receive buffer for each rising edge of $\overline{RxCLK}$ and is compared with the SYNC character at the same time.

Fig. 4-13 Internal Sync Detect Operation Example

5-bit character, No parity, 2 sync character
Sync character 1 = 01100B, Sync character 2 = 11001B



*1 to *4: As character is 5-bit, the part *1 of sync character register (lower 5-bit) is valid and the part *2 is don't care.
As to receive buffer, because of character is 5-bit and no parity, the part *3 is valid and the part *4 is not used. When the part *1 and the part *3 are matched, SYNC becomes 1. (With parity, the L.S.B of the part *4 is used for parity bit, but it is not used to compare with the sync character.)

When the receive buffer and SYNC character coincide, the uPD71051 finishes the hunt phase and becomes SYNC = 1, becomes 1 in the center of the last bit of the SYNC character. When a parity exists, SYNC becomes 1 in the center of the parity bit. When synchronized, receiving starts beginning with the bit as data.

In external SYNC detection, synchronization is achieved by giving a high level for more than one period of $\overline{\text{RxCLK}}$ to Pin SYNC by an external circuit, and the hunt phase is finished to start data receiving. At this time, the status SYNC bit becomes 1, and then becomes 0 when the status is read. The status SYNC bit is set to 1 when the SYNC input has a rising edge followed by a high level of more than one period of $\overline{\text{RxCLK}}$ even after synchronization is achieved.

The uPD71051 can be made to regain synchronization anytime by giving an enter hunt phase command when it loses synchronization.

After synchronization, a SYNC character is compared with each character regardless of whether it is internal or external detection. When coincided in comparison, SYNC (status only in external detection) becomes 1, indicating that a SYNC character has been received. In this case also, SYNC (status only in external detection) becomes 0 when the status is read.

Overrun and parity errors are checked in the same method as that of the asynchronous mode, affecting the status flag only. Parity checking is not performed in the hunt phase.

Fig. 4-14 illustrates a program example to show receiving of data sent in Fig. 4-12.

Fig. 4-14 Synchronous Mode Receive Program Example

```
SYNRX :  CALL   SYNMOD                  Set sync. mode
         MOV    AL, 10010100B           Command
         OUT    PCTRL, AL                 • Enter hunt phase
                                          • Error flag clear
                                          • Receive enable
         MOV    BW, OFFSET RXDADR       Set receive data store
                                        address
RXLEN :  IN     AL, PCTRL
         TEST1  AL, 1                   Receive the No. of receive
         BZ     RXLEN                   data
         IN     AL, PDATA
         MOV    STLEN, AL
         MOV    CL, AL                  Set the No. of receive data
         MOV    CH, 0                   to both variable and counter
RXDATA:  IN     AL, PCTRL
         TEST1  AL, 1
         BZ     RXDATA
         IN     AL, PDATA               Receive and store data as
         MOV     BW , AL                much No. of the counter
         INC    BW
         DBNZ   RXDATA
         MOV    AL, 00000000B           Command
         OUT    PCTRL, AL                 • Receive disable
         RET
STLEN    DB     ?                       Set No. of receive data
RXDADR   DB     256DUP (0)              Reserve receive data area
```

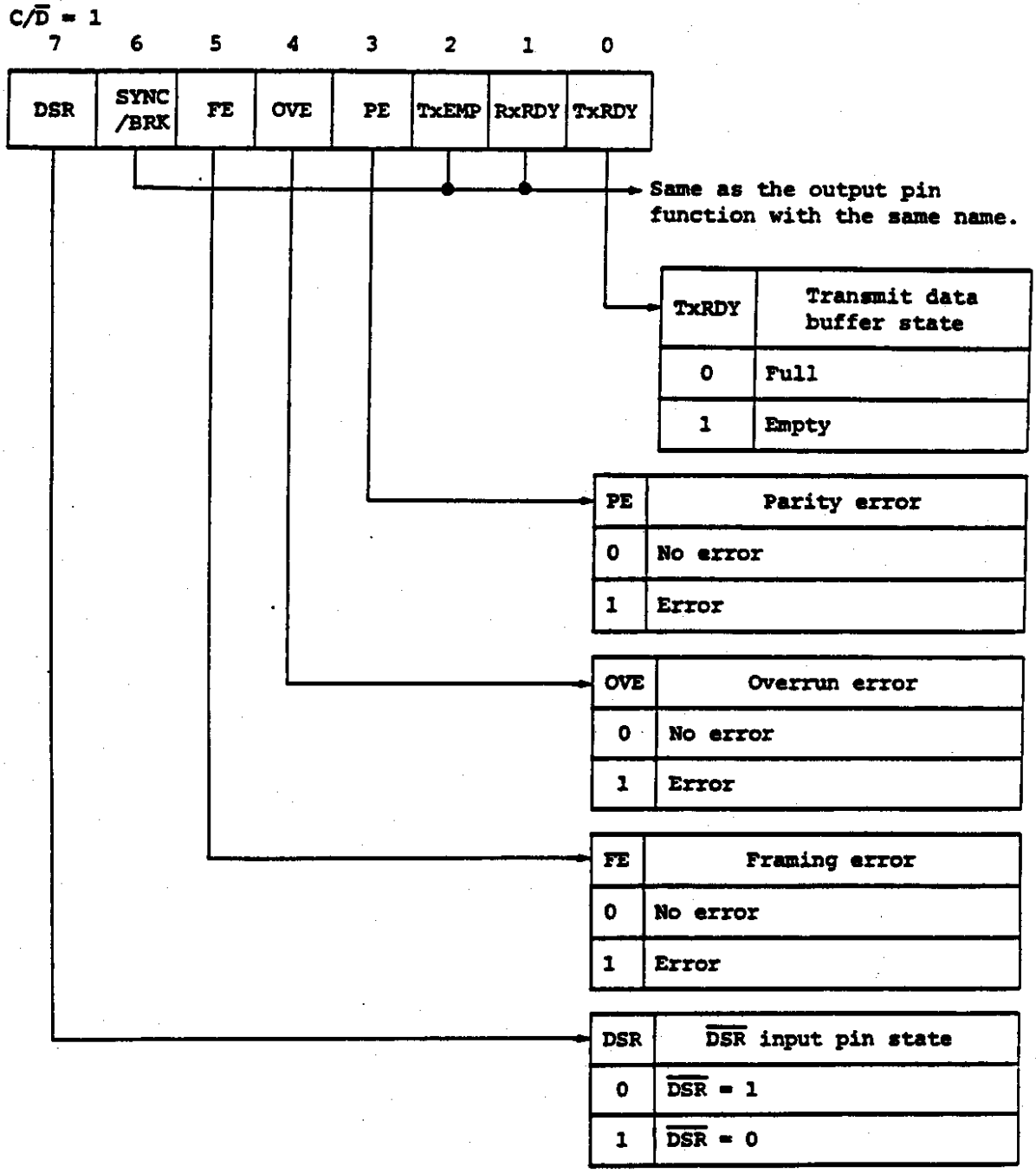
Note: The frequencies of the $\overline{\text{TxCLK}}$ on the transmitter and the $\overline{\text{RxCLK}}$ on the receiver are the same.

4.4 Status

The CPU can read the status of the uPD71051 during an operation of the uPD71051 (except in the stand-by mode). By doing this, the CPU can know data writing and reading timing, occurrence of errors during receiving, etc.

The status is read after establishing $C/\overline{D}$ = 1. Status updating is disabled during reading of the status. Note that status updating is delayed a maximum 28 clock periods after an event affecting the status has taken place.

Fig. 4-15 Status format



The individual bits are described in the following.

Bits TxEMP and RxRDY have the same meanings as those of the output pins of the same names.

Bit SYNC/BRK has the same meaning as that of Pin SYNC/BRK in almost all instances. Its status does not coincide with the pin only in external synchronization of the SYNC mode. In this case, Pin SYNC becomes input, and the status becomes 1 when a rising edge is detected in this input. The status does not become 0 until it is read even when the level of input changes to the low level. The status becomes 1 when a SYNC character is input with $\overline{\text{RxDATA}}$ input even when the input is in a low level state.

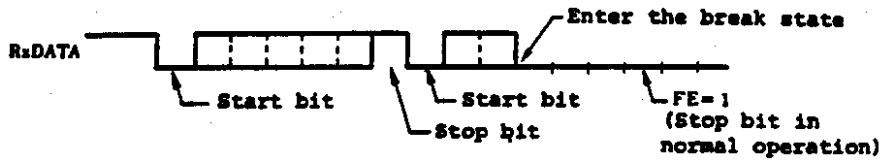
Bit DSR (data set ready) shows the status of the general-purpose input Pin $\overline{\text{DSR}}$. DSR = 1 is established when the level of $\overline{\text{DSR}}$ is low.

Bit FE (framing error) becomes 1 when more than one effective stop bit is not detected at the end of each data block during receiving operation in the asynchronous mode, indicating that a framing error has occurred.

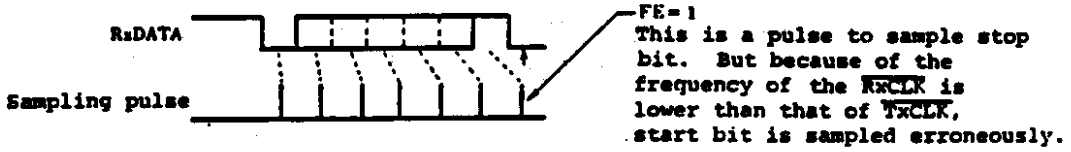
Fig. 4-16 Framing Error

1 character = 5-bit, No parity, stop bits = 1-bit

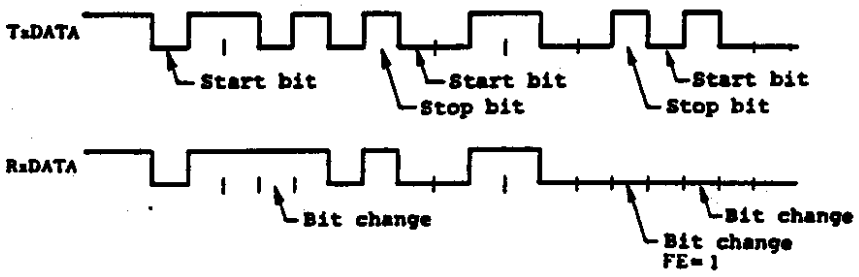
(i) In the case of break state



(ii) In the case of frequency difference between $\overline{\text{RxCLK}}$ and $\overline{\text{TxCLK}}$ is big.

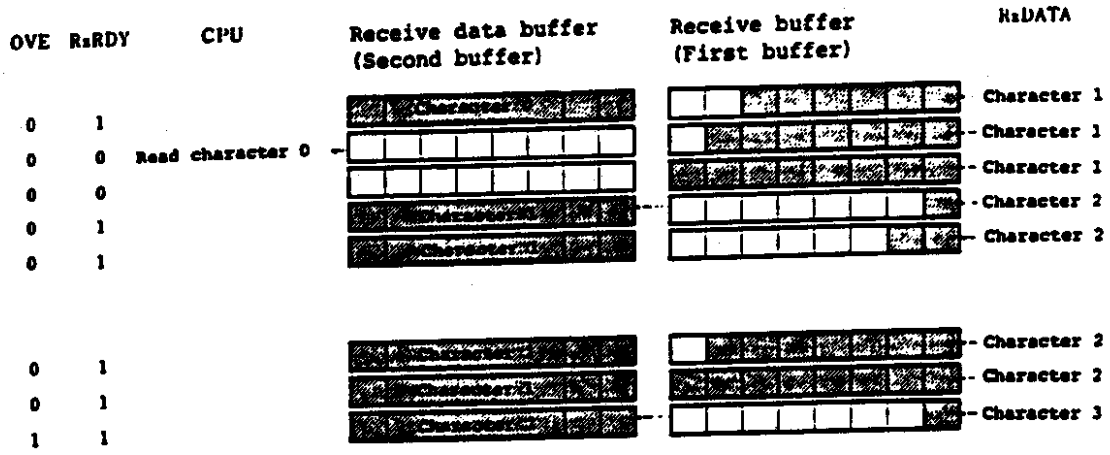


(iii) When data is changed during transmit (Using less reliable transmission



Bit OVE (overrun error) becomes 1 when reading received data by CPU during receiving is delayed, and shows that an overrun error has occurred. In this case, one piece of data received previously is lost in the receive data buffer.

Fig. 4-17 Overrun Error



Char. 1 is not read by the CPU and discarded by receiving char. 2.

Bit PE (parity error) becomes 1 when a parity error occurs while the parity is effective in a receive state.

The foregoing three errors do not disable operations of the uPD71051. All these three error flags are cleared to 0 by a command that has the ECL bit set to 1.

Bit TxRDY (transmitter ready) always becomes 1 when the send data buffer is empty. The output pin of the same name becomes 1 when the send data buffer is empty, the level of $\overline{CTS}$ is low, and TxEN = 1, and the conditions of the status and pin setting will not be the same.

Bit TxRDY = send data buffer empty

Pin TxRDY = (send data buffer empty).($\overline{CTS}$ = 0).(TxEN = 1)

5. STAND-BY MODE

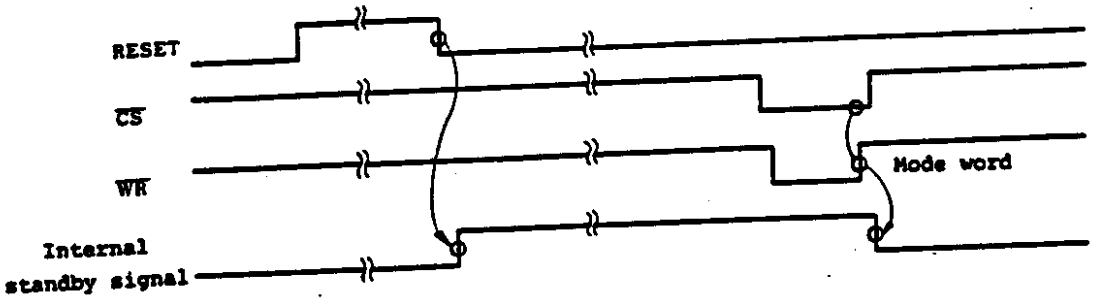
The uPD71051 consumes low power as it is based on CMOS fabrication technology. By entering into a stand-by mode, it restricts feeding of external input clocks (CLK, $\overline{\text{TxCLK}}$ and $\overline{\text{RxCLK}}$) into the inside to consume less power.

Two methods can be used to enter a stand-by mode. One method is hard resetting. Inputting a high level to Pin RESET, the device enters a stand-by mode by the falling edge of the high level. The second method is soft resetting by a command.

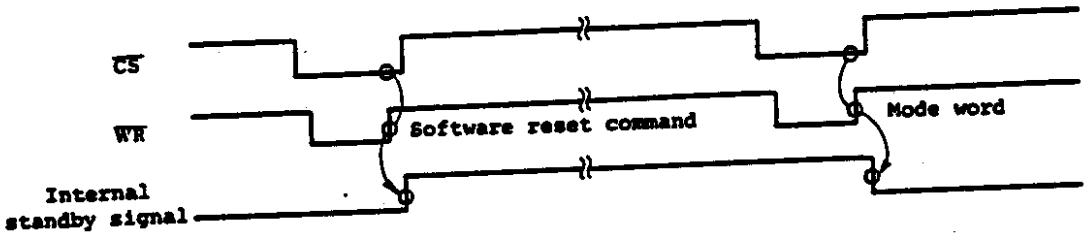
Writing of a mode word is the only way to escape from the stand-by mode. Fig. 5-1 shows timing patterns of these operations.

Fig. 5-1 Standby Mode

① Hardware reset



② Software reset



While the internal standby signal is high, the external clocks to the uPD71051 are ignored.

Note: If data ($C/\overline{D}$ = 0) is written to the uPD71051 in the standby mode, the following operations should be undefined.

Table 5-1 Output Pins State in the Standby Mode

Pin name	State
TxRDY	Low level
TxEMP	High level
TxDATA	High level
RxRDY	Low level
SYNC/BRK	Low level
$\overline{\text{DTS}}$	High level
$\overline{\text{RTS}}$	High level

6. ELECTRICAL CHARACTERISTICS

Maximum Ratings (Ta = 25°C)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		-0.5 to +7.0	V
Input voltage	V_I		-0.5 to V_{DD}+0.3	V
Output voltage	V_O		-0.5 to V_{DD}+0.3	V
Operating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

DC Characteristics (Ta = -40 to +85°C, V_{DD} = 5V±10%)

Item	Symbol	Condition	uPD71051			uPD71051-10			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
High level input voltage	V_{IH}		2.2		V_{DD}+0.3	2.2		V_{DD}+0.3	V
Low level input voltage	V_{IL}		-0.5		0.8	-0.5		0.8	V
High level output voltage	V_{OH}	I_{OH} = -400 uA	0.7xV_{DD}			0.7xV_{DD}			V
Low level output voltage	V_{OL}	I_{OL} = 2.5 mA			0.4			0.4	V
High level input leakage current	I_{LIH}	V_I = V_{DD}			10			10	uA
Low level input leakage current	I_{LIL}	V_I = 0V			-10			-10	uA
High level output leakage current	I_{LOH}	V_O = V_{DD}			10			10	uA
Low level output leakage current	I_{LOL}	V_O = 0V			-10			-10	uA
Supply current	I_{DD1}	During operating			10			10	mA
	I_{DD2}	During standby		50	100		2	50	uA

Capacitance (Ta = 25°C, V_{DD} = 0V)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz for other than measured pins, 0V			10	pF
I/O capacitance	C_{IO}				20	pF

AC Characteristics (Ta = -40 to +85°C, V_{DD} = 5V±10%)

Read Cycle

Item	Symbol	Condition	uPD71051		uPD71051-10		Unit
			MIN.	MAX.	MIN.	MAX.	
Address ($\overline{CS}$, C/$\overline{D}$) setting time (for $\overline{RD}$ ↓)	t_{SAR}		0		0		ns
Address ($\overline{CS}$, C/$\overline{D}$) maintain time (for $\overline{RD}$ ↑)	t_{HRA}		0		0		ns
$\overline{RD}$ pulse width	t_{RRL}		150		95		ns
Data delay time (for $\overline{RD}$ ↓)	t_{DRD}	C_L=150pF		120		85	ns
Data float time (for $\overline{RD}$ ↑)	t_{FRD}		10	80	10	65	ns
Port ($\overline{DSR}$, $\overline{CTS}$) setting time (for $\overline{RD}$ ↓)	t_{SPR}		20		20		t_{CYK}

Write Cycle

Item	Symbol	Condition	uPD71051		uPD71051-10		Unit
			MIN.	MAX.	MIN.	MAX.	
Address ($\overline{CS}$, C/$\overline{D}$) setting time (for $\overline{WR}$ ↑)	t_{SAW}		0		0		ns
Address ($\overline{CS}$, C/$\overline{D}$) maintain time (for $\overline{WR}$ ↑)	t_{HWA}		0		0		ns
$\overline{WR}$ pulse width	t_{WWL}		150		95		ns
Data setting time (for $\overline{WR}$ ↑)	t_{SDW}		80		80		ns
Data maintain time (for $\overline{WR}$ ↑)	t_{HWD}		0		0		ns
Port ($\overline{DTR}$, $\overline{RTS}$), TxEN delay time (for $\overline{WR}$ ↑)	t_{DWP}			8		8	t_{CYK}
Write recovery time	t_{RV}	During mode specification	6		6		t_{CYK}
		In start-stop mode	8		8		t_{CYK}
		In synchronous mode	16		16		t_{CYK}

AC Characteristics

Serial Transfer Timing

Item		Symbol	Condition	uPD71051		uPD71051-10		Unit
				MIN.	MAX.	MIN.	MAX.	
Clock cycle		t_{CYK}		125	DC	100	DC	ns
Clock pulse high level width		t_{KKH}		50		35		ns
Clock pulse low level width		t_{KKL}		35		25		ns
Clock rise time		t_{KR}		5	20	5	20	ns
Clock fall time		t_{KF}		5	20	5	20	ns
TxDATA delay time (for $\overline{\text{TxCLK}}$)		t_{DTKTD}			0.5		0.5	us
Transmitter input clock pulse low level width	1 x BR *1	t_{TKTKL}		12		12		t_{CYK}
	16 x, 64 x BR			1		1		t_{CYK}
Transmitter input clock pulse high level width	1 x BR	t_{TKTKH}		15		15		t_{CYK}
	16 x, 64 x BR			3		3		t_{CYK}

(Cont'd)

Item		Symbol	Condition	uPD71051		uPD71051-10		Unit
				MIN.	MAX.	MIN.	MAX.	
Transmitter input jack frequency	1 x BR	f_{TK}*2		DC	240	DC	300	kHz
	16 x BR			DC	1536	DC	1920	kHz
	64 x BR			DC	1536	DC	1920	kHz
Receiver input clock pulse low level width	1 x BR	f_{RKRKL}		12		12		t_{CYK}
	16 x, 64 x BR			1		1		t_{CYK}
Receiver input clock pulse high level width	1 x BR	f_{RKRKH}		15		15		t_{CYK}
	16 x, 64 x BR			3		3		t_{CYK}
Receiver input clock frequency	1 x BR	f_{RK}*2		DC	240	DC	300	kHz
	16 x BR			DC	1536	DC	1920	kHz
	64 x BR			DC	1536	DC	1920	kHz
RxDATA setting time (for sampling pulse)		t_{SRDSP}		1		1		us
RxDATA maintain time (for sampling pulse)		t_{HSPRD}		1		1		us
TxEMP delay time		t_{DTXEP}			20		20	t_{CYK}
TxRDY delay time (TxRDY ↑)		t_{DTXR}			8		8	t_{CYK}

(Cont'd)

Item	Symbol	Condition	uPD71051		uPD71051-10		Unit
			MIN.	MAX.	MIN.	MAX.	
TxRDY delay time (TxRDY ↓)	t_{DWTXR}			200		100	ns
RxRDY delay time (RxRDY ↑)	t_{DRXR}			26		26	t_{CYK}
RxRDY delay time (RxRDY ↓)	t_{DRRXR}			200		100	ns
SYNC output delay time (Internal synchronization)	t_{DRKSY}			26		26	t_{CYK}
SYNC input delay time (External synchronization)	t_{SSYRK}		18		18		t_{CYK}
Reset pulse high level width			6		6		t_{CYK}

Note 1: Baud Rate
2: The following restrictions apply to the frequency of $\overline{TxCLK}$ and $\overline{RxCLK}$:

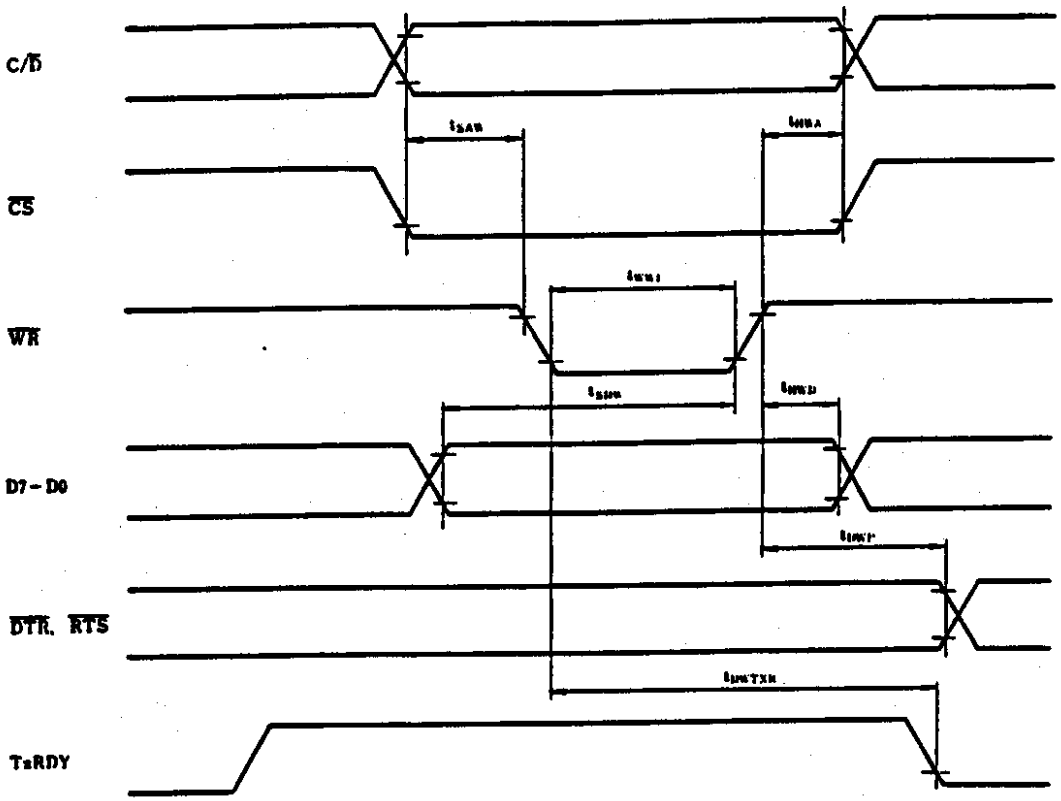
1 x BR: f_{TK}, $f_{RK} \leq 1/30\ t_{CYK}$

16x, 64 x BR: f_{TK}, $f_{RK} \leq 1/4.5\ t_{CYK}$

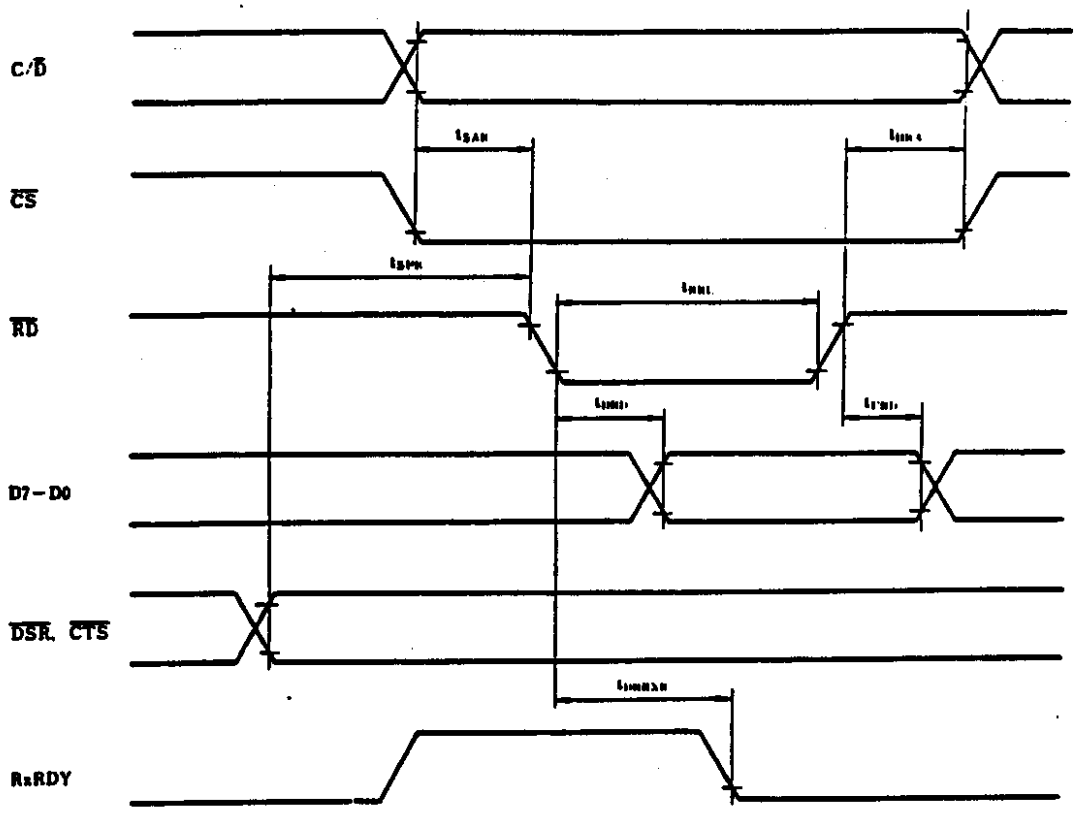
Remarks 1. The system clock is not input during a reset.
2. There is a maximum delay of 28 t_{CYK} due to the generation of events which affect status updates.

AC Test Input Waveform

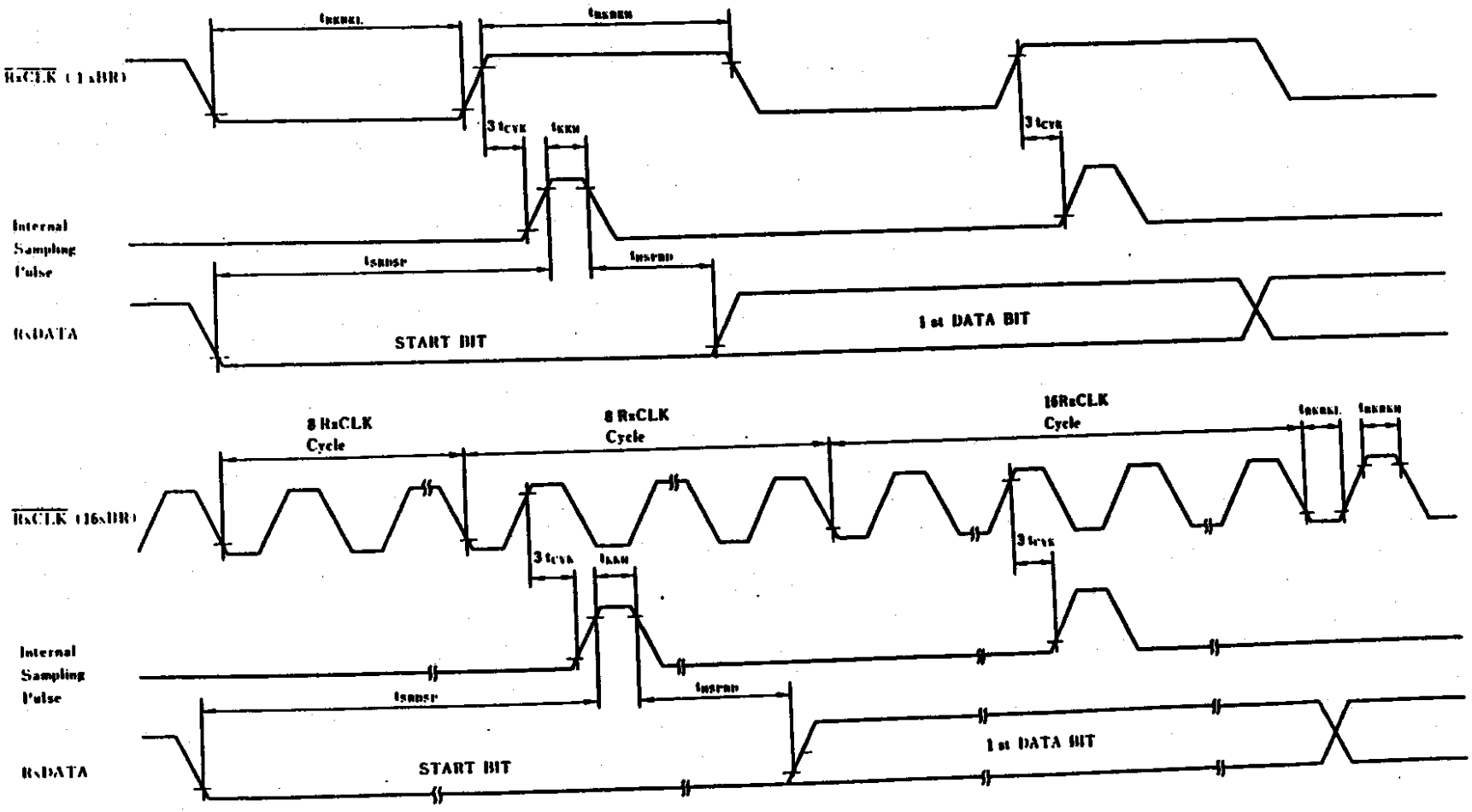
Write Data Cycle



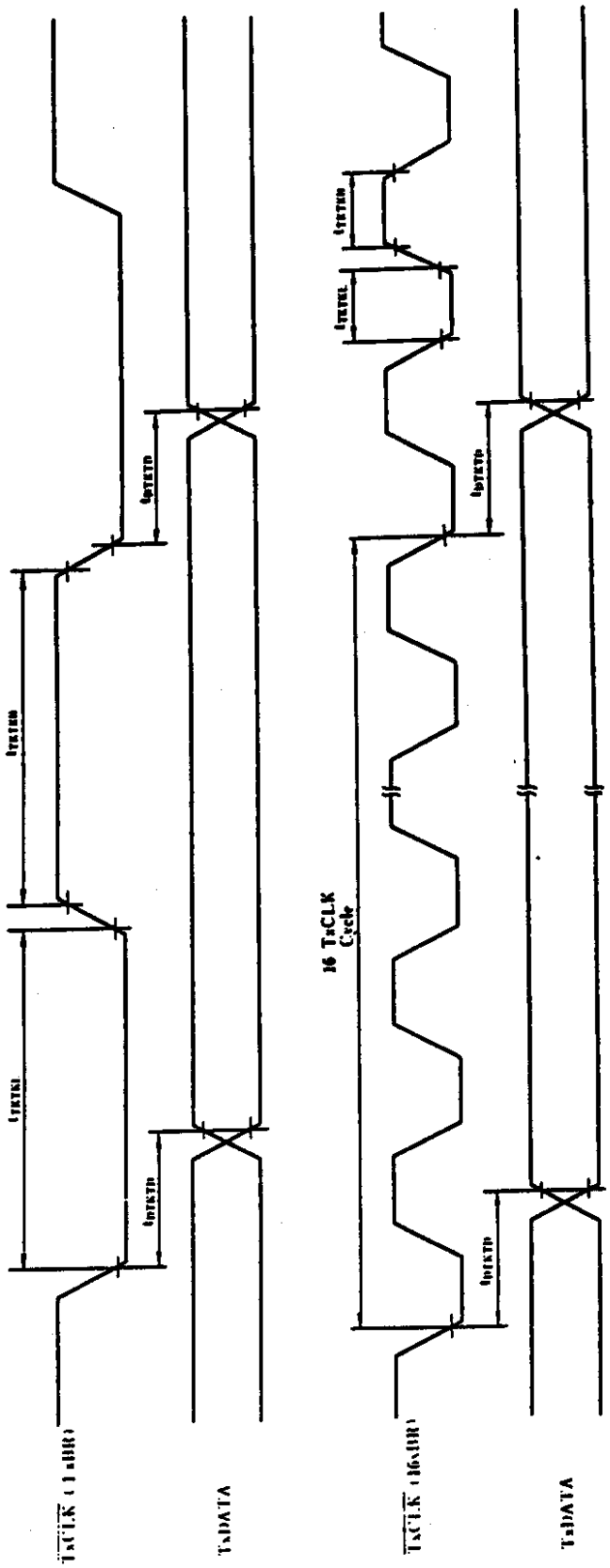
Read Data Cycle



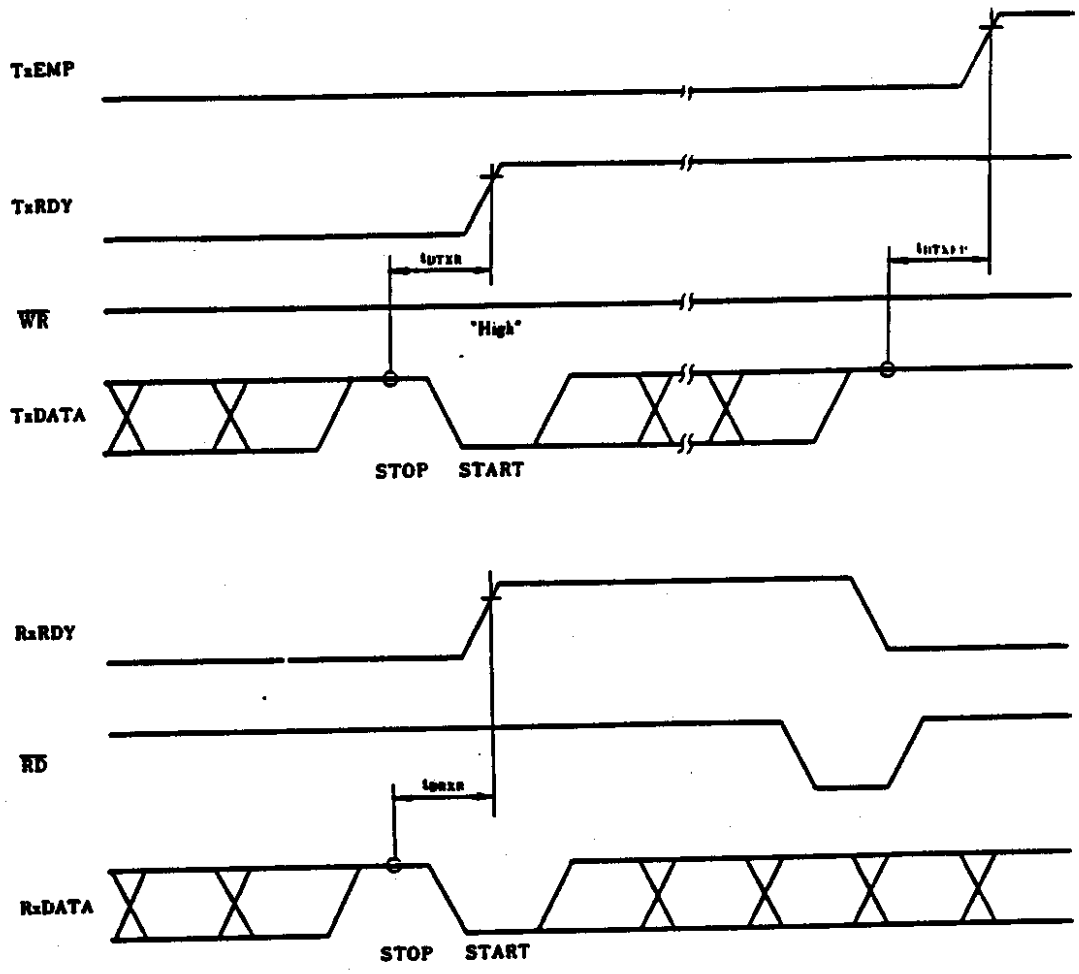
Receiver Clock and RxDATA



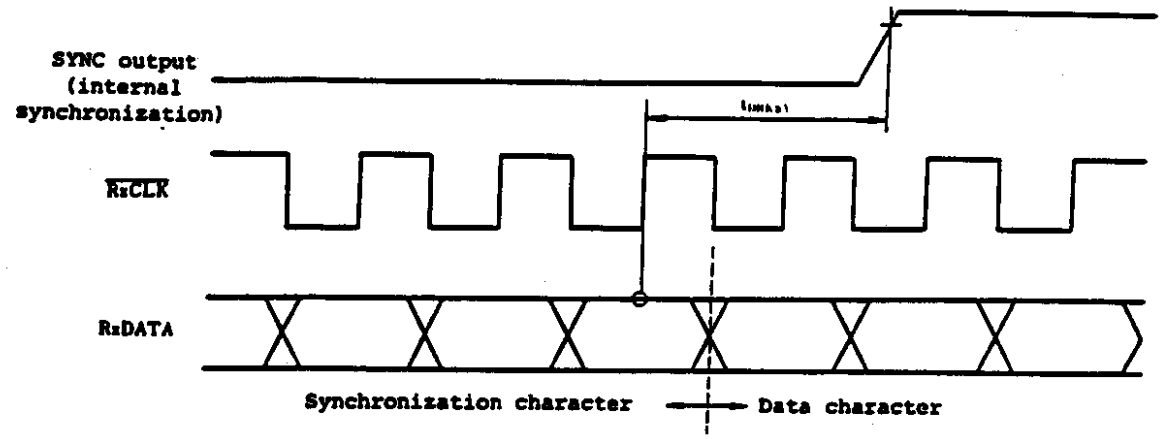
Transmitter Clock and TxDATA

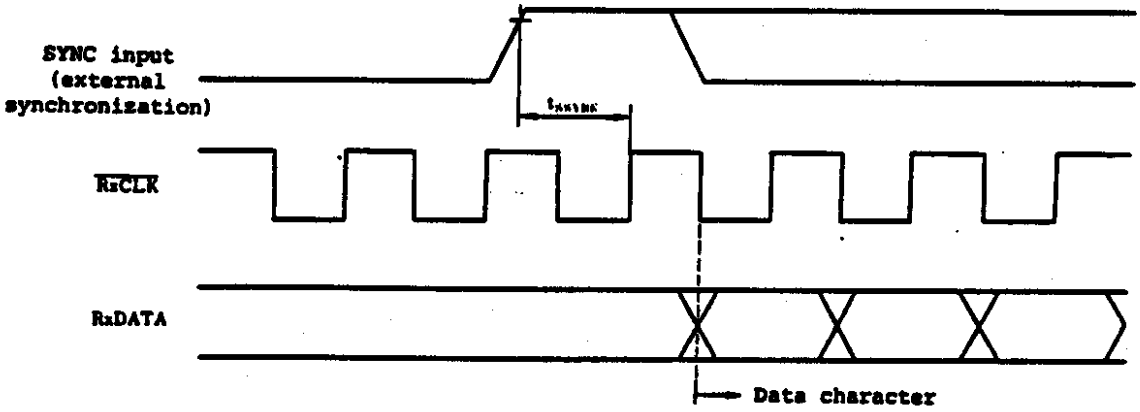


Flag Timing

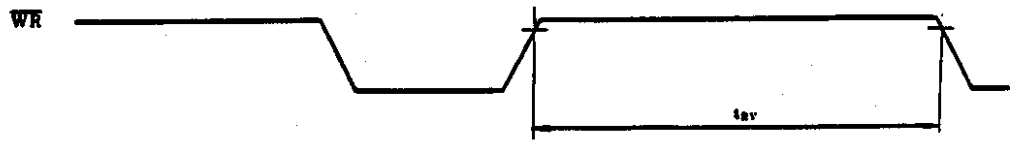


RxDATA and SYNC Timing

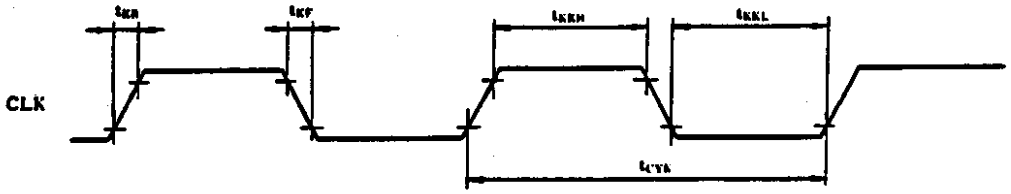




Write Recovery Time

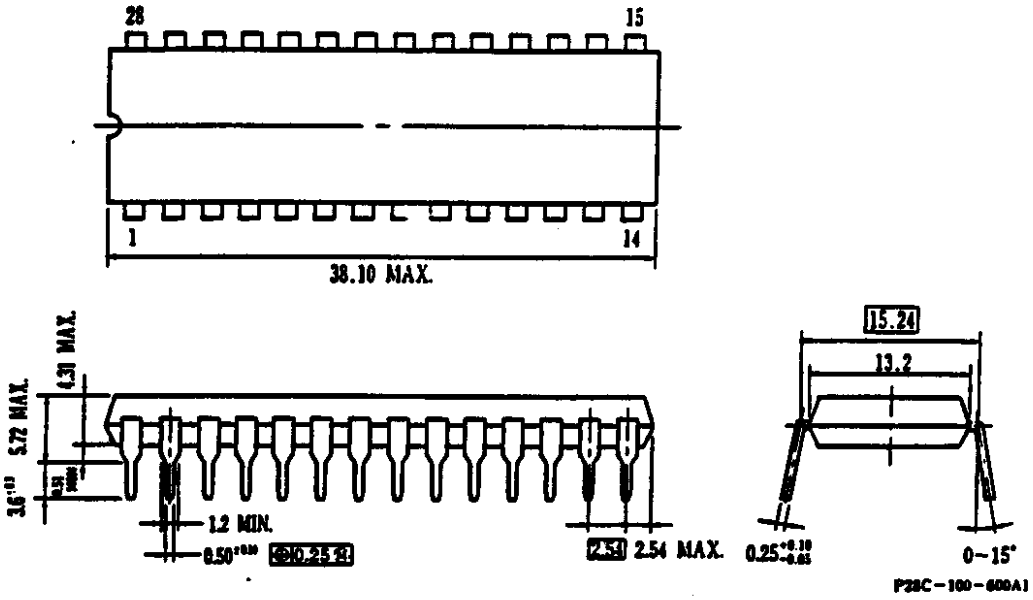


MAIN CLOCK

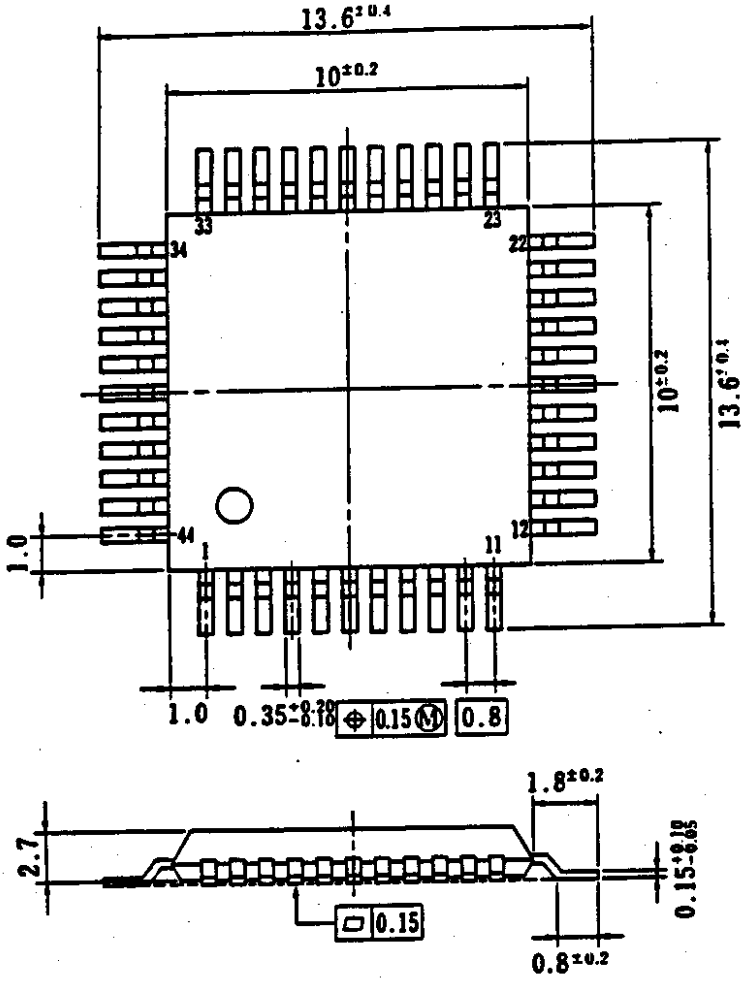


7. DIMENSIONS

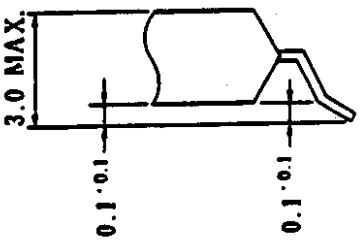
28-Pin Plastic DIP (600 mil) Dimensions (Unit: mm)



44-Pin Plastic QFP Dimensions (Unit: mm)



Detail of lead end



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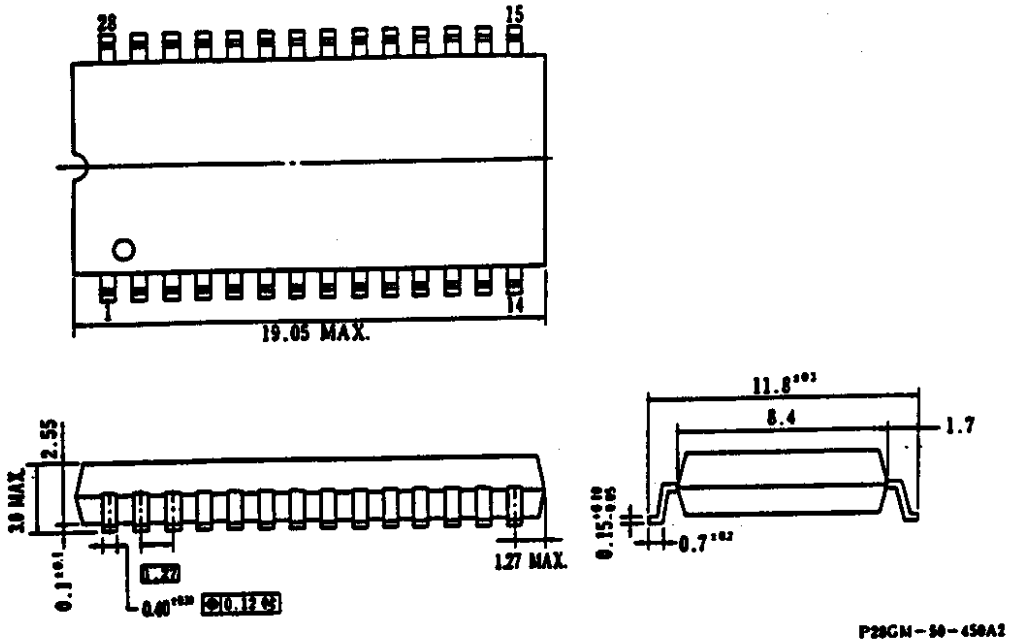
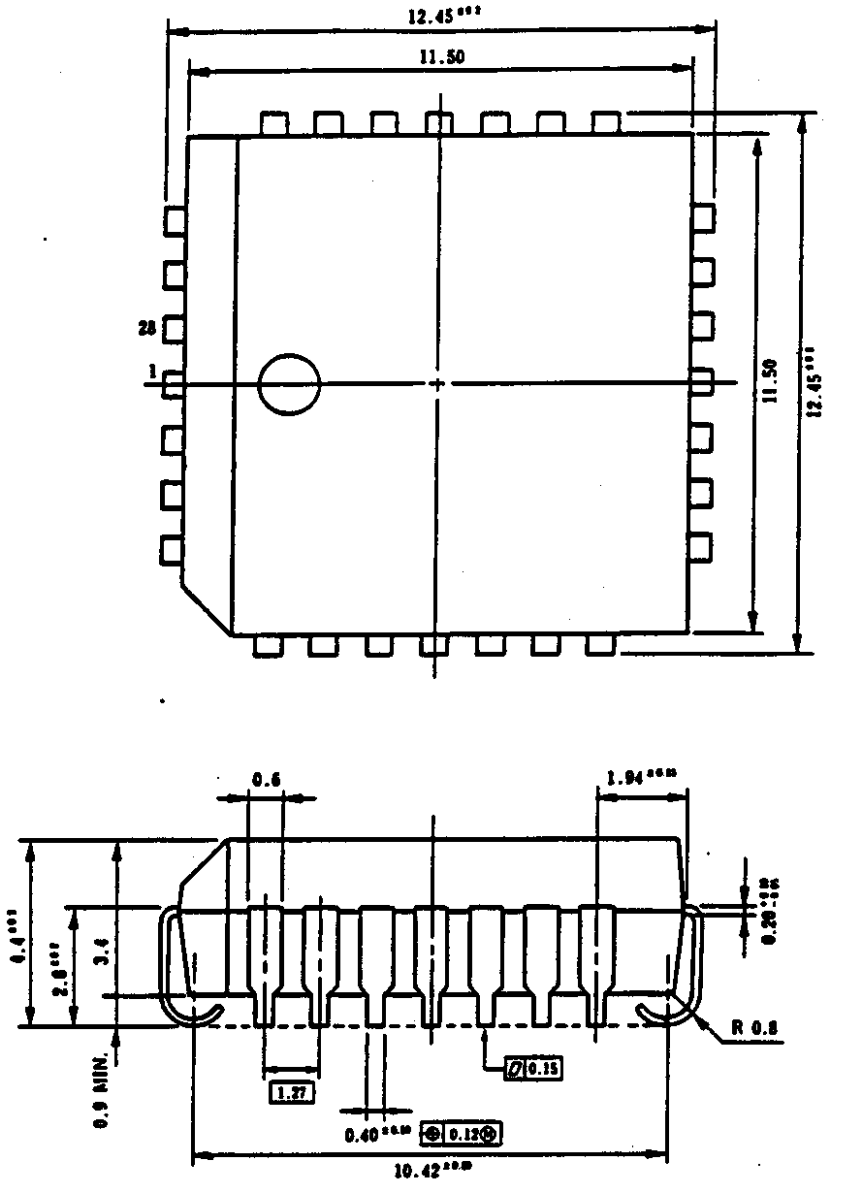
28-Pin Plastic SOP (450 mil) Dimensions (Unit: mm)



28-Pin PLCC Dimensions (Unit: mm)



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