

# Product Brief

Intel® 5000P Chipset

Embedded Computing



## Intel® 5000P Chipset for Embedded Computing

### Supporting Dual-Core Intel® Xeon® Processors 5100 and 5200 Series and Quad-Core Intel® Xeon® Processors 5300 and 5400 Series

#### Product Overview

The Intel® 5000P chipset, utilizing next-generation dual-processor server chipset technology, enables low-power consumption with improved platform reliability, accessibility, serviceability (RAS) and system manageability. Compared to previous-generation Intel® chipsets, the Intel 5000P chipset delivers higher throughput with dual, point-to-point system buses, faster memory and I/O bandwidth, and Fully Buffered DIMM (FB-DIMM) support.

The 1066 and 1333 MHz front-side bus (FSB) provides support for the Dual-Core Intel® Xeon® Processor 5100 and 5200<sup>a</sup> Series and the Quad-Core Intel® Xeon® Processor 5300 and 5400<sup>a</sup> Series. These advanced 64-bit processors combine the benefits of dual-core and quad-core processing with dual-processor capabilities (up to four or eight cores for a dual-processor platform), enabling embedded equipment manufacturers to build high-performance, power-efficient platforms with greater data throughput to perform diverse tasks simultaneously.

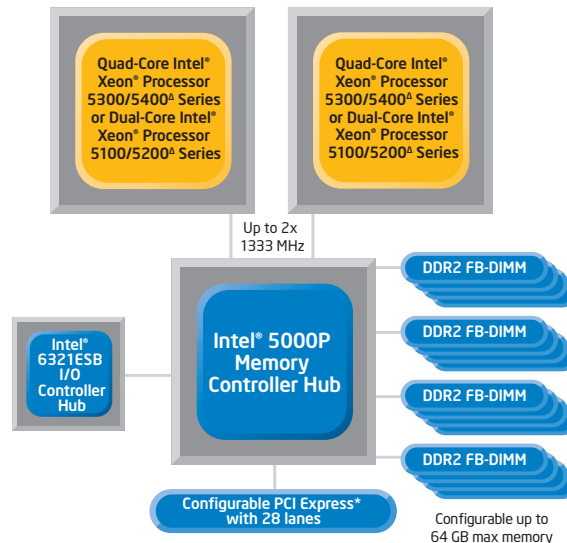
#### PCI Express\*

PCI Express has become the mainstream I/O technology for balanced platforms, providing the necessary bandwidth and lower latency to support the enhanced capabilities of the Dual- and Quad-Core

Intel® Xeon® processor. A PCIe x1 link delivers a bi-directional peak bandwidth of 500 MB/s, while x4 and x8 links provide 2 GB/s and 4 GB/s, respectively. The Intel 5000P MCH supports three x8 PCIe links and the Intel 6321ESB I/O Controller Hub (ICH) supports three x4 PCIe links. Platform designers may bifurcate each x8 link into two x4 links for configuration flexibility.

#### Advanced Platform RAS Features

- **Memory mirroring** splits the memory subsystem and duplicates the data in each half. If one set of memory fails, the other set enables continued operation and system availability.
- **DIMM sparing** swaps “defective” DIMMs with installed but otherwise unused DIMMs for high availability.
- **x4 or x8 Single Device Data Correction (SDDC)** allows the system to fix the failure of an entire DRAM device on-the-fly by removing a single DRAM from the memory map and recovering its data into a new device.
- **Demand and patrol scrubbing** proactively searches the system memory, repairing correctable errors or permanently marking the memory location as unreadable.



Intel® 5000P chipset-based platforms

- **Error Correcting Code (ECC)** detects single-bit and double-bit errors, and automatically corrects single-bit errors on internal data paths. Cyclic redundancy check (CRC) and error correction on address, command, and data paths help boost system reliability and availability.
- **Hot-plug PCIe** supports the addition of I/O devices after installation without service interruption.

### Support for Advanced Intel® Platform Technologies

The Intel 5000P chipset supports new dual-processor platforms with features that increase platform performance while improving manageability, responsiveness, efficiency and reliability. These include Intel® 64 Architecture (Intel® 64),<sup>1</sup> Enhanced Intel SpeedStep® technology, and Intel® Matrix Storage technology.<sup>2</sup>

In addition, Intel® I/O Acceleration Technology<sup>3</sup> (Intel® I/OAT) increases memory and I/O throughput and reduces system latency for data-intensive applications. This helps improve network performance by freeing up the CPU for other processing tasks.

### Expanded I/O support with Intel® 6321ESB I/O Controller Hub

The highly integrated Intel® 6321ESB ICH packs server-class I/O features into a condensed piece of silicon. It includes Gigabit Ethernet MAC, supporting two simultaneous GbE connections, and full Baseboard Management Controller. Trusted Platform Module 1.2 device support enhances platform security.

The ICH attaches directly to the MCH through the ESI interface and a x4 or x8 PCIe link. It integrates:

- Six independent Serial ATA controllers, each capable of up to 3.0 GB/second transfer rate
- Software-driven RAID 0, 1, 5 technology for the most demanding storage data transfers and storage security
- Six USB 2.0 ports
- Three PCIe x4 links
- PCI-X 64/133 bus segment

Features	Benefits
Supports two Dual- or Quad-Core Intel® Xeon® processors 5000 <sup>a</sup> series	<ul style="list-style-type: none"> <li>▪ Optimized performance for intensive, high-performance computing demands</li> </ul>
1066 and 1333 MHz dual independent buses	<ul style="list-style-type: none"> <li>▪ Increased platform system bus bandwidth delivers outstanding independent performance</li> </ul>
Advanced platform reliability, accessibility and serviceability (RAS)	<ul style="list-style-type: none"> <li>▪ Features such as memory ECC, Intel® x4 and x8 Single Device Data Correction<sup>4</sup> (SDDC), DIMM sparing, and memory mirroring for improved system reliability</li> <li>▪ 32-bit CRC on PCIe</li> <li>▪ Hot swap PCIe enhances serviceability</li> <li>▪ SMBus port connects to Intel® 5000P MCH for remote management operation</li> </ul>
PCI Express <sup>5</sup>	<ul style="list-style-type: none"> <li>▪ Serial I/O technology provides direct connection between MCH and PCI Express components/adapters with bandwidth up to 4 GB/second on each PCI Express x8 interface</li> </ul>
FB-DIMM 533 MHz and 667 MHz	<ul style="list-style-type: none"> <li>▪ Maximum memory bandwidth up to 17 GB/second memory interface for 533 MHz and up to 21 GB/second for 667 MHz</li> <li>▪ Increased DIMMs per system, providing enhanced memory scalability for memory-intensive applications</li> <li>▪ Up to 64 GB memory capacity</li> </ul>
Intel® 6700PXH 64-bit PCI Hub	<ul style="list-style-type: none"> <li>▪ Optional component for PCI/PCI-X connectivity, offering increased platform flexibility</li> <li>▪ Support for two independent 64-bit, 133 MHz PCI-X segments and two hot-plug controllers (one per segment)</li> </ul>

## Intel® 5000P Chipset for Embedded Computing

Product	Product Code	Package
Intel® 5000P Memory Controller Hub (MCH)	QG5000P	1432 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 6321ESB I/O Controller Hub (ICH)	QG6321	1284 Flip Chip-Ball Grid Array (FC-BGA)
Intel® 6700PXH 64-bit PCI Hub (optional)	QG6700PXH	567 Flip Chip-Ball Grid Array (FC-BGA)

Embedded Intel Architecture Home Page: [intel.com/design/intarch](http://intel.com/design/intarch)

<sup>a</sup> Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See [http://www.intel.com/products/processor\\_number](http://www.intel.com/products/processor_number) for details.

<sup>1</sup> 64-bit Intel® Xeon® processors with Intel® 64 architecture requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel 64 architecture. Processor will not operate (including 32-bit operation) without an Intel 64 architecture-enabled BIOS. Performance will vary depending on your hardware and software configurations. Intel 64 architecture-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

<sup>2</sup> Required Intel RAID Technology Option ROM.

<sup>3</sup> Intel® I/O Acceleration Technology requires an operating system that supports Intel I/OAT.

<sup>4</sup> In a x8 DDR memory device, the Intel® x8 Single Device Data Correction (x8 SDDC) provides error detection and correction for 1 to 8 data bits within a single device.

<sup>5</sup> Reduced power-state L0s not supported.

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information. The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request. Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order. Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting [www.intel.com](http://www.intel.com).

Copyright © 2008 Intel Corporation. All rights reserved.

Intel, the Intel logo, Intel. Leap ahead., Intel. Leap ahead. logo, Xeon, and Intel SpeedStep are trademarks of Intel Corporation in the U.S. and other countries.

\* Other names and brands may be claimed as the property of others.

Printed in USA

0108/KSC/OCG/XX/PDF

 Please Recycle

313346-003US

