Intel® I/O Controller Hub 9 (ICH9) Family

Specification Update

— For the Intel® 82801IB ICH9, 82801IR ICH9R, 82801IH ICH9DH, 82801IO ICH9DO, 82801IBM ICH9M, 82801IEM ICH9M-E, and ICH9M-SFF I/O Controller Hubs

May 2010

Notice: The Intel® I/O Controller Hub 9 (ICH9) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 316973-021

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Revision History

Revision	Description	Date
-001	• Initial Release	June 2007
-002	• Added 82801IO ICH9DO specifications • Added following Errata - Errata 4, Intel ICH9 THRM Polarity on SMBus - Errata 5, Intel ICH9 SPI_CS1# State	August 2007
-003	• Added: • - Errata: 6-ICH9 Level-Triggered Legacy IRQ, 7-ICH9 High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level • - Specification Clarifications: 1-GLANCLK High Time/Low Time Clarification	September 2007
-004	• Added: • - Errata: 8-PET Alerts on SMBus • - Specification Changes: 1-t212 Change, 2-LANRST# Timing, 3-Removing Support for USB Wake from S5 • - Specification Clarifications: 2-DC Characteristics Clarifications, 3-USB UHCI Run/Stop Bit Clarification • - Document Changes: 1-PWROK Description Correction, 2-SMBus/SMLink Connectivity Clarification, 3-External RTC Circuit Correction, 4-D31:F6:52h Register Default Value Correction, 5-SPI_CS0# Description Correction, 6-Miscellaneous Register Default Value Corrections	November 2007
-005	• Added: • - Specification Changes: 4-Addition of EHCI Parity Error Response • - Specification Clarifications: 4-BIOS VSCC and Management Engine VSCC Clarifications • - Document Changes:7-Miscellaneous Electrical Correction	February 2008
-006	• Added: • - Errata: 9-SMBus Host Controller May Hang • - Specification Clarifications: 5-Causes of SMI# /SCI Clarifications, 6-SATA Clock Gating Control Register Clarification • - Document Changes: 8-HPET Address Range Correction	March 2008
-007	• Not released, to synchronize with the specification update posting schedule	
-008	• Added: • - Errata: 10-SATA Gen1 Initialization / LPM Erratum • - Specification Changes:5-SATA Port Multipliers Removal, 6-CF9 Lock Bit Addition • - Document Changes: 9-GNT[3:0]# Pull up Enable Correction	May 2008
-009	• Added: • - Specification Clarifications: 7-CLIST1 (D25:F0:Offset C8h-C9h) Register Corrections, 8-EHCI Initialization Register 1 Clarification, 9-PCI Express* Root Port Configuration Register Clarification • - Document Changes: 10-Device 31 Interrupt Pin Register Corrections,11-D31:F0 Capability List Pointer Addition	June 2008
-010	• Added 82801IBM ICH9M and 82801IEM ICH9M-E specifications. • Moved all Specification Changes, Specification Clarifications, and Documentation Changes to the parent doc (316972-003). • Added: • Errata: 11-ICH9M LAN_PHY_PWR_CTRL Functionality	July 2008
-011	• Added: • Specification Changes: 1-Clock Slew Rate Change • Document Changes: 1-SATA Interlock Switch State (ISS) Bit Clarification, 2-GPIO34 Power Well Correction, 3-Lan Device Initialization Register, 4-HPET Timer.	September 2008

Revision	Description	Date
-012	- Updated Markings Table to include the top marking for ICH9M-SFF part. Added: - Specification Clarifications: 1- t290 and t294 Clarification	October 2008
-013	Added items: - Document Changes: 5 -Add GPIO Signal Reset Notes, 6- Correct EOIFD bit definition, 7- Update GPIO Signals and Note #4 in Section 3.2 Output and I/O Signals Planes and States 8- Correct Table 1-5 ICH9M-E Raid Support	December 2008
-014	Added items: - Specification Changes: 2- SATA Clock Request Support. - Document Changes: 9-Make correction to Table 5-40 Causes of Host and Global Resets 10- Update bit definition for SECOND_TO_STS	January 2009
-015	Added items: - Document Changes: 11- Correct typo for ICH9M-SFF package ball AC22, 12-Correct typo in Table 2-22 General Purpose I/O Signals for GPIO[5:2]	February 2009
-016	Added items: -Document Changes: 13-Correct PCI Express* DSTS register definition for bit 1 (NFED)	April 2009
-017	Added items: - Errata: 12- Intel® I/O Controller Hub 9 (ICH9) Family SATA Low Power Device Detection -Document Changes: 14 -Correct SMBCLK_CTL bit default value 15 - Correct Table 2-24 Strap selection for Boot BIOS Destination	July 2009
-018	Added items: - Errata: 13- Intel® I/O Controller Hub 9 (ICH9) PCI Express Function Disable -Document Changes: 16- Correct section 5.13.7.5 Sex-G3-Sex, Handling Power Failures regarding possible wake events following a power failure	August 2009
-019	Added items: - Errata: 14 Intel® I/O Controller Hub 9 (ICH9) Family SATA SYNC Escape	December 2009
-020	Added items: - Errata: 15 Intel® I/O Controller Hub 9 (ICH9) Family HPET Write Timing - Document Changes: 17- Correct section 10.1.45 Bit 0 definition	February 2010
-021	Added Items: -Document Changes: 18 - Correct section 13.1.23 Bits 15:2 definition	May 2010

Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Number
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	316972-004

Nomenclature

Errata are design defects or errors. These may cause the Product Name’s behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification’s impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product’s lifecycle or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Status	ERRATA
	A2	A3		
1	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) FamilyUHCI Hang with USB Reset
2	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family 1.5 Gb/s SATA Signal Voltage Level
3	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family High-speed USB 2.0 V_{HSOH}
4	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family THRM Polarity on SMBus
5	X		No Fix	Intel® I/O Controller Hub 9 (ICH9) Family SPI_CS1# State
6	X		No Fix	Intel® I/O Controller Hub 9 (ICH9) Family Level-Triggered Legacy IRQ
7	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level
8	X	X	No Fix	PET Alerts on SMBus
9	X	X	No Fix	SMBus Host Controller May Hang
10	X		No Fix	SATA Gen1 Initialization / LPM Erratum
11		X	No Fix	ICH9M LAN_PHY_PWR_CTRL Functionality
12	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family SATA Low Power Device Detection
13	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family PCI Express Function Disable
14	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family SATA SYNC Escape
15	X	X	No Fix	Intel® I/O Controller Hub 9 (ICH9) Family HPET Write Timing

Specification Changes

No.	Steppings		SPECIFICATION CHANGES
	A2	A3	
1	X	X	Clock Slew Rate Change.
2	X	X	SATA Clock Request Support

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	t290 and t294 Clarification

Documentation Changes (Sheet 1 of 2)

No.	DOCUMENTATION CHANGES
1	SATA Interlock Switch State (ISS) Bit Clarification
2	GPIO34 Power Well Correction
3	Lan Device Initialization Register

Documentation Changes (Sheet 2 of 2)

No.	DOCUMENTATION CHANGES
4	HPET Timer
5	Add GPIO Signal Reset Notes
6	Corrected EOIFD bit definition
7	Update GPIO Signals and Note #4 in Section 3.2 Output and I/O Signals Planes and States
8	Correct Table 1-5 ICH9M-E Raid Support
9	Make correction to Table 5-40 Causes of Host and Global Resets
10	Update bit definition for SECOND_TO_STS
11	Correct typo for ICH9M-SFF package ball AC22
12	Correct typo in Table 2-22 General Purpose I/O Signals for GPIO[5:2]
13	Correct PCI Express DSTS register definition for bit 1 (NFED)
14	Correct SMBCLK_CTL bit default value
15	Correct Table 2-24 Strap selection for Boot BIOS Destination
16	Correct section 5.13.7.5 Sx-G3-Sx regarding possible wake events following a power failure
17	Correct section 10.1.45 Bit 0 definition
18	Correct section 13.1.23 Bits 15:2 definition

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Identification Information

Markings

Stepping	S-Spec	Top Marking	Notes
A2	SLA9M	NH82801IB	Intel® 82801IB ICH9
A2	SLA9N	NH82801IR	Intel® 82801IR ICH9R
A2	SLA9P	NH82801IH	Intel® 82801IH ICH9DH
A2	SLAFD	NH82801IO	Intel® 82801IO ICH9DO
A3	SLB8Q	AF82801IBM	Intel® 82801IBM ICH9M
A3	SLB8P	AF82801IEM	Intel® 82801IEM ICH9M-E
A3	SLB8N	AM82801IUX	Intel® ICH9M-SFF

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Intel® ICH9 Device and Revision Identification

ICH9 Device and Revision ID Table

Device Function	Description	Intel® ICH9 Dev ID[1]	ICH9 A2 Rev ID	ICH9 A3 Rev ID	Comments
	LPC	2912h	02h	N/A	ICH9DH
		2914h	02h	N/A	ICH9DO
		2916h	02h	N/A	ICH9R
		2918h	02h	N/A	ICH9
		2917h	02h	03h	ICH9M-E
		2919h	02h	03h	ICH9M
D31:F2	SATA	2920h	02h	N/A	Desktop Non-AHCI and Non-RAID Mode (Ports 0,1, 2 and 3)
		2921h	02h	N/A	Desktop Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		2922h	02h	N/A	Desktop AHCI Mode (Ports 0-5)
		2923h	02h	N/A	Desktop AHCI Mode (Ports 0,1,4 and 5)
		2822h[3]	02h	N/A	Desktop RAID 0/1/5/10 Mode
		2928h	02h	03h	Mobile Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		2929	02h	03h	Mobile AHCI Mode (Ports 0,1,4 and 5)
		282Ah[3]	02h	03h	Mobile RAID 0/1/5/10
D31:F5	SATA	2926h	02h	N/A	Desktop Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		292Dh	02h	03h	Mobile Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	2930h	02h	03h	
D31:F6	Thermal	2932h	02h	03h	
D30:F0	DMI to PCI Bridge	244Eh	92h	N/A	Desktop
		2448h	92h	93h	Mobile

ICH9 Device and Revision ID Table

Device Function	Description	Intel® ICH9 Dev ID[1]	ICH9 A2 Rev ID	ICH9 A3 Rev ID	Comments
D29:F0	USB UHCI #1	2934h	02h	03h	
D29:F1	USB UHCI #2	2935h	02h	03h	
D29:F2	USB UHCI #3	2936h	02h	03h	
D29:F3	USB UHCI #6	2939h	02h	03h	Note: Device and Revision ID is always the same as D26:F2.
D29:F7	USB EHCI #1	293Ah	02h	03h	
D26:F0	USB UHCI #4	2937h	02h	03h	
D26:F1	USB UHCI #5	2938h	02h	03h	
D26:F2	USB UHCI #6	2939h	02h	03h	
D26:F7	USB EHCI #2	293Ch	02h	03h	
D27:F0	Intel® High Definition Audio	293Eh	02h	03h	
D28:F0	PCI Express* Port 1	2940h	02h	03h	
D28:F1	PCI Express Port 2	2942h	02h	03h	
D28:F2	PCI Express Port 3	2944h	02h	03h	
D28:F3	PCI Express Port 4	2946h	02h	03h	
D28:F4	PCI Express Port 5	2948h	02h	03h	
D28:F5	PCI Express Port 6	294Ah	02h	03h	
D25:F0	LAN	29C4h[2]	02h	03h	

NOTES:

1. ICH9 contains two SATA controllers. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the component.
2. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 294Ch is used. Refer to the ICH9 NVM Map and Programming Guide for LAN Device IDs.
3. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.

Errata

1. Intel® I/O Controller Hub 9 (ICH9) Family UHCI Hang with USB Reset

Problem: When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang.

Note: The issue has only been replicated in a synthetic reset test environment.

Implication: System may hang.

Workaround: BIOS workaround available. See latest BIOS Spec Update for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

2. Intel® I/O Controller Hub 9 (ICH9) Family 1.5 Gb/s SATA Signal Voltage Level

Problem: The ICH9 1.5Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH9 SATA 1.5 Gb/s (Gen1i and Gen1m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specification (section 7.2.1 of Serial ATA Specification, rev 2.5).

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

3. Intel® I/O Controller Hub 9 (ICH9) Family High-speed USB 2.0 V_{HSOH}

Problem: ICH9 High-speed USB 2.0 V_{HSOH} may not meet the USB 2.0 specification.

— The maximum expected V_{HSOH} is 460mV.

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

4. Intel® I/O Controller Hub 9 (ICH9) Family THRM Polarity on SMBus

Problem: When THRM#_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

Implication: If the THRM#_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#_POL is set to low, value is correct.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

5. Intel® I/O Controller Hub 9 (ICH9) Family SPI_CS1# State

Problem: After resuming from S3-S5, the ICH9 SPI_CS1# signal may initially drive a low voltage on the pin.

Implication: If only one SPI device is populated on the system, there is no impact.
If two SPI devices are populated, system may hang when resuming from S3-S5.

- When the ICH9 performs its initial read to the SPI device on SPI_CS0#, SPI_CS1# could also be asserted. BIOS may not receive correct boot data.

Workaround: Available.

1) For ME-enabled systems:
- Desktop: use ME firmware version 3.0.2.xxxx or later, or populate one SPI device.

2) For non-ME systems: populate one SPI device.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

6. Intel® I/O Controller Hub 9 (ICH9) Family Level-Triggered Legacy IRQs

Problem: When the ICH9 legacy interrupts [15:0] are configured as level triggered interrupts, the ICH9 may invert the default interrupt level from high-active to low-active.

Implication: Devices or Virtualization SW stacks which use legacy interrupts [15:0] as low-active level-triggered on the system may see performance degradation due to excessive IRQ requests.

Note: Intel has not identified any impacted devices or production virtualization system software stacks (VMMs/OS).

Workaround: Available.

- For impacted devices: BIOS or Device Driver ensures the ICH9 legacy interrupts [15:0] are configured as edge triggered.
- For impacted Virtualization SW stacks:
  - — Option 1: Virtualization SW to configure ICH9 legacy interrupt [15:0] as edge triggered
  - — Option 2: Virtualization SW should mask the low active level triggered interrupt allocated to the virtual interrupt by executing the following steps:
    . Check if platform is ICH9-based
    . If ICH9, check the interrupt polarity specified in the corresponding RTE entry of IOAPIC. If the polarity is active low, then
      a) Mask this line in the physical IOAPIC, and
      b) Virtualize the IOAPIC and the corresponding RTE entry mask field to the guest OS.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*

7. Intel® I/O Controller Hub 9 (ICH9) Family High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH9 may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

8. PET Alerts on SMBus

Problem: When using the ICH9 SMBus for Platform Event Trap (PET) alerts on a system with the Intel® Management Engine (ME) enabled, the SMBus packet headers may be corrupted if all of the following conditions are met:

- SMBus slave is the target of an external PET generating master on SMBus/SMLink
- The ME is in the middle of M0-M1 transitions
- SMBus slave receives back-to-back PET alerts of which some PET alerts are incomplete (i.e. the packet is truncated to less than 6 bytes)

Note: This issue has only been observed under a synthetic test environment.

Implication: ME firmware may stop functioning, which could cause a system hang.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

9. SMBus Host Controller May Hang

Problem: During heavy SMBus traffic utilization, the ICH9 SMBus host controller may attempt to start a transaction while the bus is busy.

Note: This issue has only been observed under a synthetic test environment.

Implication: May cause the SMBus host controller to hang.

- After boot:
  - SMBus host controller transaction may not complete.
  - External master transaction in progress targeting ICH9 SMBus slave may get NACK or timeout.
  - There is no impact to any other transaction that was in progress by an external master.
- This issue has not been observed during boot as SMBus utilization tends to be light.

Workaround: BIOS workaroud available.
Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

10. SATA Gen1 Initialization/LPM Erratum

Problem: During SATA Initialization routines or while resuming from a Link Power Managed (LPM) state, the ICH9 SATA link to Gen1 (1.5 Gb/s) devices may fail to be established.

Implication: One or more of the following symptoms may occur:

- During Boot or Resume from S4/S5: SATA Gen1 devices may not be detected, resulting in “Operating System Not Found” error.
- During Resume from S3: System may hang when attempting to initialize SATA Gen1 devices.
- During S0: If LPM is enabled and ALL SATA Gen1 devices within the system support LPM, slow SATA Gen1 performance may occur.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

11. ICH9M LAN_PHY_PWR_CTRL Functionality

Problem: LAN_PHY_PWR_CTRL output is driven low by the ICH9M A3 during a host reset with or without power cycle for up to 3 RTC clock cycles due to the pin momentarily being configured as an output GPIO.

- LAN_PHY_PWR_CTRL functionality requires a soft strap setting in the SPI descriptor and use of the integrated LAN controller in ICH9M with the Intel® 82567 PHY.

Implication: Functional failures such as system hangs or link loss with dropped packets have been observed when LAN_PHY_PWR_CTRL is tied to the LAN_DISABLE_N pin on the Intel® 82567.

Note: There are no functional implications if the pin is configured as GPIO12.

Workaround: Available

ME-Enabled Platforms: An ME FW workaround will be provided with Mobile ME FW Production Candidate release.

- Both the ME Disable bits in the SPI flash descriptor (ICHSTRP0 bit 0 & MCHSTRP0 bit 0) must be set to 0 to enable the ME FW workaround.
- MCHSTRP0 bit 7 in the SPI flash descriptor can be set to disable all other ME FW based features, while keeping the ME FW workaround enabled.

Non ME-Enabled Platforms: Remove LAN_PHY_PWR_CTRL Support on the Platform

- Isolate the LAN_PHY_PWR_CTRL signal from the LAN_DISABLE_N pin.
- LAN_DISABLE_N has a weak integrated pull-up resistor and the Intel 82567 PHY will always remain enabled with this implementation.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

12. Intel® I/O Controller Hub 9 (ICH9) Family SATA Low Power Device Detection

Problem: Intel® I/O Controller Hub 9 (ICH9)Family SATA Low Power Device Detection (SLPD) may not recognize, or may falsely detect, a SATA hot-plug event during a Partial or Slumber Link Power Management (LPM) state.

Implication: This issue affects ICH9, ICH9R, ICH9DH, ICH9DO, ICH9M, ICH9M-E and ICH9M-SFF

On systems which enable LPM, when a SATA device attached to the ICH9 is configured as External or Hot Plug capable, one of the following symptoms may occur:

- Symptom #1: A Hot-Plug or External SATA device removal which is not detected results in the OS and Intel® Matrix Storage Manager console falsely reporting the device present, or incorrectly identifying an eSATA device.
- Symptom #2: A false hot-plug removal detection may occur resulting in OS boot hang or ODD media playback hang.

Workaround: A driver workaround is available.

Status: No Fix. For steppings affected, see the *Summary Table of Change*

13. Intel® I/O Controller Hub 9 (ICH9) Family PCI Express Function Disable

Problem: Intel® I/O Controller Hub 9 (ICH9)Family PCI Express [1:16] Disable bit in Function Disable Register may not put the PCI Express Port into a link down state if a PCI Express Device is attached.

Implication: ICH9M, ICH9M-E:

PCI Express Port [1:6] with a PCI Express device attached may remain in L0 State and DMI may not be able to go into L1 State.

ICH9, ICH9R, ICH9DH, ICH9DO:

PCI Express Port [1:6] with a PCI Express device attached may remain in L0 State.

Workaround: A BIOS code change has been identified.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

14. Intel® I/O Controller Hub 9 (ICH9) Family SATA SYNC Escape

Problem: When a SYNC Escape by a SATA device occurs on a D2H FIS, the ICH9 does not set the PxIS.IFS bit to ‘1.’ This deviates from section 6.1.9 of the Rev 1.3 Serial ATA Advanced Host Controller Interface (AHCI)

Implication: There is no known observable impact. Instead of detecting the IFS bit, software will detect a timeout error caused by the SYNC escape and then respond

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

15. Intel® I/O Controller Hub 9 (ICH9) Family HPET Write Timing

Problem: A read transaction that immediately follows a write transaction to the HPET TIMn_COMP Timer 0 (108h), HPET MAIN_CNT (0F0h), or TIMn_CONF.bit 6 (100h) may return an incorrect value

Implication: There are no known functional implications with known software and operating systems.

For the HPET TIMn_COMP Timer 0 Comparator Value Register and HPET MAIN_CNT—Main Counter Value Register the issue could result in the software receiving stale data. This may result in undetermined system behavior.

Note: Timers [1:7] are not affected by this issue

For TIMERn_VAL_SET_CNF bit 6 in the TIMn_CONF—Timer n Configuration there is no known usage model for reading this bit and there are no known functional implications.

Workaround: A workaround is available.

Status: No Fix. For steppings affected, see the *Summary Table of Changes*.

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Specification Changes

1. Clock Slew Rate Change

The following change applies to Table 8-9 of the Datasheet.

Sym	Parameter	Min	Max	Unit	Notes	Figure
SATA Clock (SATA_CLKP, SATA_CLKN) / DMI Clock (DMI_CLKP, DMI_CLKN)						
tsatasl	Slew rate	1	8	V/ns	7	

2. Serial ATA Clock Request Support.

Serial ATA Clock Request is not supported on ICH9. All references to Serial ATA Clock Request are removed from the Datasheet.

In accordance to this change the bit definition for SATA Clock Request Enable bit in Section 14.1.32 SCLK - SATA Clock Gating Control Register is being changed as follows in the Datasheet.

Bit	Description
30	Reserved - R/W BIOS must program this bit to 0

Specification Clarifications

1. t290 and t294 Clarification

a. Note 23 for t290 and t294 in Table 8-22 of the Datasheet is changed as indicated below:

23. t290 and t294 are not applied to V5REF. V5REF timings are bounded by power sequencing. t290 and t294 apply during S0 to S3/S4/S5 and S0 to G3 transitions.

b. The title of Figure 8-27 and Figure 8-28 of the datasheet is changed to “S0 to S3/S4/S5 and G3 Timings”.

Documentation Changes

1. SATA Interlock Switch State (ISS) Bit Clarification

The following change applies to Section 14.4.3.7 of the Datasheet.

13	**Interlock Switch State (ISS)**— RO. For systems that support interlock switches (via CAP.SIS [ABAR+00h:bit28]), if an interlock switch exists on this port (via ISP in this register), this bit indicates the current state of the interlock switch. A 0 indicates the switch is closed, and a 1 indicates the switch is opened. For systems that do not support interlock switches (CAP.SIS=0), this bit reports 0.

2. GPIO34 Power Well Correction

Note: GPIO34 is in the VccHDA power rail. Table 2-22 of the Datasheet is updated as follows:

Name	Type	Tolerance	Power Well	Default	Description
GPIO34	I/O	1.5 V / 3.3 V	VccHDA	GPO	Mobile: Multiplexed with HDA_DOCK_RST#. Desktop: UnMultiplexed See Note 13.

13. The tolerance of this pin is determined by the voltage of VccHDA either 3.3 V or 1.5 V.

3. LAN Device Initialization Register

LAN Device Initialization Register 1 is abbreviated as LDR1 (not LDR2). This change applies to Section 12.2.6 of the Datasheet.

4. HPET Timer

The following change applies to Section 5.17.1 of the Datasheet

The main counter is clocked by the 14.31818 MHz clock, synchronized into the 125 MHz domain.

5. Add GPIO Signal Reset Notes

Add the following notes to Section 2.22 of the Datasheet above Table 2-22.

GPIO Reset Notes:

1. GPIO Configurations registers within the Core Well are reset whenever PWROK is de-asserted.
2. GPIO Configuration registers within the Suspend Well are reset when RSMRST# is asserted, CF9 reset (06h or 0Eh) event occurs, or SYS_RST# is asserted.

3. GPIO24 is an exception to the other GPIO Signals in the Suspend Well and is not reset by CF9 reset (06h or 0Eh).

6. Corrected EOIFD Bit Definition

Update the EOIFD bit definition in Section 20.1.45 of the Datasheet as follows:

Bit	Description
31:02	Reserved.
1	**EOI Forwarding Disable (EOIFD)** — R/W. When set, EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe link. 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and fowarded across the PCIe link. 1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe Link.

7. Update GPIO Signals and Note #4 in Section 3.2 Output and I/O Signals Planes and States

Make the following update to Section 3.2 Table 3-3 (UnMultiplexed GPIO Signals) and Note #4 for Table 3-2 and Table 3-3 of the Datasheet

Table 3-3(Update for both Table 3-2 and Table 3-3)with an exception to GPIO signals; refer to section 2.22 General Purpose I/O Signals for more details on GPIO state after reset.b

Signal Name	Power Plane	During Reset	Immediately after Reset	C3 / C4 / C5 / C6	S1	S3	S4 / S5
UnMultiplexed GPIO Signals							
GPIO8	Suspend	Input	Input	Defined	Defined	Defined	Defined
GPIO12	Suspend	Low	Low	Defined	Defined	Defined	Defined
GPIO13	Suspend	Input	Input	Defined	Defined	Defined	Defined
GPIO18	Core	High	See Note 2	Defined	Defined	Off	Off
GPIO20[11]	Core	Low	High	Defined	Defined	Off	Off
GPIO[28:27]	Suspend	Low	Low	Defined	Defined	Defined	Defined
GPIO49[11]	Core	High	High	Defined	Defined	Off	Off
GPIO56	Suspend	Input	Input	Defined	Defined	Defined	Defined

8. Correct Table 1-5 ICH9M-E Raid Support

Make the following correction to Section 1.3 Table 1-5 Intel of the Datasheet:

Component Name	Short Name	Intel® Matrix Storage Technology		Intel® Active Management Technology
		AHCI	RAID 0/1 Support	
ICH9 Mobile Base	ICH9M	Yes	No	No
ICH9 Mobile Enhanced	ICH9M-E	Yes	Yes	Yes

9. Make Correction to Table 5-40

Make the following correction to Table 5-4 7-3 in Section 5.13.14 Reset Behavior in the Datasheet.

Table 5-40 Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle	Host Reset with Power Cycle	Global Reset with Power Cycle
Power Failure: PWROK signal or VRMPWRGD signal goes inactive or RSMRST# asserts	No	Yes	Yes (Note 2)

10. Update bit definition for Second_TO_STS

Update the following bit definition for Second_TO_STS in Section 13.9.5 TCO2_STS - TCO2 Status Register in the Datasheet.

Bit	Description
1	**SECOND_TO_STS** — R/WC. 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = ICH10 sets this bit to 1 to indicate that the TIMEOUT bit is set and a second timeout occurred. If this bit is set and the NO_REBOOT config bit is 0, then the ICH10 will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.

11. Correct Typo for ICH9M-SFF package ball AC22

Update the following ball designation for ICH9M-SFF package ball AC22 in Figure 6-6 and Table 6-3 and remove the wording “Preliminary” from the title of Figures 6-5 and 6-6 in the Datasheet.

Update the following ball designation for ICH9M-SFF package ball AC22 in Figure 6-6 and Table 6-3

Figure 6-6 Intel-SFF Ballout(Top view-Right Side)

TP12	THRMTRIP#	VSS	STPCLK#	**AC**
VSS	IGNNE#	INTR	FERR#	**AD**
CPUPWRGD	DPRSTP#	DPSLP#	VSS	**AE**
22	**23**	**24**	**25**	

Table 6-3 ICH9M-SFF Ballout by Signal Name - (Mobile Only)

Names	**Ball**
TP12	AC22

Remove Preliminary from the title of Figure 6-5 and Figure 6-6:

Figure 6-5. Intel® ICH9M SFF Ballout(Top View-Left Side)

Figure 6-6. Intel® ICH9M SFF Ballout(Top View-Right Side)

12. Correct Typo for Table 2-22 General Purpose I/O Signals for GPIO[5:2]

Indicate the proper Note for GPIO[5:2] in Table 2-2 General Purpose I/O Signals for GPIO[5:2] in the Datasheet.

Name	Type	Tolerance	Power Well	Default	Description
GPIO[5:2]	I/OD	5 V	Core	GPI	Multiplexed with PIRQ[H:E]# (Note 7).

NOTES:

1. All GPIOs can be configured as either input or output.
2. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.
3. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Also, external devices should not be driving powered down GPIOs high. Some ICH9 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH9 driving a pin to a logic 1 to another device that is powered down.
4. The functionality that is multiplexed with the GPIO may not be utilized in desktop configuration.
5. This GPIO is not an open-drain when configured as an output.
6. SPI_CS1# and CLGPIO6 (Digital Office Only) are located in the VccCL3_3 well.

7. When this signal is configured as GPO the output stage is an open drain.

13. Correct PCI Express* DSTS register definition for bit 1 (NFED)

Update the bit definition for bit 1(NFED) in Section 20.1.27 DTST- Device Status Register Description in the Datasheet to match PCI Express* Base Specification Revision 1.1.

Section 20.1.27 DSTS—Device Status Register (PCI Express—D28:F0/F1/F2/F3/F4/F5)

Address Offset:	4Ah–4Bh	Attribute:	R/WC, RO
Default Value:	0010h	Size:	16 bits

Bit	Description
1	**Non-Fatal Error Detected (NFED)** — R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred.

14. Correct SMBCLK_CTL bit default value

Correct SMBCLK_CTL bit 2 default value defined in section 19.2.14 SMBus_PIN_CTL—SMBus Pin Control Register (SMBus—D31:F3) in the Datasheet

Bit	Description
2	**SMBCLK_CTL** — R/W. 1 = The SMBCLK pin is **not** overdriven low. The other SMBus logic controls the state of the pin. (Default) 0 = ICH9 drives the SMBCLK pin low, independent of what the other SMB logic would otherwise indicate for the SMBCLK pin.

15. Correct Table 2-24 Strap selection for Boot BIOS Destination

Correct Boot BIOS Destination strap selection definition in Table 2-24 Functional Strap Definitions (Sheet 2 of 3) in the Datasheet

<table>
<tr><th>Signal</th><th>Usage</th><th>When Sampled</th><th>Comment</th></tr>
<tr><td>GNT0#</td><td>Boot BIOS Destination Selection 1</td><td>Rising Edge of PWROK</td><td>This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
<table>
<tr><th>Bit11 (GNT0#)</th><th>Bit 10 (SPI_CS1#)</th><th>Boot BIOS Destination</th></tr>
<tr><td>0</td><td>X</td><td>SPI</td></tr>
<tr><td>1</td><td>0</td><td>PCI</td></tr>
<tr><td>1</td><td>1</td><td>LPC</td></tr>
</table>
NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.</td></tr>
<tr><td>SPI_CS1# / GPIO58 Desktop Only) / CLGPIO6 (Digital Office Only)</td><td>Boot BIOS Destination Selection 0</td><td>Rising Edge of CLPWROK</td><td>This field determines the destination of accesses to the BIOS memory range. Signals have weak internal pull-ups. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.
<table>
<tr><th>Bit11 (GNT0#)</th><th>Bit 10 (SPI_CS1#)</th><th>Boot BIOS Destination</th></tr>
<tr><td>0</td><td>X</td><td>SPI</td></tr>
<tr><td>1</td><td>0</td><td>PCI</td></tr>
<tr><td>1</td><td>1</td><td>LPC</td></tr>
</table>
NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.</td></tr>
</table>

16. Correct section 5.13.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure.

Correct selection 5.13.7.5 Sx-G3-Sx, Handling Power Failures in the Datasheet

Section 5.13.7.5 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). The following wake events can wake the system following a power loss by either RSMRST# going low and enabling by default, the enable bits reside in the RTC well or the wake event is always enabled.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH10 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V_{CC}-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.
2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.
3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.
4. PCI Express Wake# Signal: The PCIEXPWAK_DIS bit is cleared by RSMRST# going low enabling PCI Express Ports to wake the platform after a power loss. The PCIEXPWAK_STS bit is also cleared when RSMRST# goes low.
5. PME_B0: PME_B0_EN is in the RTC Well and is preserved after a power loss. The PME_B0_STS bit is also cleared when RSMRST# goes low.
6. PME: PME_EN: is in the RTC Well and is preserved after a power loss. The PME_STS bit is also cleared when RSMRST# goes low.
7. Host SMBUS: SMBUSALERT# or Slave Wake message is always enabled as Wake Event
8. ME Non-Maskable Wake: Always enabled as Wake Event.

The ICH9 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

17. Correct section 10.1.45 Bit 0 definition

Correct selection 10.1.45 CIR5—Chipset Initialization Register 5 in the Datasheet

10.1.45 CIR5—Chipset Initialization Register 5

Offset Address:	1D40h–1D47h	Attribute:	R/W
Default Value:	0000000000000000h	Size:	64-bit

Bit	Description
63:0	Reserved

18. Correct section 13.1.23 Bits 15:2 definition

Correct section 13.1.23 GEN1_DEC-LPC I/F Generic Decode Range 1 Register in the Datasheet

13.1.23 GEN1_DEC-LPC I/F Generic Decode Range 1 Register (LPC I/F-D31:F0)

Offset Address:	84h–87h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bit
		Power Well:	Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)** — R/W. **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN)** — R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F.

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