W83627EHF/EF

W83627EHG/EG

NUVOTON LPC I/O

Note: This document is both for UBC and UBH version except the specified descriptions

Date: April 7th, 2009 Revision: 1.94

TABLE OF CONTENTS-

1. GENERAL DESCRIPTION

W83627EHF/EHG/EF/EG is an evolving product from Nuvoton's most popular I/O family. They feature a whole new interface, namely LPC (Low Pin Count) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83627EHF/EHG/EF/EG include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83627EHF/EHG/EF/EG greatly reduces the number of components required for interfacing with floppy disk drives. W83627EHF/EHG/EF/EG supports one 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

W83627EHF/EHG/EF/EG provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of 230k, 460k, or 921k bps which support higher speed modems. In addition, W83627EHF/EHG/EF/EG provides IR functions: IrDA 1.0 (SIR for 1.152K bps).

W83627EHF/EHG/EF/EG supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port(EPP) and Extended Capabilities Port (ECP).And W83627EHF/EHG/EF/EG contains a Game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, they are very important for a entertainment or consumer computer.

W83627EHF/EHG/EF/EG provides flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function.

W83627EHF/EHG supports hardware status monitoring for personal computers. It can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan

speeds, and temperatures, which are very important for a high-end computer system to work stably and properly. Moreover, W83627EHF/EHG supports the Smart Fan control system, including the "Thermal Cruise™" and "Speed Cruise™" functions. Smart Fan can make system more stable and user friendly.

W83627EHF/EHG/EF/EG is made to fully comply with Microsoft© PC98 , PC99 and PC2001 System Design Guide, and meet the requirements of ACPI.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98/2000/XP™, which makes system resource allocation more efficient than ever.

The special characteristic of Super I/O product line is to avoid power rails short. This is especially true to a multi-power system where power partition is much more complex than a single-power one. Special care might be applied during layout stage or the IC will fail even though its intended function is workable.

2. FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (Serial IRQ)
- Integrated Hardware Monitor functions
- Compliant with Microsoft© PC98/PC99/PC2001 System Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input
- It is 3.3V level but 5V tolerance support

  --- Besides LPC function pins(Pin21 ~ Pin30) and H/W monitor analog pins(Pin95 ~ Pin110)

  --- Input level can up to 5V and maximum input level can be up to 5V+10%

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support one 3.5-inch or 5.25-inch floppy disk drive

- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support 3-mode FDD, and its Windows driver

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  - --- 5, 6, 7 or 8-bit characters
  - --- Even, odd or no parity bit generation/detection
  - --- 1, 1.5 or 2 stop bits generation
- Internal diagnostic capabilities:
  - --- Loop-back controls for communications link fault isolation
  - --- Break, parity, overrun, framing error simulation
- Programmable baud rate generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to 921k bps for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) - Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) - Compatible with IEEE 1284 specification

- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axis (X, Y) and two button (A, B) controllers

MIDI Port

- The baud rate is 31.25 K baud
- 16-byte input FIFO
- 16-byte output FIFO

Keyboard Controller

- 8042 based with optional F/W from AMIKKEY™-2, Phoenix MultiKey/42™ or customer code with 2K bytes of programmable ROM, and 256 bytes of RAM
- Asynchronous Access to Two Data Registers and One status Register
- Software compatibility with the 8042
- Support PS/2 mouse
- Support port 92
- Support both interrupt and polling modes
- Fast Gate A20 and Hardware Keyboard Reset
- 8 Bit Timer/ Counter
- Support binary and BCD arithmetic
- 6 MHz, 8 MHz, 12 MHz, or 16 MHz operating frequency

General Purpose I/O Ports

- 48 programmable general purpose I/O ports

- GPIO port 1 and 4 can not only serve as simple I/O ports but also watch dog timer output, Power LED output, Suspend LED output
- Functional in power down mode (GP24 ~ GP27, GPIO-3, GPIO-4, GPIO-5)

OnNow Functions

- Keyboard Wake-Up by programmable keys
- Mouse Wake-Up by programmable buttons
- On Now Wake-Up from all of the ACPI sleeping states (S1-S5)

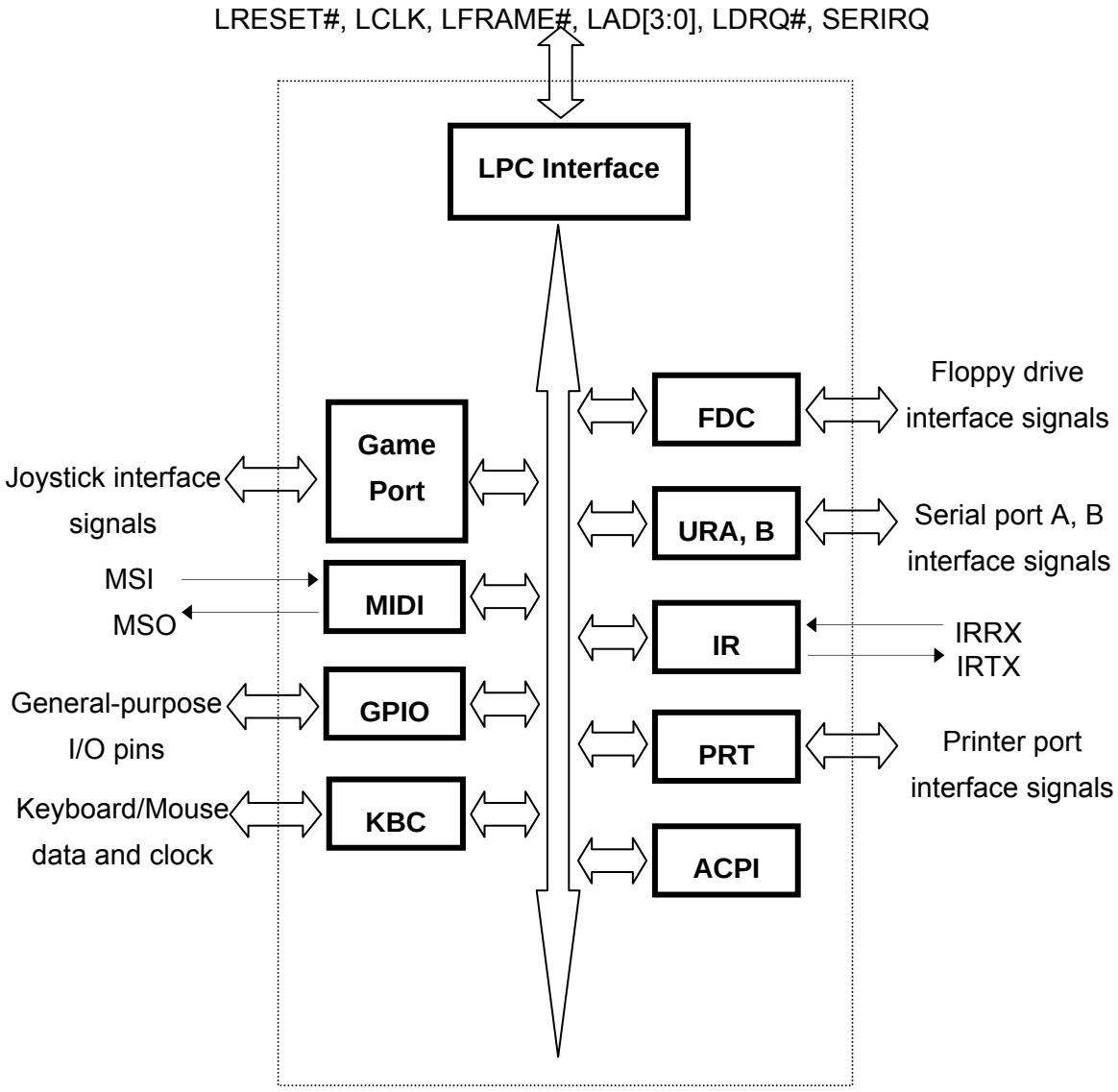
Hardware Monitor Functions (For W83627EHF/EHG only)

- Smart Fan control system, support SMART FAN™ I - "Thermal Cruise™" and "Speed Cruise™" Mode , SMART FAN™ III function
- 3 thermal inputs from optionally remote thermistors or Pentium™ II/III/4 thermal diode output
- 10 voltage inputs (CPUVCORE, VIN[0..4] and intrinsic 3VCC, AVCC , 3VSB, VBAT)
- 5 fan speed monitoring inputs
- 4 fan speed control
- Dual mode for fan control (PWM & DC)
- Build in case open detection circuit
- Programmable hysteresis and setting points for all monitored items
- Over temperature indicate output
- Issue SMI#, OVT# to activate system protection
- Nuvoton Hardware Doctor™ support
- 6 VID inputs / outputs
- Provide I^2C interface to read/write registers

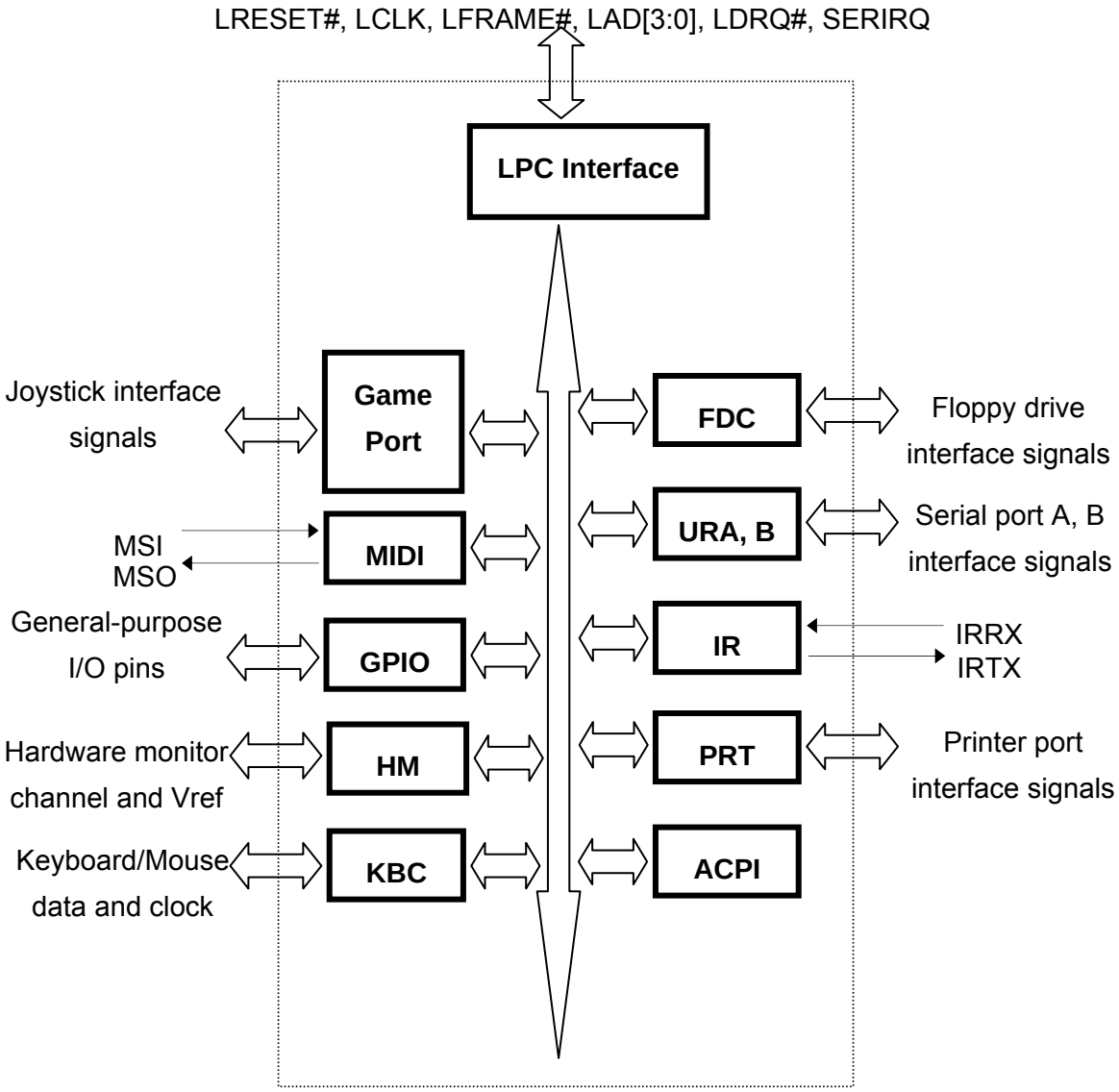
Package

- 128-pin PQFP

3. BLOCK DIAGRAM

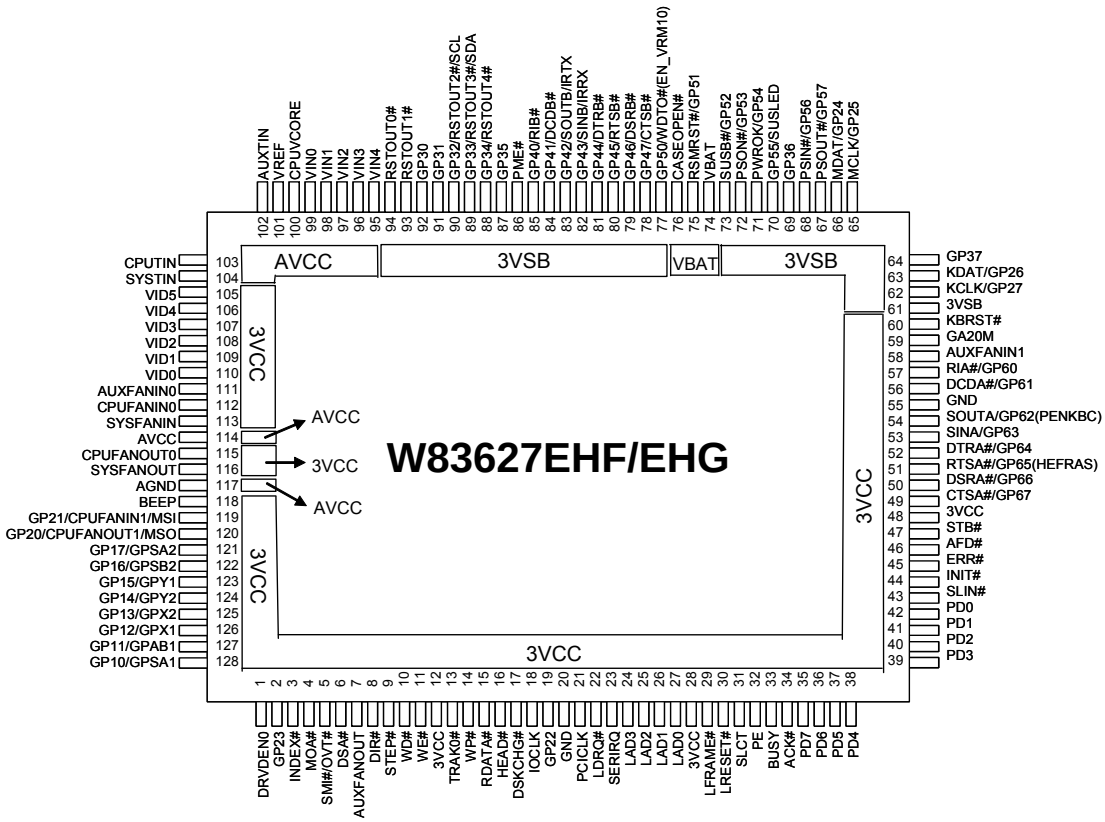


W83627EF/EG

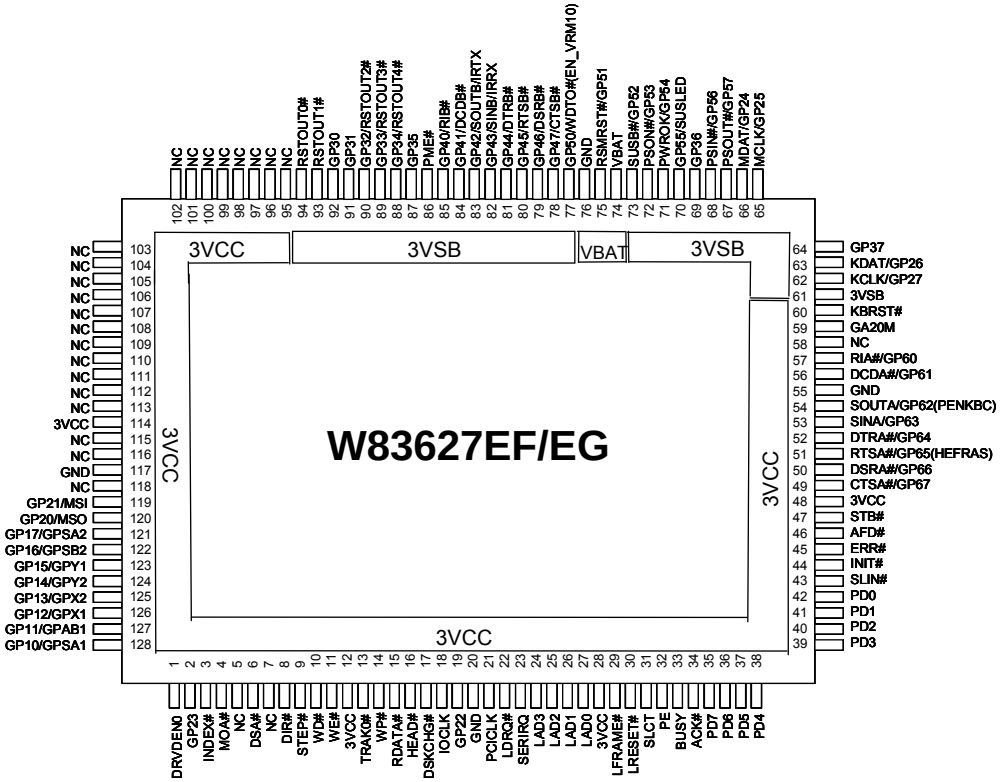


W83627EHF/EHG

4. PIN CONFIGURATION



Pin Layout for W83627EHF/EHG



Pin Layout for W83627EF/EG

5. PIN DESCRIPTION

Note: Please refer to Section 18.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin

AIN - Analog input pin

IN_{cs} - CMOS level Schmitt-triggered input pin

IN_{t} - TTL level input pin

IN_{td} - TTL level input pin with internal pull down resistor

IN_{ts} - TTL level Schmitt-triggered input pin

IN_{tsp3} - 3.3V TTL level Schmitt-triggered input pin

IN_{tu} - TTL level input pin with internal pull up resistor

IN_{tsu} - TTL level Schmitt-triggered input pin with internal pull up resistor

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{12t} -3.3V TTL level bi-directional pin with 12 mA source-sink capability

I/OD_{12ts} - 3.3V TTL level bi-directional Schmitt-triggered pin. Open-drain output with 12 mA sink capability

I/OD_{16cs} - CMOS level Schmitt-triggered bi-directional pin. Open-drain output with 16 mA sink capability

I/OD_{24t} - TTL level bi-directional pin. Open-drain output with 24 mA sink capability

OUT_{8} - TTL level output pin with 8 mA source-sink capability

OUT_{12} -3.3V TTL level output pin with 12 mA source-sink capability

OUT_{24} - TTL level output pin with 24 mA source-sink capability

OD_{8} - Open-drain output pin with 8 mA sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

5.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
IOCLK	18	IN_{t}	System clock input, which is selective by the register according to the input frequency either 24MHz or 48MHz. Default is 48MHz.
PME#	86	OUT_{12}	Generated PME event.

SYMBOL	PIN	I/O	FUNCTION
PCICLK	21	IN_t	PCI clock 33 MHz input.
LDRQ#	22	OUT_{12}	Encoded DMA Request signal.
SERIRQ	23	I/O_{12t}	Serial IRQ Input/Output.
LAD[3:0]	24-27	I/O_{12t}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	29	IN_t	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	30	IN_t	Reset signal. It can connect to PCIRST# signal on the host.

5.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	3	IN_{csu}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
MOA#	4	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.

SYMBOL	PIN	I/O	FUNCTION
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	13	IN_{tsu}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
WP#	14	IN_{tsu}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
RDATA#	15	IN_{tsu}	The read data input signal from the FDD. This input pin can be pulled up internally by a 1 KΩ(±50%). The resistor also can be disabled/enabled by bit 7 of LD0-CRF0(FIPURDWN). Default is disabled.
HEAD#	16	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	17	IN_{tsu}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin can be pulled up internally by a 1 KΩ(±50%) . The resistor also can be disabled / enabled by bit 7 of LD0-CRF0 (FIPURDWN). Default is disabled.

5.3 Multi-Mode Parallel Port

SYMBOL	PIN	I/O	FUNCTION
SLCT	31	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
PE	32	IN_{ts}	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
BUSY	33	IN_{ts}	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
ACK#	34	IN_{ts}	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
ERR#	45	IN_{ts}	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
SLIN#	43	OD_{12} /OUT_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

SYMBOL	PIN	I/O	FUNCTION
INIT#	44	OD_{12} /OUT_{12}	PRINTER MODE: INIT# Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
AFD#	46	OD_{12} /OUT_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
STB#	47	OD_{12} /OUT_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD0	42	I/O_{12ts}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD1	41	I/O_{12ts}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD2	40	I/O_{12ts}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD3	39	I/O_{12ts}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD4	38	I/O_{12ts}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

SYMBOL	PIN	I/O	FUNCTION
PD5	37	I/O_{12ts}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD6	36	I/O_{12ts}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
PD7	35	I/O_{12ts}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

5.4 Serial Port & Infrared Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA#	49	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP67		I/OD_{12t}	General purpose I/O port 6 bit 7.
CTSB#	78	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
GP47***		I/OD_{12t}	General purpose I/O port 4 bit 7.
DSRA#	50	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP66		I/OD_{12t}	General purpose I/O port 6 bit 6.

SYMBOL	PIN	I/O	FUNCTION
DSRB#	79	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
GP46*		I/OD_{12t}	General purpose I/O port 4 bit 6.
RTSA#	51	OUT_8	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
HEFRAS		IN_{td}	During power-on reset, this pin is pulled down internally(20K±30%) and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
GP65		I/O_8	General purpose I/O port 6 bit 5.
RTSB#	80	OUT_{12}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
GP45***		I/OD_{12t}	General purpose I/O port 4 bit 5.
DTRA#	52	OUT_8	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate.
GP64		I/O_8	General purpose I/O port 6 bit 4.
DTRB#	81	OUT_{12}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
GP44*		I/OD_{12t}	General purpose I/O port 4 bit 4.
SINA	53	IN_t	Serial Input. It is used to receive serial data through the communication link.
GP63		I/OD_{12}	General purpose I/O port 6 bit 3.
SINB	82	IN_t	Serial Input. It is used to receive serial data through the communication link.

SYMBOL	PIN	I/O	FUNCTION
IRRX			IR Receiver input.
GP43***		I/OD_{12}	General purpose I/O port 4 bit 3.
SOUTA	54	OUT_8	UART A Serial Output. It is used to transmit serial data out to the communication link.
PENKBC		IN_{td}	During power on reset, this pin is pulled down internally(20K ± 30%)and is defined as PENKBC, which provides the power on value for CR24 bit 2. A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up.
GP62		I/O_8	General purpose I/O port 6 bit 2.
SOUTB	83	OUT_{12}	UART B Serial Output. It is used to transmit serial data out to the communication link.
IRTX			IR Transmitter output.
GP42*		I/OD_{12}	General purpose I/O port 4 bit 2.
DCDA#	56	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP61		I/OD_{12}	General purpose I/O port 6 bit 1.
DCDB#	84	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
GP41***		I/OD_{12}	General purpose I/O port 4 bit 1.
RIA#	57	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP60	57	I/OD_{12}	General purpose I/O port 6 bit 0.
RIB#	85	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
GP40*		I/OD_{12}	General purpose I/O port 4 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.5 KBC Interface

SYMBOL	PIN	I/O	FUNCTION
GA20M	59	OUT_{12}	Gate A20 output. This pin is high after system reset. (KBC P21)
KBRST#	60	OUT_{12}	Keyboard reset. This pin is high after system reset. (KBC P20)
KCLK	62	I/OD_{16ts}	Keyboard Clock.
GP27		I/OD_{16t}	General purpose I/O port 2 bit 7.
KDAT	63	I/OD_{16ts}	Keyboard Data.
GP26		I/OD_{16t}	General purpose I/O port 2 bit 6.
MCLK	65	I/OD_{16ts}	PS2 Mouse Clock.
GP25		I/OD_{16t}	General purpose I/O port 2 bit 5.
MDAT	66	I/OD_{16ts}	PS2 Mouse Data.
GP24		I/OD_{16t}	General purpose I/O port 2 bit 4.

5.6 Hardware Monitor Interface

SYMBOL	PIN	I/O	FUNCTION
BEEP	118	OD_8	Beep function for hardware monitor. This pin is low after system reset. **(for H version only, C version is tri-state)**
CASEOPEN#	76	IN_t	CASE OPEN detected. An active low level input from an external device when case is opened. This signal can be latched if pin VBAT is connect to battery, even W83627EHF/EHG is power off. This pin is VSS for W83627EF/EG.**Pull down is recommended if useless**. **(For H version only, C version is falling edge trigger only)**
VIN4	95	AIN	0V to 2.048V FSR Analog Inputs. (FSR: Full Scale Register)

SYMBOL	PIN	I/O	FUNCTION
VIN3	96	AIN	0V to 2.048V FSR Analog Inputs.
VIN2	97	AIN	0V to 2.048V FSR Analog Inputs.
VIN1	98	AIN	0V to 2.048V FSR Analog Inputs.
VIN0	99	AIN	0V to 2.048V FSR Analog Inputs.
CPUVCORE	100	AIN	0V to 2.048V FSR Analog Inputs.
VREF	101	AOUT	Reference Voltage (2.048V) for temperature maturation.
AUXTIN	102	AIN	Temperature sensor 3 inputs. It is used for temperature maturation.
CPUTIN	103	AIN	Temperature sensor 2 inputs. It is used for CPU temperature maturation.
SYSTIN	104	AIN	Temperature sensor 1 input. It is used for system temperature maturation.
OVT#	5	OD_{12}	Over temperature Shutdown Output. It indicated the temperature is over temperature limit.
SMI#		OD_{12}	System Management Interrupt channel output. (Default after PCIRST)
VID5 VID4 VID3 VID2 VID1 VID0	105 106 107 108 109 110	I/O_{12}	VID input detect, also with output control.
AUXFANIN1	58	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
AUXFANIN0	111	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.

SYMBOL	PIN	I/O	FUNCTION
CPUFANIN0	112		
SYSFANIN	113		
CPUFANIN1	119	I/O_{12ts}	0V to +3.3V amplitude fan tachometer input. (Default)
MSI		IN_{ts}	MIDI serial data input.
GP21		I/OD_{12ts}	General purpose I/O port 2 bit 1.
AUXFANOUT	7	AOUT/ OD_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode. (For H version, while SYSFANOUT or CPUFANOUT0 be selected to PWM Mode, either of them can be open-drain or push-pull output. The controlled bits are CR24h bit[4:3]. Open-drain output is default.)
CPUFANOUT0	115		
SYSFANOUT	116		
CPUFANOUT1	120	AOUT/ OUT_{12t}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
MSO		OUT_{12t}	MIDI serial data output.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

5.7 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
GPSA1	128	IN_{ts}	Active-low, Joystick I switch input 1. (Default)
GP10*		I/OD_{12ts}	General purpose I/O port 1 bit 0.
GPSB1	127	IN_{ts}	Active-low, Joystick II switch input 1. (Default)
GP11**		I/OD_{12ts}	General purpose I/O port 1 bit 1.

SYMBOL	PIN	I/O	FUNCTION
GPX1	126	I/OD_{12ts}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP12*			General purpose I/O port 1 bit 2.
GPX2	125	I/OD_{12ts}	Joystick II timer pin. This pin connects to X positioning variable resistors for the Joystick. (Default)
GP13**			General purpose I/O port 1 bit 3.
GPY2	124	I/OD_{12ts}	Joystick II timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP14*			General purpose I/O port 1 bit 4.
GPY1	123	I/OD_{12ts}	Joystick I timer pin. This pin connects to Y positioning variable resistors for the Joystick. (Default)
GP15**			General purpose I/O port 1 bit 5.
GPSB2	122	IN_{ts}	Active-low, Joystick II switch input 2. (Default)
GP16*		I/OD_{12ts}	General purpose I/O port 1 bit 6.
GPSA2	121	IN_{ts}	Active-low, Joystick I switch input 2. (Default)
GP17**		I/OD_{12ts}	General purpose I/O port 1 bit 7.
MSI	119	IN_{ts}	MIDI serial data input. (Default)
CPUFANIN1		I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.
GP21		I/OD_{12ts}	General purpose I/O port 2 bit 1.
MSO	120	OUT_{12t}	MIDI serial data output. (Default)

SYMBOL	PIN	I/O	FUNCTION
CPUFANOUT1		AOUT/ OUT_{12t}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
GP20		I/OD_{12t}	General purpose I/O port 2 bit 0.

Note. The * sign see 5.10.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

5.8 ACPI Interface

SYMBOL	PIN	I/O	FUNCTION
PSIN	68	IN_{td}	Panel Switch Input. This pin is high active with an internal pull down resistor.
GP56		I/OD_{12t}	General purpose I/O port 5 bit 6.
PSOUT#	67	OD_{12}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.
GP57		I/OD_{12t}	General purpose I/O port 5 bit 7.
VBAT	74	PWR	+3.3V on-board battery for the digital circuitry.
RSTOUT0#	94	OD_{12}	Secondary LRESET# output 0.
RSTOUT1#	93	OUT_{12}	Secondary LRESET# output 1.
RSTOUT2#	90	OUT_{12}	Secondary LRESET# output 2.
GP32		I/OD_{12t}	General purpose I/O port 3 bit 2.
SCL		IN_t	Serial Bus clock.
RSTOUT3#	89	OUT_{12}	Secondary LRESET# output 3.
GP33		I/OD_{12t}	General purpose I/O port 3 bit 3.
SDA		I/OD_{12t}	Serial bus bi-directional Data.
RSTOUT4#	88	OUT_{12}	Secondary LRESET# output 4.

SYMBOL	PIN	I/O	FUNCTION
GP34		I/OD_{12t}	General purpose I/O port 3 bit 4.

5.9 General Purpose I/O Port

5.9.1 GPIO Power Source

SYMBOL	POWER SOURCE
GPIO port 1	3VCC
GPIO port 2 (Bit0-3)	3VCC
GPIO port 2 (Bit4-7)	3VSB
GPIO port 3	3VSB
GPIO port 4	3VSB
GPIO port 5	3VSB
GPIO port 6	3VCC

5.9.2 GPIO-1 Interface

see 5.7 Game Port

5.9.3 GPIO-2 Interface

SYMBOL	PIN	I/O	FUNCTION
GP20	120	I/OD_{12t}	General purpose I/O port 2 bit 0.
CPUFANOUT1		AOUT/ OUT_{12}	DC/PWM fan output control. CPUFANOUT0 & AUXFANOUT are default PWM Mode, CPUFANOUT1 & SYSFANOUT are default DC Mode.
MSO		OUT_{12}	MIDI serial data output. (Default)
GP21	119	I/OD_{12ts}	General purpose I/O port 2 bit 1.
CPUFANIN1		I/O_{12ts}	0V to +3.3V amplitude fan tachometer input.

SYMBOL	PIN	I/O	FUNCTION
MSI		IN_{ts}	MIDI serial data input. (Default)
GP22	19	I/OD_{12t}	General purpose I/O port 2 bit 2.
GP23	2	I/OD_{12t}	General purpose I/O port 2 bit 3.
GP24	66	I/OD_{16t}	General purpose I/O port 2 bit 4.
MDAT		I/OD_{16ts}	PS2 Mouse Data.
GP25	65	I/OD_{16t}	General purpose I/O port 2 bit 5.
MCLK		I/OD_{16ts}	PS2 Mouse Clock.
GP26	63	I/OD_{16t}	General purpose I/O port 2 bit 6.
KDAT		I/OD_{16ts}	Keyboard Data.
GP27	62	I/OD_{16t}	General purpose I/O port 2 bit 7.
KCLK		I/OD_{16ts}	Keyboard Clock.

5.9.4 GPIO-3 Interface

SYMBOL	PIN	I/O	FUNCTION
GP30	92	I/OD_{12t}	General purpose I/O port 3 bit 0.
GP31	91	I/OD_{12t}	General purpose I/O port 3 bit 1
GP32	90	I/OD_{12t}	General purpose I/O port 3 bit 2.
RSTOUT2#		OUT_{12}	Secondary LRESET# output 2.
SCL		IN_{t}	Serial Bus clock.
GP33	89	I/OD_{12t}	General purpose I/O port 3 bit 3.
RSTOUT3#		OUT_{12}	Secondary LRESET# output 3.
SDA		I/OD_{12t}	Serial bus bi-directional Data.

SYMBOL	PIN	I/O	FUNCTION
GP34	88	I/OD_{12t}	General purpose I/O port 3 bit 4.
RSTOUT4#		OUT_{12}	Secondary LRESET# output 4.
GP35	87	I/OD_{12t}	General purpose I/O port 3 bit 5
GP36	69	I/OD_{12ts}	General purpose I/O port 3 bit 6
GP37	64	I/OD_{12ts}	General purpose I/O port 3 bit 7

5.9.5 GPIO-4 Interface

see 5.4 Serial Port B

5.9.6 GPIO-5 Interface

SYMBOL	PIN	I/O	FUNCTION
GP50	77	I/O_{12t}	General purpose I/O port 5 bit 0.
EN_VRM10		IN_{td}	During VSB power reset (RSMRST), this pin is pulled down internally and is defined as VID transition voltage level, which provides the value for CR2C bit 3. A 1 kΩ is reserved to pull down and a 1 kΩ is recommended if intends to pull up.
WDTO#		OUT_{12}	Watchdog timer output signal.
GP51	75	I/OD_{12t}	General purpose I/O port 5 bit 1.
RSMRST#		OD_{12}	Resume reset signal output.
GP52	73	I/OD_{12t}	General purpose I/O port 5 bit 2.
SUSB#		IN_t	System S3 states input.
GP53	72	I/OD_{12t}	General purpose I/O port 5 bit 3.
PSON#		OD_{12}	This pin generates the PWRCTL# signal while the power failure.
GP54	71	I/OD_{12t}	General purpose I/O port 5 bit 4.
PWROK		OD_{12}	This pin generates the PWROK signal while the VCC come in.

SYMBOL	PIN	I/O	FUNCTION
GP55	70	I/O_{12t}	General purpose I/O port 5 bit 5. (This pin is push-pull output mode)
SUSLED		OUT_{12}	Suspended LED output. (This pin is push-pull output mode)
GP56	68	I/OD_{12t}	General purpose I/O port 5 bit 6.
PSIN		IN_{td}	Panel Switch Input. This pin is high active with an internal pull down resistor.
GP57	67	I/OD_{12t}	General purpose I/O port 5 bit 7.
PSOUT#		OD_{12}	Panel Switch Output. This signal is used for Wake-Up system from $S5_{cold}$ state. This pin is pulse output, active low.

5.9.7 GPIO-6 Interface

see 5.4 Serial Port A

5.9.8 GPIO-1 and GPIO-4 with WDTO# / SUSLED / PLED multi-function

SYMBOL	PIN	I/O	FUNCTION
GPxx*	---	I/OD_{12t}	This GPxx* can be served GPIO or Watchdog timer output signal.
WDTO#		OD_{12}	
GPxx**	---	I/OD_{12t}	This GPxx** can be served GPIO or Power LED output signal.
PLED		OD_{12}	
GPxx***	---	I/OD_{12t}	This GPxx*** can be served GPIO or Suspend LED output signal.
SUSLED		OD_{12}	

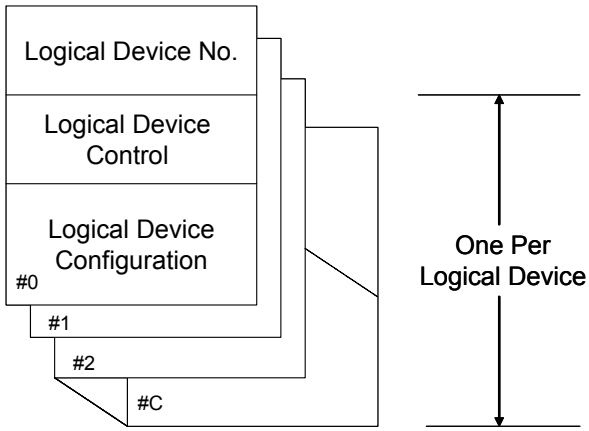
5.10 POWER PINS

SYMBOL	PIN	FUNCTION
3VSB	61	+3.3V stand-by power supply for the digital circuitry.
VBAT	74	+3V on-board battery for the digital circuitry.
3VCC	12,28,48	+3.3V power supply for driving 3V on host interface.

AVCC	114	Analog +3.3V power input. Internally supplier to all analog circuitry.
AGND	117	Internally connected to all analog circuitry. The ground reference for all analog inputs.
GND	20,55	Ground.

6. CONFIGURATION REGISTER ACCESS PROTOCOL

The W83627EHF/EHG/EF/EG uses Super I/O protocol to access configuration registers to set up different types of configurations. The W83627EHF/EHG/EF/EG has totally twelve Logical Devices (from Logical Device 0 to Logical Device B with the exception of Logical Device 4 for backward compatibility) corresponding to twelve individual functions: FDC (Logical Device 0), Parallel Port (Logical Device 1), UARTA (Logical Device 2), UARTB (Logical Device 3), Keyboard Controller (Logical Device 5), GPIO1, GPIO6, Game Port & MIDI Port(Logical Device 7), WDTO# & PLED (Logical Device 8), GPIO2, 3, 4, 5 & SUSLED (Logical Device 9), ACPI (Logical Device A), and Hardware Monitor (Logical Device B),. Each Logical Device has its own configuration registers (above CR30). The host can access those registers by writing an appropriate Logical Device Number into the Logical Device select register at CR7.

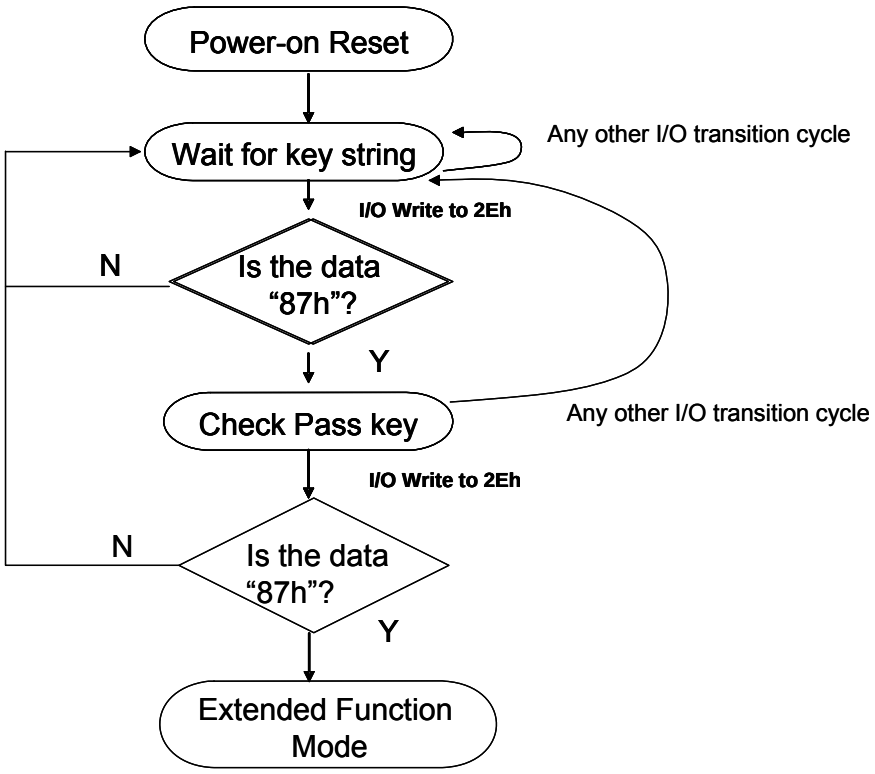


Devices of I/O Base Address

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
0	FDC	100h ~ FF8h
1	Parallel Port	100h ~ FF8h
2	UART A	100h ~ FF8h

LOGICAL DEVICE NUMBER	FUNCTION	I/O BASE ADDRESS
3	UART B	100h ~ FF8h
4	Reserved	
5	Keyboard Controller	100h ~ FFFh
6	Reserved	
7	GPIO1, GPIO 6, Game Port & MIDI port	100h ~ FFFh
8	WDTO# & PLED	Reserved
9	GPIO 2, 3, 4, 5 & SUSLED	Reserved
A	ACPI	Reserved
B	Hardware Monitor	100h ~ FFEh

6.1 Configuration Sequence



To program the W83627EHF/EHG/EF/EG configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

6.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

6.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

6.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

6.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR26 bit 6) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV DX, 2EH
MOV         AL, 87H
OUT DX, AL
```

```
OUT DX, AL
;-------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV AL, 07H
OUT DX, AL              ; point to Logical Device Number Reg.
MOV DX, 2FH
MOV AL, 01H
OUT DX, AL              ; select Logical Device 1
;
MOV DX, 2EH
MOV AL, F0H
OUT DX, AL              ; select CRF0
MOV DX, 2FH
MOV       AL, 3CH
OUT DX, AL              ; update CRF0 with value 3CH
;-------------------------------------------------------------------------
; Exit the Extended Function Mode
;-------------------------------------------------------------------------
MOV DX, 2EH
MOV       AL, AAH
OUT DX, AL
```

Chip (Global) Control Registers

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
02h	Write Only		Software Reset
07h	R/W	00h	Logical Device
20h	Read Only	A0h	Chip ID, MSB
21h	Read Only	2xh	Chip ID, LSB
22h	R/W	FFh	Device Power Down
23h	R/W	00h	Immediate Power Down
24h	R/W	0100_0ss0b	Global Option
25h	R/W	00h	Interface Tri-state Enable
26h	R/W	0s000000b	Global Option
27h	Reserved		

INDEX	R/W	DEFAULT VALUE	DESCRIPTION
28h	R/W	50h	Global Option
29h	R/W	00h	Multi-function Pin Selection
2Ah	R/W	00h	I^2C pin select
2Bh	Reserved		
2Ch	R/W	E2h	Multi-function Pin Selection
2Dh	R/W	21h	Multi-function Pin Selection
2Eh	R/W	00h	Reserved
2Fh	R/W	00h	Reserved

S: Strapping; x: chip version.

7. HARDWARE MONITOR

7.1 General Description

The W83627EHF/EHG can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stable and properly. W83627EHF/EHG provides LPC interface to access hardware.

An 8-bit analog-to-digital converter (ADC) was built inside W83627EHF/EHG. The W83627EHF/EHG can simultaneously monitor 6 analog voltage inputs (intrinsic monitor VBAT, 3VSB, 3VCC,& AVCC power), 5 fan tachometer inputs, 3 remote temperature, one case-open detection signal. The remote temperature sensing can be performed by thermistors or directly from Intel™ Deschutes CPU thermal diode output. Also the W83627EHF/EHG provides: 4 PWM (pulse width modulation) outputs for the fan speed control or 4 DCFAN outputs for the fan speed control; beep tone output for warning; SMI#(through SERIRQ or OVT# pin) , OVT# signals for system protection events.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Nuvoton's Hardware Doctor™ or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and masked interrupts.

An optional beep tone could be used as warning signals when the monitored parameters are out of the preset range.

7.2 Access Interface

W83627EHF/EHG provides two interface for microprocessor to read/write hardware monitor internal registers.

7.2.1 LPC interface

The first interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports are set by W83627EHF/EHG itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

Port 295h: Index port.

Port 296h: Data port.

The register structure is showed as the Figure 7.1

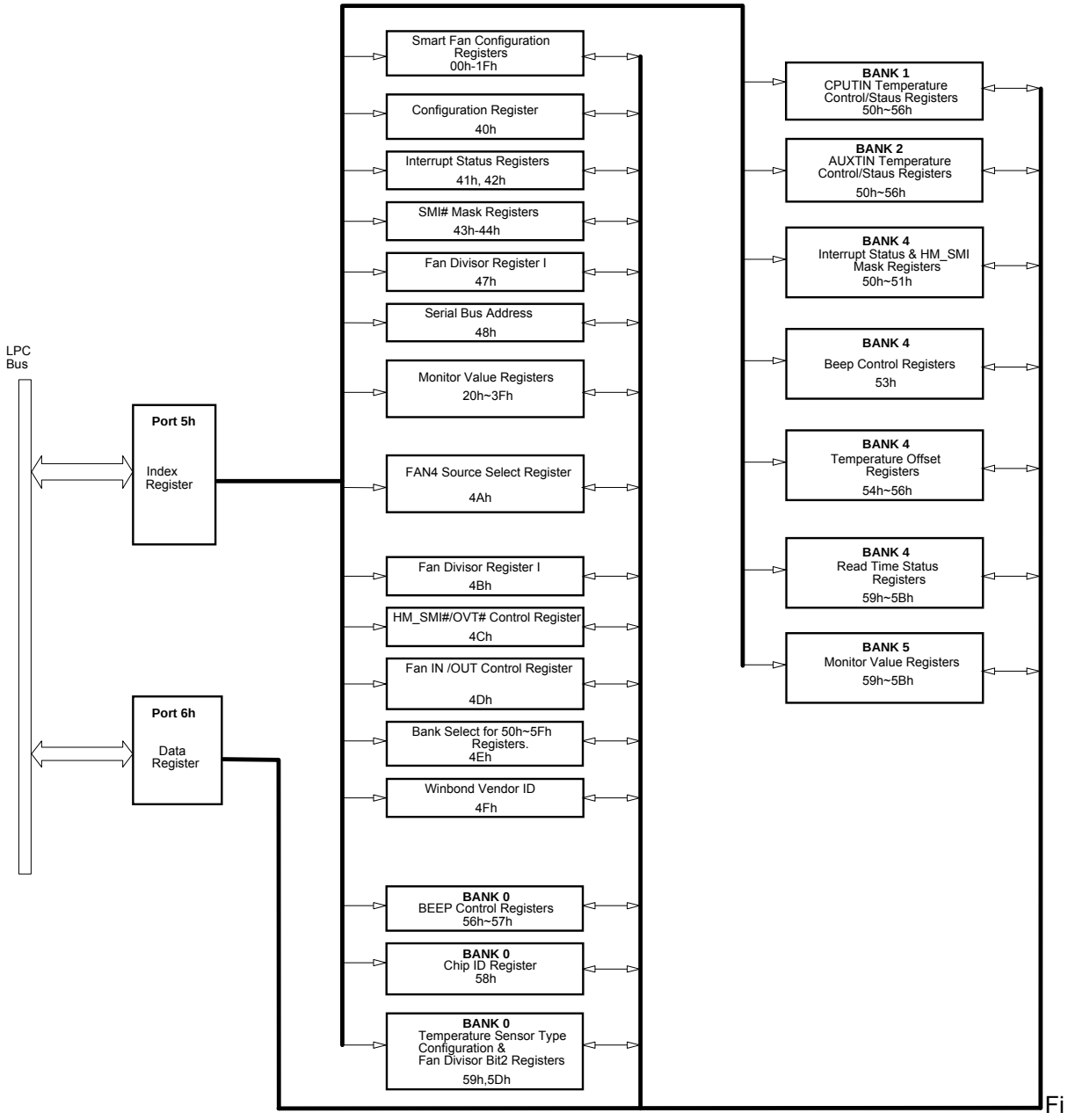


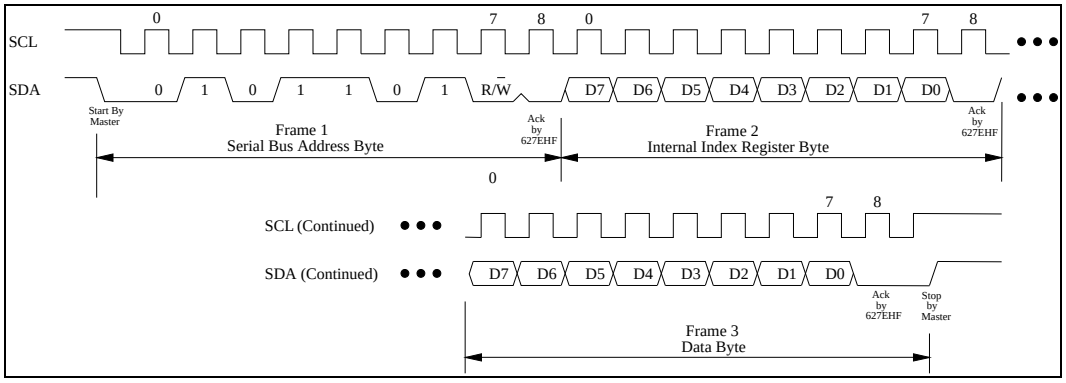
Figure 7.1 : LPC interface access diagram

7.2.2 I²C interface

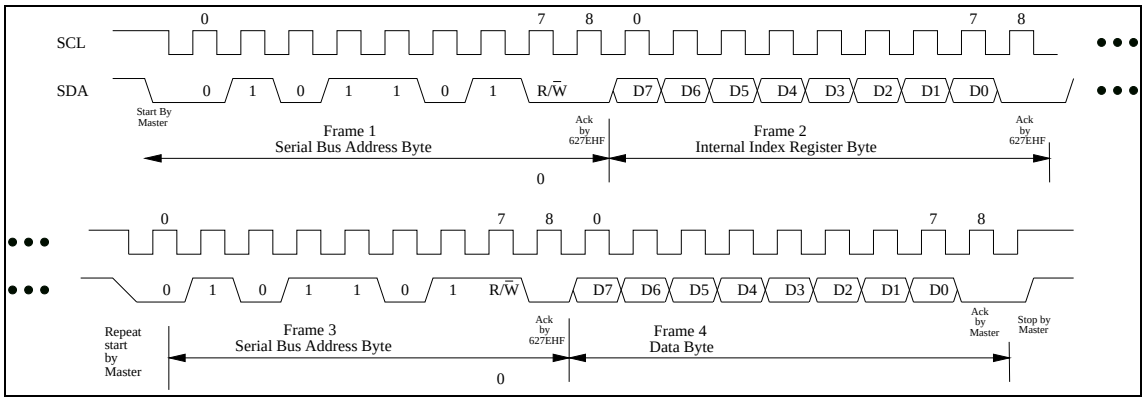
The second interface uses I²C Serial Bus. W83627EHF/EHG has a programmable serial bus address. It defined at Index 48h.

7.2.2.1. Serial bus (I^2C) access timing

(a) Serial bus write to internal address register followed by the data byte



(b) Serial bus read from a register



7.3 Analog Inputs

The maximum input voltage of the analog pin is 2.048V because the 8-bit ADC has a 8mV LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU Vcore voltage, VBAT(pin 74), 3VSB(pin 61), 3VCC(pin 12) , AVCC(pin 114) voltage can directly connected to these analog inputs. The +12V voltage inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 7.2 shows.

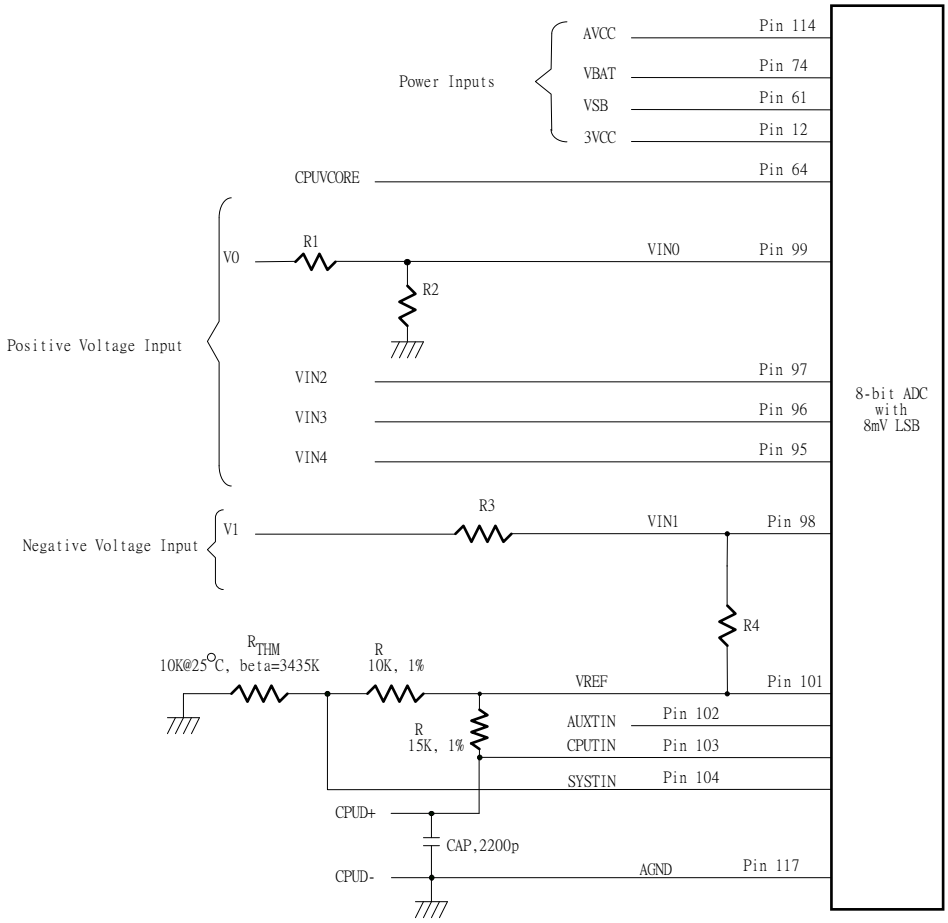


Figure 7.2

7.3.1 Monitor over 2.048V voltage

The +12V input voltage can be expressed as following equation.

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 56K Ohms and 10K Ohms, respectively, when the input voltage V_0 is 12V. The node voltage of VIN0 can be subject to less than 2.048V for the maximum input range of the 8-bit ADC.

The -12V input voltage can be expressed as following equation.

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

The value of R3 and R4 can be selected to 232K Ohms and 10K Ohms, respectively, when the input voltage V_1 is -12V. The node voltage of VIN1 can be subject to less than 2.048V for the maximum input range of the 8-bit ADC.

Both of pin 12 and pin 114 are connected to the power supply VCC with +3.3V. There are two functions in these 2 pins with 3.3V. The first function is to supply internal (digital/analog) power in the W83627EHF/EHG and the second function is that this voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The W83627EHF/EHG internal two serial resistors are 34 KΩ and 34 KΩ so that input voltage to ADC is 1.65V which is less than 2.048V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V.

The Pin 61 is connected to 3.3 VSB voltage. W83627EHF/EHG monitors this voltage and the internal two serial resistors are 34 KΩ and 34 KΩ so that input voltage to ADC is 1.65V which less than 2.048V of ADC maximum input voltage.

7.3.2 CPUVCORE voltage detection method

W83627EHF/EHG provides one detection methods for CPUVCORE(pin 100).

The LSB of this mode is 8mV. This means that the detected voltage equals to the reading of this voltage register multiplies 8mV. The formula is as the following:

Detected Voltage = $\text{Reading} * 0.008$ V

7.3.3 Temperature Measurement Machine

The temperature data format is 8-bit two's-complement for sensor SYSTIN and 9-bit two's-complement for sensor CPUTIN and AUXTIN. The 8-bit temperature data can be obtained by reading the Index[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the Bank1/Bank2 Index[50h] and the LSB from the Bank1/Bank2 Index[51h] bit 7. The format of the temperature data is show in Table 7.1.

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 7.1

7.3.3.1. Monitor temperature from thermistor

The W83627EHF/EHG can connect three thermistors to measure three different environment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 7.2, the themistor is connected by a serial resistor with 10K Ohms, then connect to VREF (pin 101).

7.3.3.2. Monitor temperature from Pentium II™/Pentium III™ thermal diode

The W83627EHF/EHG can alternate the thermistor to Pentium II™/Pentium III™ thermal diode and the circuit connection is shown as Figure 7.3. The pin of Pentium II™/ Pentium III™ D- is connected to AGND(pin 117) and the pin D+ is connected to temperature sensor pin in the W83627EHF/EHG. The resistor R=15K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=2200pF should be added to filter the high frequency noise.

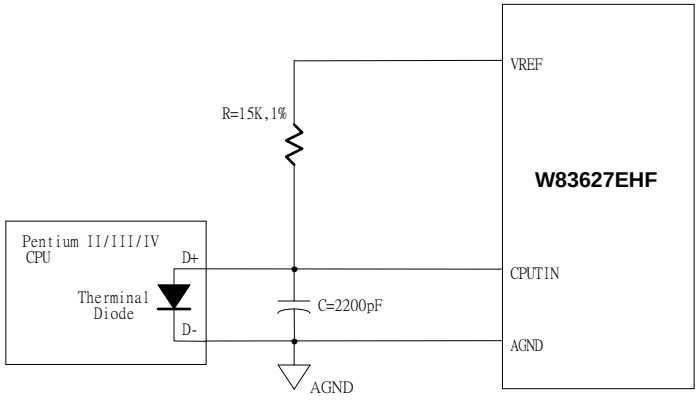


Figure 7.3

7.4 FAN Speed Count and FAN Speed Control

7.4.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over **+3.3V**. If the input signals from the tachometer outputs are over the **+3.3V**, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 7.4.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register Bank0 Index 28h, 29h, 2Ah, 3Fh and Bank5 53h, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at Bank0 Index 47h.bit7~4, Index 4Bh.bit7~6, Index 4Ch.bit7, Index 59h.bit7.bit3~2 and Index 5Dh.bit5~7 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count.

Divisor	Nominal RPM	Time per Revolution	Counts	70% RPM	Time for 70%
1	8800	6.82 ms	*153*	6160	9.84 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms

Divisor	Nominal RPM	Time per Revolution	Counts	70% RPM	Time for 70%
128	68	872.64 ms	*153*	48	1246.72 ms

Table 7.2

7.4.2 Fan speed control

W83627EHF/EHG provides two controllable methods for Fan speed control. One is PWM duty cycle output and the other is DC voltage output. Either PWM or DC output can be programmed at Bank0 Index 04h.bit1~0, Index 12h.bit0 and Index 62h.bit6.

7.4.2.1. PWM Duty Cycle Output

The W83627EHF/EHG provides maximum 4 sets for fan PWM speed control. The duty cycle of PWM can be programmed by a 8-bit registers which are defined in the Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The default duty cycle is set to **100%**, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Dutycycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

The PWM clock frequency also can be program and defined in the Bank0 Index 00h, Index 02h, Index 10h and Index 60h.

7.4.2.2. DC Voltage Output

The W83627EHF/EHG has a 6 bit DAC which produces 0 to 3.3 volts DC output that provides maximum 4 sets for fan speed control. The analog output can be programmed in the Bank0 Index 01h, Index 03h, Index 11h and Index 61h. The default value is 111111YY,YY is reserved 2 bits, that is default output value is nearly 3.3 V. The expression of output voltage can be represented as follow ,

$$\mathit{OutputVoltage}(V) = 3VCC \times \frac{\text{Programmed 6 - bit Register Value}}{64}$$

7.5 Conversion Sequence and Conversion Time

The conversion sequence and conversion time of the W83627EHF/EHG include the voltage and temperature conversion time. The sample rate of the W83627EHF/EHG is 22.5 KHz. 24 cycles are needed to complete the ADC conversion of the temperature (worst case), and 16 cycles are needed for the ADC conversion of the voltage. The W83627EHF/EHG has 10 voltage sets and 3 temperature sets.

The monitor time of the 3 temperature sets: 3* 24 * 0.044mS = 3.168 ms

The 10 voltage sets: 10 * 16 * 0.044 ms = 7.04 ms

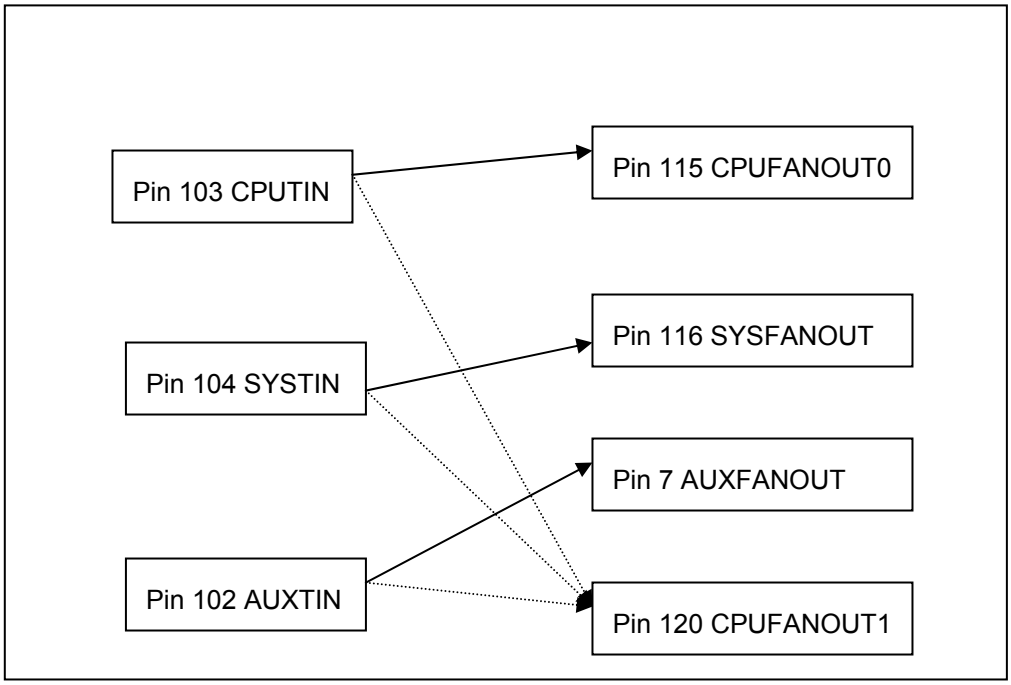
Total conversion time = 3.168 + 7.04 = 10.208 ms

Please note that the suggested time interval for the most updated data is 20 ms.

7.6 Smart Fan Control

SMART FAN™ I :

Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode. When enable Smart Fan, the Fan output will start from previous setting of Bank0 Index 01h, Index 03h, Index 11h and Index 61h to increase or decrease.



7.6.1 Thermal Cruise mode

There are maximum 4 pairs of Temperature/Fan output control at this mode: SYSTIN with SYSFANOUT, CPUTIN with CPUFANOUT0, AUXTIN with AUXFANOUT and CPUFANOUT1 depends on Bank0 Index 4Ah.bit7~6 setting that is temperature source selection.

W83627EHF/EHG provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS, as long as the real temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 20% output) and automatically controlled its output with the temperature varying. Three conditions may occur :

(1) If the temperature still exceeds the high limit (ex: 58°C), Fan output will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit(ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area(ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), Fan output will decrease slowly to 0 until the temperature exceeds the low limit.

In other words, If “current temperature” > “High Limit”, increase fan speed;

If “current temperature” < “Low Limit”, decrease fan speed;

Otherwise, keep the fan speed.

Figure 7.6 PWM fan mode and Figure 7.7 DC fan mode illustrate the Thermal Cruise mode

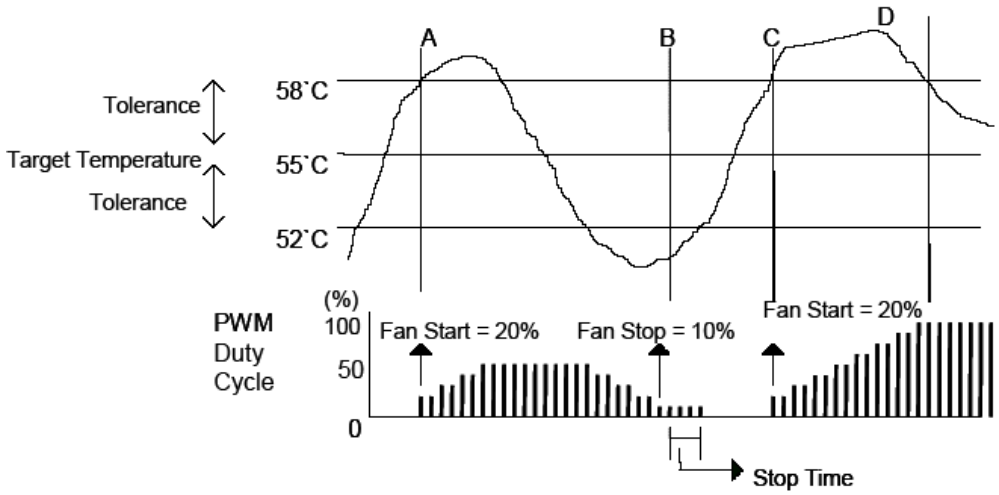


Figure 7.6

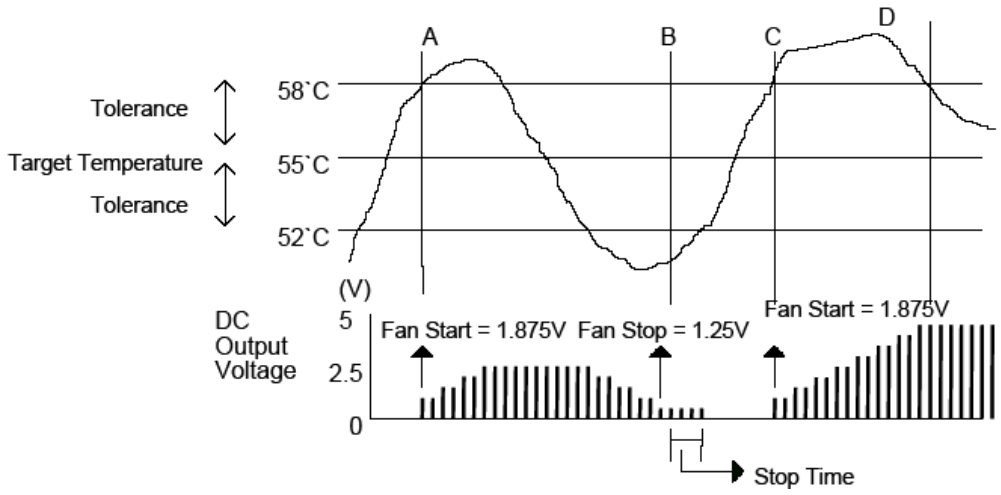


Figure 7.7

(c) One more protection is provided that Fan output will not be decreased to 0 in the above (3) situation in order to keep the fans running with a minimum speed. By setting Bank0 Index12h.bit3~5 to 1, Fan output will be decreased to the "Stop Output Value" which are defined at Bank0 Index08h, Index09h and Index17h.

(d)

7.6.2 Fan Speed Cruise mode

There are 4 pairs of Fan input/Fan output control at this mode: SYSFANIN with SYSFANOUT, CPUFANIN0 with CPUFANOUT0, AUXFANIN with AUXFANOUT and CPUFANIN1 with CPUFANOUT1. At this mode, W83627EHF/EHG provides the Smart Fan system which can control the fan speed automatically depend on current fan speed to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ± 10) by BIOS. As long as the fan speed count is the specific range, Fan output will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), Fan output will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit(ex. 160-10), Fan output will be decreased to keep the count higher than the low limit. See Figure 7.8 example.

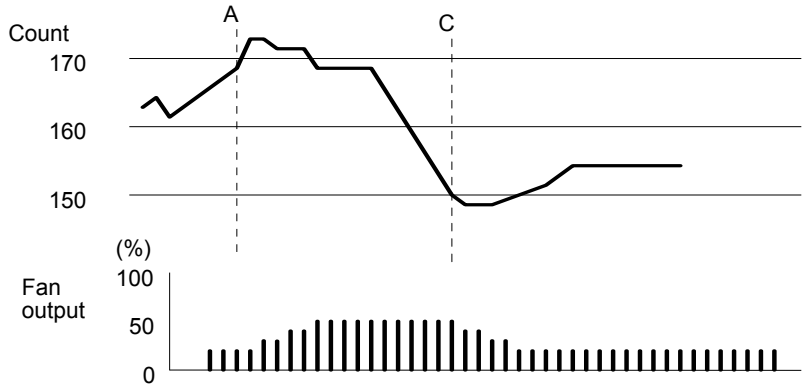


Figure 7.8

7.6.3 Manual Control Mode

Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software. The programming method must be set fan configuration at bank 0 index 04h,bit5-4 to 1,index 62h bit5~4 to 1. Then table 7.3-1 displayed current temperature and fan output value at Smart Fan I Mode Besides, these tables 7.3-2 and 7.3-3 used to setting thermal mode or speed cruise mode of Smart Fan I mode.

Table 7.3-1 Display Register- at Smart Fan I Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 50H ,51H	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 27H	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 50h,51h	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 03h	CPUFANOUT0 Output Value Select	FFh	Bit7-0 CPUFANOUT Value
Current SYSFANOUT	Bank0 01h	SYSFANOUT Output Value Select	FFh	Bit7-0 SYSFANOUT

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Output Value				Value
Current AUXFANOUT Output Value	Bank0 11h	AUXFANOUT1 Output Value Select	FFh	Bit7-0 AUXFANOUT Value
Current CPUFANOUT1 Output Value	Bank0 61h	CPUFANOUT1 Output Value Select	FFh	Bit7-0 CPUFANOUT1 Value

Table 7.3-2 Relative Register-at Thermal Cruise Mode of Smart Fan I control mode

THERMAL-CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP-DOWN TIME	STEP-UP TIME
SYSFANOUT	CR[05h]	CR[07h] Bit0-3	CR[0Ah]	CR[08]h	CR[12h] Bit5	CR[0Ch]	CR[0Eh]	CR[0Fh]
CPUFANOUT0	CR[06h]	CR[07h] Bit4-7	CR[0Bh]	CR[09h]	CR[12h] Bit4	CR[0Dh]		
AUXFANOUT	CR[13h]	CR[14h] Bit0-3	CR[16h]	CR[15h]	CR[12h] Bit3	CR[17h]		
CPUFANOUT1	CR[63h]	CR[62h] Bit0-3	CR[65h]	CR[64h]	CR[12h] Bit6	CR[66h]		

Table 7.3-3 Relative Register-at Speed Cruise Mode of Smart Fan I control mode

THERMAL-CRUISE MODE	TARGET-SPEED COUNT	TOLERANCE	KEEP MIN. FAN OUTPUT VALUE	STEP-DOWN TIME	STEP-UP TIME

SYSFANOUT	CR[05h]	CR[07h] Bit0-3	CR[12h] Bit5	CR[0Eh]	CR[0Fh]
CPUFANOUT0	CR[06h]	CR[07h] Bit4-7	CR[12h] Bir4		
AUXFANOUT	CR[13h]	CR[14h] Bit0-3	CR[12h] Bit3		
CPUFANOUT1	CR[63h]	CR[62h] Bit0-3	CR[12h] Bit6		

SMART FAN™ III

Concept

SMART FAN™ III mode sets a target temperature through BIOS or application software and W83627EHF/EHG controls the fan speed so that the temperature could meet the target temperature set in the BIOS or software. Only Pin115 (CPUFANOUT0) and Pin120 (CPUFANOUT1) in W83627EHF/EHG support SMART FAN™ III. Pin115 (CPUFANOUT0) pairs with Pin103 (CPUTIN); while Pin120 (CPUFANOUT1) pairs with Pin104 (SYSTIN), Pin103 (CPUTIN), or Pin102 (AUXTIN), which is defined in Bank0 Index 4Ah.bit7~6.

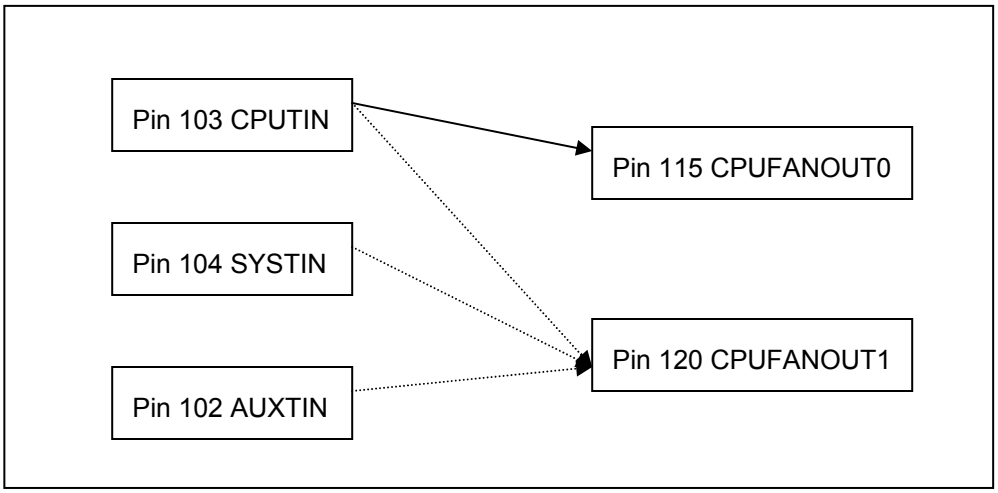


Figure 7.9, 7.10, and 7.11 illustrate SMART FAN™ III mode, and the algorithm of fan speed control is described as follows:

(1) Figure 7.9 shows the initial condition of SMART FAN™ III. Target Temperature, Temperature Tolerance, Maximum Fan Output and Minimum Fan Output must be set first. If the currently measured temperature is within the (Target Temperature ± Temperature Tolerance), the fan speed remains constant.

(2) In the case that currently measured temperature goes beyond (Target Temperature + Temperature Tolerance), which is shown in Figure 7.10, fan speed jumps up to the next step. "Step" here refers to the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h.

(3) Meanwhile, original Target Temperature dynamically shifts to (Target Temperature + Temperature Tolerance), and new Target Temperature, named Target Temperature 1, is formed. In other words, Target Temperature 1 equals original Target Temperature plus Temperature Tolerance.

(4) If the currently measured temperature is within the (Target Temperature 1 ± Temperature Tolerance) then, the fan speed remains constant. Otherwise, fan speed jumps up to the next step again. Target Temperature then dynamically shifts to (Target Temperature 1 + Temperature Tolerance), and new Target Temperature again, named Target Temperature 2, is formed.

(5) The fan-speed-up and Target Temperature comparison-then-shift process continue until currently measured temperature locates within (Target Temperature X ± Temperature Tolerance), or fan output speed reaches its maximum speed.

(6) Please be noted that "Speed-up Slope" shown in the Figure 7.10 must be an integer. In other words, $\frac{Max.FanOutput - InitialOutput}{Steps}$ must be an integer; otherwise, it may lead to register overflow.

(7) In the case that currently measured temperature goes below (Target Temperature − Temperature Tolerance), which is shown in Figure 7.11, fan speed slows down by one step. "Step" here refers to the value in the CPUFANOUT Output Value Select Register, Bank0 Index03h or Index61h.

(8) Meanwhile, original Target Temperature dynamically shifts to (Target Temperature − Temperature Tolerance), and new Target Temperature, named Target Temperature 1, is formed. In other words, Target Temperature 1 equals original Target Temperature minus Temperature Tolerance.

(9) If the currently measured temperature is within the (Target Temperature 1 ± Temperature Tolerance) then, the fan speed remains constant. Otherwise, fan speed slows down by one step again. Target Temperature then dynamically shifts to (Target Temperature 1 − Temperature Tolerance), and new Target Temperature again, named Target Temperature 2, is formed.

(10) The fan-slow-down and Target Temperature comparison-then-shift process continue until currently measured temperature locates within (Target Temperature X ± Temperature Tolerance), or fan output speed hits its minimum speed.

(11) Please be noted that "Speed-down Slope" shown in the Figure 7.11 must be an integer. In other words, $\frac{InitialOutput - Min.FanOutput}{Step}$ must be an integer; otherwise, it may lead to register overflow.

(12) In the case that the temperature is always lower than (Target Temperature X – Temperature Tolerance), and, for some reason, the fan speed would like to be kept at the minimum speed, Stop Value, instead of being stopped, set register Bank0 12h.bit 4. Set bit 4 to 1, fan speed will always keep at the value set in Bank0 Index09h when temperature is always below (Target Temperature X – Temperature Tolerance). Set bit 4 to 0, fan speed will decrease to 0 after a time period set in Bank0 Index 0Dh.

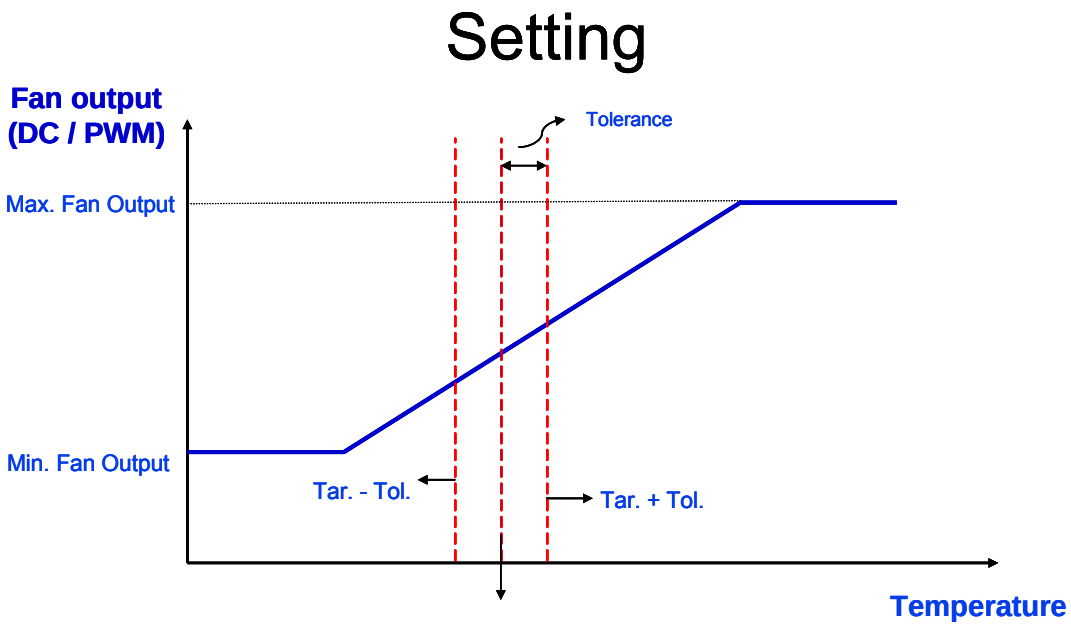


Figure 7.9

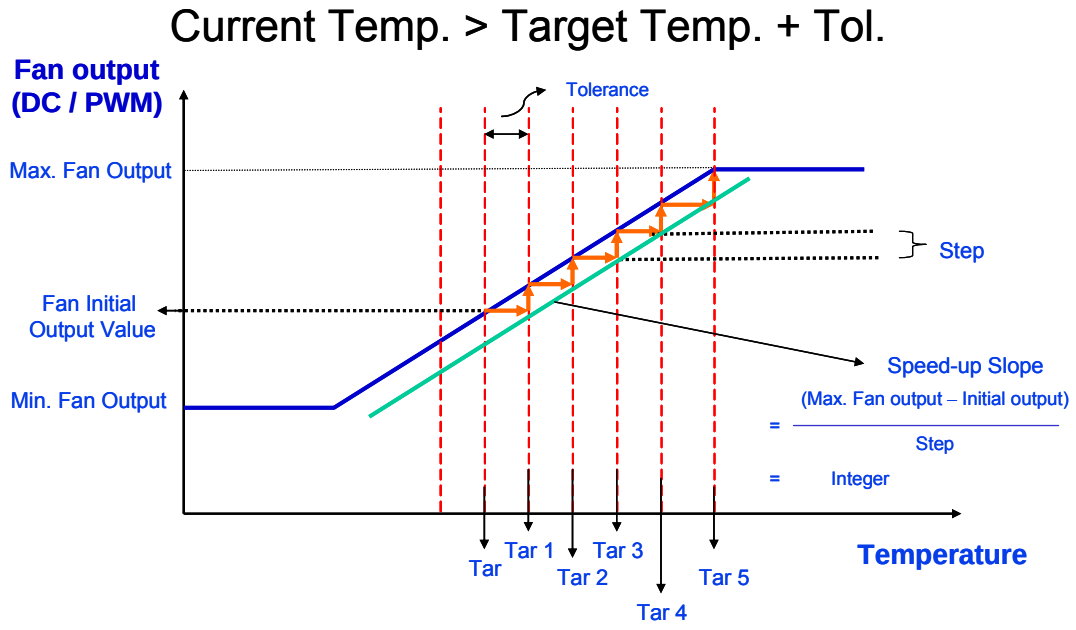


Figure 7.10

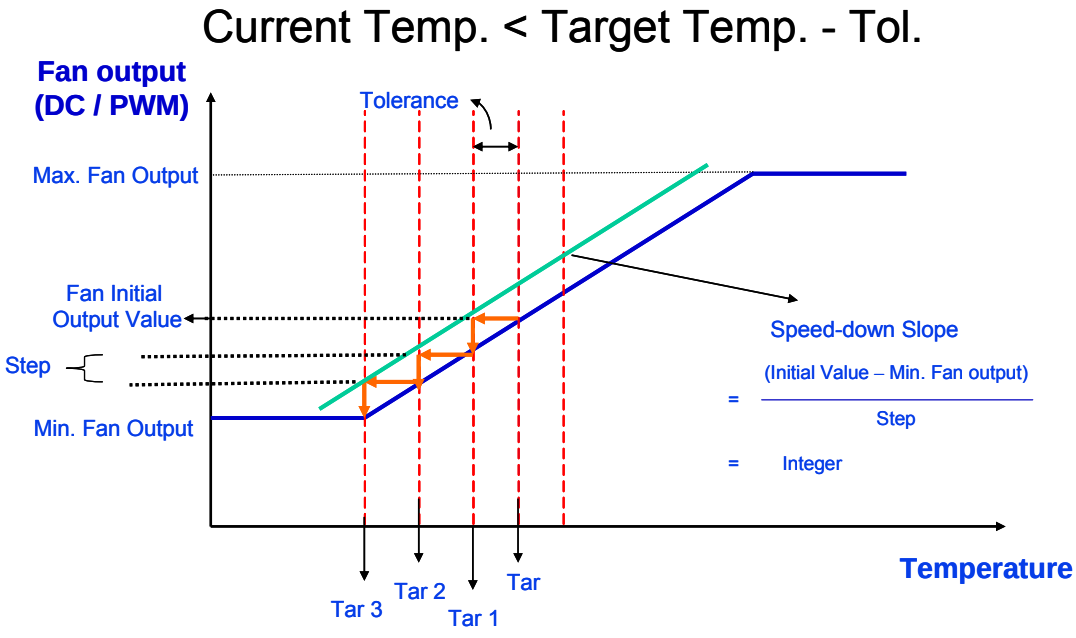


Figure 7.11

7.6.4 Smart Fan™ III Mode

Smart Fan™ III control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software. The programming method must be set fan configuration at bank 0 index 04h,bit5-4,index 12h bit2~1 index 62h bit5~4.Before enabling Smart Fan™ III mode ,you have to set relative registers as table 7.4-2. In addition to the required registers, the device has a the following registers that further configure and enable the fan speed control functionality .Then Table 7.4-1 displayed current temperature and fan output value at Smart Fan™ III mode , Besides, the table 7.4-2 used to setting at Smart Fan™ III mode

Table 7.4-1 Display Register- at Smart Fan™ III Mode

DESCRIPTION	REGISTER ADDRESS	REGISTER NAME	ATTRIBUTE	BIT DATA
Current CPU Temperature	Bank1 50h ,51h	CPUTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current SYS Temperature	Bank 0 27h	SYSTIN Temperature Sensor	Read only	8 MSB, 1°C
Current AUX Temperature	Bank2 50h,51h	AUXTIN Temperature Sensor	Read only	8 MSB, 1°C bit 7, 0.5 °C
Current CPUFANOUT0 Output Value	Bank0 03h	CPUFANOUT0 Output Value Select	FFh	Bit7-0 CPUFANOUT Value
Current SYSFANOUT Output Value	Bank0 01h	SYSFANOUT Output Value Select	FFh	Bit7-0 SYSFANOUT Value

Table 7.4-2 Relative Register-at Smart Fan™ III control mode

Smart Fan™ III Mode	Target Temperature	Tolerance	Stop Value (Min. Fan Output)	Max. Fan Output	Stop Time
CPUFANOUT0	CR[06h]	CR[07h] bit 4-7	CR[09h]	CR[67h]	CR[0Dh]
CPUFANOUT1	CR[63h]	CR[62h] bit 0-3	CR[64h]	CR[69h]	CR[66h]

Smart Fan™ III Mode	Output Step	Step Down Time	Step Up Time	Keep Min. Fan Output value	
CPUFANOUT0	CR[68h]	CR[0Eh]	CR[0Fh]	CR[12h] bit 4	
CPUFANOUT1	CR[6Ah]	CR[0Eh]	CR[0Fh]	CR[12h] bit 6	

7.7 SMI# interrupt mode

The SMI#/OVT# pin is a multi-function pin. The function is selected at Configuration Register CR[29h] bit 6.

7.7.1 Voltage SMI# mode

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 7.12)

7.7.2 Fan SMI# mode

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 7.13)

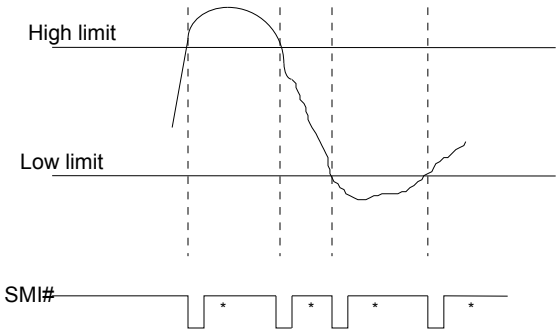
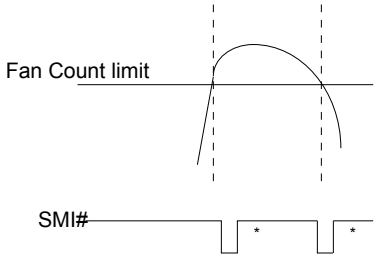


Figure 7.12



*Interrupt Reset when Interrupt Status Registers are read

Figure 7.13

7.7.3 Temperature SMI# mode

7.7.3.1. Temperature sensor 1(SYSTIN) SMI# interrupt has 3 modes

(1) Comparator Interrupt Mode

Setting the T_{HYST} (Temperature Hysteresis) limit to 127°C will set temperature sensor 1 SMI# to the Comparator Interrupt Mode. Temperature exceeds T_O (Over Temperature) Limit causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_O , the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_O. (Figure 7.14)

Setting the T_{HYST} lower than T_O will set temperature sensor 1 SMI# to the Interrupt Mode. The following are two kinds of interrupt modes, which are selected by Bank0 Index 4Ch bit5:

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 7.15)

(3) One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure 7.16)

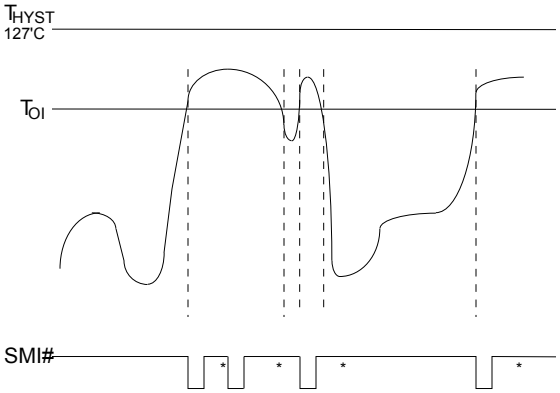


Figure 7.14

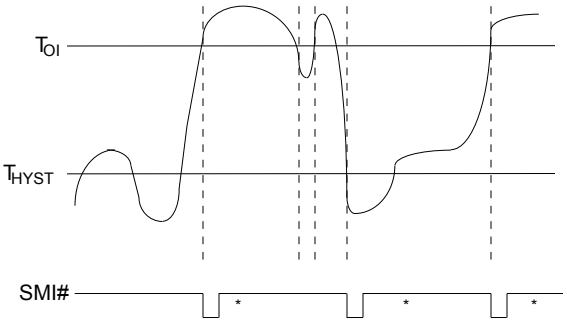
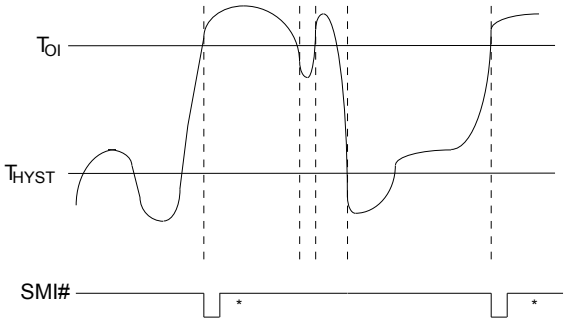


Figure 7.15

*Interrupt Reset when Interrupt Status Registers are read



*Interrupt Reset when Interrupt Status Registers are read

Figure 7.16

7.7.3.2. Temperature sensor 2(CPUTIN) and sensor 3(AUXTIN) SMI# interrupt has two modes

It is programmed at Bank0 Index 4Ch.bit 6.

(1) Comparator Interrupt Mode

Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 7.17)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 7.18)

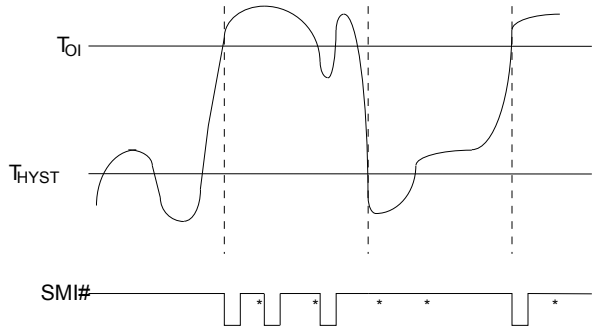
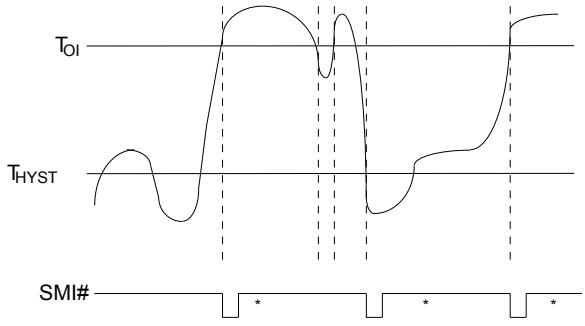


Figure 7.17



*Interrupt Reset when Interrupt Status Registers are read

Figure 7.18

7.8 OVT# interrupt mode

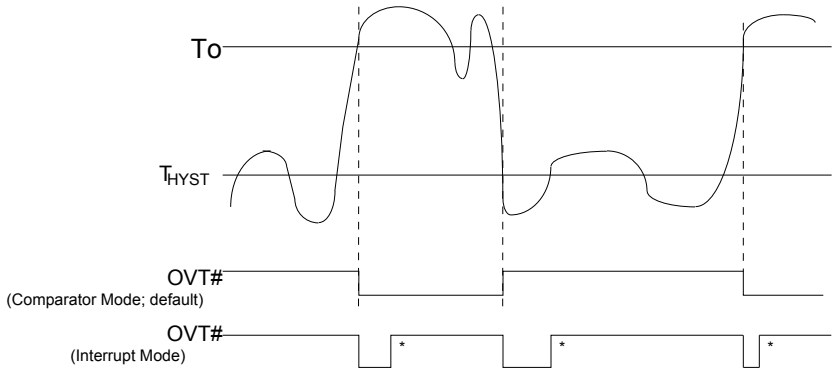
The SMI#/OVT# pin (pin 5) is a multi-function pin. The function is selected at Configuration Register CR[29h] bit 6. The OVT# mode selection bits are at Bank0 Index18h bit4, Bank1 Index 52h bit1 and Bank2 Index 52h bit1.

(1) Comparator Mode:

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 7.19)

(2) Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 7.19)



*Interrupt Reset when Temperature sensor registers are read

Figure 7.19

7.9 Registers and RAM

Address Port and Data Port are set in the register CR60 and CR61 of Device B which is Hardware Monitor Device. The value in CR60 is high byte and that in CR61 is low byte. For example, setting CR60 to 02 and CR61 to 90 causes the Address Port to be 0x295 and Data Port to be 0x296.

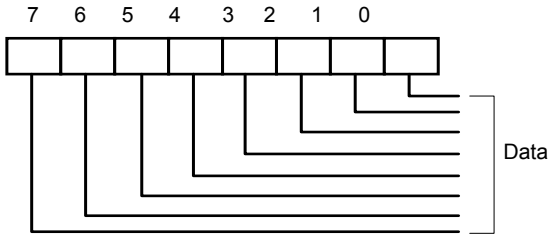
7.9.1 Address Port (Port x5h)

Address Port: Port x5h

Power on Default Value 00h

Attribute: Bit 6:0 Read/write , Bit 7: Reserved

Size: 8 bits



Bit7: Reserved

Bit 6-0: Read/Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

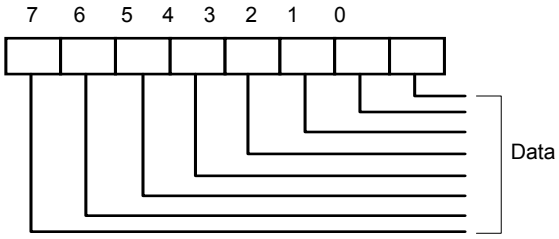
7.9.2 Data Port (Port x6h)

Data Port: Port x6h

Power on Default Value 00h

Attribute: Read/write

Size: 8 bits



Bit 7-0: Data to be read from or to be written to RAM and Register.

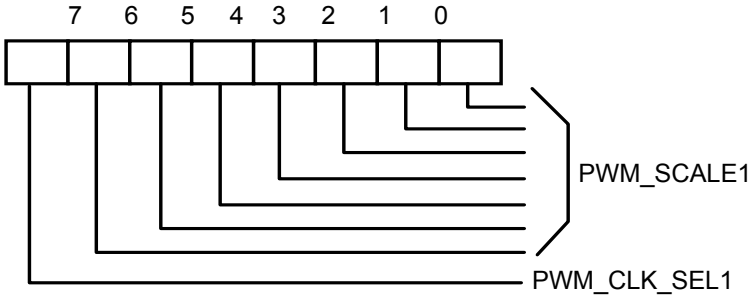
7.9.3 SYSFANOUT PWM Output Frequency Configuration Register - Index 00h (*Bank 0*)

Register Location: 00h

Power on Default Value: 04h

Attribute: Read/Write

Size: 8 bits



The register is meaningful when SYSFANOUT be programmed as PWM output.

Bit 7: SYSFANOUT PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-0: SYSFANOUT PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1

02h : divider is 2

03h : divider is 3

:

:

the formula is $$\text{PWM output frequency} = \frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$$

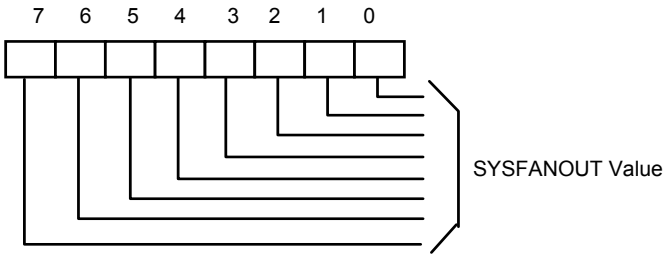
7.9.4 SYSFANOUT Output Value Select Register - Index 01h (*Bank 0*)

Register Location: 01h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



(1)If SYSFANOUT be programmed as PWM output (Bank0 Index 04h.bit0 is 0)

Bit 7-0: SYSFANOUT PWM Duty Cycle. Write FFh, SYSFANOUT is always logical High which means duty cycle is 100%. Write 00h, SYSFANOUT is always logical Low which means duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If SYSFANOUT be programmed as DC Voltage output (Bank0 Index 04h.bit0 is 1)

Bit 7-2: SYSFANOUT voltage control.

Bit 1-0: Reserved.

$$\textbf{OUTPUT Voltage} = AVCC * \frac{FANOUT}{64}$$

If AVCC= 3.3V , output voltage table is

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE
0	0	0	0	0	0	0	1	0	0	0	0	0	1.65
0	0	0	0	0	1	0.05	1	0	0	0	0	1	1.70

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE
0	0	0	0	1	0	0.10	1	0	0	0	1	0	1.75
0	0	0	0	1	1	0.15	1	0	0	0	1	1	1.80
0	0	0	1	0	0	0.21	1	0	0	1	0	0	1.86
0	0	0	1	0	1	0.26	1	0	0	1	0	1	1.91
0	0	0	1	1	0	0.31	1	0	0	1	1	0	1.96
0	0	0	1	1	1	0.36	1	0	0	1	1	1	2.01
0	0	1	0	0	0	0.41	1	0	1	0	0	0	2.06
0	0	1	0	0	1	0.46	1	0	1	0	0	1	2.11
0	0	1	0	1	0	0.52	1	0	1	0	1	0	2.17
0	0	1	0	1	1	0.57	1	0	1	0	1	1	2.22
0	0	1	1	0	0	0.62	1	0	1	1	0	0	2.27
0	0	1	1	0	1	0.67	1	0	1	1	0	1	2.32
0	0	1	1	1	0	0.72	1	0	1	1	1	0	2.37
0	0	1	1	1	1	0.77	1	0	1	1	1	1	2.42
0	1	0	0	0	0	0.83	1	1	0	0	0	0	2.48
0	1	0	0	0	1	0.88	1	1	0	0	0	1	2.53
0	1	0	0	1	0	0.93	1	1	0	0	1	0	2.58
0	1	0	0	1	1	0.98	1	1	0	0	1	1	2.63
0	1	0	1	0	0	1.03	1	1	0	1	0	0	2.68
0	1	0	1	0	1	1.08	1	1	0	1	0	1	2.73
0	1	0	1	1	0	1.13	1	1	0	1	1	0	2.78
0	1	0	1	1	1	1.19	1	1	0	1	1	1	2.84
0	1	1	0	0	0	1.24	1	1	1	0	0	0	2.89
0	1	1	0	0	1	1.29	1	1	1	0	0	1	2.94
0	1	1	0	1	0	1.34	1	1	1	0	1	0	2.99

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	OUTPUT VOLTAGE
0	1	1	0	1	1	1.39	1	1	1	0	1	1	3.04
0	1	1	1	0	0	1.44	1	1	1	1	0	0	3.09
0	1	1	1	0	1	1.50	1	1	1	1	0	1	3.15
0	1	1	1	1	0	1.55	1	1	1	1	1	0	3.20
0	1	1	1	1	1	1.60	1	1	1	1	1	1	3.25

Table 7.4 .

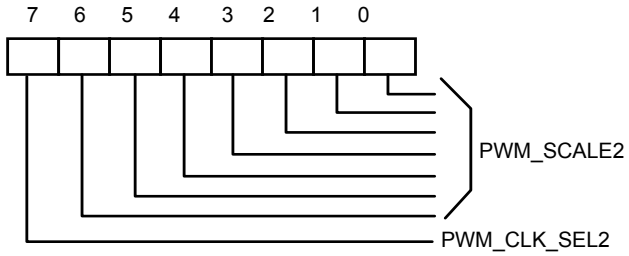
7.9.5 CPUFANOUT0 PWM Output Frequency Configuration Register - Index 02h (*Bank 0*)

Register Location: 02h

Power on Default Value: 04h

Attribute: Read/Write

Size: 8 bits



The register is meaningful when CPUFANOUT0 be programmed as PWM output.

Bit 7: CPUFANOUT0 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-0: CPUFANOUT0 PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1

02h : divider is 2

03h : divider is 3

:

:

the formula is PWM output frequency = $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$

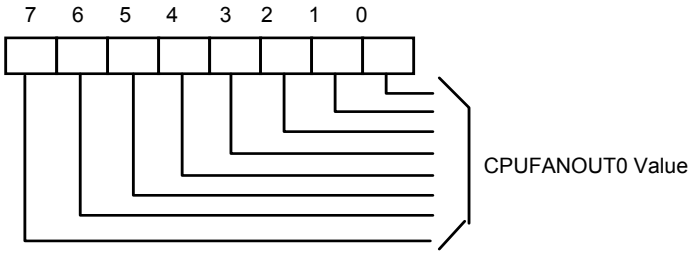
7.9.6 CPUFANOUT0 Output Value Select Register - Index 03h (*Bank 0*)

Register Location: 03h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



(1)If CPUFANOUT0 be programmed as PWM output (Bank0 Index 04h.bit1 is 0)

Bit 7-0: CPUFANOUT0 PWM Duty Cycle. Write FFh, CPUFANOUT0 duty cycle is 100%. Write 00h, CPUFANOUT duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If CPUFANOUT0 be programmed as DC Voltage output (Bank0 Index 04h.bit1 is 1)

Bit 7-2: CPUFANOUT0 voltage control.

Bit 1-0: Reserved.

OUTPUT Voltage = $AVCC * \frac{FANOUT}{64}$

Note. See the Table 7.4

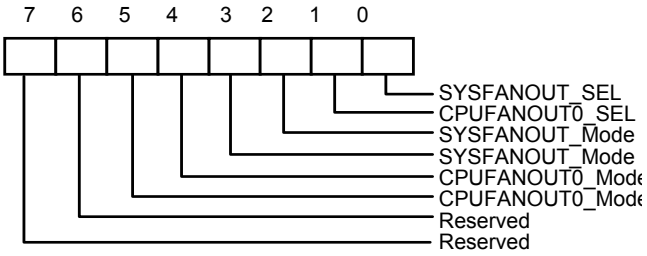
7.9.7 FAN Configuration Register I - Index 04h (*Bank 0*)

Register Location: 04h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved

Bit 5-4: CPUFANOUT0 mode control.

Set 00, CPUFANOUT0 is as Manual Mode. (Default).

Set 01, CPUFANOUT0 is as Thermal Cruise Mode.

Set 10, CPUFANOUT0 is as Fan Speed Cruise Mode.

Set 11, CPUFANOUT0 is as SMART FAN™ III Mode

Bit 3-2: SYSFANOUT mode control.

Set 00, SYSFANOUT is as Manual Mode. (Default).

Set 01, SYSFANOUT is as Thermal Cruise Mode.

Set 10, SYSFANOUT is as Fan Speed Cruise Mode.

Set 11, Reserved and no function.

Bit 1: CPUFANOUT0 output mode selection. Set to 0, CPUFANOUT0 pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, CPUFANOUT0 pin is as DC voltage output which can provide analog voltage output. (Default 0)

Bit 0: SYSFANOUT output mode selection. Set to 0, SYSFANOUT pin is as PWM duty cycle output so that it can drive a logical high or low signal. Set to 1, SYSFANOUT pin is as DC voltage output which can provide analog voltage output. (Default 1)

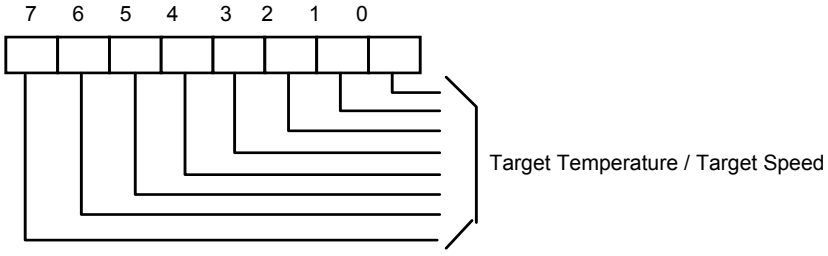
7.9.8 SYSTIN Target Temperature Register/ SYSFANIN Target Speed Register - Index 05h (*Bank 0*)

Register Location: 05h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode:

Bit 7: Reserved.

Bit 6-0: SYSTIN Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit 7-0: SYSFANIN Target Speed.

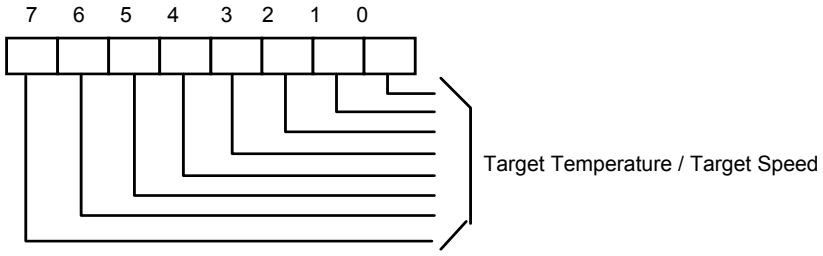
7.9.9 CPUTIN Target Temperature Register/ CPUFANIN0 Target Speed Register - Index 06h (*Bank 0*)

Register Location: 06h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode or SMARTFAN III mode:

Bit 7: Reserved.

Bit 6-0: CPUTIN Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit 7-0: CPUFANIN0 Target Speed.

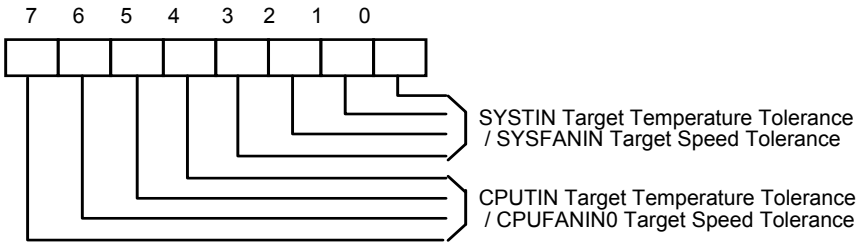
7.9.10 Tolerance of Target Temperature or Target Speed Register - Index 07h (*Bank 0*)

Register Location: 07h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode or SMARTFAN III mode:

Bit 7-4: Tolerance of CPUTIN Target Temperature.

Bit 3-0: Tolerance of SYSTIN Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit 7-4: Tolerance of CPUFANIN0 Target Speed.

Bit 3-0: Tolerance of SYSFANIN Target Speed.

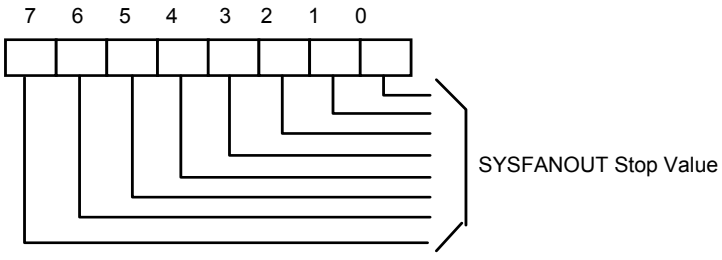
7.9.11 SYSFANOUT Stop Value Register - Index 08h (*Bank 0*)

Register Location: 08h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, SYSFANOUT value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

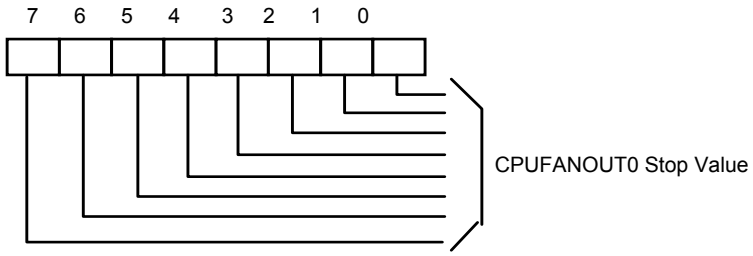
7.9.12 CPUFANOUT0 Stop Value Register - Index 09h (*Bank 0*)

Register Location: 09h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode or SMARTFAN III mode, CPUFANOUT0 value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

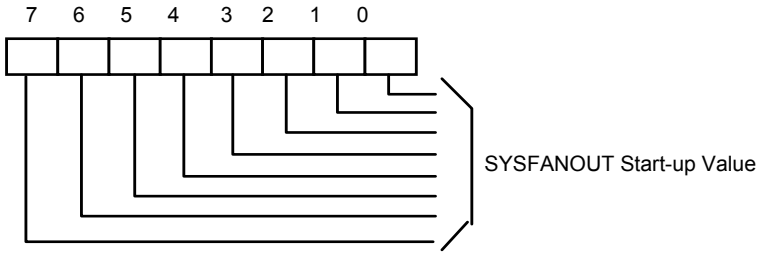
7.9.13 SYSFANOUT Start-up Value Register - Index 0Ah (*Bank 0*)

Register Location: 0Ah

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, SYSFANOUT value will increase from 0 to this register value to provide a minimum value to turn on the fan.

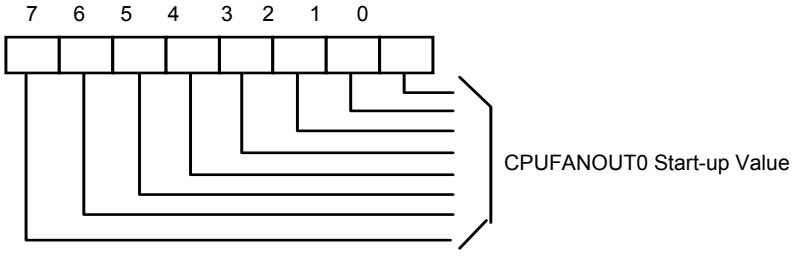
7.9.14 CPUFANOUT0 Start-up Value Register - Index 0Bh (*Bank 0*)

Register Location: 0Bh

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, CPUFANOUT0 value will increase from 0 to this register value to provide a minimum value to turn on the fan.

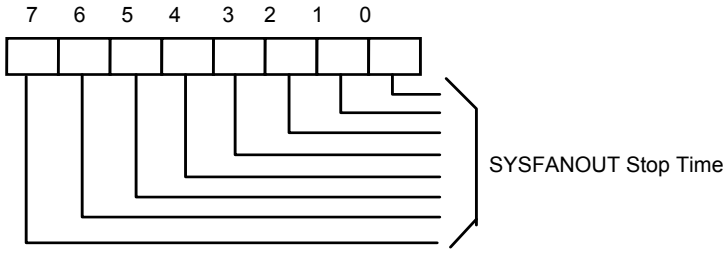
7.9.15 SYSFANOUT Stop Time Register - Index 0Ch (*Bank 0*)

Register Location: 0Ch

Power on Default Value: 3Ch

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, this register determines the time of which SYSFANOUT value is from stop value to 0.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

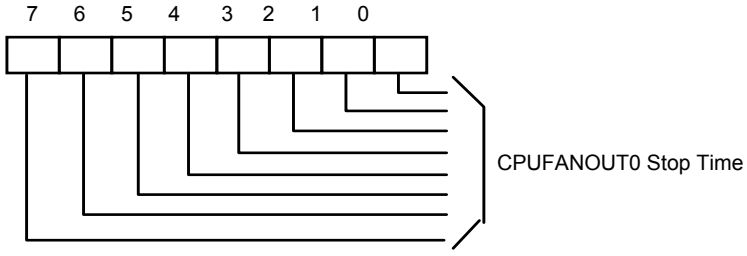
7.9.16 CPUFANOUT0 Stop Time Register - Index 0Dh (*Bank 0*)

Register Location: 0Dh

Power on Default Value: 3Ch

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode or SMARTFAN III mode, this register determines the time of which CPUFANOUT0 value is from stop value to 0.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

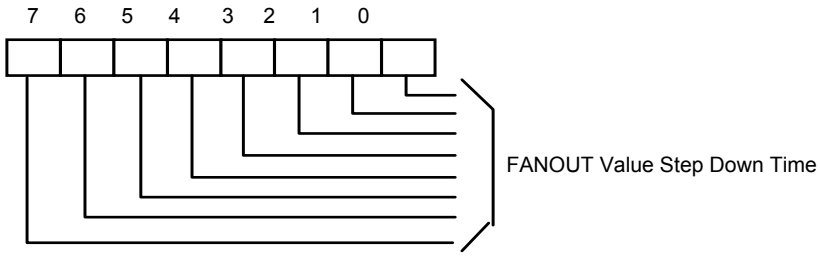
7.9.17 Fan Output Step Down Time Register - Index 0Eh (*Bank 0*)

Register Location: 0Eh

Power on Default Value: 0Ah

Attribute: Read/Write

Size: 8 bits



This register determines the speed of FANOUT decreasing its value in Smart Fan Control mode.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 1 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 4 seconds.

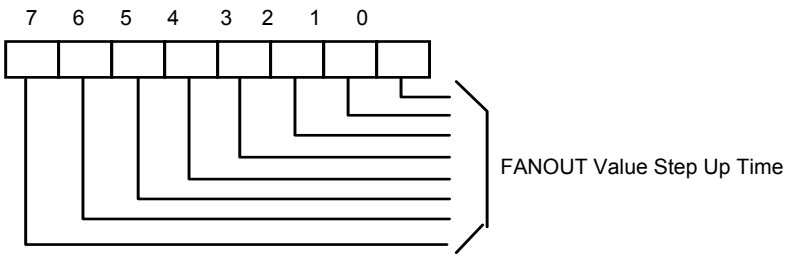
7.9.18 Fan Output Step Up Time Register - Index 0Fh (*Bank 0*)

Register Location: 0Fh

Power on Default Value: 0Ah

Attribute: Read/Write

Size: 8 bits



This register determines the speed of FANOUT increasing the its value in Smart Fan Control mode.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 1 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 4 seconds.

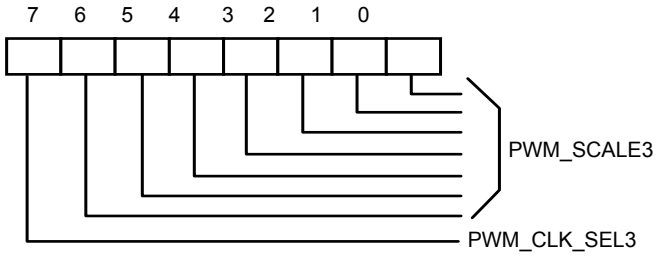
7.9.19 AUXFANOUT PWM Output Frequency Configuration Register - Index 10h (*Bank 0*)

Register Location: 10h

Power on Default Value: 04h

Attribute: Read/Write

Size: 8 bits



The register is meaningful when AUXFANOUT be programmed as PWM output.

Bit 7: AUXFANOUT PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-0: AUXFANOUT PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1

02h : divider is 2

03h : divider is 3

:

:

the formula is **PWM output frequency =** $\frac{\text{Input Clock}}{\text{Pre\_Scale Divider}} * \frac{1}{256}$

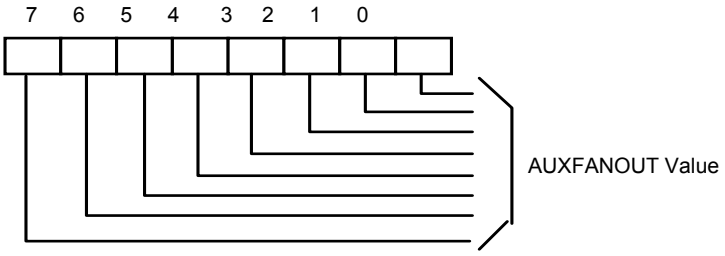
7.9.20 AUXFANOUT Output Value Select Register - Index 11h (*Bank 0*)

Register Location: 11h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



(1)If AUXFANOUT be programmed as PWM output (Bank0 Index 12h.bit0 is 0)

Bit 7-0: AUXFANOUT PWM Duty Cycle. Write FFh, AUXFANOUT duty cycle is 100%. Write 00h, AUXFANOUT duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If AUXFANOUT be programmed as DC Voltage output (Bank0 Index 12h.bit0 is 1)

Bit 7-2: AUXFANOUT voltage control.

Bit 1-0: Reserved.

OUTPUT Voltage = $AVCC * \frac{FANOUT}{16}$

Note. See the Table 7.4

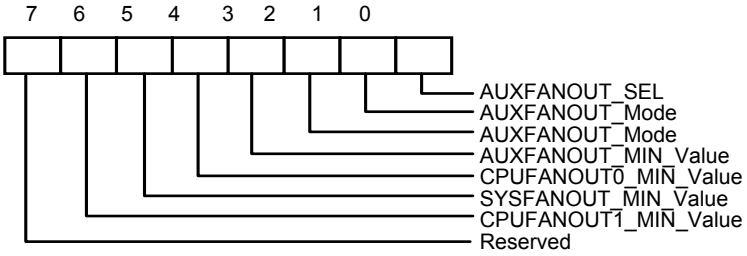
7.9.21 FAN Configuration Register II - Index 12h (*Bank 0*)

Register Location: 12h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved

Bit 6: Set 1, CPUFANOUT1 value will decrease to and keep the value set in Index 64h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, CPUFANOUT1 value will decrease to 0 when temperature goes below target range.

Bit 5: Set 1, SYSFANOUT value will decrease to and keep the value set in Index 08h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, SYSFANOUT value will decrease to 0 when temperature goes below target range.

Bit 4: Set 1, CPUFANOUT0 value will decrease to and keep the value set in Index 09h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, CPUFANOUT0 value will decrease to 0 when temperature goes below target range.

Bit 3: Set 1, AUXFANOUT value will decrease to and keep the value set in Index 17h when temperature goes below target range. This is to maintain the fan speed in a minimum value.

Set 0, AUXFANOUT value will decrease to 0 when temperature goes below target range.

Bit 2-1: AUXFANOUT mode control.

Set 00, AUXFANOUT is as Manual Mode. (Default).

Set 01, AUXFANOUT is as Thermal Cruise Mode.

Set 10, AUXFANOUT is as Fan Speed Cruise Mode.

Set 11, reserved and no function.

Bit 0: AUXFANOUT output mode selection. Set to 0, AUXFANOUT pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, AUXFANOUT pin is as DC voltage output which can provide analog voltage output. (Default 0)

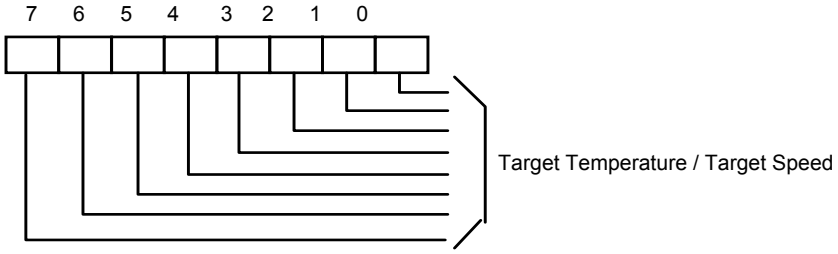
7.9.22 AUXTIN Target Temperature Register/ AUXFANIN0 Target Speed Register - Index 13h (*Bank 0*)

Register Location: 13h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode:

Bit 7: Reserved.

Bit 6-0: AUXTIN Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit 7-0: AUXFANIN0 Target Speed.

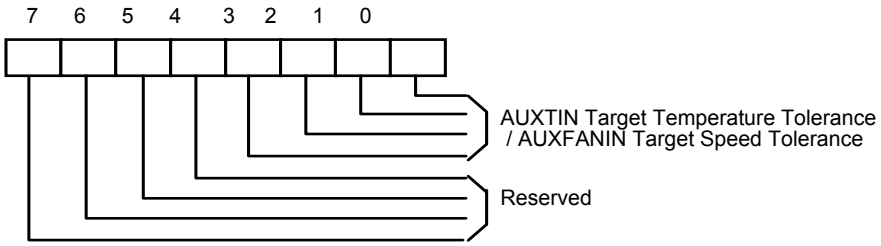
7.9.23 Tolerance of Target Temperature or Target Speed Register - Index 14h (*Bank 0*)

Register Location: 14h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode:

Bit 3-0: Tolerance of AUXTIN Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit 3-0: Tolerance of AUXFANIN0 Target Speed.

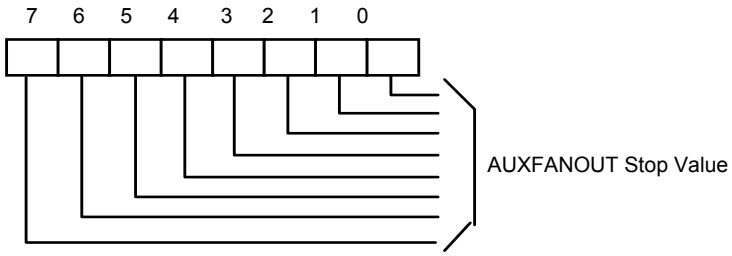
7.9.24 AUXFANOUT Stop Value Register - Index 15h (*Bank 0*)

Register Location: 15h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, AUXFANOUT value will decrease to this value. This register should be written a non-zero minimum output value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

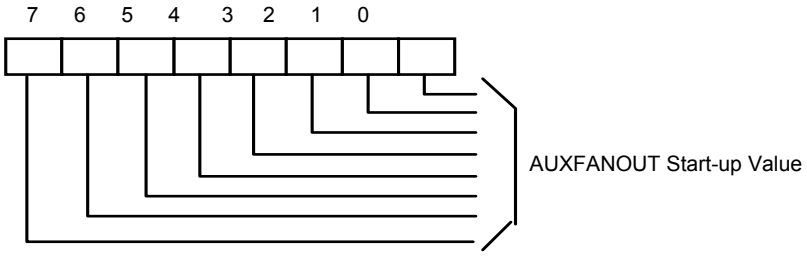
7.9.25 AUXFANOUT Start-up Value Register - Index 16h (*Bank 0*)

Register Location: 16h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, AUXFANOUT value will increase from 0 to this register value to provide a minimum value to turn on the fan.

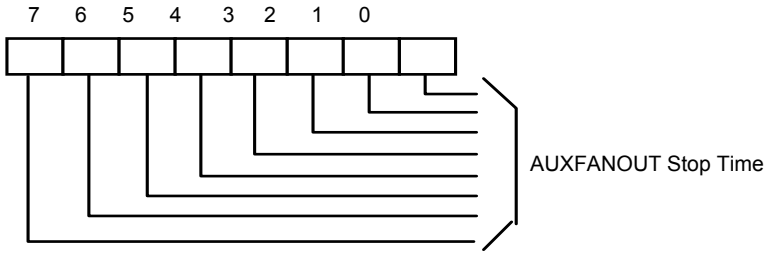
7.9.26 AUXFANOUT Stop Time Register - Index 17h (*Bank 0*)

Register Location: 17h

Power on Default Value: 3Ch

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, this register determines the time of which AUXFANOUT value is from stop value to 0.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

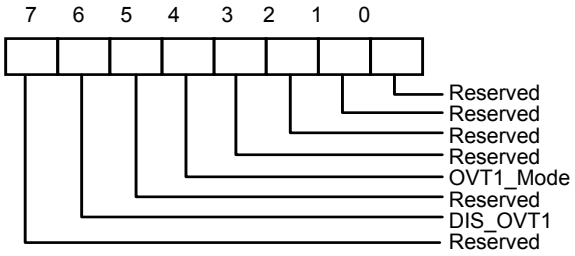
7.9.27 OVT# Configuration Register - Index 18h (*Bank 0*)

Register Location: 18h

Power on Default Value: 43h

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved.

Bit 6: Set to 1, disable temperature sensor SYSTIN over-temperature (OVT#) output. Set to 0, enable the SYSTIN OVT# output.

Bit 5: Reserved.

Bit 4: SYSTIN OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 3-1: Reserved.

Bit 0: Reserved.

7.9.28 Reserved - Index 19h-1Fh (*Bank 0*)

7.9.29 Value RAM — Index 20h- 3Fh (*Bank 0*)

ADDRESS A6-A0	DESCRIPTION
20h	CPUVCORE reading
21h	VIN0 reading
22h	AVCC reading
23h	3VCC reading
24h	VIN1 reading
25h	VIN2 reading
26h	VIN3 reading
27h	SYSTIN temperature sensor reading

ADDRESS A6-A0	DESCRIPTION
28h	SYSFANIN reading Note: This location stores the number of counts of the internal clock per revolution.
29h	CPUFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Ah	AUXFANIN0 reading Note: This location stores the number of counts of the internal clock per revolution.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN0 High Limit
2Eh	VIN0 Low Limit
2Fh	AVCC High Limit
30h	AVCC Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN1 High Limit
34h	VIN1 Low Limit
35h	VIN2 High Limit
36h	VIN2 Low Limit
37h	VIN3 High Limit
38h	VIN3 Low Limit

ADDRESS A6-A0	DESCRIPTION
39h	SYSTIN temperature sensor High Limit
3Ah	SYSTIN temperature sensor Hysteresis Limit
3Bh	SYSFANIN Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Ch	CPUFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Dh	AUXFANIN0 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Eh	CPUFANIN1 Fan Count Limit **Note:** It is the number of counts of the internal clock for the Low Limit of the fan speed.
3Fh	CPUFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.

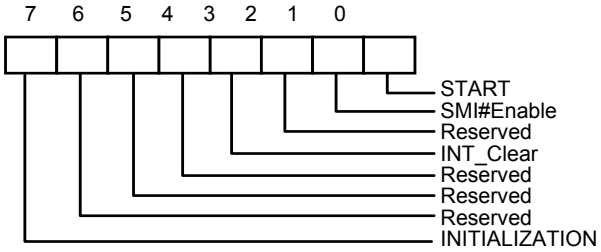
7.9.30 Configuration Register - Index 40h (*Bank 0*)

Register Location: 40h

Power on Default Value: 03h

Attribute: Read/Write

Size: 8 bits



Bit 7: A one restores power on default value to some registers. This bit clears itself since the power on default is zero.

Bit 6: Reserved

Bit 5: Reserved

Bit 4: Reserved

Bit 3: A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.

Bit 2: Reserved

Bit 1: A one enables the SMI# Interrupt output.

Bit 0: A one enables startup of monitoring operations, a zero puts the part in standby mode.

Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

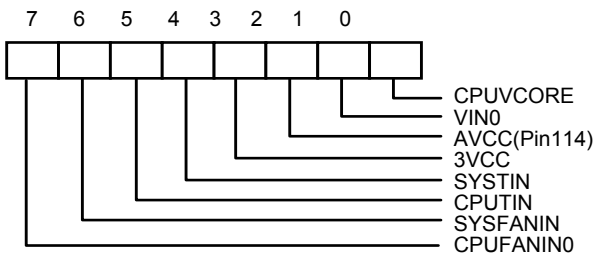
7.9.31 Interrupt Status Register 1 - Index 41h (*Bank 0*)

Register Location: 41h

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7: A one indicates the fan count limit of CPUFANIN0 has been exceeded.

Bit 6: A one indicates the fan count limit of SYSFANIN has been exceeded.

Bit 5: A one indicates a High limit of CPUTIN temperature has been exceeded.

Bit 4: A one indicates a High limit of SYSTIN temperature has been exceeded.

Bit 3: A one indicates a High or Low limit of 3VCC has been exceeded.

Bit 2: A one indicates a High or Low limit of AVCC has been exceeded.

Bit 1: A one indicates a High or Low limit of VIN0 has been exceeded.

Bit 0: A one indicates a High or Low limit of CPUVCORE has been exceeded.

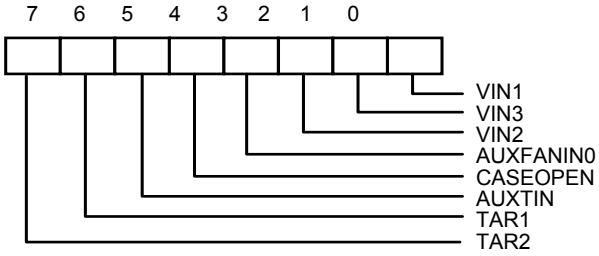
7.9.32 Interrupt Status Register 2 - Index 42h (*Bank 0*)

Register Location: 42h

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7: A one indicates that the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 6: A one indicates that the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™.

Bit 5: A one indicates a High limit of AUXTIN temperature has been exceeded.

Bit 4: A one indicates case has been opened.

Bit 3: A one indicates the fan count limit of AUXFANIN0 has been exceeded.

Bit 2: A one indicates a High or Low limit of VIN2 has been exceeded.

Bit 1: A one indicates a High or Low limit of VIN3 has been exceeded.

Bit 0: A one indicates a High or Low limit of VIN1 has been exceeded.

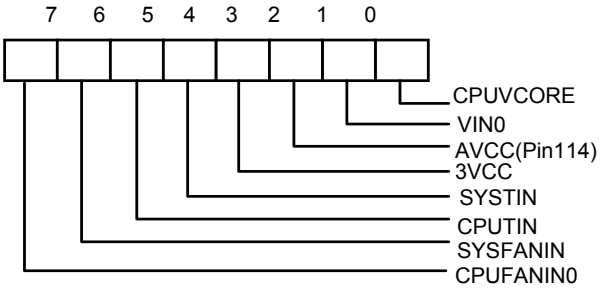
7.9.33 SMI# Mask Register 1 - Index 43h (*Bank 0*)

Register Location: 43h

Power on Default Value: DEh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

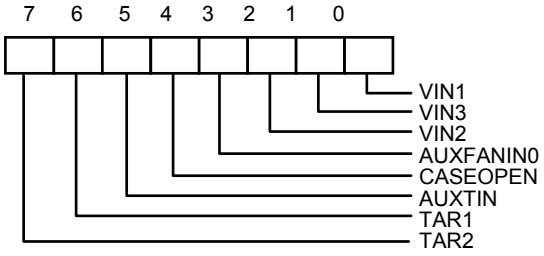
7.9.34 SMI# Mask Register 2 - Index 44h (*Bank 0*)

Register Location: 44h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

7.9.35 Reserved Register - Index 45h (*Bank 0*)

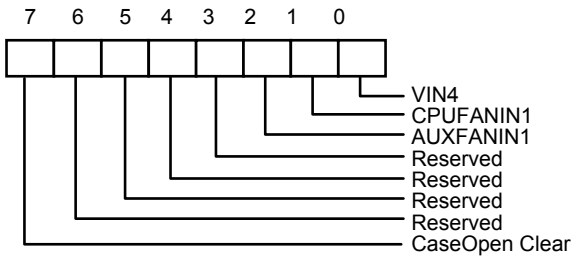
7.9.36 SMI# Mask Register 3 - Index 46h (*Bank 0*)

Register Location: 46h

Power on Default Value: 07h

Attribute: Read/Write

Size: 8 bits



Bit 7: CASEOPEN Clear Control. Write 1 to this bit will clear CASEOPEN status. This bit won't be self cleared, please write 0 after event be cleared. The function is as same as LDA, CR[E6h] bit 5.

Bit 6-3: Reserved.

Bit 2-0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

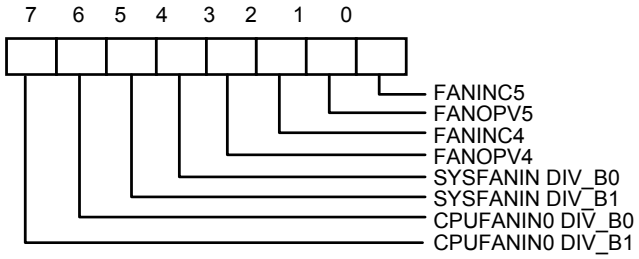
7.9.37 Fan Divisor Register I - Index 47h (*Bank 0*)

Register Location: 47h

Power on Default Value: 55h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: CPUFANIN0 Divisor bit1:0.

Bit 5-4: SYSFANIN Divisor bit1:0.

Bit 3: CPUFANIN1 output value if bit 0 sets to 0. Write 1, pin119(CPUFANIN1) always generates a logic high signal. Write 0, pin119 always generates a logic low signal. This bit is default 0.

Bit 2: CPUFANIN1 Input Control. Set to 1, pin119 (CPUFANIN1) acts as FAN tachometer input, which is default value. Set to 0, this pin119 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

Bit 1: AUXFANIN1 output value if bit 0 sets to 0. Write 1, pin58(AUXFANIN1) always generates a logic high signal. Write 0, pin58 always generates a logic low signal. This bit is default 0.

Bit 0: AUXFANIN1 Input Control. Set to 1, pin58 (AUXFANIN1) acts as FAN tachometer input, which is default value. Set to 0, this pin58 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

Note : Please refer to Bank0 Index 5Dh , Fan divisor table.

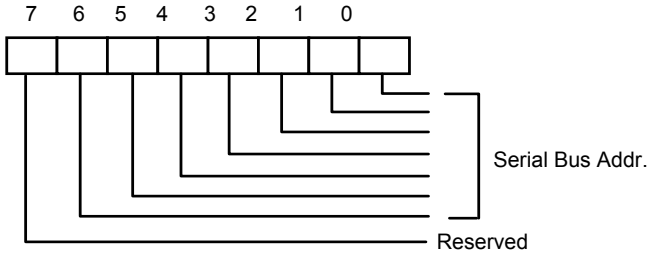
7.9.38 Serial Bus Address Register - Index 48h (*Bank 0*)

Register Location: 48h

Power on Default Value: 2Dh

Attribute: Read/Write

Size: 8 bits



Bit 7: Reserved (Read Only).

Bit 6-0: Serial Bus address <7:1>.

7.9.39 Reserved - Index 49h (*Bank 0*)

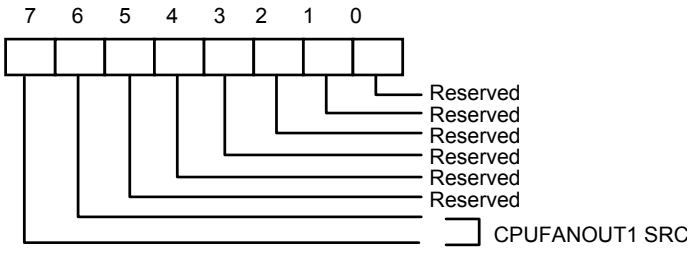
7.9.40 CPUFANOUT1 with Temperature source Select - Index 4Ah (*Bank 0*)

Register Location: 4Ah

Power on Default Value: 64h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Select Temperature source for CPUFANOUT1 at Thermal Cruise mode or SMART FAN™ III Mode

<7:6> = 00 – SYSTIN.

<7:6> = 01 - CPUTIN.(Default)

<7:6> = 10 - AUXTIN.

<7:6> = 11 – Reserved.

Bit 5-0: Reserved.

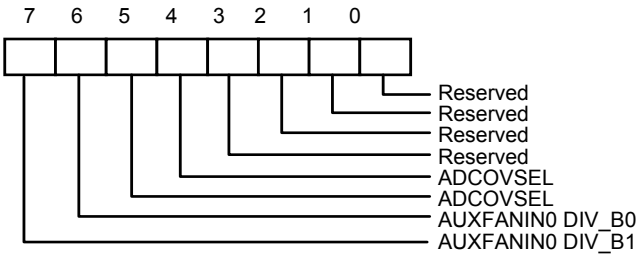
7.9.41 Fan Divisor Register II - Index 4Bh (*Bank 0*)

Register Location: 4Bh

Power on Default Value: 44h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: AUXFANIN0 Divisor bit1:0.

Note : Please refer to Bank0 Index 5Dh , Fan divisor table.

Bit 5-4: Select A/D Converter Clock Input.

<5:4> = 00 - default. ADC clock select 22.5 Khz.

<5:4> = 01- ADC clock select 5.6 Khz. (22.5K/4)

<5:4> = 10 - ADC clock select 1.4Khz. (22.5K/16)

<5:4> = 11 - ADC clock select 0.35 Khz. (22.5K/64)

Bit 3-2: These two bits should be set to 01h. The default value is 01h.

Bit 1-0: Reserved.

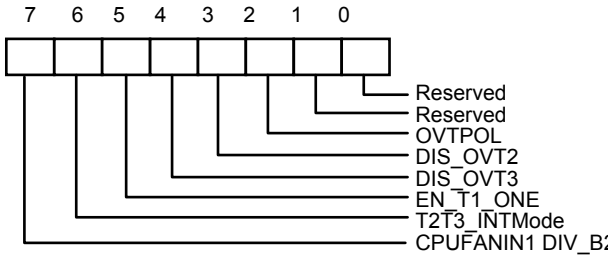
7.9.42 SMI#/OVT# Control Register - Index 4Ch (*Bank 0*)

Register Location: 4Ch

Power on Default Value: 10h

Attribute: Read/Write

Size: 8 bits



Bit 7: CPUFANIN1 Divisor bit2.

Bit 6: Set to 1, the SMI# output type of Temperature CPUTIN/AUXTIN is set to Comparator Interrupt mode. Set to 0, the SMI# output type is set to Two-Times Interrupt mode. (Default 0)

Bit 5: Set to 1, the SMI# output type of temperature SYSTIN is One-Time interrupt mode. Set to 0, the SMI# output type is Two-Times interrupt mode.

Bit 4: Disable temperature sensor AUXTIN over-temperature (OVT) output if set to 1. Set to 0, enable AUXTIN OVT output through pin OVT#. (Default 1)

Bit 3: Disable temperature sensor CPUTIN over-temperature (OVT) output if set to 1. Set to 0, enable CPUTIN OVT output through pin OVT#. (Default 0)

Bit 2: Over-temperature polarity. Write 1, OVT# active high. Write 0, OVT# active low. (Default 0)

Bit 1-0: Reserved.

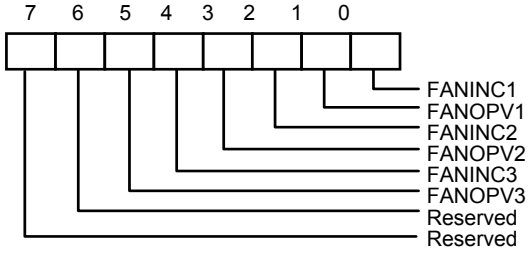
7.9.43 FAN IN/OUT Control Register - Index 4Dh (*Bank 0*)

Register Location: 4Dh

Power on Default Value: 15h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: AUXFANIN0 output value if bit 4 sets to 0. Write 1, pin111(AUXFANIN0) always generates a logic high signal. Write 0, pin111 always generates a logic low signal. This bit is default 0.

Bit 4: AUXFANIN0 Input Control. Set to 1, pin111(AUXFANIN0) acts as FAN tachometer input, which is default value. Set to 0, this pin111 acts as FAN control signal and the output value of FAN control is set by this register bit 5.

Bit 3: CPUFANIN0 output value if bit 2 sets to 0. Write 1, pin112(CPUFANIN0) always generates a logic high signal. Write 0, pin112 always generates a logic low signal. This bit is default 0.

Bit 2: CPUFANIN0 Input Control. Set to 1, pin112(CPUFANIN0) acts as FAN tachometer input, which is default value. Set to 0, this pin112 acts as FAN control signal and the output value of FAN control is set by this register bit 3.

Bit 1: SYSFANIN output value if bit 0 sets to 0. Write 1, pin113(SYSFANIN) always generates a logic high signal. Write 0, pin113 always generates a logic low signal. This bit is default 0.

Bit 0: SYSFANIN Input Control. Set to 1, pin113(SYSFANIN) acts as FAN tachometer input, which is default value. Set to 0, this pin113 acts as FAN control signal and the output value of FAN control is set by this register bit 1.

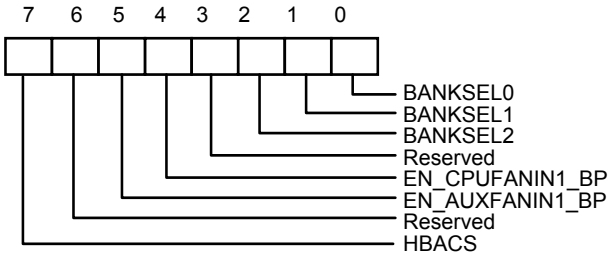
7.9.44 Register 50h ~ 5Fh Bank Select Register - Index 4Eh (*Bank 0*)

Register Location: 4Eh

Power on Default Value: 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: HBACS - High byte access. Set to 1, access Index 4Fh high byte register.

Set to 0, access Index 4Fh low byte register. (default 1)

Bit 6: Reserved. This bit should be set to 0.

Bit 5: BEEP output control for AUXFANIN1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for CPUFANIN1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: Reserved. This bit should be set to 0.

Bit 2-0: Index ports 0x50~0x5F Bank select.

Set to 0, select Bank0.

Set to 1, select Bank1.

Set to 2, select Bank2.

Set to 3, select Bank3.

Set to 4, select Bank4.

Set to 5, select Bank5.

Set to 6, select Bank6.

Set to 7, select Bank7.

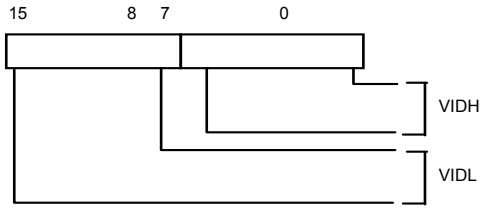
7.9.45 Nuvoton Vendor ID Register - Index 4Fh (*Bank 0*)

Register Location: 4Fh

Power on Default Value: <15:0> = 5CA3h

Attribute: Read Only

Size: 16 bits



Bit 15-8: Vendor ID High Byte if Index 4Eh.bit7=1. Default 5Ch.

Bit 7-0: Vendor ID Low Byte if Index 4Eh.bit7=0. Default A3h.

7.9.46 Nuvoton Test Register - Index 50h-55h (Bank 0)

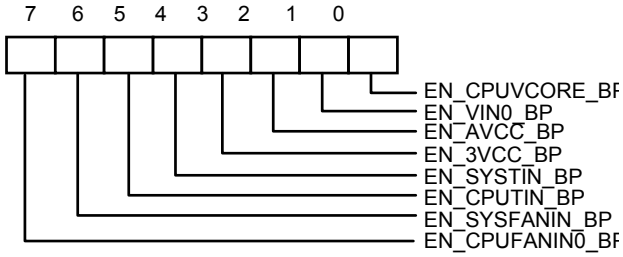
7.9.47 BEEP Control Register 1 - Index 56h (*Bank 0*)

Register Location: 56h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: BEEP output control for CPUFANIN0 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 6: BEEP output control for SYSFANIN if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 5: BEEP output control for temperature CPUTIN if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for temperature SYSTIN if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for 3VCC if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2: BEEP output control for AVCC if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN0 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for CPUVCORE if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

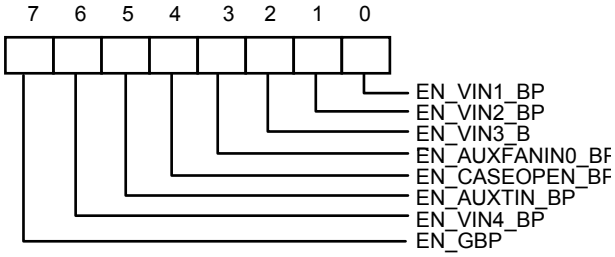
7.9.48 BEEP Control Register 2 - Index 57h (*Bank 0*)

Register Location: 57h

Power on Default Value: 80h

Attribute: Read/Write

Size: 8 bits



Bit 7: Global BEEP Control. Write 1, enable global BEEP output, which is default value. Write 0, disable all BEEP output.

Bit 6: BEEP output control for VIN4 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 5: BEEP output control for temperature AUXTIN if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 4: BEEP output control for CASEOPEN if case has been opened. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 3: BEEP output control for AUXFANIN0 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 2: BEEP output control for VIN3 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 1: BEEP output control for VIN2 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for VIN1 if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

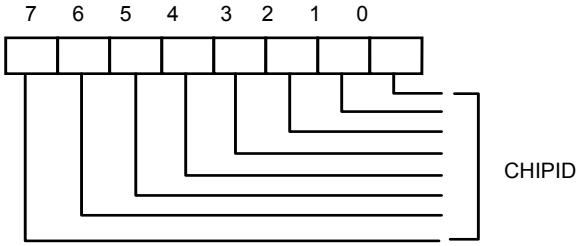
7.9.49 Chip ID - Index 58h (*Bank 0*)

Register Location: 58h

Power on Default Value: A1h

Attribute: Read Only

Size: 8 bits



Bit 7-0: Nuvoton Chip ID number. Read this register will return A1h.

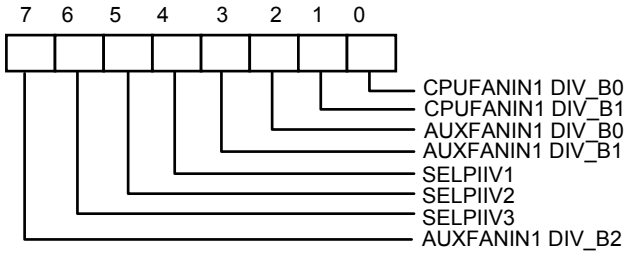
7.9.50 Diode Selection Register - Index 59h (*Bank 0*)

Register Location: 59h

Power on Default Value: 70h

Attribute: Read/Write

Size: 8 bits



Bit 7: AUXFANIN1 Divisor bit2.

Bit 6: Diode mode selection of temperature AUXTIN if Index 5Dh bit3 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

Bit 5: Diode mode selection of temperature CPUTIN if Index 5Dh bit2 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

Bit 4: Diode mode selection of temperature SYSTIN if Index 5Dh bit1 is 1. Set this bit to 1, select Pentium II CPU compatible thermal diode.

Bit 3-2: AUXFANIN1 Divisor bit 1:0.

Bit 1-0: CPUFANIN1 Divisor bit 1:0.

7.9.51 Reserved - Index 5Ah-5Ch (*Bank 0*)

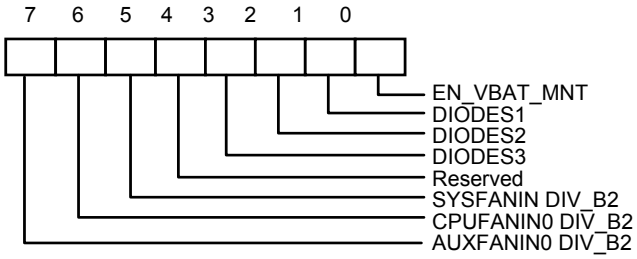
7.9.52 VBAT Monitor Control Register - Index 5Dh (*Bank 0*)

Register Location: 5Dh

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: AUXFANIN0 Divisor bit2.

Bit 6: CPUFANIN0 Divisor bit2.

Bit 5: SYSFANIN Divisor bit2.

Bit 4: Reserved.

Bit 3: Sensor type selection of AUXTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 2: Sensor type selection of CPUTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 1: Sensor type selection of SYSTIN. Set to 1, select diode sensor. Set to 0, select thermistor sensor.

Bit 0: Set to 1, enable battery voltage monitor. Set to 0, disable battery voltage monitor. After set this bit from 0 to 1, the monitored value will be updated to the VBAT reading value register after one monitor cycle time.

Fan divisor table:

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	0	***1***	1	0	0	***16***

BIT 2	BIT 1	BIT 0	FAN DIVISOR	BIT 2	BIT 1	BIT 0	FAN DIVISOR
0	0	1	***2***	1	0	1	***32***
0	1	0	***4***	1	1	0	***64***
0	1	1	***8***	1	1	1	***128***

Table 7.3

7.9.53 Reserved Register - Index 5Eh-5Fh (*Bank 0*)

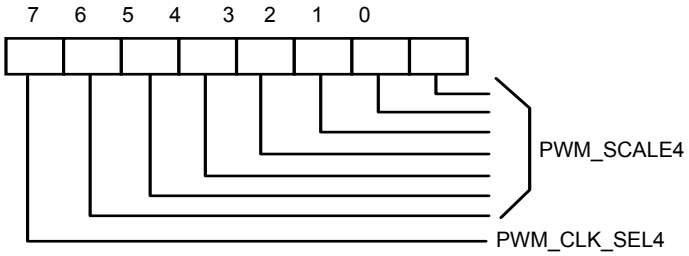
7.9.54 CPUFANOUT1 PWM Output Frequency Configuration Register - Index 60h (*Bank 0*)

Register Location: 60h

Power on Default Value: 04h

Attribute: Read/Write

Size: 8 bits



The register is meaningful when CPUFANOUT1 be programmed as PWM output.

Bit 7: CPUFANOUT1 PWM Input Clock Source Select. This bit selects the clock source of PWM output frequency.

Set to 0, select 24 MHz.

Set to 1, select 180 KHz.

Bit 6-0: CPUFANOUT1 PWM Pre-Scale divider. This is the divider of clock source of PWM output frequency. The maximum divider is 128 (7Fh). This divider should not be set to 0.

01h : divider is 1

02h : divider is 2

03h : divider is 3

:

:

the formula is $$PWM\ output\ frequency = \frac{Input\ Clock}{Pre\_Scale\ Divider} * \frac{1}{256}$$

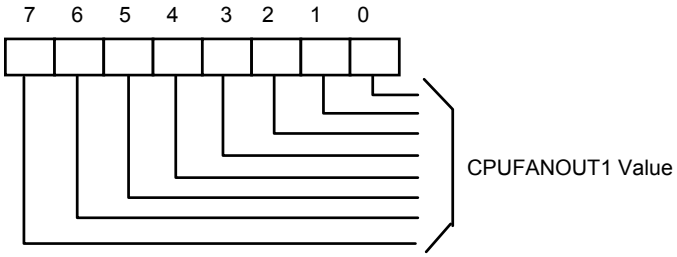
7.9.55 CPUFANOUT1 Output Value Select Register - Index 61h (*Bank 0*)

Register Location: 61h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



(1)If CPUFANOUT1 be programmed as PWM output (Bank0 Index 62h.bit6 is 0)

Bit 7-0: CPUFANOUT1 PWM Duty Cycle. Write FFh, CPUFANOUT1 duty cycle is 100%. Write 00h, CPUFANOUT1 duty cycle is 0%.

Note. XXh: PWM Duty Cycle output percentage is (XX/256*100%) during one cycle.

(2)If CPUFANOUT1 be programmed as DC Voltage output (Bank0 Index 62h.bit6 is 1)

Bit 7-2: CPUFANOUT1 voltage control.

Bit 1-0: Reserved.

OUTPUT Voltage = $$AVCC * \frac{FANOUT}{64}$$

Note. See the Table 7.4

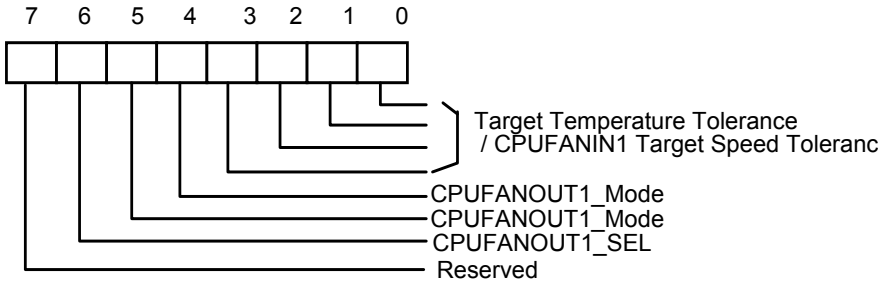
7.9.56 FAN Configuration Register III - Index 62h (*Bank 0*)

Register Location: 62h

Power on Default Value: 40h

Attribute: Read/Write

Size: 8 bits



Bit7: Reserved.

Bit 6: CPUFANOUT1 output mode selection. Set to 0, CPUFANOUT1 pin is as PWM output duty cycle so that it can drive a logical high or low signal. Set to 1, CPUFANOUT1 pin is as DC voltage output which can provide analog voltage output. (Default 1)

Bit 5-4: CPUFANOUT1 mode control.

Set 00, CPUFANOUT1 is as Manual Mode. (Default).

Set 01, CPUFANOUT1 is as Thermal Cruise Mode.

Set 10, CPUFANOUT1 is as Fan Speed Cruise Mode.

Set 11, CPUFANOUT1 is SMART FAN™ III Mode.

(1)When at Thermal Cruise mode or SMART FAN™ III mode:

Bit3-0: Tolerance of select temperature source Target Temperature.

(2)When at Fan Speed Cruise mode:

Bit3-0: Tolerance of CPUFANIN1 Target Speed.

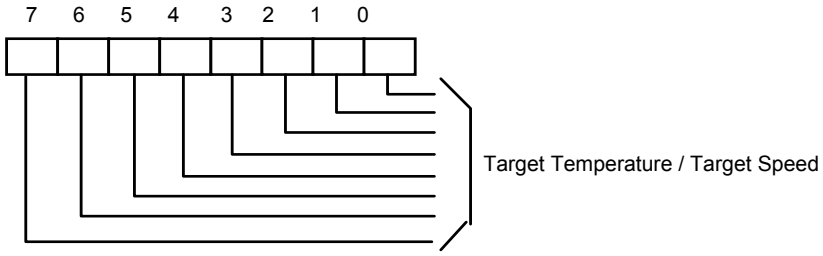
7.9.57 Target Temperature Register/ CPUFANIN1 Target Speed Register - Index 63h (*Bank 0*)

Register Location: 63h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



(1)When at Thermal Cruise mode or SMART FAN™ III mode:

Bit 7: Reserved.

Bit 6-0: Target Temperature of select temperature source.

(2)When at Fan Speed Cruise mode:

Bit 7-0: CPUFANIN1 Target Speed.

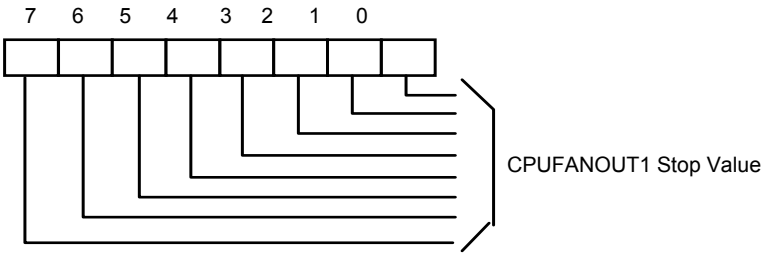
7.9.58 CPUFANOUT1 Stop Value Register - Index 64h (*Bank 0*)

Register Location: 64h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode or SMART FAN™ III mode, CPUFANOUT1 value will decrease to this value. This register should be written a non-zero minimum stop value.

Please note that Stop Value does not mean that fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimam value, and this is Stop Value.

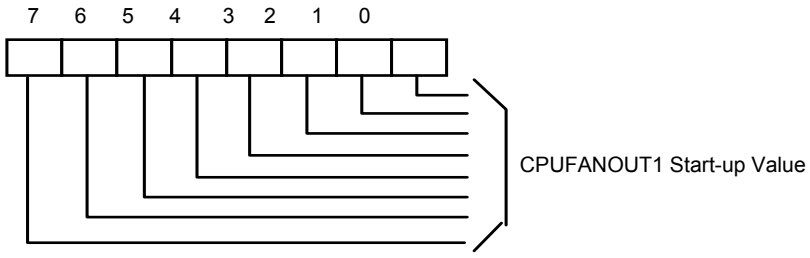
7.9.59 CPUFANOUT1 Start-up Value Register - Index 65h (*Bank 0*)

Register Location: 65h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode, CPUFANOUT1 value will increase from 0 to this register value to provide a minimum value to turn on the fan.

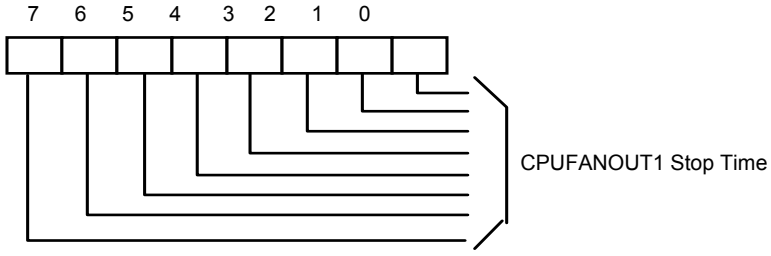
7.9.60 CPUFANOUT1 Stop Time Register - Index 66h (*Bank 0*)

Register Location: 66h

Power on Default Value: 3Ch

Attribute: Read/Write

Size: 8 bits



When at Thermal Cruise mode or SMART FAN™ III mode, this register determines the time of which CPUFANOUT1 value is from stop value to 0.

(1)When at PWM output:

The unit of this register is 0.1 second. The default time is 6 seconds.

(2)When at DC Voltage output:

The unit of this register is 0.4 second. The default time is 24 seconds.

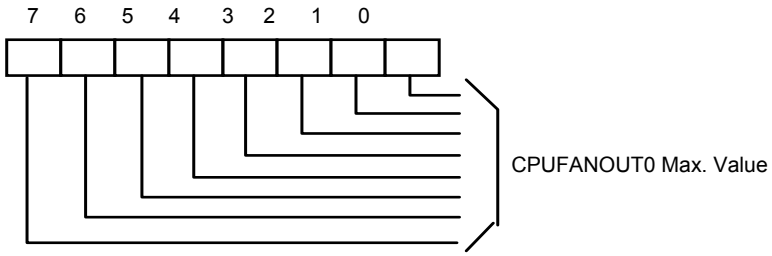
7.9.61 CPUFANOUT0 Maximum Output Value Register - Index 67h (*Bank 0*)

Register Location: 67h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



When at SMART FAN™ III mode, CPUFANOUT0 value will increase to this value. This register should be written a non-zero value that cannot lower than Stop value.

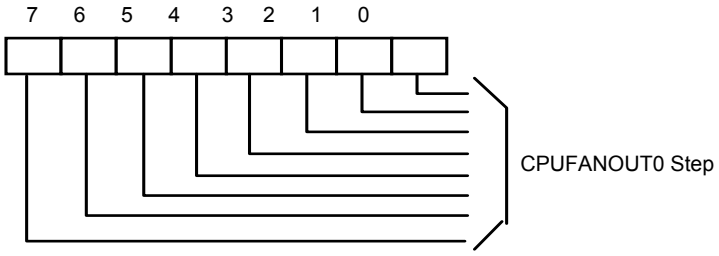
7.9.62 CPUFANOUT0 Output Step Value Register - Index 68h (*Bank 0*)

Register Location: 68h

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



This register determines the value that CPUFANOUT0 in SMART FAN™ III mode decreased or increased to the next speed.

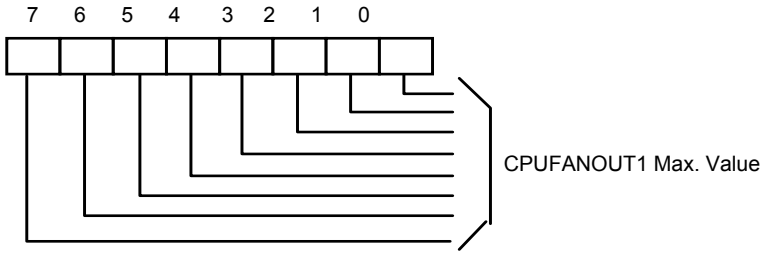
7.9.63 CPUFANOUT1 Maximum Output Value Register - Index 69h (*Bank 0*)

Register Location: 69h

Power on Default Value: FFh

Attribute: Read/Write

Size: 8 bits



When at SMART FAN™ III mode, CPUFANOUT1 value will increase to this value. This register should be written a non-zero value that cannot lower than Stop value.

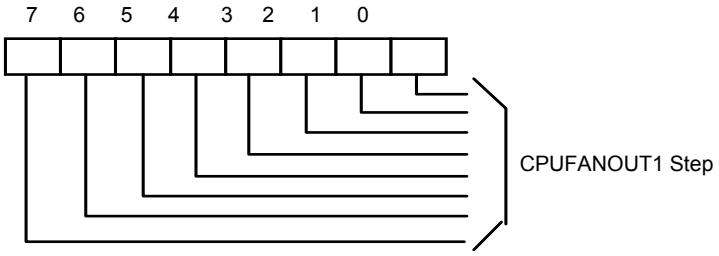
7.9.64 CPUFANOUT1 Output Step Value Register - Index 6Ah (*Bank 0*)

Register Location: 6Ah

Power on Default Value: 01h

Attribute: Read/Write

Size: 8 bits



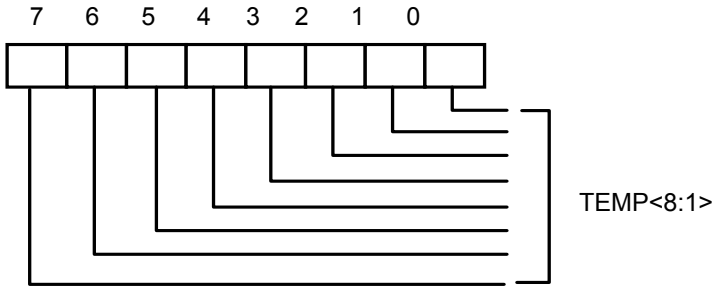
This register determines the value that CPUFANOUT1 in SMART FAN™ III mode decreased or increased to the next speed.

7.9.65 CPUTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (*Bank 1*)

Register Location: 50h

Attribute: Read Only

Size: 8 bits



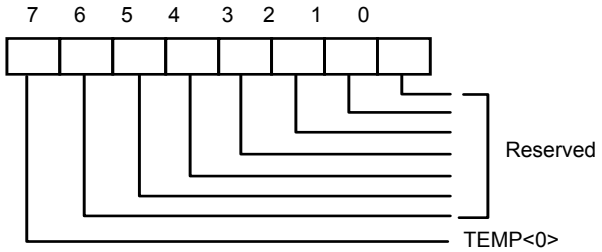
Bit 7-0: Temperature <8:1> of CPUTIN sensor, which is high byte, means 1°C.

7.9.66 CPUTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank 1*)

Register Location: 51h

Attribute: Read Only

Size: 8 bits



Bit 7: Temperature <0> of CPUTIN sensor, which is low byte, means 0.5°C.

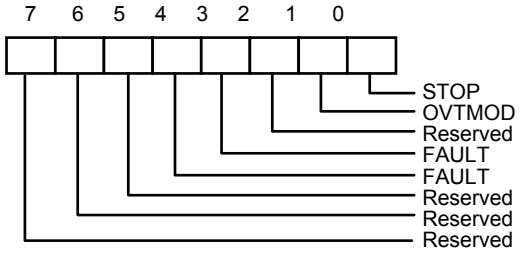
Bit 6-0: Reserved.

7.9.67 CPUTIN Temperature Sensor Configuration Register - Index 52h (*Bank 1*)

Register Location: 52h

Power on Default Value: 00h

Size: 8 bits



Bit 7-5: Read Only - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

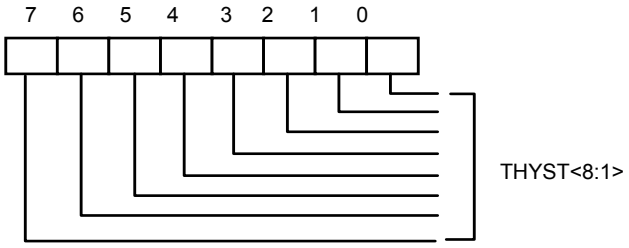
7.9.68 CPUTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 1*)

Register Location: 53h

Power on Default Value: 4Bh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

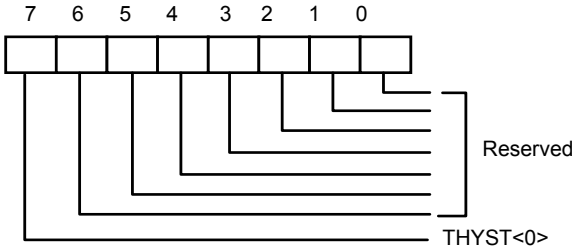
7.9.69 CPUTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 1*)

Register Location: 54h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

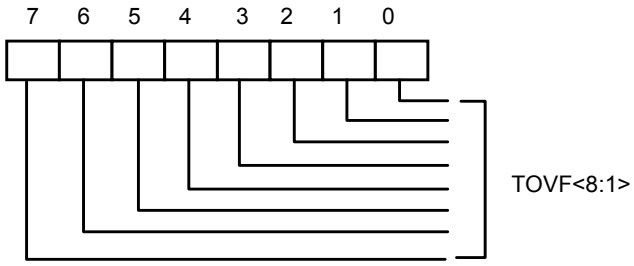
7.9.70 CPUTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (*Bank1*)

Register Location: 55h

Power on Default Value: 50h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

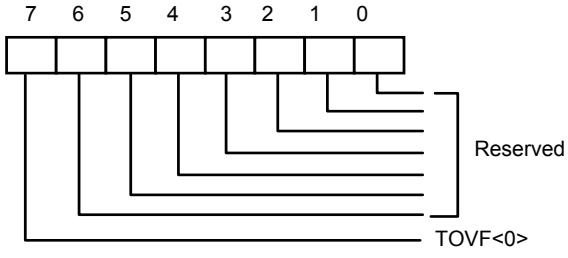
7.9.71 CPUTIN Temperature Sensor Over-temperature (Low Byte) Register - Index 56h (*Bank 1*)

Register Location: 56h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Over-temperature bit 0, which is low Byte.

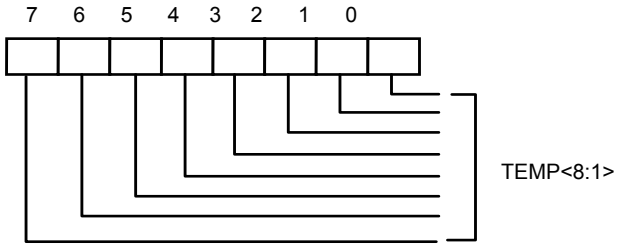
Bit 6-0: Reserved.

7.9.72 AUXTIN Temperature Sensor Temperature (High Byte) Register - Index 50h (*Bank 2*)

Register Location: 50h

Attribute: Read Only

Size: 8 bits



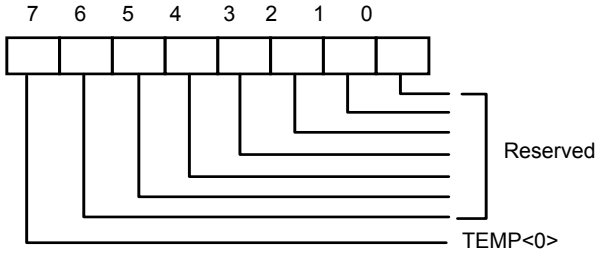
Bit 7: Temperature <8:1> of AUXTIN sensor, which is high byte, means 1°C.

7.9.73 AUXTIN Temperature Sensor Temperature (Low Byte) Register - Index 51h (*Bank 2*)

Register Location: 51h

Attribute: Read Only

Size: 8 bits



Bit 7: Temperature <0> of AUXTIN sensor, which is low byte, means 0.5°C.

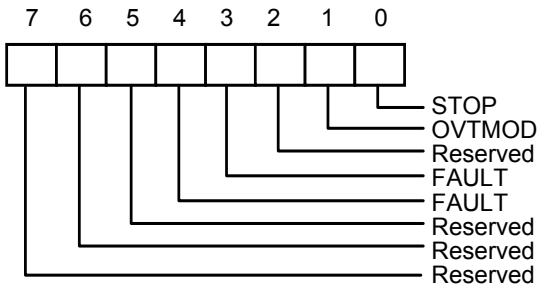
Bit 6-0: Reserved.

7.9.74 AUXTIN Temperature Sensor Configuration Register - Index 52h (*Bank 2*)

Register Location: 52h

Power on Default Value: 00h

Size: 8 bits



Bit 7-5: Read - Reserved. This bit should be set to 0.

Bit 4-3: Read/Write - Number of faults to detect before setting OVT# output to avoid false tripping due to noise.

Bit 2: Read - Reserved. This bit should be set to 0.

Bit 1: Read/Write - OVT# mode select. This bit default is set to 0, which is compared mode. When set to 1, interrupt mode will be selected.

Bit 0: Read/Write - When set to 1 the sensor will stop monitor.

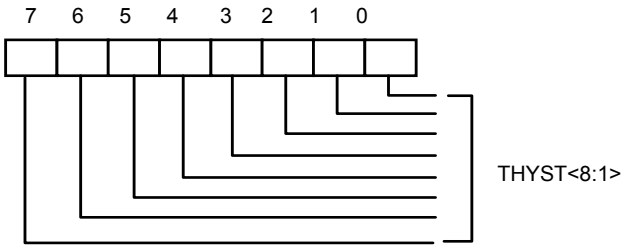
7.9.75 AUXTIN Temperature Sensor Hysteresis (High Byte) Register - Index 53h (*Bank 2*)

Register Location: 53h

Power on Default Value 4Bh

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

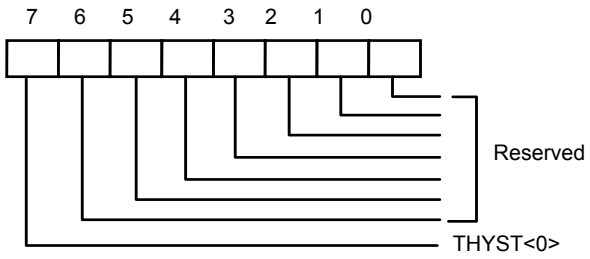
7.9.76 AUXTIN Temperature Sensor Hysteresis (Low Byte) Register - Index 54h (*Bank 2*)

Register Location: 54h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Hysteresis temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

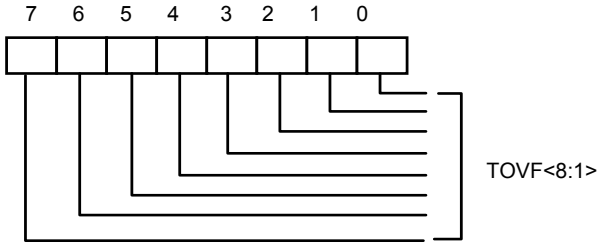
7.9.77 AUXTIN Temperature Sensor Over-temperature (High Byte) Register - Index 55h (*Bank 2*)

Register Location: 55h

Power on Default Value: 50h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

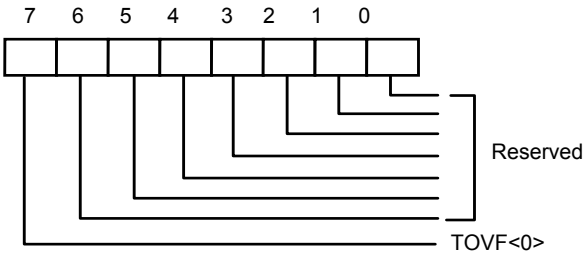
7.9.78 AUXTIN Temperature Sensor Over-temperature(Low Byte) Register - Index 56h (*Bank 2*)

Register Location: 56h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7: Over-temperature bit 0, which is low Byte.

Bit 6-0: Reserved.

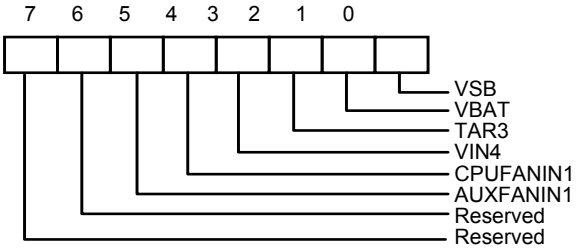
7.9.79 Interrupt Status Register 3 - Index 50h (*Bank 4*)

Register Location: 50h

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: A one indicates the fan count limit of AUXFANIN1 has been exceeded.

Bit 4: A one indicates the fan count limit of CPUFANIN1 has been exceeded.

Bit 3: A one indicates a High or Low limit of VIN4 has been exceeded.

Bit 2: A one indicates that the AUXTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of Smart Fan™.

Bit 1: A one indicates a High or Low limit of VBAT has been exceeded.

Bit 0: A one indicates a High or Low limit of VSB has been exceeded.

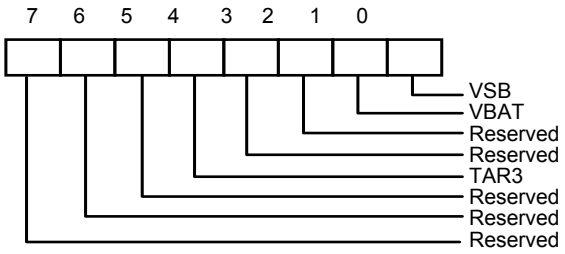
7.9.80 SMI# Mask Register 4 - Index 51h (*Bank 4*)

Register Location: 51h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-5: Reserved.

Bit 4: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 3-2: Reserved.

Bit 1: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

Bit 0: A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.

7.9.81 Reserved Register - Index 52h (*Bank 4*)

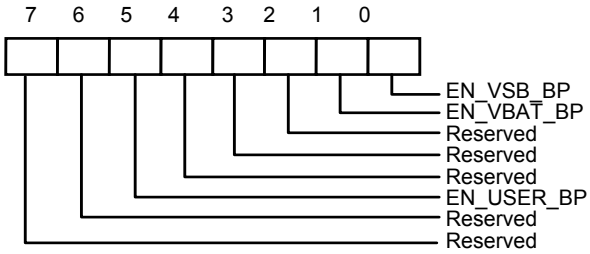
7.9.82 BEEP Control Register 3 - Index 53h (*Bank 4*)

Register Location: 53h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-6: Reserved.

Bit 5: User define BEEP output function. Write 1, the BEEP is always active. Write 0, this function is inactive. (Default 0)

Bit 4-2: Reserved.

Bit 1: BEEP output control for VBAT if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

Bit 0: BEEP output control for VSB if the monitor value exceeds the limit value. Write 1, enable BEEP output. Write 0, disable BEEP output, which is default value.

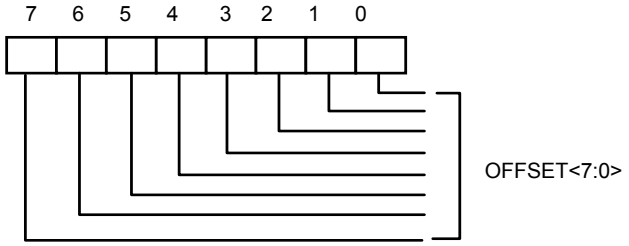
7.9.83 SYSTIN Temperature Sensor Offset Register - Index 54h (*Bank 4*)

Register Location: 54h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: SYSTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

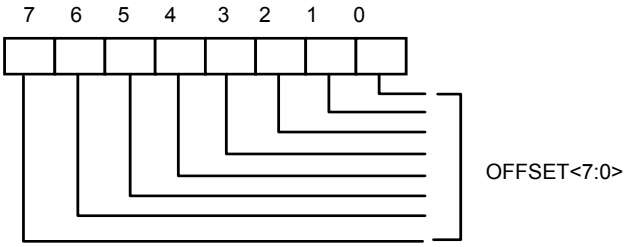
7.9.84 CPUTIN Temperature Sensor Offset Register - Index 55h (*Bank 4*)

Register Location: 55h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: CPUTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

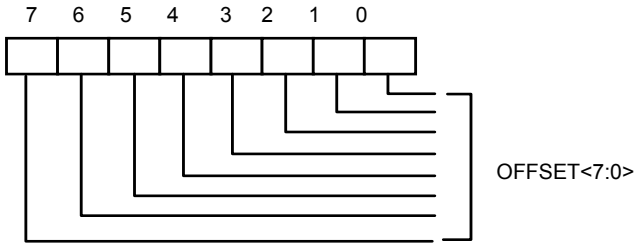
7.9.85 AUXTIN Temperature Sensor Offset Register - Index 56h (*Bank 4*)

Register Location: 56h

Power on Default Value: 00h

Attribute: Read/Write

Size: 8 bits



Bit 7-0: AUXTIN temperature offset value. The value in this register will be added to the monitored value so that the reading value will be the sum of the monitored value and the offset value.

7.9.86 Reserved Register - Index 57h-58h (*Bank 4)*

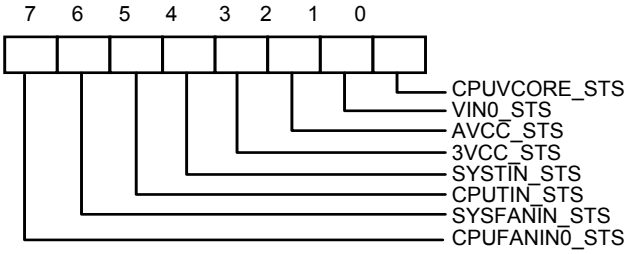
7.9.87 Real Time Hardware Status Register I - Index 59h (*Bank 4*)

Register Location: 59h

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7: CPUFANIN0 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 6: SYSFANIN status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 5: CPUTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 4: SYSTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 3: 3VCC Voltage status. Read 1, the voltage of 3VCC is over/under the limit value. Read 0, the voltage of 3VCC is in the limit range.

Bit 2: AVCC Voltage status. Set 1, the voltage of AVCC is over/under the limit value. Read 0, the voltage of AVCC is in the limit range.

Bit 1: VIN0 Voltage status. Set 1, the voltage of VIN0 is over/under the limit value. Read 0, the voltage of VIN0 is in the limit range.

Bit 0: CPUVCORE Voltage status. Read 1, the voltage of CPUVCORE is over/under the limit value. Read 0, the voltage of CPUVCORE is in the limit range.

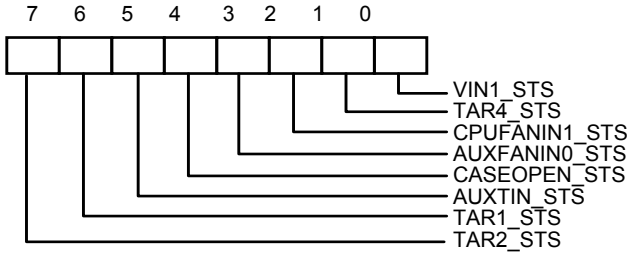
7.9.88 Real Time Hardware Status Register II - Index 5Ah (*Bank 4*)

Register Location: 5Ah

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7: Smart Fan of CPUFANIN0 warning status. Read 1, the CPUTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 6: Smart Fan of SYSFANIN warning status. Read 1, the SYSTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 5: AUXTIN temperature sensor status. Read 1, the temperature exceeds the over-temperature limit value. Read 0, the temperature is in under the hysteresis value.

Bit 4: Case Open status. Read 1, the case open is detected and latched. Read 0, the case is not latched open.

Bit 3: AUXFANIN0 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 2: CPUFANIN1 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 1: Smart Fan of CPUFANIN1 warning status. Read 1, the select temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 0: VIN1 Voltage status. Read 1, the voltage of VIN1 is over/under the limit value. Read 0, the voltage of VIN1 is in the limit range.

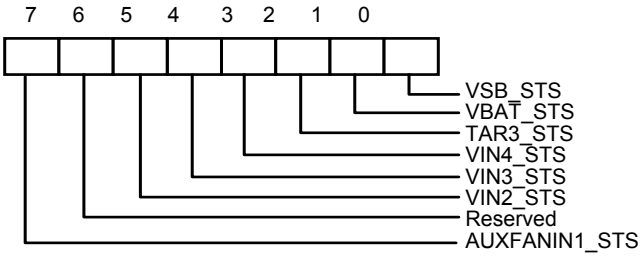
7.9.89 Real Time Hardware Status Register III - Index 5Bh (*Bank 4*)

Register Location: 5Bh

Power on Default Value: 00h

Attribute: Read Only

Size: 8 bits



Bit 7: AUXFANIN1 status. Read 1, the fan speed count is over the limit value. Read 0, the fan speed count is in the limit range.

Bit 6: Reserved.

Bit 5: VIN2 Voltage status. Read 1, the voltage of VIN2 is over/under the limit value. Read 0, the voltage of VIN21 is in the limit range.

Bit 4: VIN3 Voltage status. Read 1, the voltage of VIN3 is over/under the limit value. Read 0, the voltage of VIN3 is in the limit range.

Bit 3: VIN4 Voltage status. Read 1, the voltage of VIN4 is over/under the limit value. Read 0, the voltage of VIN4 is in the limit range.

Bit 2: Smart Fan of AUXFANIN warning status. Read 1, the AUXTIN temperature has been over the target temperature for 3 minutes with full fan speed at thermal cruise mode of SmartFan™. Read 0, the temperature does not reach the warning range yet.

Bit 1: VBAT Voltage status. Read 1, the voltage of VBAT is over/under the limit value. Read 0, the voltage of VBAT is in the limit range.

Bit 0: VSB Voltage status. Read 1, the voltage of VSB is over/under the limit value. Read 0, the voltage of VSB is in the limit range.

7.9.90 Reserved Register - Index 5Ch-5Dh (*Bank 4*)

7.9.91 Value RAM 2 — Index 50h-59h *(Bank 5)*

ADDRESS A6-A0	DESCRIPTION
50h	VSB reading
51h	VBAT reading. The reading is meaningless if EN_VBAT_MNT bit(Bank0 Index 5Dh.bit0) is not set.
52h	VIN4 reading
53h	AUXFANIN1 reading Note: This location stores the number of counts of the internal clock per revolution.
54h	3VSB High Limit
55h	3VSB Low Limit
56h	VBAT High Limit
57h	VBAT Low Limit
58h	VIN4 High Limit
59h	VIN4 Low Limit
5Ah	Reserved
5Bh	Reserved
5Ch	AUXFANIN1 Fan Count Limit

ADDRESS A6-A0	DESCRIPTION
	Note: It is the number of counts of the internal clock for the Low Limit of the fan speed.

7.9.92 Nuvoton Test Register - Index 50h-57h (*Bank 6*)

8. FLOPPY DISK CONTROLLER

8.1 FDC Functional Description

The floppy disk controller (FDC) of the W83627EHF/EHG/EF/EG integrates all of the logic required for floppy disk control. The FDC implements a FIFO which provides better system performance in multi-master systems, and the digital data separator supports data rates up to 2 M bits/sec.

The FDC includes the following blocks: Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core. The rest of this section discusses these blocks through the following topics: FIFO, Data Separator, Write Precompensation, Perpendicular Recording mode, FDC core, FDC commands, and FDC registers.

8.1.1 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM (Request for Master) and DIO (Data Input/Output) bits in the Main Status Register.

The FIFO is defaulted to disabled mode after any form of reset, which maintains PC/AT hardware compatibility. The default values can be changed through the configure command. The advantage of the FIFO is that it lets the system have a larger DMA latency without causing disk errors. The following tables give several examples of the delays with the FIFO. The data are based upon the following formula:

DELAY = THRESHOLD # x (1 / DATA RATE) * 8 - 1.5 μs

FIFO THRESHOLD	MAXIMUM DELAY UNTIL SERVICING AT 500K BPS
	Data Rate
1 Byte	1 x 16 μs - 1.5 μs = 14.5 μs
2 Byte	2 x 16 μs - 1.5 μs = 30.5 μs
8 Byte	8 x 16 μs - 1.5 μs = 6.5 μs
15 Byte	15 x 16 μs - 1.5 μs = 238.5 μs
FIFO THRESHOLD	**MAXIMUM DELAY UNTIL SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 x 8 μs - 1.5 μs = 6.5 μs

2 Byte	2 x 8 μs - 1.5 μs = 14.5 μs
8 Byte	8 x 8 μs - 1.5 μs = 62.5 μs
15 Byte	15 x 8 μs - 1.5 μs = 118.5 μs

At the start of a command, the FIFO is always disabled, and command parameters must be sent based upon the RQM and DIO bit settings in the Main Status Register. When the FDC enters the command execution phase, it clears the FIFO off any data to ensure that invalid data are not transferred.

An overrun or underrun terminates the current command and data transfer. Disk writes complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled by the specify command and are initiated by the FDC when the LDRQ pin is activated during a data transfer command.

8.1.2 Data Separator

The function of the data separator is to lock onto incoming serial read data. When a lock is achieved, the serial front-end logic in the chip is provided with a clock that is synchronized with the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial-to-parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The control logic generates RDD and RWD for every pulse input, and any data pulse input is synchronized and then adjusted immediately by error adjustment. A digital integrator keeps track of the speed changes in the input data stream.

8.1.3 Write Precompensation

The write precompensation logic minimizes bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and depends on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known, so, depending on the pattern, the bit is shifted either early or late, relative to the surrounding bits.

8.1.4 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. Perpendicular mode requires a 1 Mbps data rate for the FDC, and, at this data rate, the FIFO manages the host interface bottleneck due to the high speed of data transfer to and from the disk.

FDC Core

The W83627EHF/EHG/EF/EG FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor, and the result may be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information are provided to the microprocessor.

The next section introduces each of the commands.

8.1.5 FDC Commands

Command Symbol Descriptions:

C: Cylinder Number 0 - 256

D: Data Pattern

DIR: Step Direction

DIR = 0: step out

	DIR = 1: step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of Track
FIFOTHR:	FIFO Threshold
GAP:	Gap Length Selection
GPL:	Gap Length
H:	Head Number
HDS:	Head Number Select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, and PTRTRK bits to prevent being affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number
R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sectors per Cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time

ST0: Status Register 0

ST1: Status Register 1

ST2: Status Register 2

ST3: Status Register 3

WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	MT MFM SK 0 0 1 1 0	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	---------- C ----------	Sector ID information prior to command execution
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and system
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(2) Read Deleted Data

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	MT MFM SK 0 1 1 0 0	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	---------- C ----------	Sector ID information prior to command execution
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and system
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 MFM 0 0 1 0 0 1 0	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
Execution			The first correct ID information on the cylinder is stored in the Data Register
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Disk status after the command has been completed
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(5) Verify

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	MT MFM SK 1 0 1 1 0	Command codes
	W	EC 0 0 0 0 HDS DS1 DS0	
	W	---------- C ----------	Sector ID information prior to command execution
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
		---------- DTL/SC ----------	
Execution			No data transfer takes place
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(6) Version

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 1 0 0 0 0	Command code

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Result	R	1 0 0 1 0 0 0 0	Enhanced controller

(7) Write Data

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	MT MFM 0 0 0 1 1 0 1	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	---------- C ----------	Sector ID information prior to Command execution
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and the system
Result	R	---------- ST0 ----------	Status information after Command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after Command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(8) Write Deleted Data

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	MT MFM 0 0 1 0 0 1	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	---------- C ----------	Sector ID information prior to command execution
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
	W	---------- EOT ----------	
	W	---------- GPL ----------	
	W	---------- DTL ----------	
Execution			Data transfer between the FDD and the system
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- C ----------	Sector ID information after command execution
	R	---------- H ----------	
	R	---------- R ----------	
	R	---------- N ----------	

(9) Format A Track

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 MFM 0 0 1 1 0 1	Command codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	---------- N ----------	Bytes per Sector
	W	---------- SC ----------	Sectors per Cylinder
	W	---------- GPL ----------	Gap 3
	W	---------- D ----------	Filler Byte
Execution for Each Sector: (Repeat)	W	---------- C ----------	Input Sector Parameters
	W	---------- H ----------	
	W	---------- R ----------	
	W	---------- N ----------	
Result	R	---------- ST0 ----------	Status information after command execution
	R	---------- ST1 ----------	
	R	---------- ST2 ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	
	R	---------- Undefined ----------	

(10) Recalibrate

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 0 0 1 1 1	Command codes

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
	W	0 0 0 0 0 0 0 DS1 DS0	
Execution			Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 0 1 0 0 0	Command code
Result	R R	---------- ST0 ---------- ---------- PCN ----------	Status information at the end of each seek operation

(12) Specify

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W W W	0 0 0 0 0 0 1 1 | ---------SRT ---------- | --------- HUT ---------- | |---------- HLT ----------| ND	Command codes

(13) Seek

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 0 1 1 1 1	Command codes

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
	W W	0 0 0 0 0 HDS DS1 DS0 ---------- NCN ----------	
Execution	R		Head positioned over proper cylinder on the diskette

(14) Configure

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W W W W	0 0 0 1 0 0 1 1 0 0 0 0 0 0 0 0 0 EIS EFIFO POLL | ------ FIFOTHR ----| | ----------PRETRK ---------- |	Configure information
Execution			Internal registers written

(15) Relative Seek

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W W W	1 DIR 0 0 1 1 1 1 0 0 0 0 0 0 0 0 HDS DS1 DS0 | ---------- RCN ---------- |	Command codes

(16) Dumpreg

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 0 1 1 1 0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------	
	R	---------- PCN-Drive 1 ----------	
	R	---------- PCN-Drive 2----------	
	R	---------- PCN-Drive 3 ----------	
	R	--------SRT ---------- | --------- HUT --------	
	R	---------- HLT ----------| ND	
	R	---------- SC/EOT ----------	
	R	LOCK 0 D3 D2 D1 D0 GAP	
	R	WG	
	R	0 EIS EFIFO POLL | ------ FIFOTHR --------	
		----------PRETRK ----------	

(17) Perpendicular Mode

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 1 0 0 1 0	Command Code
	W	OW 0 D3 D2 D1 D0 GAP WG	

(18) Lock

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	LOCK 0 0 1 0 1 0 0	Command Code
Result	R	0 0 0 LOCK 0 0 0 0	

(19) Sense Drive Status

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	0 0 0 0 0 1 0 0	Command Code
	W	0 0 0 0 0 HDS DS1 DS0	
Result	R	---------- ST3 ----------	Status information about the disk drive

(20) Invalid

PHASE	R/W	D7 D6 D5 D4 D3 D2 D1 D0	REMARKS
Command	W	---------- Invalid Codes ----------	Invalid codes (no operation-FDC goes to standby state)
Result	R	---------- ST0 ----------	ST0 = 80h

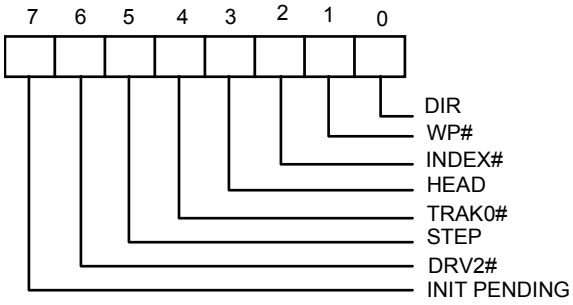
8.2 Register Descriptions

There are several status, data, and control registers in the W83627EHF/EHG/EF/EG. These registers are defined below, and the rest of this section provides more details about each one of them.

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

8.2.1 Status Register A (SA Register) (Read base address + 0)

Along with the SB register, the SA register is used to monitor several disk-interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

RESERVED (Bit 6)

STEP (Bit 5):

This bit indicates the complement of the STEP# output.

TRAK0#(Bit 4):

This bit indicates the value of the TRAK0# input.

HEAD (Bit 3):

This bit indicates the complement of the HEAD# output.

0 side 0

1 side 1

INDEX#(Bit 2):

This bit indicates the value of the INDEX# output.

WP#(Bit 1):

0 disk is write-protected

1 disk is not write-protected

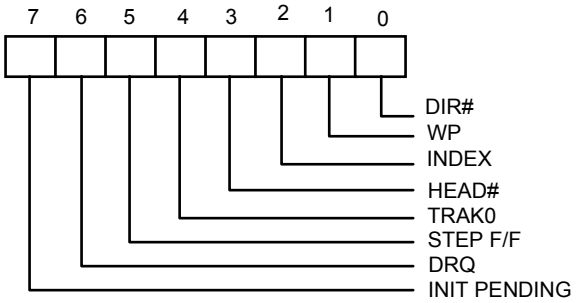
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of the DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of the latched STEP# output.

TRAK0 (Bit 4):

This bit indicates the complement of the TRAK0# input.

HEAD# (Bit 3):

This bit indicates the value of the HEAD# output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of the INDEX# output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

DIR# (Bit 0)

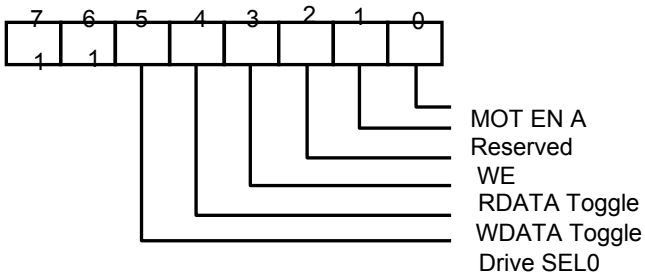
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

8.2.2 Status Register B (SB Register) (Read base address + 1)

Along with the SA register, the SB register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of the DO REGISTER, bit 0 (drive-select bit 0).

WDATA Toggle (Bit 4):

This bit changes state on every rising edge of the WD# output pin.

RDATA Toggle (Bit 3):

This bit changes state on every rising edge of the RDATA# output pin.

WE (Bit 2):

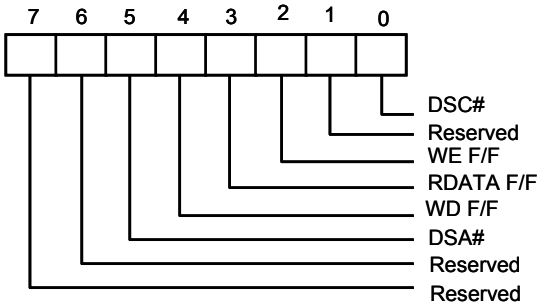
This bit indicates the complement of the WE# output pin.

RESERVED (Bit 1)

MOT EN A (Bit 0)

This bit indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



RESERVED (Bit 7)

RESERVED (Bit 6)

DSA# (Bit 5):

This bit indicates the status of the DSA# output pin.

WD F/F (Bit 4):

This bit indicates the complement of the WD# output pin, which is latched on every rising edge of the WD# output pin.

RDATA F/F (Bit 3):

This bit indicates the complement of the latched RDATA# output pin.

WE F/F (Bit 2):

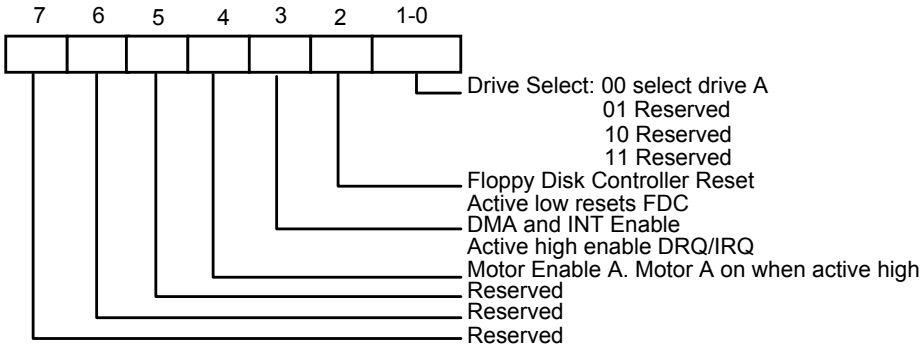
This bit indicates the complement of the latched WE# output pin.

RESERVED (Bit 1)

RESERVED (Bit 0)

8.2.3 Digital Output Register (DO Register) (Write base address + 2)

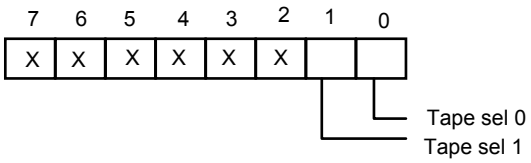
The Digital Output Register is a write-only register that controls drive motors, drive selection, DRQ/IRQ enable, and FDC reset. The bit definitions are as follows:



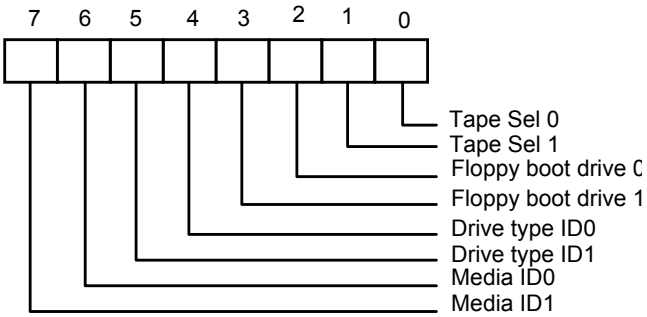
8.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information for the floppy disk drive.

In normal floppy mode, this register only has bits 0 and 1, and the bit definitions are as follows:



If the three-mode FDD function is enabled (EN3MODE = 1 in LD0 CRF0, Bit 0), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read-only. These two bits reflect the value of LD0 CRF1, bits 5 and 4.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits in LD0 CRF2. Which two bits are reflected depends on the last drive selection in the DO register.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of LD0 CRF1, bits 7 and 6.

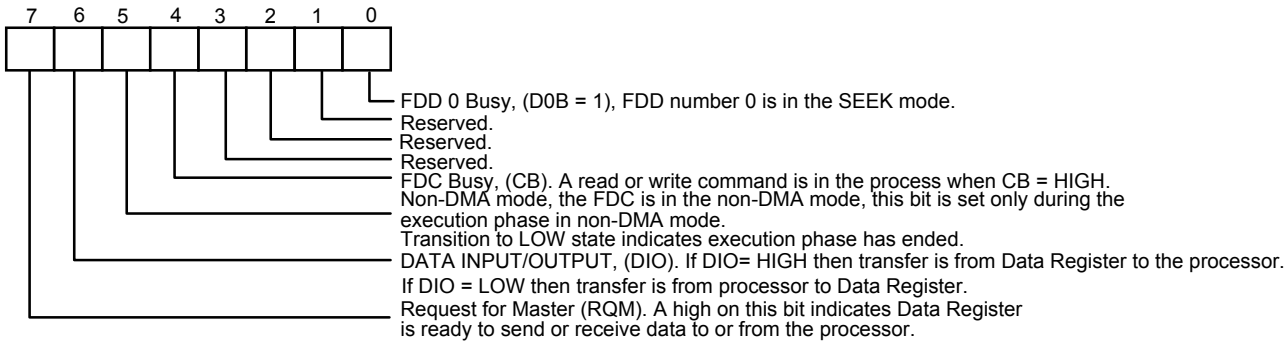
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved for the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

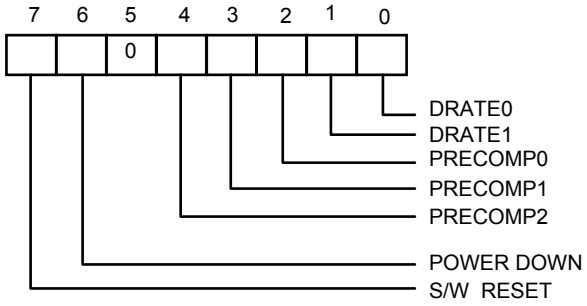
8.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



8.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. However, in PC-AT and PS/2 Model 30 and PS/2 modes, the data rate is controlled by the CC register, not by the DR register. As a result, the real data rate is determined by the most recent write to either the DR or CC register. The bit definitions for this register are as follows:



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for every combination of these bits.

PRECOMP			PRECOMPENSATION DELAY	
2	1	0	250K - 1 Mbps	2 Mbps Tape drive
0	0	0	Default Delays	Default Delays
0	0	1	41.67 ns	20.8 ns
0	1	0	83.34 ns	41.17 ns
0	1	1	125.00 ns	62.5ns
1	0	0	166.67 ns	83.3 ns
1	0	1	208.33 ns	104.2 ns

PRECOMP			PRECOMPENSATION DELAY	
2	1	0	250K - 1 Mbps	2 Mbps Tape drive
1	1	0	250.00 ns	125.00 ns
1	1	1	0.00 ns (disabled)	0.00 ns (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 ns
300 KB/S	125 ns
500 KB/S	125 ns
1 MB/S	41.67ns
2 MB/S	20.8 ns

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write-current control.

00 500 KB/S (MFM), 250 KB/S (FM), RWC# = 1

01 300 KB/S (MFM), 150 KB/S (FM), RWC# = 0

10 250 KB/S (MFM), 125 KB/S (FM), RWC# = 0

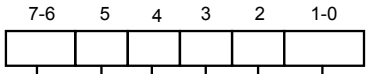
11 1 MB/S (MFM), Illegal (FM), RWC# = 1

The 2 MB/S data rate for the tape drive is only supported by setting DRATE1 and DRATE0 to 01, as well as setting DRT1 and DRT0 (CRF4 and CRF5 for logical device 0) to 10. Please see the functional description of CRF4 or CRF5 and the data rate table for individual data-rate settings.

8.2.7 FIFO Register (R/W base address + 5)

The FIFO register consists of four status registers in a stack, and only one register is presented to the data bus at a time. The FIFO register stores data, commands, and parameters, and it provides disk-drive status information. In addition, data bytes pass through the data register to program or obtain results after a command. In the W83627EHF/EHG/EF/EG, this register is disabled after reset. The FIFO can enable it and change its values through the configure command.

Status Register 0 (ST0)



US1, US0 Drive Select:
00 Drive A selected
01 Reserved
10 Reserved
11 Reserved

HD Head address:
1 Head selected
0 Head selected

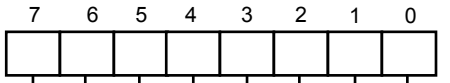
NR Not Ready:
1 Drive is not ready
0 Drive is ready

EC Equipment Check:
1 When a fault signal is received from the FDD or the track
0 signal fails to occur after 77 step pulses
0 No error

SE Seek end:
1 seek end
0 seek error

IC Interrupt Code:
00 Normal termination of command
01 Abnormal termination of command
10 Invalid command issue
11 Abnormal termination because the ready signal from FDD changed state during command execution

Status Register 1 (ST1)



Missing Address Mark. 1 When the FDC cannot detect the data address mark or the data address mark has been deleted.

NW (Not Writable). 1 If a write Protect signal is detected from the diskette drive during execution of write data.

ND (No DATA). 1 If specified sector cannot be found during execution of a read, write or verifly data.

Not used. This bit is always 0.

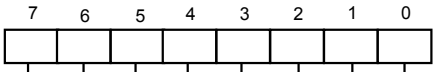
OR (Over Rum). 1 If the FDC is not serviced by the host system within a certain time interval during data transfer.

DE (data Error).1 When the FDC detects a CRC error in either the ID field or the data field.

Not used. This bit is always 0.

EN (End of track). 1 When the FDC tries to access a sector beyond the final sector of a cylinder.

Status Register 2 (ST2)



MD (Missing Address Mark in Data Field).
1 If the FDC cannot find a data address mark (or the address mark has been deleted) when reading data from the media
0 No error

BC (Bad Cylinder)
1 Bad Cylinder
0 No error

SN (Scan Not satisfied)
1 During execution of the Scan command
0 No error

SH (Scan Equal Hit)
1 During execution of the Scan command, if the equal condition is satisfied
0 No error

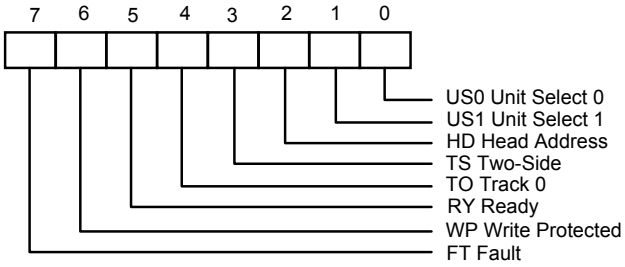
WC (Wrong Cylinder)
1 Indicates wrong Cylinder

DD (Data error in the Data field)
1 If the FDC detects a CRC error in the data field
0 No error

CM (Control Mark)
1 During execution of the read data or scan command
0 No error

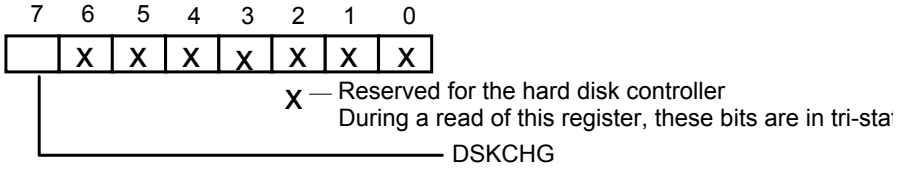
Not used. This bit is always 0

Status Register 3 (ST3)

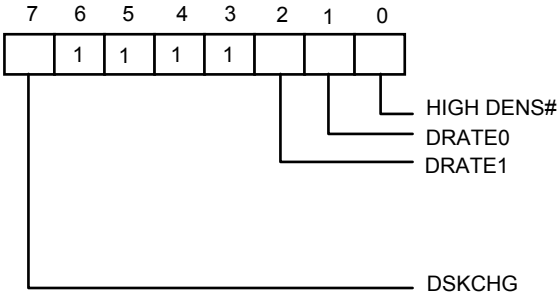


8.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit, read-only register used for diagnostic purposes. In PC/XT or PC/AT mode, only bit 7 is checked by the BIOS. When the register is read, bit 7 shows the complement of DSKCHG#, while the other bits remain in tri-state. The bit definitions are as follows:



In PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the complement of the DSKCHG# input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):

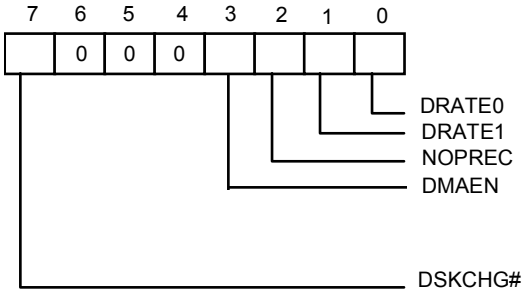
These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.

HIGHDENS# (Bit 0):

0 500 KB/S or 1 MB/S data rate (high-density FDD)

1 250 KB/S or 300 KB/S data rate

In PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the status of the DSKCHG# input.

Bit 6-4: These bits are always a logic 0 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO register, bit 3.

NOPREC (Bit 2):

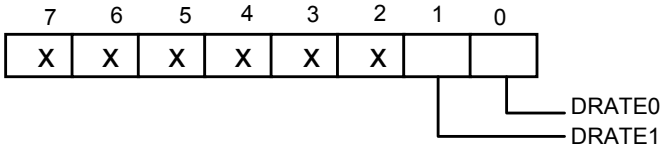
This bit indicates the value of the NOPREC bit in the CC REGISTER.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.

8.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In PC/AT and PS/2 mode, the bit definitions are as follows:



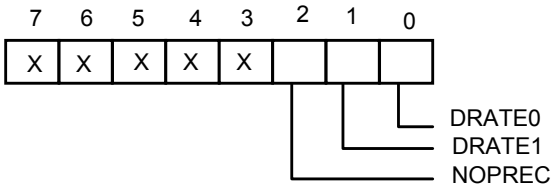
X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.

In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit disables the precompensation function. It can be set by the software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC. See DR register bits 1 and 0 (Data Rate Register (DR Register) (Write base address + 4)) for how the settings correspond to individual data rates.

9. UART PORT

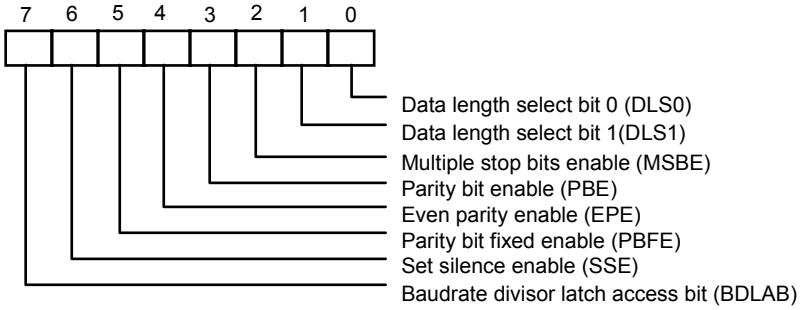
9.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format for transmission and to convert serial data into parallel format during reception. The serial data format is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one-and-a-half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include a complete modem control capability and 16-byte FIFOs for reception and transmission to reduce the number of interrupts presented to the CPU.

9.2 Register Description

9.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communication, including data length, stop bit, parity, and baud rate selection.



Bit 7: BDLAB. When this bit is set to logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logical 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to logical 1,

(1) if EPE is logical 1, the parity bit is fixed as logical 0 when transmitting and checking.

(2) if EPE is logical 0, the parity bit is fixed as logical 1 when transmitting and checking.

Bit 4: EPE. When PBE is set to logical 1, this bit counts the number of logical 1's in the data word bits and determines the parity bit. When this bit is set to logical 1, the parity bit is set to logical 1 if an even number of logical 1's are sent or checked. When the bit is set to logical 0, the parity bit is logical 1 if an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set to logical 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to logical 0, one stop bit is sent and checked.

(2) If MSBE is set to logical 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked.

(3) If MSBE is set to logical 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.

Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0

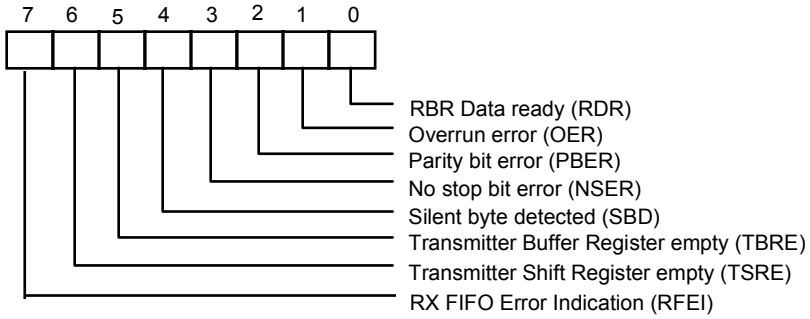
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

**: These bits are always 0 in 16450 Mode.

9.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.



Bit 7: RFEI. In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop-bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, an interrupt is generated to notify the CPU to write the next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.

Bit 4: SBD. This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.

Bit 3: NSER. This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.

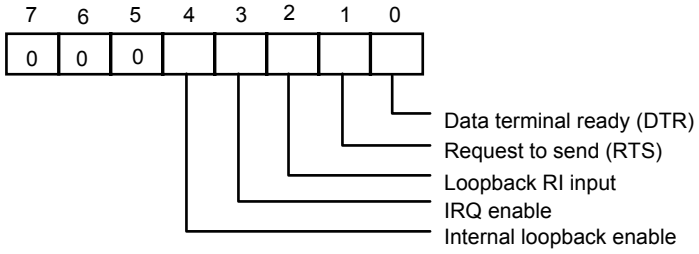
Bit 2: PBER. This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.

Bit 1: OER. This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.

Bit 0: RDR. This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

9.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.



Bit 4: When this bit is set to logical 1, the UART enters diagnostic mode, as follows:

(1) SOUT is forced to logical 1, and SIN is isolated from the communication link.

(2) The modem output pins are set to their inactive state.

(3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR)→DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to logical 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.

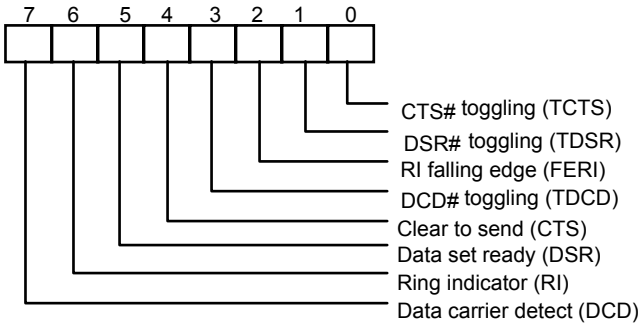
Bit 2: This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.

Bit 1: This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.

Bit 0: This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

9.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of the four input pins used with handshake peripherals such as modems and records changes on these pins.



Bit 7: This bit is the opposite of the DCD# input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6: This bit is the opposite of the RI # input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5: This bit is the opposite of the DSR# input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4: This bit is the opposite of the CTS# input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3: TDCD. This bit indicates that the DCD# pin has changed state after HSR was read by the CPU.

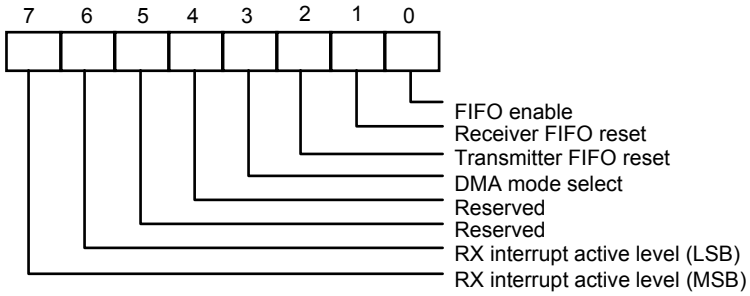
Bit 2: FERI. This bit indicates that the RI # pin has changed from low to high after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the DSR# pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the CTS# pin has changed state after HSR was read by the CPU.

9.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is set to logical 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.

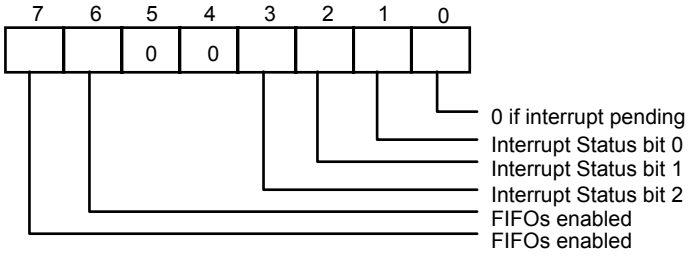
Bit 2: Setting this bit to logical 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.

Bit 1: Setting this bit to logical 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.

Bit 0: This bit enables 16550 (FIFO) mode. This bit should be set to logical 1 before the other UFR bits are programmed.

9.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.



Bit 7, 6: These two bits are set to logical 1 when UFR, bit 0 = 1.

Bit 5, 4: These two bits are always logical 0.

Bit 3: In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. See the table below.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.

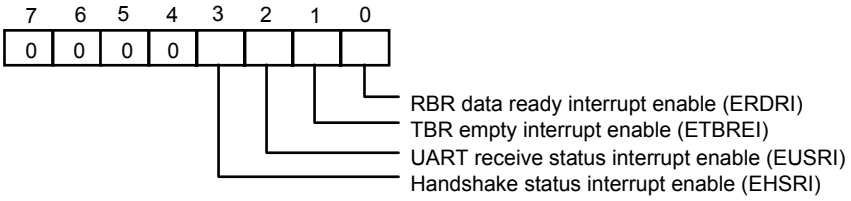
ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

9.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.



Bit 7-4: These four bits are always logical 0.

Bit 3: EHSRI. Set this bit to logical 1 to enable the handshake status register interrupt.

Bit 2: EUSRI. Set this bit to logical 1 to enable the UART status register interrupt.

Bit 1: ETBREI. Set this bit to logical 1 to enable the TBR empty interrupt.

Bit 0: ERDRI. Set this bit to logic 1 to enable the RBR data ready interrupt.

9.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (CR0C, bits 7 and 6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

9.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10. PARALLEL PORT

10.1 Printer Interface Logic

The W83627EHF/EHG/EF/EG parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The W83627EHF/EHG/EF/EG supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP) on the parallel port.

The following tables show the pin definitions for different modes of the parallel port.

HOST CONNECTOR	PIN NUMBER OF W83627EHF/EHG/ EF/EG	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	nAFD	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1] , ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF W83627EHF/EHG/EF/EG	PIN ATTRIBUTE	SPP
1	36	O	nSTB
2	31	I/O	PD0
3	30	I/O	PD1
4	29	I/O	PD2
5	28	I/O	PD3
6	27	I/O	PD4
7	26	I/O	PD5
8	24	I/O	PD6
9	23	I/O	PD7
10	22	I	nACK
11	21	I	BUSY
12	19	I	PE
13	18	I	SLCT
14	35	O	nAFD
15	34	I	nERR
16	33	O	nINIT
17	32	O	nSLIN

10.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1

0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.

2. These registers are available only in EPP mode.

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

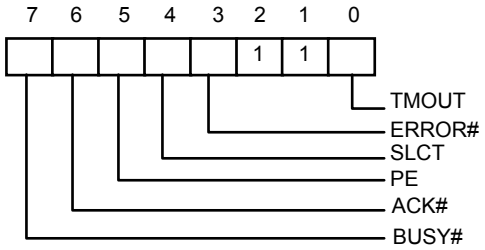
Each register (or pair of registers, in some cases) is discussed below.

10.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

10.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:



Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or in an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.

Bit 5: A logical 1 means the printer has detected the end of paper.

Bit 4: A logical 1 means the printer is selected.

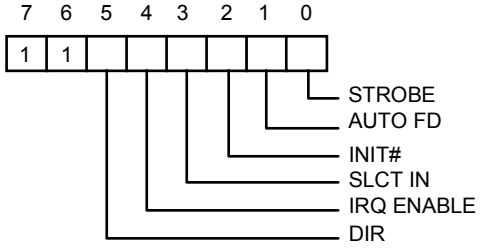
Bit 3: A logical 0 means the printer has encountered an error condition.

Bit 1, 2: Reserved. These two bits are always read as logical 1.

Bit 0: This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means that no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

10.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:



Bit 7, 6: These two bits are always read as logical 1. They can be written.

Bit 5: Direction control bit

When this bit is logical 1, the parallel port is in input mode (read); when it is logical 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A logical 1 allows an interrupt to occur when ACK# changes from low to high.

Bit 3: A logical 1 selects the printer.

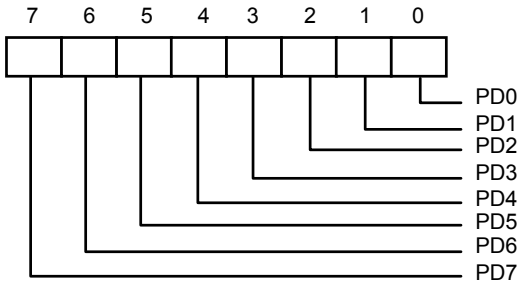
Bit 2: A logical 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A logical 1 causes the printer to line-feed after a line is printed.

Bit 0: A logical 1 generates an active-high pulse for a minimum of 0.5μs to clock data into the printer. Valid data must be present for a minimum of 0.5μs before and after the strobe pulse.

10.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

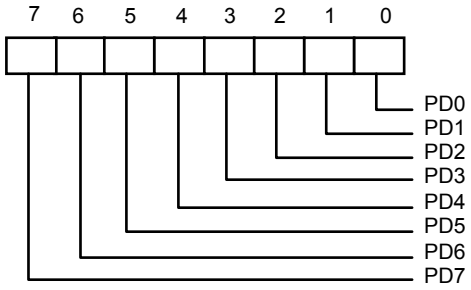


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

10.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:



When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle. During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

10.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
NWrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
NWait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

10.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μs have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

10.2.7.1. EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

10.2.7.2. EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts; however, it does not finish until nWait changes from active low to inactive high.

10.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the W83627EHF/EHG/EF/EG parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The W83627EHF/EHG/EF/EG ECP supports the following modes.

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

10.3.1 ECP Register and Bit Map

The next two tables list the registers used in the ECP mode and provide a bit map of the parallel port and ECP registers.

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by the configuration register or the hardware setting.

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.

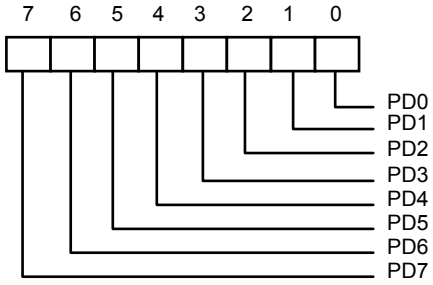
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

10.3.2 Data and ecpAFifo Port

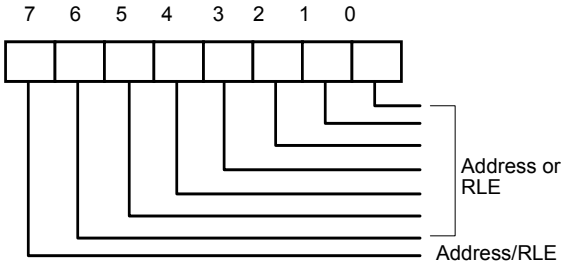
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



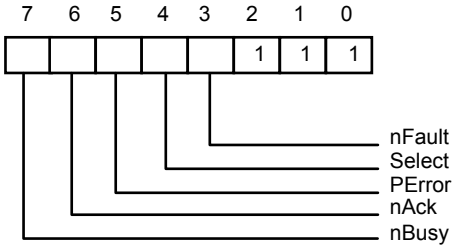
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:



10.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:



Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

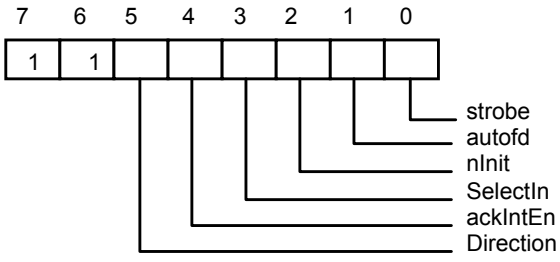
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logical 1 during a read.

10.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 7, 6: These two bits are always read as logical one and cannot be written.

Bit 5: If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes,

0 the parallel port is in output mode.

1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.

Bit 3: This bit is inverted and output to the SLIN# output.

0 The printer is not selected.

1 The printer is selected.

Bit 2: This bit is output to the INIT# output.

Bit 1: This bit is inverted and output to the AFD# output.

Bit 0: This bit is inverted and output to the STB# output.

10.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

10.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

10.3.7 TFIFO (Test FIFO Mode) Mode = 110

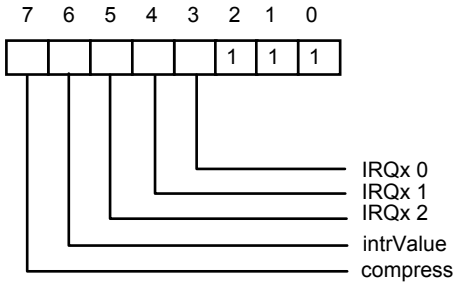
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

10.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10h is returned indicating an 8-bit implementation.

10.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7: This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

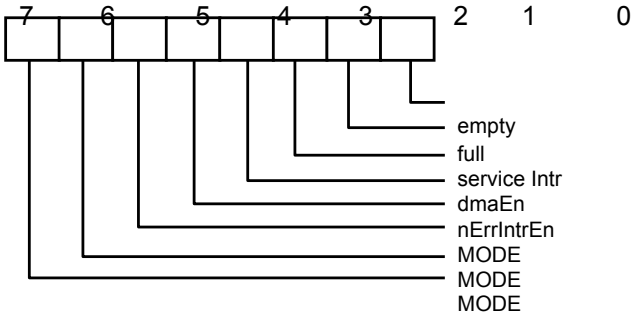
Bit 5-3: Reflects the IRQ resource assigned for ECP port.

CNFGB[5:3]	IRQ RESOURCE
000	Reflects other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0: These five bits are logical 1 during a read and can be written.

10.3.10 ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: Read/Write. These bits select the mode.

000 Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.

001 PS/2 Parallel Port mode. In addition to the functions of the SPP mode, this mode has an extra trait: Direction is able to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.

010 Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode functions only when direction is 0.

011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.

100 EPP Mode. EPP mode is activated if the EPP mode is selected.

101 Reserved.

110 Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.

111 Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of nFault.

0 Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR.

Bit 3: Read/Write

1 Enables DMA.

0 Disables DMA unconditionally.

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.

0 Enables one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be reset to logical 0 to re-enable the interrupts.

(a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached.

(b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO.

(c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least one free byte.

1 The FIFO is completely full; it cannot accept another byte.

Bit 0: Read only

0 The FIFO contains at least one byte of data.

1 The FIFO is completely empty.

10.3.11 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
NStrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.

NAME	TYPE	DESCRIPTION
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

10.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

10.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

10.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

10.3.12.3. Data Compression

The W83627EHF/EHG/EF/EG hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

10.3.13 FIFO Operation

The FIFO threshold is set in LD0 CRO0, bit 6 ~ 3. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

10.3.14 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

10.3.15 Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

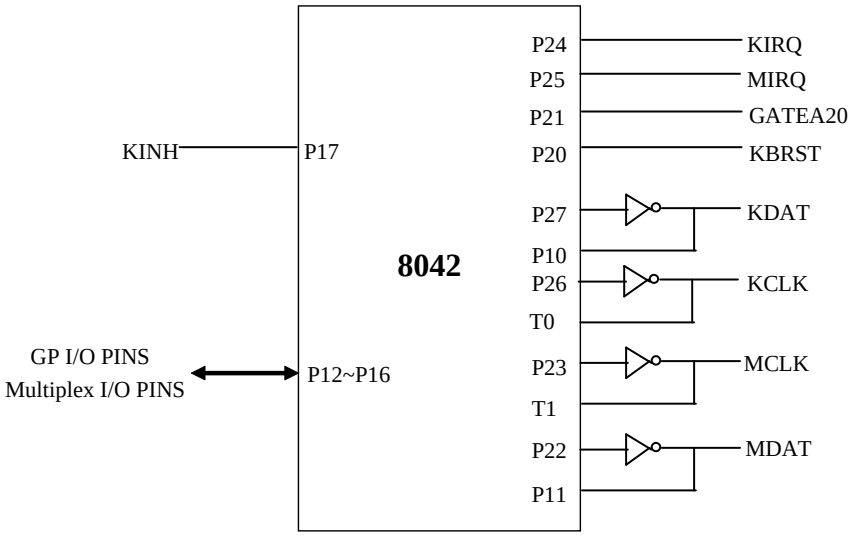
1. To the ecpDFifo at 400h and ecpAFifo at 000h
2. From the ecpDFifo located at 400h
3. To / from the tFifo at 400h.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

11. KEYBOARD CONTROLLER

The W83627EHF/EHG/EF/EG KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.



Keyboard and Mouse Interface

11.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60h (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

11.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

11.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

BIT	BIT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

11.4 Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
</table>

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>ABh</td><td>Interface Test
<table><tr><th>BIT</th><th>BIT DEFINITION</th></tr><tr><td>00</td><td>No Error Detected</td></tr><tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr><tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr><tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr><tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr></table></td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port (P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into the STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into the STATUS register</td></tr>
<tr><td>D0h</td><td>Send Port 2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set / reset GateA20 line based on system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from the Keyboard</td></tr>
<tr><td>D3h</td><td>Send data back to the system as if it came from Auxiliary Device</td></tr>
<tr><td>D4h</td><td>Output next received byte of data from system to Auxiliary Device</td></tr>
<tr><td>E0h</td><td>Reports the status of the test inputs</td></tr>
<tr><td>FXh</td><td>Pulse only RC (the reset line) low for 6μs if the Command byte is even</td></tr>
</table>

11.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

11.5.1 KB Control Register

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	Reserved	Reserved	Reserved	P92EN	HGA20	HKBRST#

KCLKS1, KCLKS0

These two bits select the KBC clock rate.

00: KBC clock input is 6 MHz

01: KBC clock input is 8 MHz

10: KBC clock input is 12 MHz

11: KBC clock input is 16 MHz

P92EN (Port 92 Enable)

1: Enables Port 92 to control GATEA20 and KBRESET.

0: Disables Port 92 functions.

HGA20 (Hardware GATEA20)

1: Selects hardware GATEA20 control logic to control GATE A20 signal.

0: Disables hardware GATEA20 control logic function.

HKBRST# (Hardware Keyboard Reset)

1: Selects hardware KB RESET control logic to control KBRESET signal.

0: Disables hardware KB RESET control logic function.

When the KBC receives data that follows a "D1" command, the hardware control logic sets or clears GATEA20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an "FE" command, the KBRESET is pulse low for 6μs (Min.) with a 14μs (Min.) delay.

GATEA20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATEA20 and KBRESET are merged with Port92 when the P92EN bit is set.

11.5.2 Port 92 Control Register

BIT	7	6	5	4	3	2	1	0
NAME	Res. (0)	Res. (0)	Res. (1)	Res. (0)	Res. (0)	Res. (1)	SGA20	PLKBRST#

SGA20 (Special GATE A20 Control)

1: Drives GATE A20 signal to high.

0: Drives GATE A20 signal to low.

PLKBRST# (Pull-Low KBRESET)

A logical 1 on this bit causes KBRESET to drive low for 6 μS(Min.) with a 14 μS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

12. POWER MANAGEMENT EVENT

The PME# (pin 86) signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the W83627EHF/EHG/EF/EG are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the W83627EHF/EHG/EF/EG won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events Note.1.

1) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
2) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the W83627EHF/EHG/EF/EG supports include:

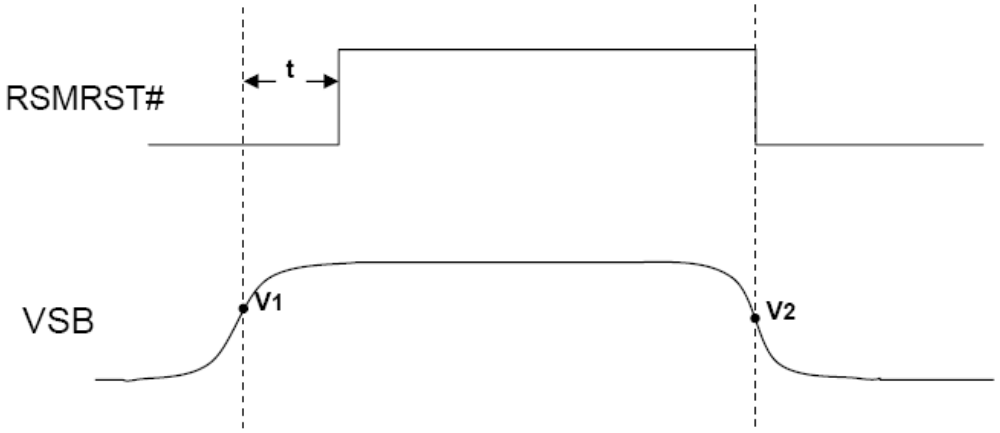
- Mouse IRQ event
- Keyboard IRQ event
- Printer IRQ event
- Floppy IRQ event
- UART A IRQ event
- UART B IRQ event
- Hardware Monitor IRQ event
- WDTO# event
- MIDI IRQ event
- RIB (UARTB Ring Indicator) event

12.1 Resume Reset Logic

The RSMRST# (Pin 75) signal is a reset output and is used as the 3VSB power-on reset signal for the South Bridge.

When the W83627EHF/EHG/EF/EG detects the 3VSB voltage rises to “V1”, it then starts a delay – “t” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in the following figure and table.



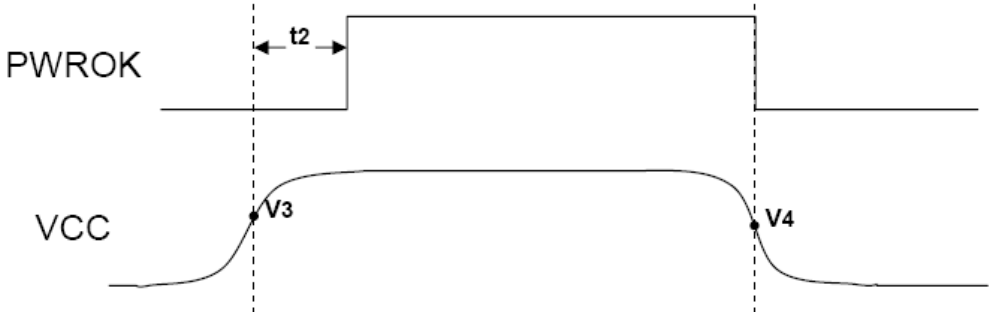
SYMBOL	MIN.	MAX.	UNIT
t	80	130	mS
V1	2.6	2.65	V
V2	2.4	2.45	V

12.2 PWROK Generation

The PWROK (Pin 71) signal is an output and is used as the 3VCC power-on reset signal.

When the W83627EHF/EHG/EF/EG detects the 3VCC voltage rises to “V3”, it then starts a delay – “t2” before the rising edge of PWROK asserting. If the 3VCC voltage falls below “V4”, the PWROK de-asserts immediately.

Timing and voltage parameters are shown in figure and table.



SYMBOL	MIN.	MAX.	UNIT
t2	300	600	mS
V3	2.6	2.65	V
V4	2.4	2.45	V

Originally, the t2 timing is between 300 mS to 600 mS, but it can be changed to 200 mS to 300 mS by programming Logical Device A, CR[E6h], bit 3 to "1". Furthermore, the W83627EHF/EHG/EF/EG provides four different extra delay time of PWROK for various demands. The four extra delay time are designed at Logical Device A, CR[E6h], bits 2~1. The following table shows the definitions of Logical Device A, CR[E6h] bits 3 ~1.

LOGICAL DEVICE A, CR[E6H] BIT	DEFINITION
3	PWROK_DEL (first stage) **(VSB)** Set the delay time when rising from PWROK_LP to PWROK_ST. 0: 300 ~ 600 mS. 1: 200 ~ 300 mS.
2~1	PWROK_DEL **(VSB)** Set the delay time when rising from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 mS 10: 96 mS 11: Delay 250 mS

For example, if Logical Device A, CR[E6h] bit 2 is set to “0” and bits 2~1 are set to “10”, the range of t2 timing is from 396(300 + 96) mS to 596(500 + 96) mS.

13. SERIALIZED IRQ

The W83627EHF/EHG/EF/EG supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

13.1 Start Frame

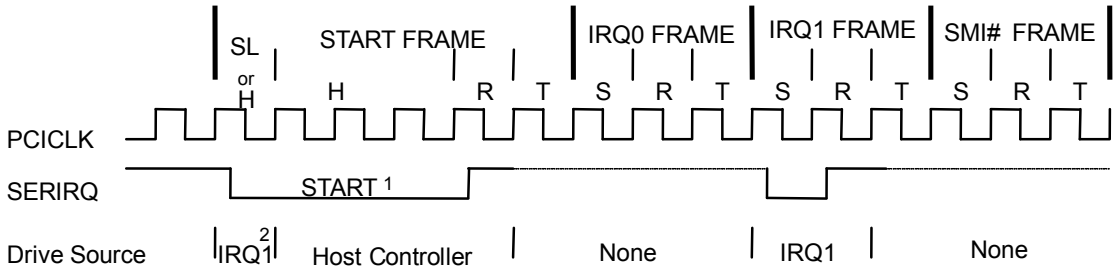
There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the W83627EHF/EHG/EF/EG drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the W83627EHF/EHG/EF/EG from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.



H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the W83627EHF/EHG/EF/EG because IRQ1 of the W83627EHF/EHG/EF/EG needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

13.2 IRQ/Data Frame

Once the Start Frame has been initiated, the W83627EHF/EHG/EF/EG must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the W83627EHF/EHG/EF/EG drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the W83627EHF/EHG/EF/EG device drives the SERIRQ high. During the Turn-around phase, the W83627EHF/EHG/EF/EG device leaves the SERIRQ tri-stated. The W83627EHF/EHG/EF/EG starts to drive the SERIRQ line from the beginning of "IRQ0 FRAME" based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 13.1.

Table 13.1 SERIRQ Sampling Periods

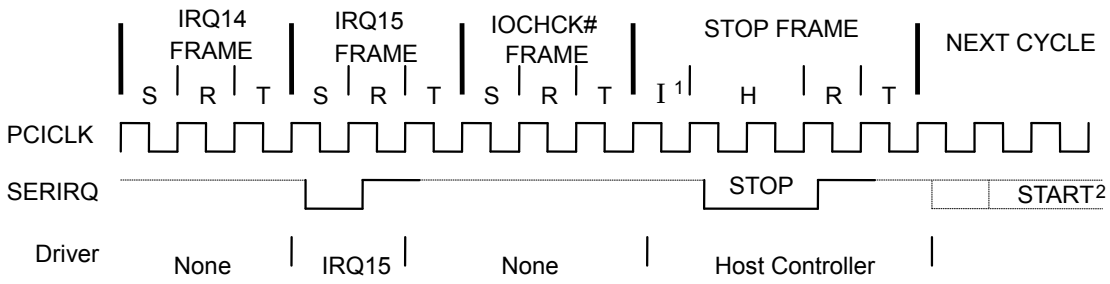
SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	-
2	IRQ1	5	Keyboard
3	SMI#	8	-
4	IRQ3	11	UART B
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	-
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

13.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.



H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

14. WATCHDOG TIMER

The WDTO# pin is a multi-function pin with GP50 functions and is configured to the WDTO# function, if Configuration Register CR[2Dh], bit 0 is set to zero.

The Watchdog Timer of the W83627EHF/EHG/EF/EG consists of an 8-bit programmable time-out counter and a control and status register. The time-out counter ranges from 1 to 255 minutes in the minute mode, or 1 to 255 seconds in the second mode. The units of Watchdog Timer counter are selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

The W83627EHF/EHG/EF/EG outputs a low signal to the WDTO# pin (pin 77) when a time-out event occurs. In other words, when the value is counted down to zero, the timer stops, and the W83627EHF/EHG/EF/EG sets the WDTO# status bit in Logical Device 8, CR[F7h], bit[4], outputting a low signal to the WDTO# pin(pin 77). Writing a zero will clear the status bit and the WDTO# pin returns to high. Writing a zero will clear the status bit. This bit will also be cleared if LRESET# or PWROK# signal is asserted.

Additionally, GP40 (pin 85), GP42 (pin 83), GP44 (pin 81) and GP46 (pin 79) provides an alternative WDTO# function. This function can be configured by the relative GPIO control register.

Please note that the output type of WDTO# (pin 77) and GP42 (pin 83) is push-pull and that of GP40 (pin 85), GP44 (pin 81) and GP46 (pin 79) is open-drain.

15. VID INPUTS AND OUTPUTS

The W83627EHF/EHG/EF/EG provides eight pins for VID input or output function. The default function is VID input. These pins can be configured to VID output function by setting Logical Device B, CR[F0h], bit 7 to 0. The configuration is applied to the 8 pins as a group. None of them can be individually set to input or output.

15.1 VID Input Detection

The W83627EHF/EHG/EF/EG supports Intel VRM 9/10/11 and AMD VRM VID detections. H/W strapping and S/W programming can set the following three input levels. a) and b) can be set by H/W strapping or S/W programming, while c) can only be set by S/W programming.

a) TTL (Vih = 2 V; Vil = 0.8V) –

1) Add a pulled-down resistor at Pin 77(EN_GTL), or

2) Set Configuration Register CR[2Ch], bit 3 to “0”;

b) GTL (Vih = 0.6 V; Vil = 0.4 V) – (Default)

1) No extra pulled-up resistor needed, or

2) Set Configuration Register CR[2Ch], bit 3 to “1”;

c) AMD VRM (Vih = 1.4V; Vil = 0.8V) –

Set Configuration Register CR[2Ch], bit 3 to “1” and Logical Device B, CR[F0h], but 6 to “1”.

The input data can be read in the data register at Logical Device B, CR[F1h], bit 7 ~ 0. It is a read/write register where bit 7~0 corresponds to VID pin 7~0. Please note that in the input mode, writes to this register have no effect.

15.2 VID Output Control

The output type of the eight VID pins is push-pull, and they drive to 3VCC (3.3V) when configured to the output mode. The output data can be set in the data register (Logical Device B, CR[F1h], bit 7 ~ 0). The written data can be read if Configuration Register CR[2Ch], bit 3 is set to “0”.

16. PCI RESET BUFFERS

The W83627EHF/EHG/EF/EG has five copies of LRESET# output buffers. LRESET# is LPC Interface Reset, to which PCI Reset is connected. The five copies of LRESET# in the W83627EHF/EHG/EF/EG are designated RSTOUT0#, RSTOUT1#, RSTOUT2#, RSTOUT3# and RSTOUT4#. All of them are powered by a 3VSB power.

RSTOUT0# is an open-drain output buffer of LRESET#. This signal needs an external pulled-up resistor of 3.3V or 5V.

RSTOUT1#, RSTOUT2#, RSTOUT3# and RSTOUT4# are push-pull output buffers of LRESET#. Each of them outputs 3.3V, voltage and the state is low when the 3VSB power is the only power source.

17. CONFIGURATION REGISTER

17.1 Chip (Global) Control Register

CR 02h. (Software Reset; Write Only)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	Write "1" Only	Software RESET.

CR 07h. (Logical Device; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Logical Device Number.

CR 20h. (Chip ID, MSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 88h (higher byte).

CR 21h. (Chip ID, LSB; Read Only)

BIT	READ / WRITE	DESCRIPTION
7~0	Read Only	Chip ID number = 6Xh (lower byte). X for IC version

CR 22h. (Device Power Down; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	HM Power Down. 0: Power down. 1: No power down.
5	R / W	URB Power Down. 0: Power down. 1: No power down.

BIT	READ / WRITE	DESCRIPTION
4	R / W	URA Power Down. 0: Power down. 1: No power down.
3	R / W	PRT Power Down. 0: Power down. 1: No power down.
2	Reserved.	
1	Reserved.	
0	R / W	FDC Power Down. 0: Power down. 1: No power down.

CR 23h. (IPD; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	IPD (Immediate Power Down). When set to 1, whole chip is put into power down mode immediately.

CR 24h. (Global Option; Default 0100_0ss0b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	CLKSEL => Input clock rate selection = 0 The clock input on pin18 is 24MHz. = 1 The clock input on pin18 is 48MHz. (Default)
5	Reserved.	
4	R / W	Enable SYSFANOUT as Output Buffer (For H version only) =0 SYSFANOUT is Open-Drain. (Default) =1 SYSFANOUT can drive logical high or logical low.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Enable CPUFANOUT0 as Output Buffer (For H version only) =0 CPUFANOUT0 is Open-Drain. (Default) =1 CPUFANOUT0 can drive logical high or logical low.
2	Read Only	ENKBC => Enable keyboard controller = 0 KBC is disabled after hardware reset. = 1 KBC is enabled after hardware reset. This bit is read only, and set/reset by power-on strapping pin (PIN54; SOUTA).
1	Reserved.	
0	R / W	PNPCVS => = 0 The compatible PNP address select registers have default values. = 1 The compatible PNP address select registers have no default value.

CR 25h. (Interface tri-state Enable; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	URBTRI
4	R / W	URATRI
3	R / W	PRTTRI
2~1	Reserved.	
0	R / W	FDCTRI.

CR 26h. (Global Option; Default 0s000000b) s: value by strapping

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	SEL4FDD => = 0 Select two FDD mode. = 1 Select four FDD mode.
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA# (pin 51).
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4	Reserved.	
3	R / W	DSFDLGRQ => = 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register (base address + 2) bit 3 is effective on selecting IRQ. = 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register (base address + 2) bit 3 is not effective on selecting IRQ.
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR register (base address + 2) bit 4 is effective on selecting IRQ. = 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR register (base address + 2) bit 4 is not effective on selecting IRQ.

BIT	READ / WRITE	DESCRIPTION
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is effective on selecting IRQ. = 1 Disable UART A legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is not effective on selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable UART B legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is effective on selecting IRQ. = 1 Disable UART B legacy mode on IRQ selection, then HCR register (base address + 4) bit 3 is not effective on selecting IRQ.

CR 27h. (Reserved)

CR 28h. (Global Option; Default 50h)

BIT	READ / WRITE	DESCRIPTION
7~5	Reserved.	
4	R / W	Select to enable/disable decoding of BIOS ROM range 000E xxxxh. = 0 Enable decoding of BIOS ROM range at 000E xxxxh. = 1 Disable decoding of BIOS ROM range at 000E xxxxh.
3	R / W	Select to enable/disable decoding of BIOS ROM range FFFE xxxxh. = 0 Enable decoding of BIOS ROM range at FFFE xxxxh. = 1 Disable decoding of BIOS ROM range at FFFE xxxxh.
2~0	R / W	PRTMODS2 ~ 0 => = 0xx Parallel Port Mode. = 1xx Reserved.

CR 29h. (OVT#/SMI#, UART A, Game port & MIDI pin select; Default 04h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	PIN5 function select = 0 PIN5 → OVT# = 1 PIN5 → SMI#.
5~4	Reserved.	
3	R / W	PIN49~54,56~57 function select = 0 PIN49~54,56~57 → UART A. = 1 PIN49~54,56~57 → GPIO6.
2~1	R / W	PIN119~120 function select Bit-2 / Bit-1 / PIN119~PIN120 function 0 / 0 / PIN 119~120 → CPUFANIN1, CPUFANOUT1 0 / 1 / PIN 119~120 → GP21, GP20 1 / x / PIN 119~120 → MSI, MSO (Default)
0	R / W	PIN121~128 function select = 0 PIN121~128 → Game Port. = 1 PIN121~128 → GPIO1.

CR 2Ah. (I^2C pin select; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1	R / W	PIN89, PIN90 function select (I^2C interafce) = 0 {PIN89, PIN90} → set by CR2C [6:5]. = 1 {PIN89, PIN90} → SDA, SCL.

BIT	READ / WRITE	DESCRIPTION
0	R / W	KB, MS pin function select = 0 KB, MS function. = 1 GPIO function.

CR 2Bh. (Reserved)

CR 2Ch. (GPIO3, GPIO4 multi-function selection; Default 00h) **(VSB Power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	PIN88 Select = 0 PIN88→ GP34 = 1 PIN88→ RSTOUT4#
6	R / W	PIN89 Select = 0 PIN89→ GP33 = 1 PIN89→ RSTOUT3# ***Note: The bit will be ignored while CR2A bit-1 is High.***
5	R / W	PIN90 Select = 0 PIN90→ GP32 = 1 PIN90→ RSTOUT2# ***Note: The bit will be ignored while CR2A bit-1 is High.***
4	Reserved	
3	R / W	EN_VRM10 Configure bit = 0 VID input voltage is TTL. = 1 VID input voltage is VRM10. The bit is strapping by PIN77 (GP50).--- Pull high to 3VSB.
2	R / W	EN_PWRDN. **(VBAT)** = 0 Thermal shutdown function is disabled. = 1 Enable thermal shutdown function.

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1~0</td><td>R / W</td><td>PIN78~85 function select
<table>
<tr><th>Bit-1</th><th>Bit-0</th><th>PIN78~PIN85 function</th></tr>
<tr><td>0</td><td>0</td><td>PIN82 → Reserved (tri-state)
PIN83 → Reserved (always low)
Others → GPIO4</td></tr>
<tr><td>0</td><td>1</td><td>PIN82 → IRRX
PIN83 → IRTX
Others → GPIO4</td></tr>
<tr><td>1</td><td>0</td><td>PIN 78~85 → GPIO4</td></tr>
<tr><td>1</td><td>1</td><td>PIN 78~85 → UART B</td></tr>
</table></td></tr>
</table>

CR 2Dh. (GPIO5 and power control signals multi-function selection; default 21h) (VSB Power)

BIT	READ / WRITE	DESCRIPTION
7	R / W	PIN67 Select (reset by RSMRST#) = 0 PIN67→ PSOUT# = 1 PIN67→ GPIO57
6	R / W	PIN68 Select (reset by RSMRST#) = 0 PIN68→ PSIN = 1 PIN68→ GPIO56
5	R / W	PIN70 Select (reset by RSMRST#) = 0 PIN70→ SUSLED = 1 PIN70→ GPIO55
4	R / W	PIN71 Select (reset by RSMRST#) = 0 PIN71→ PWROK = 1 PIN71→ GPIO54

BIT	READ / WRITE	DESCRIPTION
3	R / W	PIN72 Select (reset by RSMRST#) = 0 PIN72→ PSON# = 1 PIN72→ GPIO53
2	R / W	PIN73 Select (reset by RSMRST#) = 0 PIN73→ SUSB# = 1 PIN73→ GPIO52
1	R / W	PIN75 Select (reset by RSMRST#) = 0 PIN75→ RSMRST# = 1 PIN75→ GPIO51
0	R / W	PIN77 Select (reset by RSMRST#) = 0 PIN77→ WDTO# = 1 PIN77→ GPIO50

CR 2Eh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

CR 2Fh. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Test Mode Bits: Reserved for Nuvoton.

17.2 Logical Device 0 (FDC)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h,F0h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select FDC I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 06h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for FDC.

CR 74h. (Default 02h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	
2~0	R / W	These bits select DRQ resource for FDC. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 8Eh)

BIT	READ / WRITE	DESCRIPTION
7	R / W	This bit controls the internal pull-up resistors of the FDC input pins RDATA#, INDEX#, TRAK0#, DSKCHG# and WP#. 0: The internal pull-up resistors of FDC are turned on. 1: The internal pull-up resistors of FDC are turned off. (Default)
6	R / W	This bit determines the polarity of all FDD interface signals. 0: FDD interface signals are active low. 1: FDD interface signals are active high.

BIT	READ / WRITE	DESCRIPTION
5	R / W	When this bit is logic 0, indicates a second drive is installed and is reflected in status register A. (PS2 mode only)
4	R / W	Swap Drive 0, 1 Mode => 0: No Swap. 1: Drive and Motor select 0 and 1 are swapped.
3~2	R / W	Interface Mode. 00: Model 30. 01: PS/2. 10: Reserved. 11: AT Mode
1	R / W	FDC DMA Mode. 0: Burst Mode is enabled 1: Non-Burst Mode.
0	R / W	Floppy Mode. 0: Normal Floppy Mode. 1: Enhanced 3-mode FDD.

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Boot Floppy. 00: FDD A. 01: FDD B. 10: FDD C. 11: FDD D.
5~4	R / W	Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.
3~2	R / W	Density Select. 00: Normal. 01: Normal. 10: 1 (Forced to logic 1). 11: 0 (Forced to logic 0).
1	R / W	DISFDDWR => 0: Enable FDD write. 1: Disable FDD write (forces pins WE, WD stay high).
0	R / W	SWWP => 0: Normal, use WP to determine whether the FDD is write protected or not. 1: FDD is always write-protected.

CR F2h. (Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	FDD D Drive Type.
5~4	R / W	FDD C Drive Type.
3~2	R / W	FDD B Drive Type.
1~0	R / W	FDD A Drive Type.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	0: Enable FDC Pre-compensation. 1: Disable FDC Pre-compensation.
5	Reserved.	
4~3	R / W	Data Rate Table selection (Refer to TABLE A). 00: Select regular drives and 2.88 format. 01: 3-mode drive. 10: 2 Meg Tape. 11: Reserved.
2	Reserved.	
1~0	R / W	Drive Type selection (Refer to TABLE B).

CR F5h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Same as FDD0 of CR F5h.

TABLE A

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1

DRIVE RATE TABLE SELECT		DATA RATE		SELECTED DATA RATE		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0 (PIN 2)	DRVDEN1 (PIN 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5"“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	

DTYPE0	DTYPE1	DRVDEN0 (PIN 2)	DRVDEN1 (PIN 3)	DRIVE TYPE
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

17.3 Logical Device 1 (Parallel Port)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h, 78h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select PRT I/O base address. <100h : FFCh> on 4 bytes boundary (EPP not supported) or <100h : FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h. (Default 07h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PRT.

CR 74h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~3	Reserved.	

BIT	READ / WRITE	DESCRIPTION
2~0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h. (Default 3Fh)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6~3	R / W	ECP FIFO Threshold.
2~0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). 000: Standard and Bi-direction (SPP) mode. 001: EPP – 1.9 and SPP mode. 010: ECP mode. 011: ECP and EPP – 1.9 mode. 100: Printer Mode. 101: EPP – 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP – 1.7 mode.

17.4 Logical Device 2 (UART A)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 03h, F8h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 1 I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 04h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~2	Reserved.	
1~0	R / W	00: UART A clock source is 1.8462 MHz (24 MHz / 13). 01: UART A clock source is 2 MHz (24 MHz / 12). 10: UART A clock source is 24 MHz (24 MHz / 1). 11: UART A clock source is 14.769 MHz (24 MHz / 1.625).

17.5 Logical Device 3 (UART B)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 02h, F8h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Serial Port 2 I/O base address <100h : FF8h> on 8 bytes boundary.

CR 70h. (Default 03h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for Serial Port 2.

CR F0h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: No reception delay when SIR is changed from TX mode to RX mode. 1: Reception delay 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.
2	R / W	0: No transmission delay when SIR is changed from RX mode to TX mode. 1: Transmission delay 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.
1~0	R / W	00: UART B clock source is 1.8462 MHz (24 MHz / 13). 01: UART B clock source is 2 MHz (24 MHz / 12). 10: UART B clock source is 24 MHz (24 MHz / 1). 11: UART B clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Reserved.

BIT	READ / WRITE	DESCRIPTION
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Through SINB / SOUTB. 1: Through IRRX / IRTX.
5~3	R / W	IRMODE => IR function mode selection. See below table.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: SOUTB pin of UART B function or IRTX pin of IR function in normal condition. 1: Inverse SOUTB pin of UART B function or IRTX pin of IR function.
0	R / W	0: SINB pin of UART B function or IRRX pin of IR function in normal condition. 1: Inverse SINB pin of UART B function or IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX

IR MODE	IR FUNCTION	IRTX	IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

17.6 Logical Device 5 (Keyboard Controller)

CR 30h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 00h,60h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the first KBC I/O base address <100h : FFFh> on 1 byte boundary.

CR 62h, 63h. (Default 00h,64h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select the second KBC I/O base address <100h : FFFh> on 1 byte boundary.

CR 70h. (Default 01h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h. (Default 0Ch)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h. (Default83h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	KBC clock rate selection 00: 6MHz 01: 8MHz 10: 12MHz 11: 16MHz
5~3	Reserved.	
2	R / W	0: Port 92 disable. 1: Port 92 enable.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

17.7 Logical Device 7 (GPIO1, GPIO6, Game Port & MIDI Port)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: GPIO6 is inactive. 1: Activate GPIO6.
2	R / W	0: MIDI Port is inactive. 1: Activate MIDI Port.
1	R / W	0: Game Port is inactive. 1: Activate Game Port.

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO1 is inactive. 1: Activate GPIO1.

CR 60h, 61h. (Default 02h, 01h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select Game Port base address <100h : FFFh> on 1 byte boundary.

CR 62h, 63h. (Default 03h, 30h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select MIDI Port base address <100h : FFEh> on 2 bytes boundary.

CR 70h. (Default 09h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for MIDI Port.

CR F0h. (GPIO1 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an Output port 1: The respective GPIO1 PIN is programmed as an Input port.

CR F1h. (GPIO1 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. (GPIO1 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. (GPIO1 I/O register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → PLED
6	R / W	0: GPIO16 1: GPIO16 → WDTO#
5	R / W	0: GPIO15 1: GPIO15 → PLED
4	R / W	0: GPIO14 1: GPIO14 → WDTO#
3	R / W	0: GPIO13 1: GPIO13 → PLED
2	R / W	0: GPIO12 1: GPIO12 → WDTO#

BIT	READ / WRITE	DESCRIPTION
1	R / W	0: GPIO11 1: GPIO11 → PLED
0	R / W	0: GPIO10 1: GPIO10 → WDTO#

CR F4h. (GPIO6 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an Output port 1: The respective GPIO6 PIN is programmed as an Input port.

CR F5h. (GPIO6 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. (GPIO6 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. (Game Port PAD control register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	Joystick Power Down 0: Joystick Power Down Disable. 1: Joystick Power Down Enable.

17.8 Logical Device 8 (WDTO# & PLED)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: WDTO# is inactive. 1: Activate WDTO#.

CR F5h. (WDTO#, PLED and KBC P20 control mode register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Select Power LED mode. 00: Power LED pin is tri-stated. 01: Power LED pin is driven low. 10: Power LED pin outputs 1Hz pulse with 50% duty cycle. 11: Power LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
5	Reserved.	
4	R / W	Faster 1000 times for WDTO# count mode. 0: Disable. 1: Enable. (If bit-3 is Second Mode , the count mode be 1/1000 Sec.) (If bit-3 is Minute Mode , the count mode be 1/1000 Min.)
3	R / W	Select WDTO# count mode. 0: Second Mode. 1: Minute Mode.

BIT	READ / WRITE	DESCRIPTION
2	R / W	Enable the rising edge of KBC reset (P20) to issue time-out event. 0: Disable. 1: Enable.
1	R / W	Disable / Enable the WDTO# output low pulse to the KBRST# pin (PIN60) 0: Disable. 1: Enable.
0	Reserved.	

CR F6h. (WDTO# counter register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. If the bit 7 and 6 of CR F7h are set, any Mouse Interrupt or Keyboard Interrupt event will also cause the reload of previously-loaded non-zero value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after 1 second/minute 02h: Time-out occurs after 2 second/minutes 03h: Time-out occurs after 3 second/minutes ……..... FFh: Time-out occurs after 255 second/minutes

CR F7h. (WDTO# control & status register; Default 00h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by mouse interrupt. 1: Watchdog timer is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset watch-dog timer enable 0: Watchdog timer is not affected by keyboard interrupt. 1: Watchdog timer is reset by keyboard interrupt.
5	Write “1” Only	Trigger WDTO# event. This bit is self-clearing.
4	R / W	WDTO# status bit 0: Watchdog timer is running. 1: Watchdog timer issues time-out event.
3~0	R / W	These bits select IRQ resource for WDTO#. (02h for SMI# event.)

17.9 Logical Device 9 (GPIO2,GPIO3, GPIO4, GPIO5 & SUSLED) (VSB Power)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: GPIO5 is inactive. 1: Activate GPIO5
2	R / W	0: GPIO4 is inactive. 1: Activate GPIO4.
1	R / W	0: GPIO3 is inactive. 1: Activate GPIO3.
0	R / W	0: GPIO2 is inactive. 1: Activate GPIO2.

CR E0h. (GPIO5 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an Output port 1: The respective GPIO5 PIN is programmed as an Input port.

CR E1h. (GPIO5 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. (GPIO5 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. (GPIO2 register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an Output port 1: The respective GPIO2 PIN is programmed as an Input port

CR E4h. (GPIO2 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E5h. (GPIO2 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F0h. (GPIO3 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an Output port 1: The respective GPIO3 PIN is programmed as an Input port.

CR F1h. (GPIO3 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. (GPIO3 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. (Suspend LED mode register; Default 00h) **(VBAT power)**

BIT	READ / WRITE	DESCRIPTION
7~6	R / W	Select Suspend LED mode. 00: Suspend LED pin is tri-stated. 01: Suspend LED pin is driven low. 10: Suspend LED pin outputs 1Hz pulse with 50% duty cycle. 11: Suspend LED pin outputs $^1/_4$Hz pulse with 50% duty cycle.
5~0	Reserved.	

CR F4h. (GPIO4 I/O register; Default FFh)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an Output port 1: The respective GPIO4 PIN is programmed as an Input port.

CR F5h. (GPIO4 Data register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Data register For Output ports, the respective bits can be read/written and produced to pins.
	Read Only	For Input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. (GPIO4 Inversion register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. (GPIO4 multi-function select register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → SUSLED
6	R / W	0: GPIO46 1: GPIO46 → WDTO#
5	R / W	0: GPIO45 1: GPIO45 → SUSLED
4	R / W	0: GPIO44 1: GPIO44 → WDTO#
3	R / W	0: GPIO43 1: GPIO43 → SUSLED
2	R / W	0: GPIO42 1: GPIO42 → WDTO#
1	R / W	0: GPIO41 1: GPIO41 → SUSLED
0	R / W	0: GPIO40 1: GPIO40 → WDTO#

17.10 Logical Device A (ACPI)

(CR30, CR70 are VCC powered; CRE0~F7 are VRTC powered)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for PME#.

CR E0h. (Default 01h) **(VBAT power)**

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_PSIN => Disable panel switch input to turn system power supply on. 0: PSIN is wire-AND and connected to PSOUT#. 1: PSIN is blocked and cannot affect PSOUT#.
6	R / W	Enable KBC wake-up 0: Disable keyboard wake-up function via PSOUT#. 1: Enable keyboard wake-up function via PSOUT#.
5	R / W	Enable Mouse wake-up 0: Disable mouse wake-up function via PSOUT#. 1: Enable mouse wake-up function via PSOUT#.

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the following table for the detailed.

<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of either left or right MS button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the MS left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the MS right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the MS left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the MS right button.</td></tr>
</table>
</td></tr>
<tr><td>3</td><td colspan="2">Reserved.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from keyboard can wake up the system.</td></tr>
</table>

CR E1h. (KBC Wake-Up Index Register; Default 00h) **(VSB power)**

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up index register. It is the index register of CRE2, which is the access window of keyboard pre-determined key combination characters. The first set of wake up key combination is in the range of 0x00 - 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combination can be read through 0x10 – 0x1E.

CR E2h. (KBC Wake-Up Data Register; Default ffh) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	Keyboard wake-up data register. It is the data register of the keyboard pre-determined key combination characters, which is indexed by CRE1.

CR E3h. (Event Status Register; Default 08h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	Read Only Read-Clear	This event status is caused by VSB power off/on.
4	Read Only Read-Clear	If E4[7] is 1 => This bit is 0: When power-loss occurs and VSB power is on, indicate that turn on system power. This bit is 1: When power-loss occurs and VSB power is on, indicate that turn off system power. If E4[7] is 0 => This bit is always 0.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: The thermal shutdown event issued.

BIT	READ / WRITE	DESCRIPTION
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: The PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: The mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: The keyboard wake-up event issued.

CR E4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	Power loss control bit 2 0： Indicates that PSON#（Pin 72）outputs logic low after PSOUT# issues a low pulse. 1： Indicates that PSON#（Pin 72）will output logic low after resume from AC power loss if SUSB#（Pin 73）is logic high.
6~5	R / W	Power loss control bits <1：0> => **(VBAT)** 00: System always turns off when come back from power loss state. 01: System always turns on when come back from power loss state. 10: System turns off / on when come back from power loss state depend on the state before power loss. 11: User define the state before power loss.(The last state set at CRE6[4])
4	Reserved	
3	R / W	Keyboard wake-up options. **(LRESET#)** (e) 0: Password or sequence hot keys programmed in the registers. 1: Any key.

BIT	READ / WRITE	DESCRIPTION
2	R / W	Enable the hunting mode for all wake-up events set in CRE0. This bit is cleared when any wake-up events is captured. **(LRESET#)** 0: Disable. 1: Enable.
1~0	Reserved.	

CR E5h. (Reserved)

BIT	READ / WRITE	DESCRIPTION
7~0	Reserved.	

CR E6h. (Default 1Ch)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => **(VSB)** 3 keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.
6	Reserved.	
5	R / W	CASEOPEN Clear Control. **(VSB)** Write 1 to this bit will clear CASEOPEN status. This bit won't be self cleared, please write 0 after event be cleared. The function is as same as Index 46h bit 7 of H/W Monitor part.
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF.
3	R / W	PWROK_DEL (first stage) **(VSB)** Set the delay rising time from PWROK_LP to PWROK_ST. 0: 300 ~ 600 ms. 1: 200 ~ 300 ms.

BIT	READ / WRITE	DESCRIPTION
2~1	R / W	PWROK_DEL **(VSB)** Set the delay rising time from PWROK_ST to PWROK. 00: No delay time. 01: Delay 32 ms 10: 96 ms 11: Delay 250 ms
0	R / W-Clear	PWROK_TRIG => Write 1 to re-trigger POWEROK signals from low to high.

CR E7h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => **(VSB)** Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => **(VSB)** Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => **(VSB)** Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.

BIT	READ / WRITE	DESCRIPTION
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s long PSOUT# pulse when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (for SiS & VIA chipsets) 0: Disable. 1: Enable.
3	R / W	Select WDTO# reset source **(VSB)** 0: Watchdog timer is reset by LRESET#. 1: Watchdog timer is reset by PWROK
2~1	Reserved.	
0	R / W	Hardware Monitor RESET source select **(VBAT)** 0: PWROK 1: LRESET#

CR E8h. (Reserved)

CR F2h. (Default 7Ch) (VSB power)

BIT	READ / WRITE	DESCRIPTION
7	Reserved.	
6	R / W	Enable RSTOUT4# function. 0: Disable RSTOUT4#. 1: Enable RSTOUT4#.
5	R / W	Enable RSTOUT3# function. 0: Disable RSTOUT3#. 1: Enable RSTOUT3#.
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#.
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#.
1	Reserved.	
0	R / W	EN_PME => 0: Disable PME. 1: Enable PME.

CR F3h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W-Clear	PME status of the Mouse IRQ event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC IRQ event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the FDC IRQ event. Write 1 to clear this status.
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDTO# event. Write 1 to clear this status.
1	R / W-Clear	PME status of the MIDI IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F6h. (Default 00h) **(VSB power)**

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5	R / W	0: Disable PME interrupt of the Mouse IRQ event. 1: Enable PME interrupt of the Mouse IRQ event.
4	R / W	0: Disable PME interrupt of the KBC IRQ event. 1: Enable PME interrupt of the KBC IRQ event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	R / W	0: Disable PME interrupt of the FDC IRQ event. 1: Enable PME interrupt of the FDC IRQ event.
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h. (Default 00h) **(VSB power)**

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3	R / W	0: Disable PME interrupt of the HM IRQ event. 1: Enable PME interrupt of the HM IRQ event.
2	R / W	0: Disable PME interrupt of the WDTO# event. 1: Enable PME interrupt of the WDTO# event.
1	R / W	0: Disable PME interrupt of the MIDI IRQ event. 1: Enable PME interrupt of the MIDI IRQ event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

17.11 Logical Device B (Hardware Monitor, for W83627EHF/EHG only)

CR 30h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~1	Reserved.	
0	R / W	0: Logical device is inactive. 1: Activate the logical device.

CR 60h, 61h. (Default 00h, 00h)

BIT	READ / WRITE	DESCRIPTION
7~0	R / W	These two registers select HM base address <100h : FFEh> on 2 bytes boundary.

CR 70h. (Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~4	Reserved.	
3~0	R / W	These bits select IRQ resource for HM.

CR F0h. (VID Control register; Default C1h)

BIT	READ / WRITE	DESCRIPTION
7	R / W	VID I/O Control (CRF1[5:0]) 0: VID output mode. 1: VID input mode.
6-0	Reserved.	

CR F1h. (VID Data Register; Default 00h)

BIT	READ / WRITE	DESCRIPTION
7~6	Reserved.	
5~0	R / W	VID[5:0] Data Register.

18. SPECIFICATIONS

18.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	3.3V ± 5%	V
VI	Input Voltage	-0.5 to 3VCC+0.5	V
	Input Voltage (5V tolerance)	-0.5 to 6	V
VBAT	RTC Battery Voltage VBAT	2.2 to 4.0	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

18.2 DC CHARACTERISTICS

(T_a = 0°C to 70°C, V_{DD} = 3.3V ± 5%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RTC Battery Quiescent Current	IBAT			2.4	μA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	I_{SB}			2.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
I/O_{8t} - TTL level bi-directional pin with 8mA source-sink capability						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOL = 8 mA
Output High Voltage	VOH	2.4			V	IOH = - 8 mA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12t} - TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24t} - TTL level bi-directional pin with 24mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12tp3} – 3.3V TTL level bi-directional pin with 12mA source-sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} - TTL level Schmitt-trigger bi-directional pin with 12mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24ts} - TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}= 3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{24tsp3} – 3.3V TTL level Schmitt-trigger bi-directional pin with 24mA source-sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{12t} - TTL level bi-directional pin and open-drain output with 12mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{24t} - TTL level bi-directional pin and open-drain output with 24mA sink capability						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{12ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD_{24ts} - TTL level Schmitt-trigger bi-directional pin and open drain output with 24mA sink capability						

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	
Hystersis	V_{TH}	0.5	1.2		V	V_{DD}=3.3V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/OD12$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD16$_{cs}$ - CMOS level Schmitt-trigger bi-directional pin and open drain output with 16mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD12$_{csd}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull down resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
I/OD12$_{csu}$ - CMOS level Schmitt-trigger bi-directional pin with internal pull up resistor and open drain output with 12mA sink capability						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
O4 - Output pin with 4mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -4 mA
O8 - Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
O_{12} - Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
O_{16} - Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
O_{24} - Output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
O_{12p3} - 3.3V output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{24p3} - 3.3V output pin with 24mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12} - Open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{24} - Open drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
OD_{12p3} - 3.3V open drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tp3} - 3.3V TTL level input pin						

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{td} - TTL level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tu} - TTL level input pin with internal pull up resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{tsp3} - 3.3 V TTL level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3 V

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_C - CMOS level input pin						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cd} - CMOS level input pin with internal pull down resistor						
Input Low Voltage	V_{IL}			1.5	V	
Input High Voltage	V_{IH}	3.5			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{cs} - CMOS level Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	1.3	1.5	1.7	V	V_{DD} = 3.3V
Hystersis	V_{TH}	1.5	2		V	V_{DD} = 3.3V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{csu} - CMOS level Schmitt-trigger input pin with internal pull up resistor						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 3.3V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 3.3V

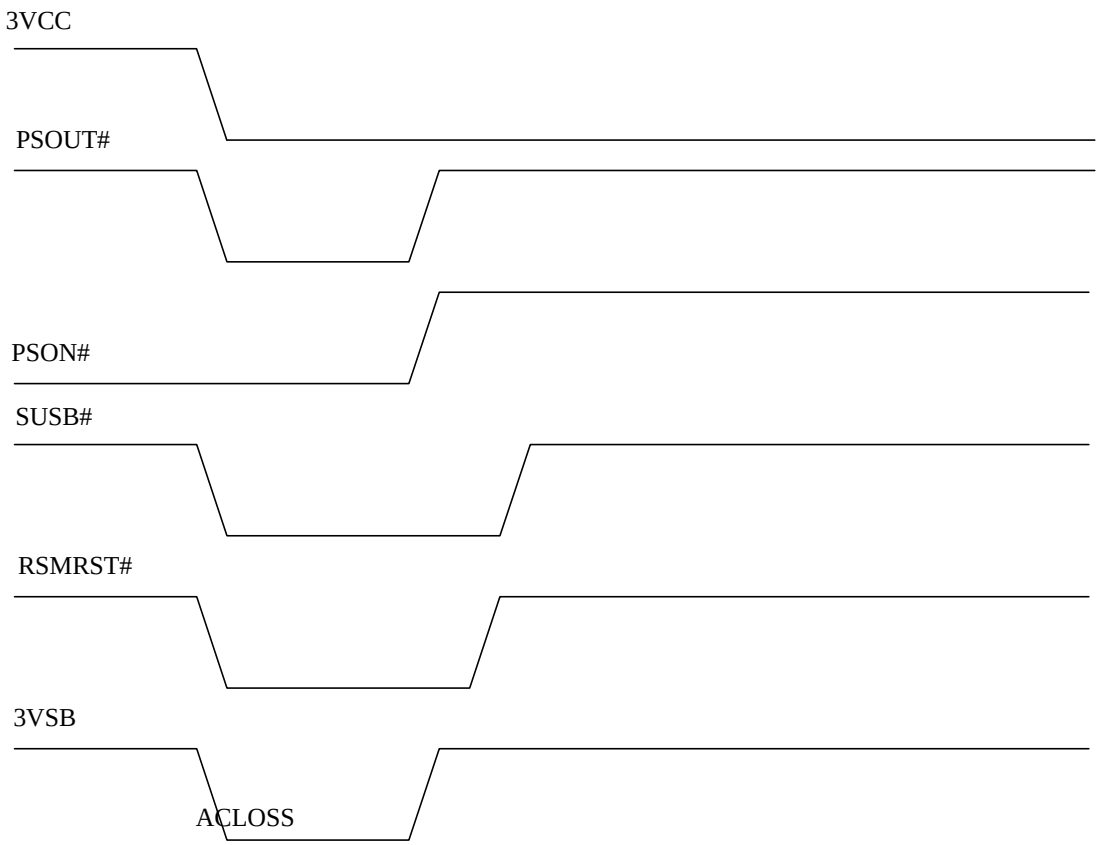
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Hystersis	V_{TH}	0.5	1.2		V	V_{DD} = 3.3V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

18.3 AC CHARACTERISTICS

18.3.1 AC Power Failure Resume Timing

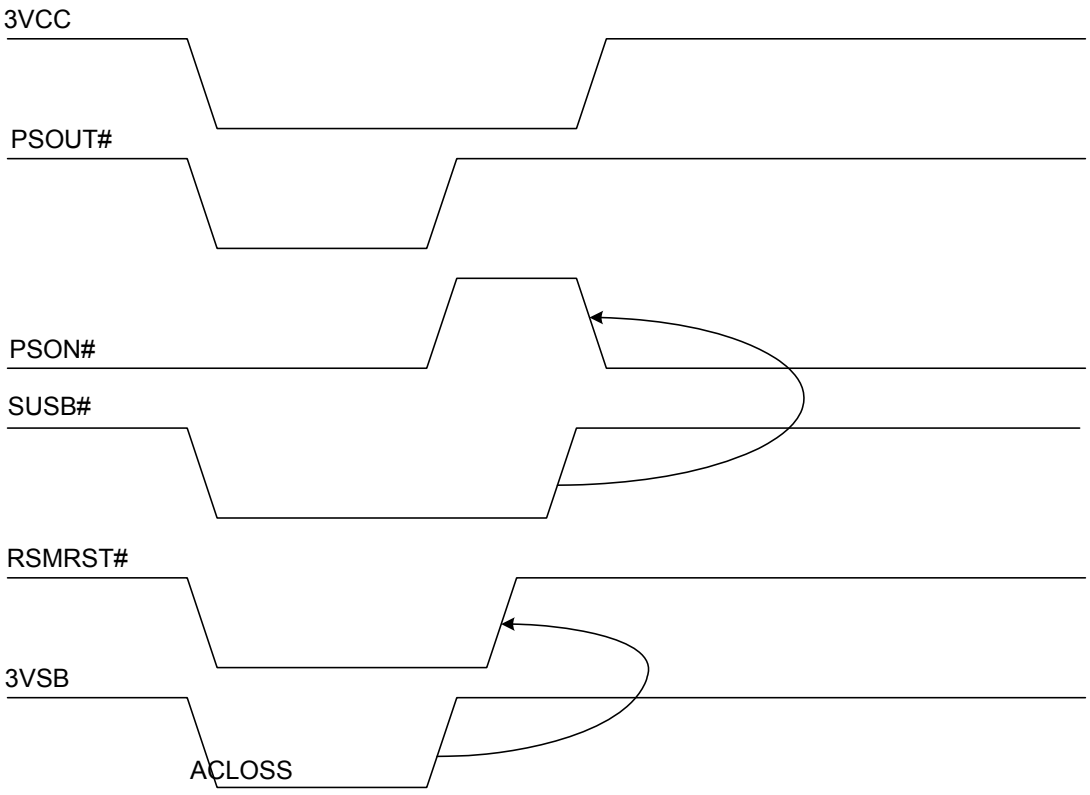
1. Logical Device A, CR[E4h] bit7 = “0” and CR[E4h] bits[6:5] are selected to “OFF” state

(“OFF” means always being turned off or the previous state is off)



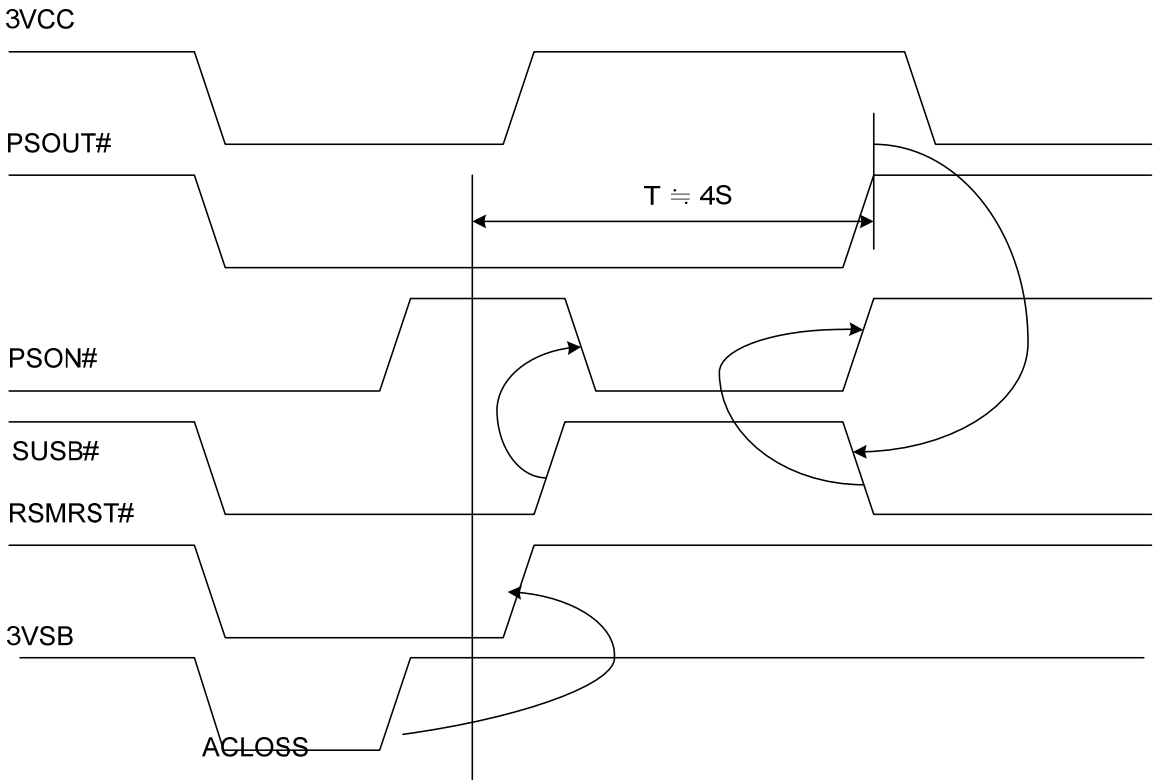
2. Logical Device A, CR[E4h] bit7 = “0” and CR[E4h] bits[6:5] are selected to “ON” state

(“ON” means always being turned on or the previous state is on)



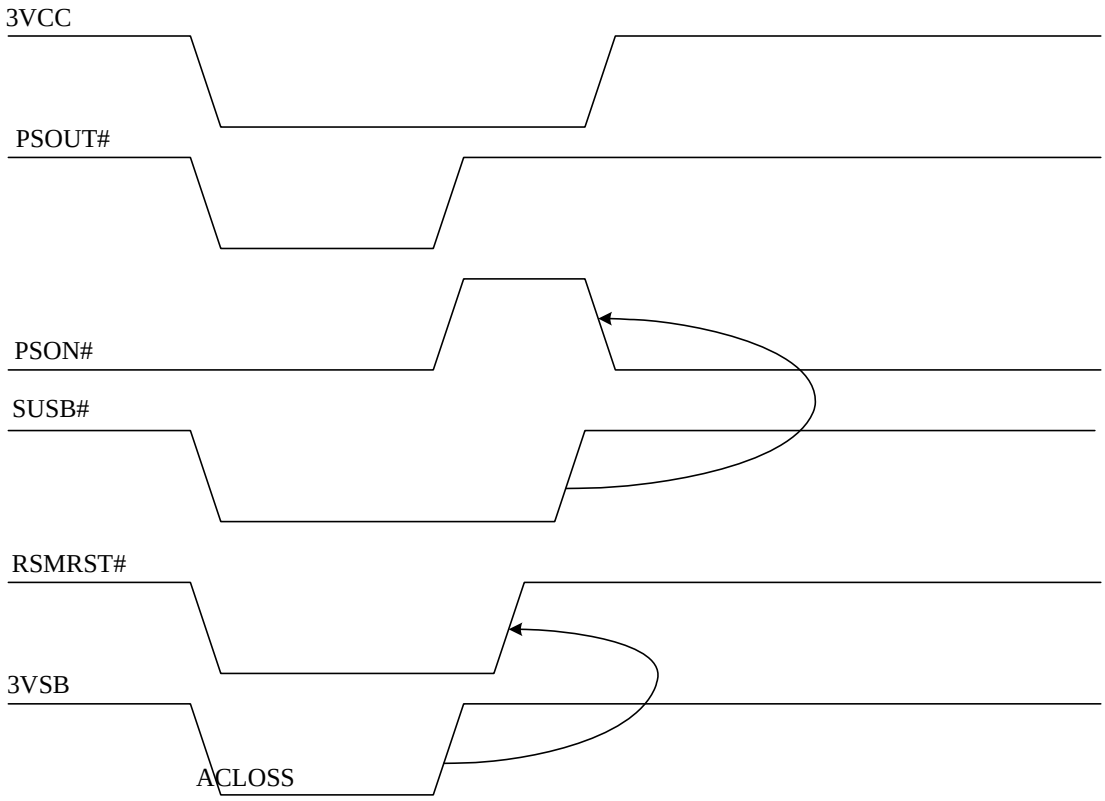
3. Logical Device A, CR[E4h] bit7 = “1” and CR[E4h] bits[6:5] are selected to “OFF” state

(“OFF” means always being turned off or the previous state is off)



4. Logical Device A, CR[E4h] bit7 = “1” and CR[E4h] bits[6:5] are selected to “ON” state

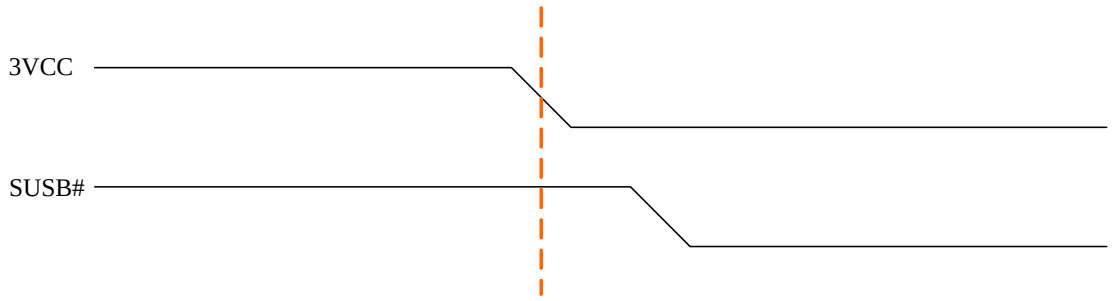
(“ON” means always being turned on or the previous state is on)



**** What's the definition of former state at AC power failure?**

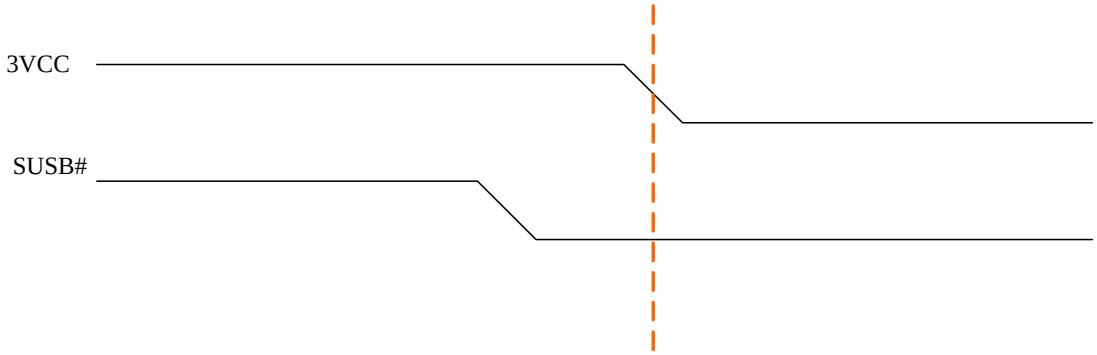
1) The previous state is "ON"

3VCC falls to 2.6V and SUSB# keeps at VIH 2.0V



2) The previous state is "OFF"

3VCC falls to 2.6V and SUSB# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the W83627EHF/EHG/EF/EG adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Logical Device A, CR E4h

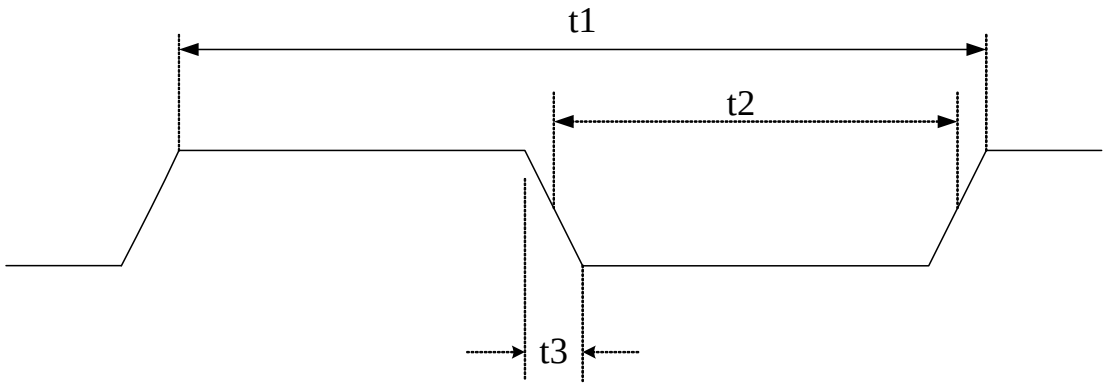
6~5	R / W	Power-loss control bits => (**VBAT**) 00: System always turns off when it returns from power-loss state. 01: System always turns on when it returns from power-loss state. 10: System turns off / on when it returns from power-loss state depending on the state before the power loss. 11: User defines the state before the power loss.(The previous state is set at CRE6[4])

Logical Device A, CR E6h

4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

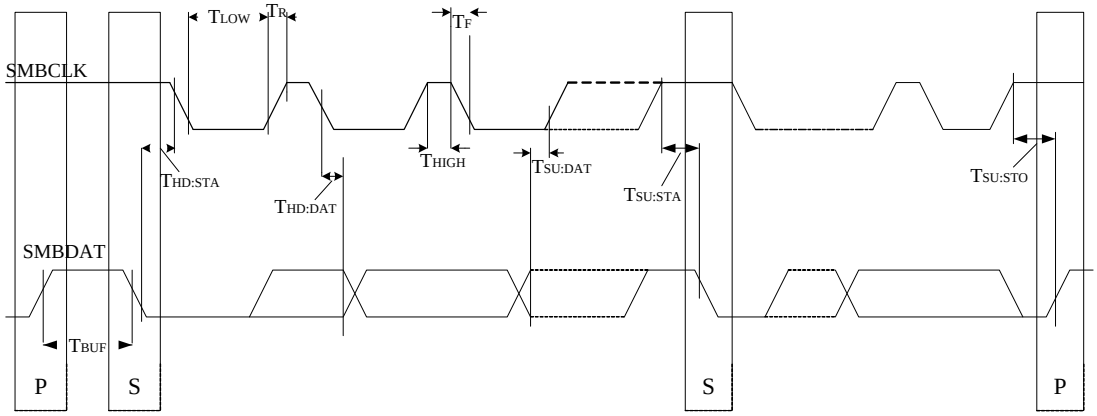
18.3.2 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

18.3.3 SMBus Timing



SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_{BUF}	Bus Free Time between Stop and Start Condition	4.7	-	uS
$T_{HD:STA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated	4.0	-	uS
$T_{SU:STA}$	Repeated Start Condition setup time	4.7	-	uS
$T_{SU:STO}$	Stop Condition setup time	4.0	-	uS
$T_{HD:DAT}$	Data hold time	2.3	-	uS
$T_{SU:DAT}$	Data setup time	0	-	nS
T_{LOW}	Clock low period	4.7	-	uS
T_{HIGH}	Clock high period	4.0	50	uS
T_F	Clock/Data Falling Time	-	300	nS
T_R	Clock/Data Rising Time	-	1000	nS

18.3.4 Floppy Disk Drive Timing

FDC: Data rate = 1MB, 500KB, 300KB, 250KB/sec.

PARAMETER	SYM.	MIN.	TYP. (NOTE 1)	MAX.	UNIT
DIR# setup time to STEP#	TDST	1.0/1.6 /2.0/4.0			µS
DIR# hold time from STEP#	TSTD	24/40 /48/96			µS
STEP# pulse width	TSTP	6.8/11.5 /13.8/27.8	7/11.7 /14/28	7.2/11.9 /14.2/28.2	µS
STEP# cycle width	TSC	NOTE 2	NOTE 2	NOTE 2	mS
INDEX# pulse width	TIDX	125/250 /417/500			nS
RDATA# pulse width	TRD	40			nS
WD# pulse width	TWD	100/185 /225/475	125/210 /250/500	150/235 /275/525	nS

Notes:

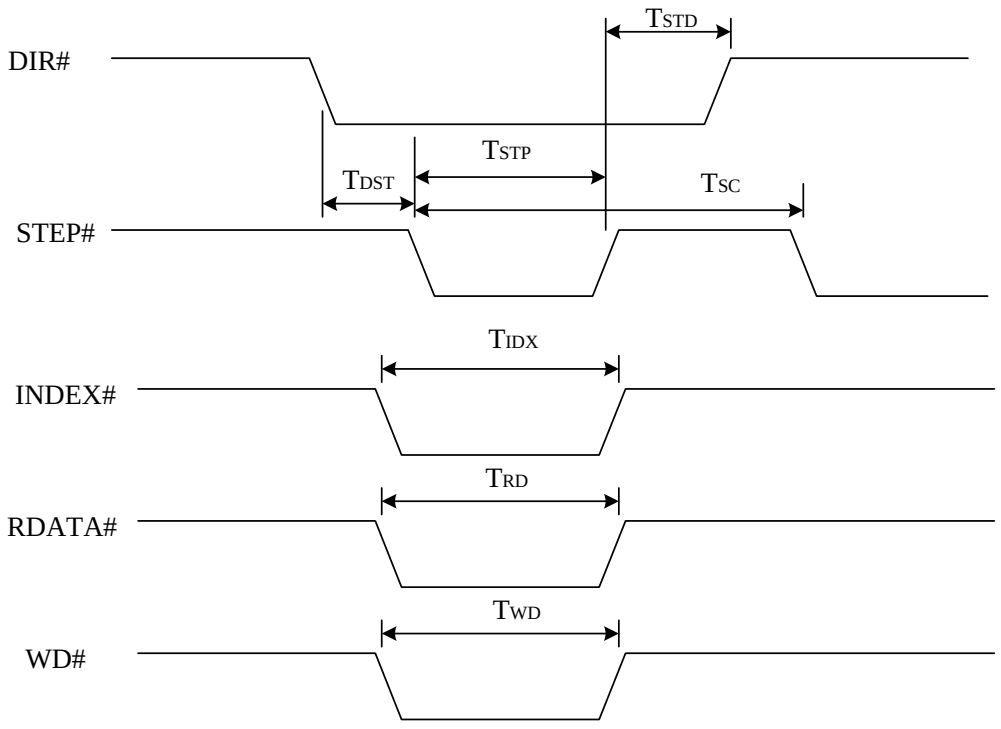
1. Typical values for T = 25°C and normal supply voltage.
2. Programmable from 0.5 mS through 32 mS as described in step rate table.
   (Please refer to the description of the SPECIFY command set.)

Step Rate Table

DATA RATE / SRT	1MB/S	500KB/S	300KB/S	250KB/S

DATA RATE / SRT	1MB/S	500KB/S	300KB/S	250KB/S
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1.0	2	3.33	4
F	0.5	1	1.67	2

Floppy Disk Driving Timing



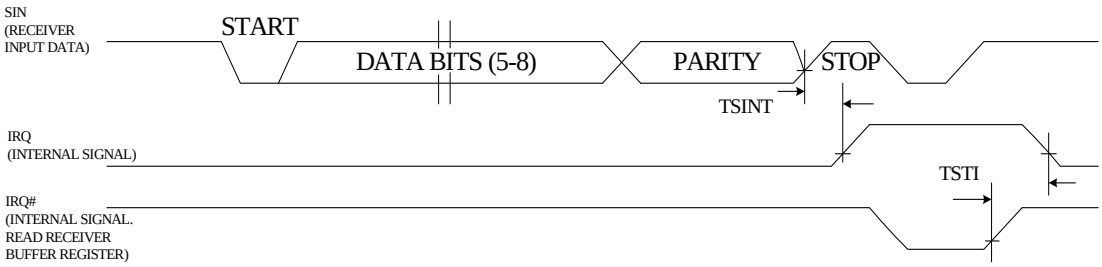
18.3.5 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT

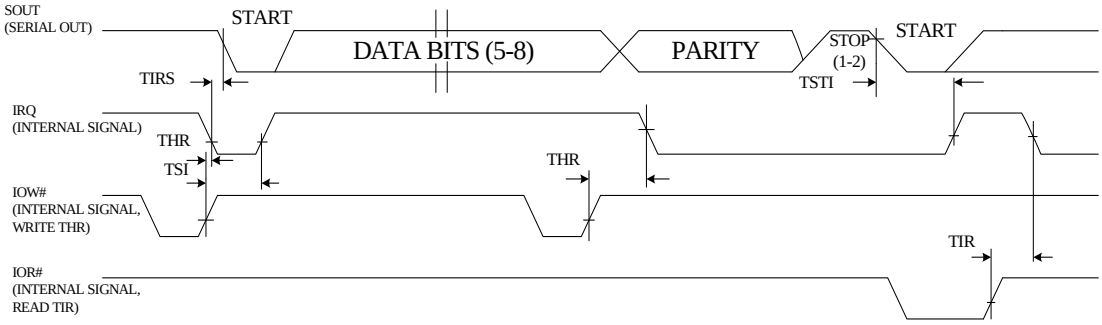
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

Receiver Timing

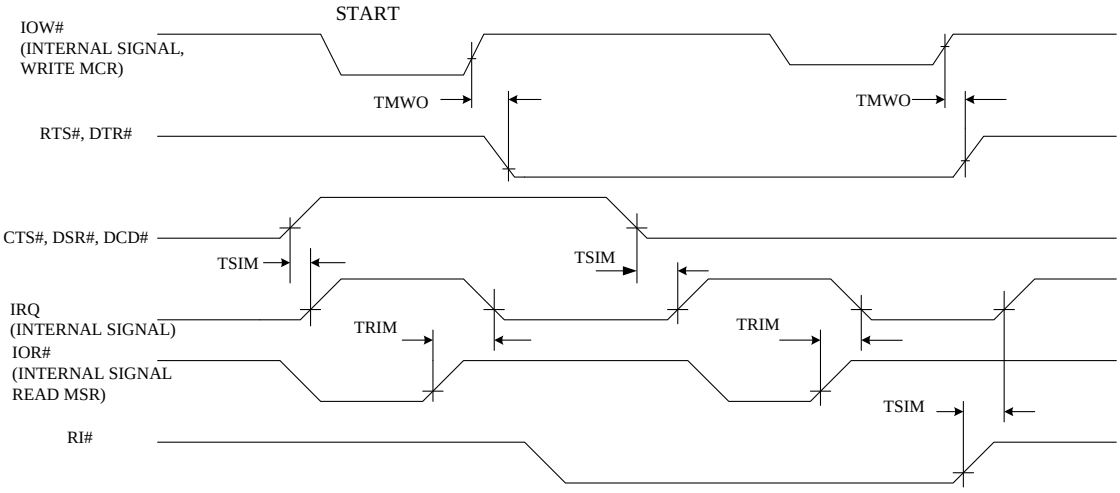


UART Transmitter Timing



18.3.5.1. Modem Control Timing

MODEM Control Timing

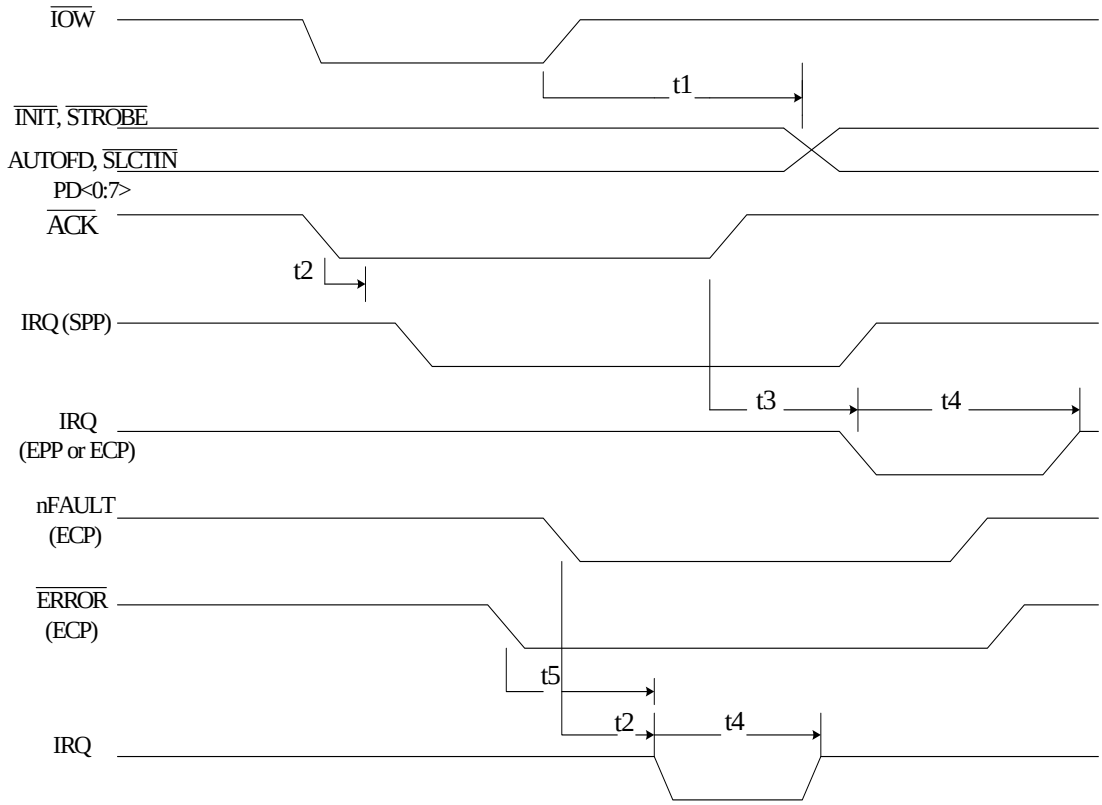


18.3.6 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

18.3.7 Parallel Port

18.3.7.1. Parallel Port Timing



18.3.7.2. EPP Data or Address Read Cycle Timing Parameters

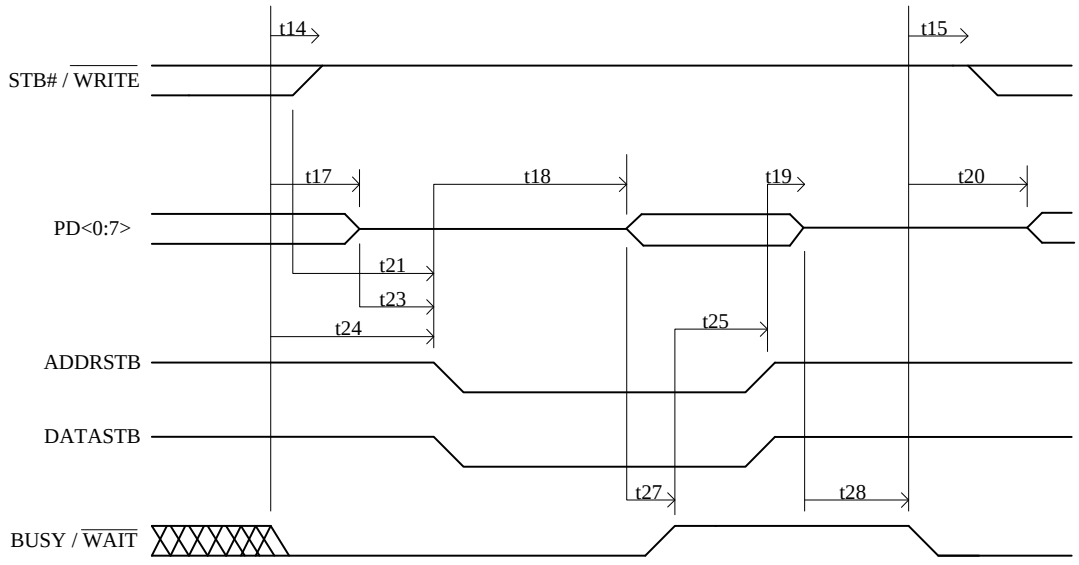
PARAMETER	SYM.	MIN.	MAX.	UNIT
WAIT Asserted to WRITE Deasserted	t14	0	185	nS
Deasserted to WRITE Modified	t15	60	190	nS
WAIT Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
WAIT Deasserted to PD Drive	t20	60	190	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS
PARAMETER	SYM.	MIN.	MAX.	UNIT
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	μS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		μS

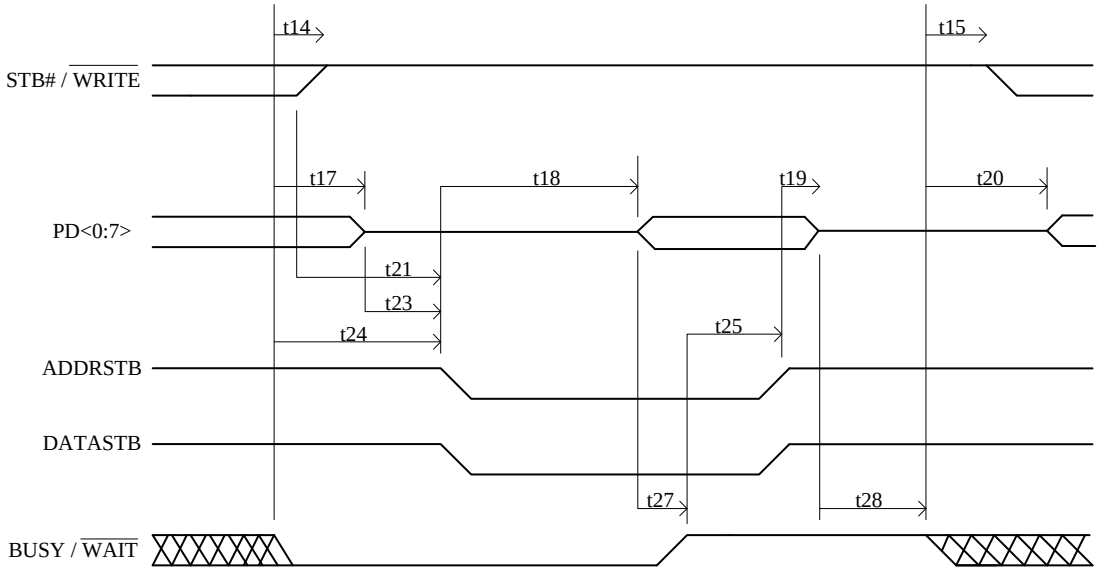
18.3.7.3. EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



18.3.7.4. EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



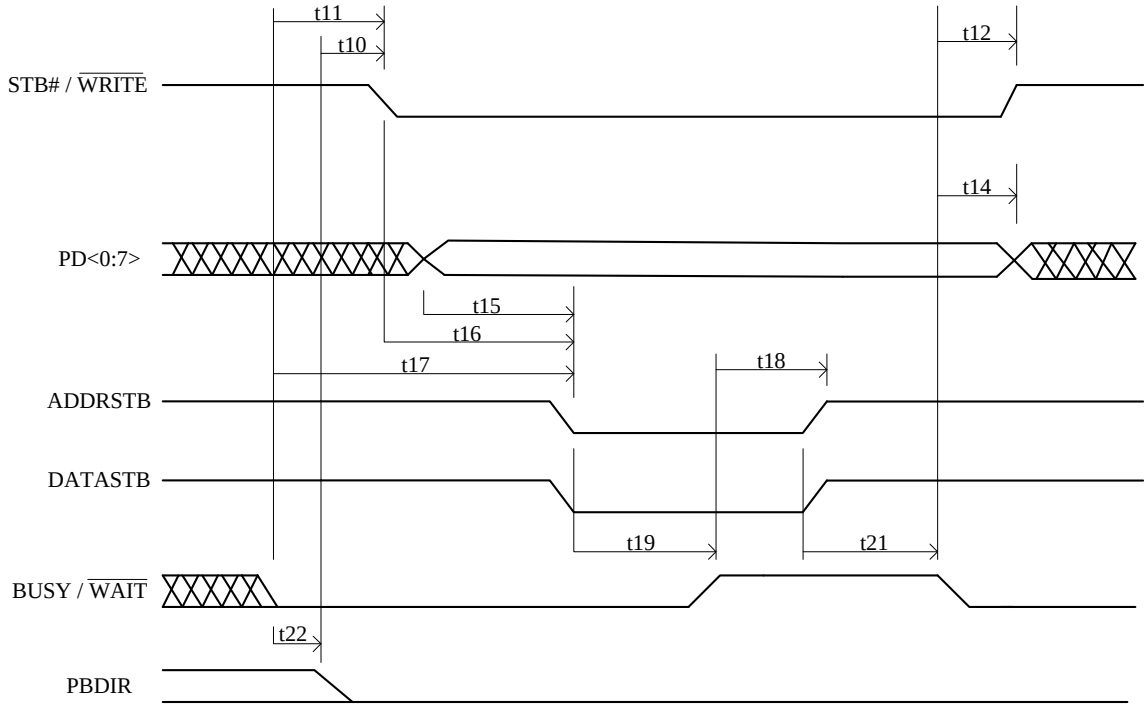
18.3.7.5. EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	μS
Time out	t20	10	12	μS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{WRITE}}$ Deasserted and PD invalid	t22	0		nS
$\overline{\text{WRITE}}$ to Command Asserted	t16	5	35	nS

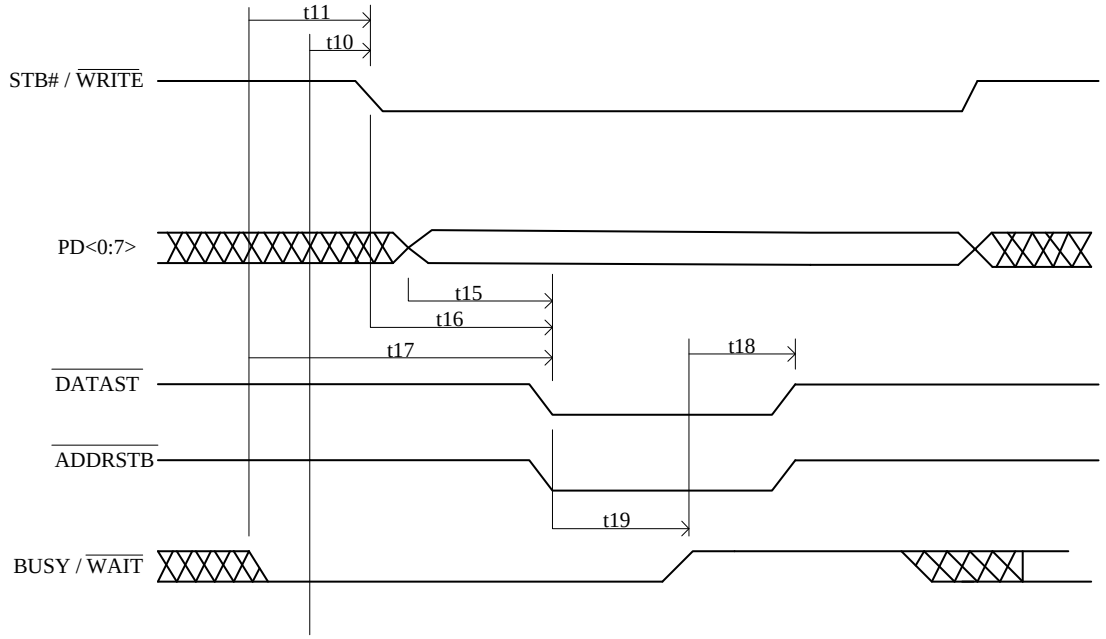
18.3.7.6. EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



18.3.7.7. EPP Data or Address Write Cycle (EPP Version 1.7)

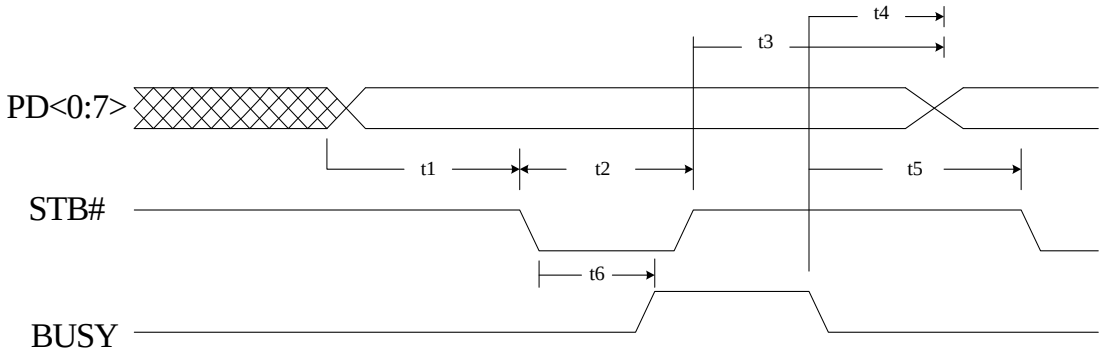
EPP Data or Address Write Cycle (EPP Version 1.7)



18.3.7.8. Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

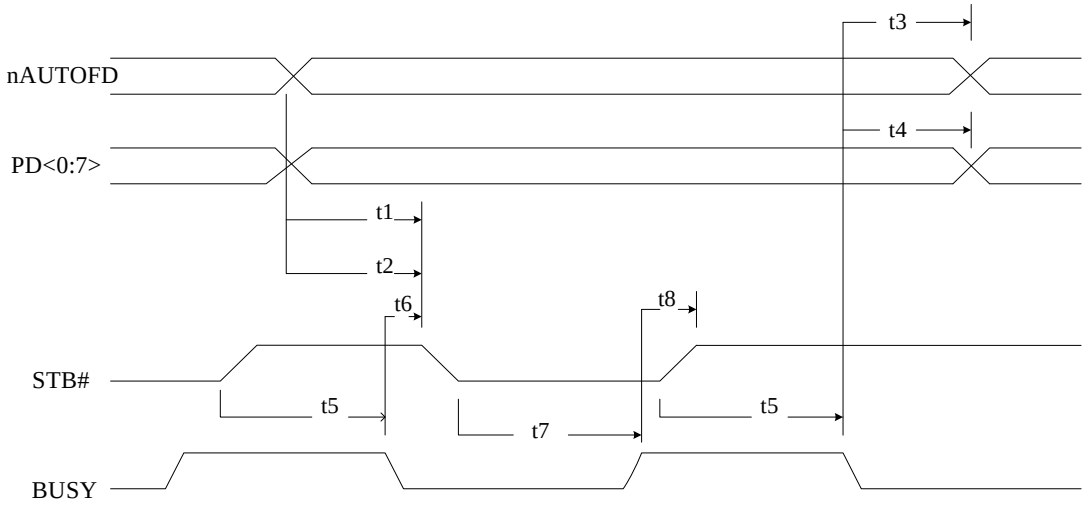
18.3.7.9. Parallel FIFO Timing



18.3.7.10. ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

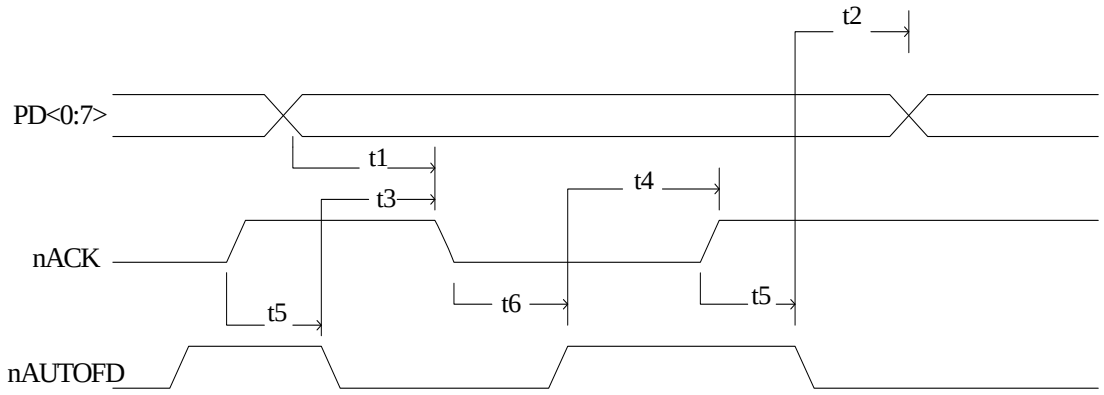
18.3.7.11. ECP Parallel Port Forward Timing



18.3.7.12. ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

18.3.7.13. ECP Parallel Port Reverse Timing

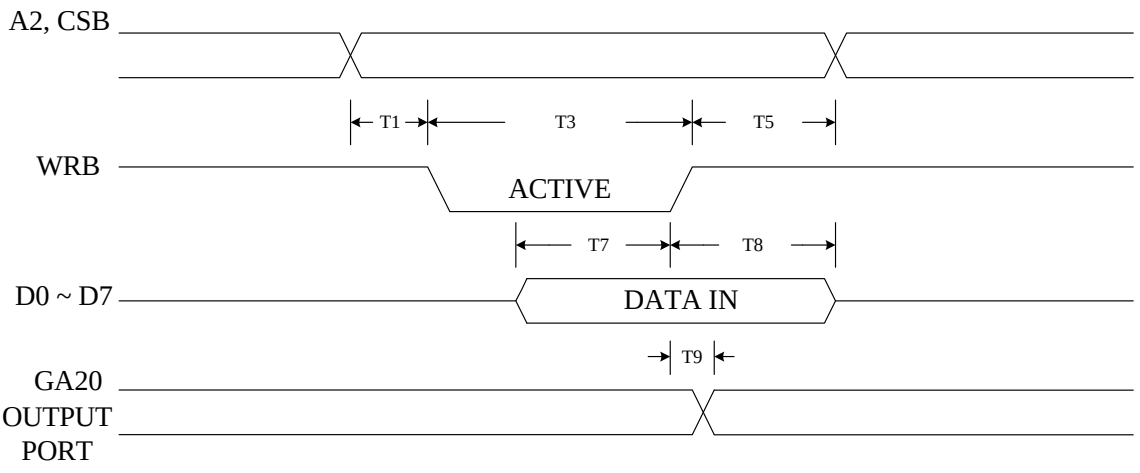


18.3.8 KBC Timing Parameters

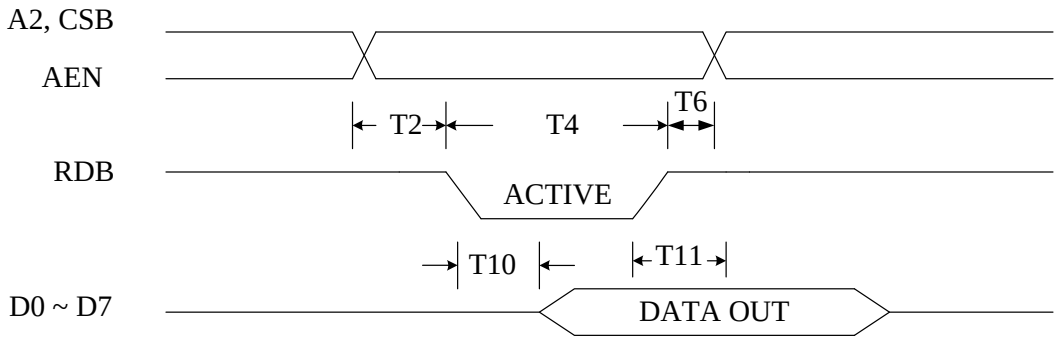
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	μS
T13	K/B Clock Period	20		μS
T14	K/B Clock Pulse Width	10		μS

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
T15	Data Valid Before Clock Falling (RECEIVE)	4		μS
T16	K/B ACK After Finish Receiving	20		μS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		μS
T21	Input Clock Period (6–16 Mhz)	63	167	nS
T22	Duration of CLK inactive	30	50	μS
T23	Duration of CLK active	30	50	μS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	μS
T25	Time of inhibit mode	100	300	μS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	μS
T27	Duration of CLK inactive	30	50	μS
T28	Duration of CLK active	30	50	μS
T29	Time from DATA transition to falling edge of CLK	5	25	μS

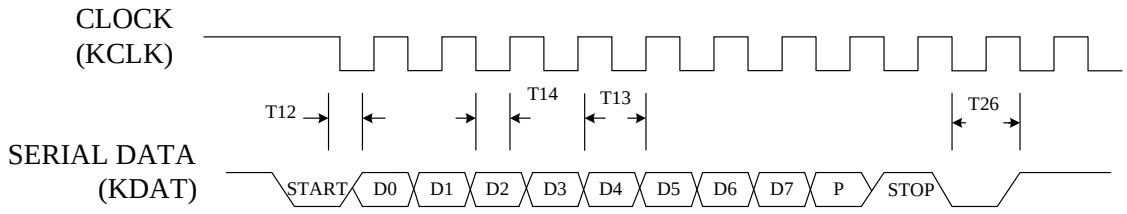
18.3.8.1. Writing Cycle Timing



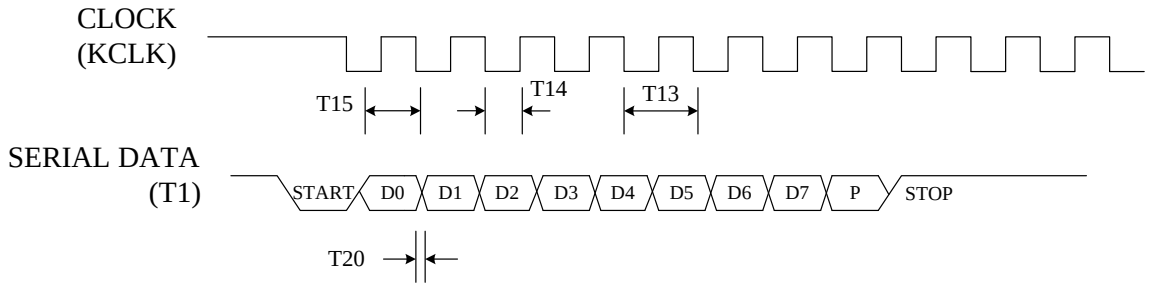
18.3.8.2. Read Cycle Timing



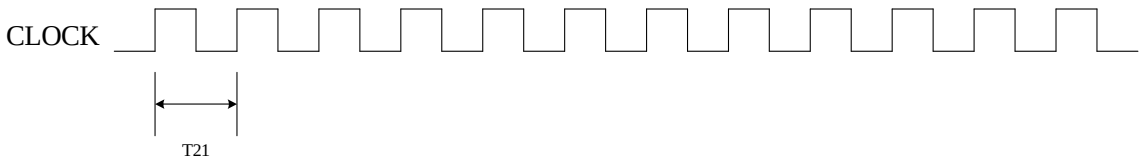
18.3.8.3. Send Data to K/B



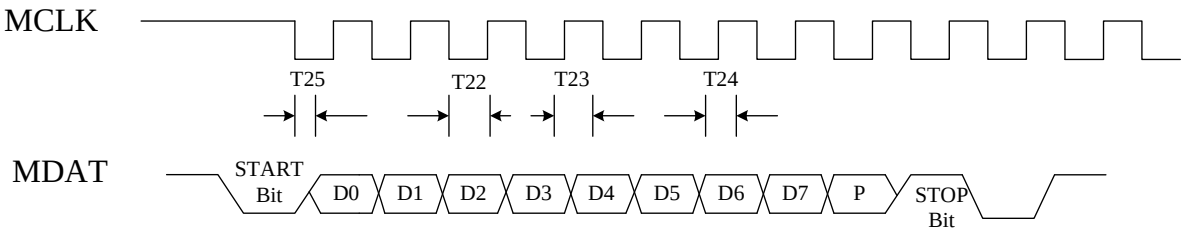
18.3.8.4. Receive Data from K/B



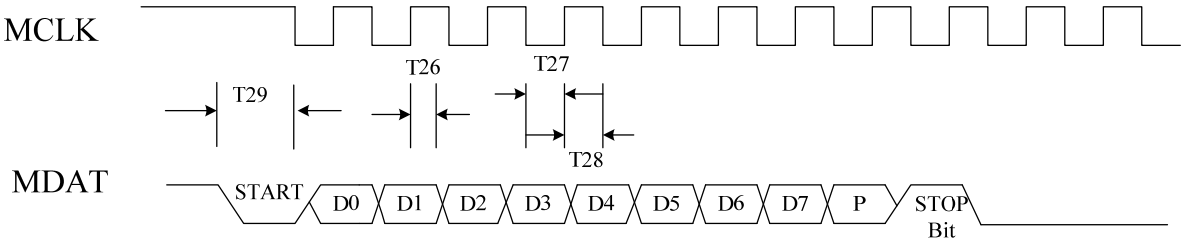
18.3.8.5. Input Clock



18.3.8.6. Send Data to Mouse



18.3.8.7. Receive Data from Mouse



18.3.9 GPIO Timing Parameters

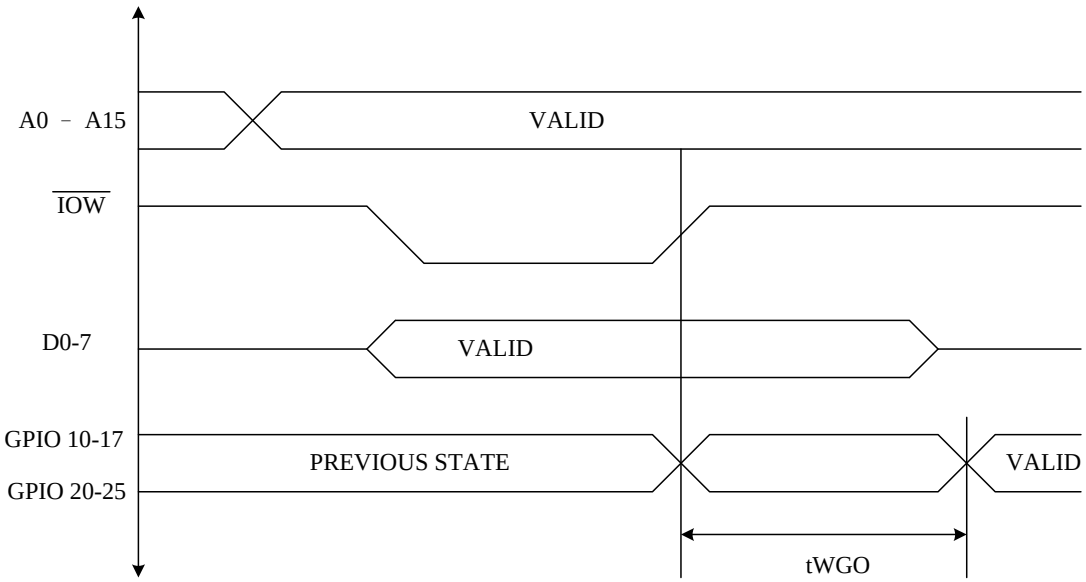
SYMBOL	PARAMETER	MIN.	MAX.	UNIT

t_{WGO}	Write data to GPIO update		300(Note 1)	ns
t_{SWP}	SWITCH pulse width	16		msec

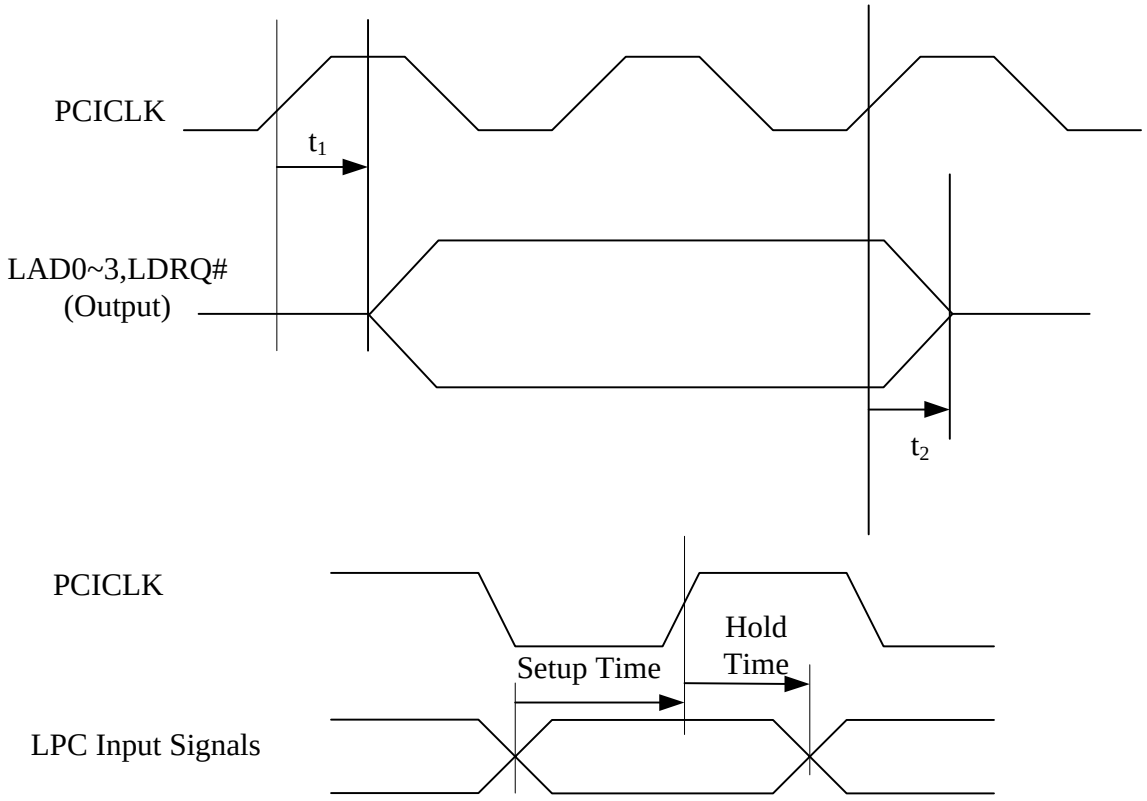
Note: Refer to Microprocessor Interface Timing for Read Timing.

18.3.9.1. GPIO Write Timing

GPIO Write Timing diagram

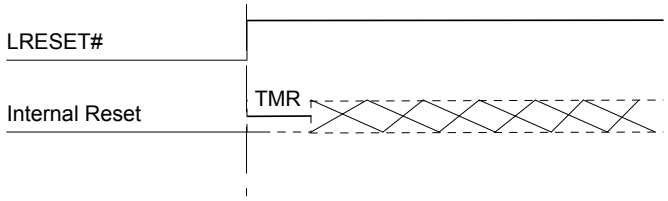


18.4 LPC Timing



SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
t_1	Output Valid Delay	4	11	nS
t_2	Float Delay	4	11	nS
t_3	LAD[3:0] Setup Time	14		nS
t_4	LAD[3:0] Hold Time	0		nS
t_5	LFRAME# Setup Time	12		nS
t_6	LFRAME# Hold Time	0		nS
t_7	Period	30	33.3	nS

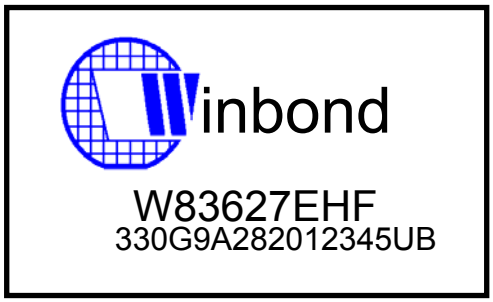
18.5 Reset Timing

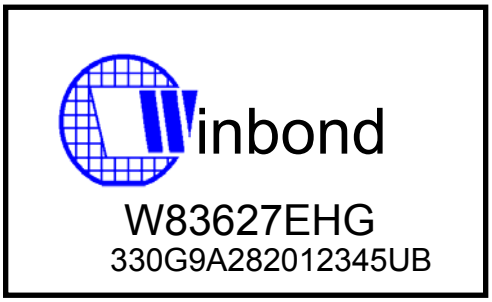


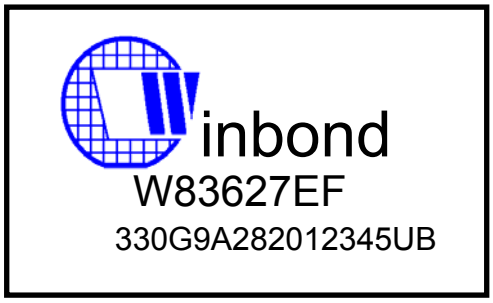
SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
TMR	Internal Reset Time	30	33.3	nS

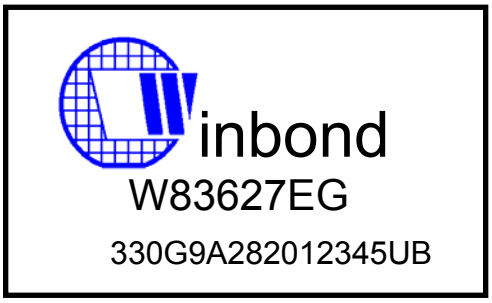
Note: The LRESET# width is dependent on the processor clock. The LRESET# must be active after the clock is stable.

19. TOP MARKING SPECIFICATION









1st line: Winbond (Nuvoton) logo

2nd line: the type number: W83627EHF/EF, W83627EHG/EG (Pb-free package)

3rd line: the tracking code 030A7C282012345UA

330: packages made in '03, week 30

G: assembly house ID; G means GR, A means ASE ... etc.

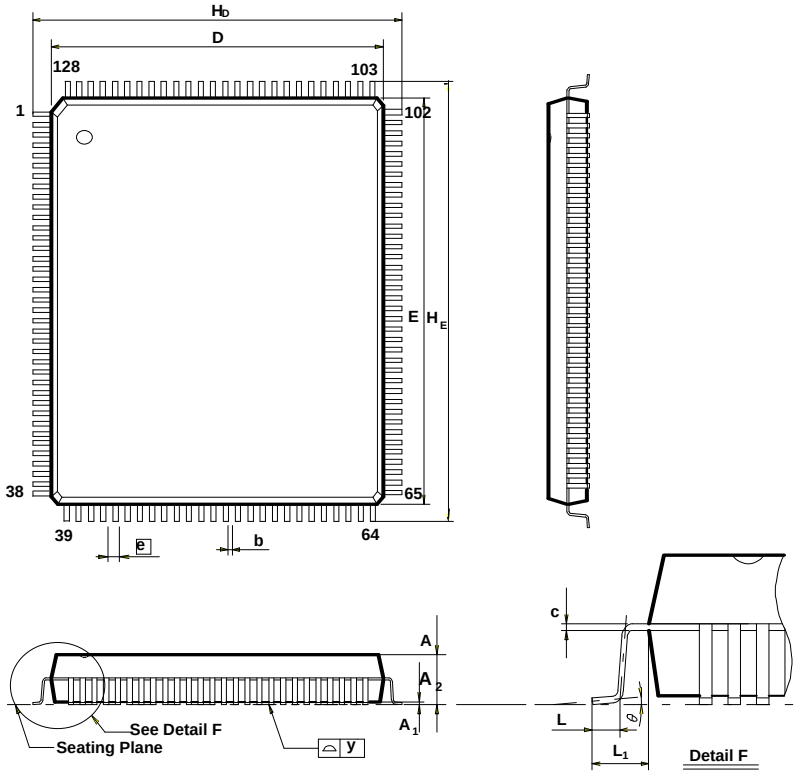
9: code version; 9 means code 009

A: IC revision; A means version A, B means version B

282012345: wafer production series lot number

UB: Winbond (Nuvoton) internal use.

20. PACKAGE SPECIFICATION



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.134	—	—	3.40
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.107	0.113	2.57	2.72	2.87
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e		0.020			0.50	
H_D	0.669	0.677	0.685	17.00	17.20	17.40
H_E	0.905	0.913	0.921	23.00	23.20	23.40
L	0.023	0.031	0.039	0.60	0.80	1.00
L_1	0.055	0.063	0.071	1.40	1.60	1.80
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

128-pin (QFP, 14x20x2.75mm foot print 3.2mm)

21. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.5	10/01/2004	N.A.	1. First published preliminary version.
0.51	11/09/2004	N.A.	1. Correct typo at 5.11.
0.52	12/07/2004	N.A.	1. Correct DC CHARACTERISTICS description 2. Update Demo Circuit 3. Add Pb-free part no:W83627EHG
0.6	03/18/2005	N.A.	1. Add SMART FANTM III description
0.61	06/10/2005	N.A.	1. Update application circuit
0.62	07/06/2005	N.A.	1. Add new part W83627EF and W83627EG.
0.63	07/19/2005	N.A.	1. Update pin configuration and application circuit
1.0	9/13/2005	N.A.	1. Correct information and add AC Power Loss Timing chart
1.1	02/14/2006	18	1. Correct LPT function pins description.
1.2	08/04/2006	79, 80	1. Remove “2N3904 activation” selection
1.3	10/03/2006	105, 106	1. Correct description of CRF0 of Logical Device 2/3 (UARTA/B)
1.4	10/23/2006	1, 3, 65, 70	1. Correct the description of W83627EHF/EHG/EF/EG only supports “one” floppy disk drive 2. Correct the Hardware Monitor Device, Bank 0, Index 4Ah, bits[7:6] 3. Add a beep control bit for VIN4 at Hardware Monitor Device, Bank 0, Index 57h, bit 6

VERSION	DATE	PAGE	DESCRIPTION
1.5	04/20/2007	N.A.	1. Remove all the descriptions about Serial Peripheral Interface functions 2. Add new chapters for Configuration Register Access Protocol, Power Management, Serialized IRQ, Watchdog Timer, VID Inputs and Outputs, and PCI Reset Buffers. 3. Add new section of Conversion Sequence and Conversion Time in Chapter 7 Hardware Monitor. 4. Modify "Absolute Maximum Ratings" in Chapter 18 Specifications. 5. Remove "V_{DD} is 5V± 10% tolerance" from the description of DC Characteristics in Chapter 18 Specifications. 6. Update AC Timing parameters and waveforms.
1.6	05/10/2007	N.A.	1. Correct the Data hold and setup time of section 18.3.3 SMBus Timing
1.7	08/13/2007	40, 261, 262	1. Update the description of 7.5 Conversion Sequence and Conversion Time. 2. Add a note to 18.5 Reset Timing. 3. Update the title of Chapter 19 from "How to Read the Top Marking" to "Top Marking Specification".
1.8	08/17/2007	260, 261	1. Update 18.4 LPC Timing and 18.5 Reset Timing
1.9	09/10/2007	85	1. Update 7.9.44 Register 50h~55h Bank Select Register – Index 4Eh (Bank 0)

VERSION	DATE	PAGE	DESCRIPTION
1.91	11/06/2007	224	1. Update “KBRST” to “KBRST#”. 2. Update the rating of 3VCC in 18.1 Absolute Maximum Rating.
1.92	07/25/2008	10, 264	1. Update Chapter 4 Pin Configuration. 2. Move Revision History to the last chapter. 3. Change Winbond logo to Nuvoton.
1.93	08/01/2008	11-26	1. Update the descriptions of pin 13, 14, 15, 17 ,21, 22, 23, 29, 30, 51, 53, 54, 64, 69, 77, 80, 81, 89, 90, 119, and 120 -128.
1.94	04/07/2009	273	1. Update Chapter 20, package specification.

Important Notice

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