Intel® 845G/845GL/845GV Chipset

Specification Update

Intel® 82845G/82845GL/82845GV Graphics and Memory Controller Hub (GMCH)

October 2003

Notice: The Intel® 82845G/82845GL/82845GV GMCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298657-007

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release.	July 2002
-002	Added information for the 82845GV component	October 2002
-003	(1) Added Errata #1, GMBUS Protocol Erratum (2) Added "B1" stepping to the Summary Table of Changes (3) Added a new "Q-Spec" number to the Component Marking Information Table	December 2002
-004	(1) Added Documentation Change #A1,B1,C1, Remove Note in Graphics Control Register (Device 0), Bit [3] (2) Added Documentation Change #A2,B2,C2, CAPREG Register Update (3) Added Documentation Change #A3,B3,C3, RID Register Update (4) Modified the Summary Table of Changes to allow differentiation of Specification Update items to the specific 82845G, 82845GL, or 82845GV chipset (5) Added Specification Change C1, 82845GV Adds DDR333 Capability (6) Added Erratum #A2,B2,C2, VGA Panning (7) Added Erratum #A3,B3,C3, VGA Timing	May 2003
-005	(1) Added Specification Change C2, 82845GV Adds DDR333 Capability Only at FSB 533 MHz	June 2003
-006	(1) Added Specification Clarification #C1, 82845GV FSB, Memory, and Internal Graphics Frequency Use for QD76 and SL6PU Devices (2) Added Specification Clarification #C2, 82845GV FSB, Memory, and Internal Graphics Frequency Use for QD66 and SL6NR Devices	Aug 2003
-007	(1) Added Errata #A4, DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata	Oct 2003

Preface

This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 845G/845GL/845GV Chipset Datasheet: Intel® 82845G/82845GL/82845GV Graphics and Memory Controller Hub (GMCH)	290746-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel 82845G/82845GL/82845GV GMCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel 82845G/82845GL/82845GV GMCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A1	8086h	2560h	01h
B1	8086h	2560h	03h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 82845G/82845GL GMCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A1	QD14, QD15, QD16	SL66F	RG82845G	82845G Desktop
A1	QD17, QD18	SL66G	RG82845GL	82845GL Desktop
A1	QD69	SL6NR	RG82845GV	82845GV Desktop
B1	QD71, QD72	SL6PR	RG82845G	82845G Desktop
B1	QD73	SL6PT	RG82845GL	82845GL Desktop
B1	QD76	SL6PU	RG82845GV	82845GV Desktop

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed Intel 82845G/82845GL/82845GV GMCH steppings. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Errata that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded: This item is either new or modified from the previous version of the document

Note: Each Specification Update item is prefaced with a capital letter to distinguish the product. The key below details the letters that are used in this Intel® 845G/845GL/845GV Chipset Specification Update.

A = Intel® 82845G Graphics and Memory Controller Hub (GMCH)

B = Intel® 82845GL Graphics and Memory Controller Hub (GMCH)

C = Intel® 82845GV Graphics and Memory Controller Hub (GMCH)

NO.	SPECIFICATION CHANGES
C1	82845GV Adds DDR333 Capability
C2	82845GV Adds DDR333 Capability Only at FSB 533 MHz

NO.	A1	B1	PLANS	ERRATA
1	X	X	NoFix	GMBUS Protocol
A2,B2,C2	X	X	NoFix	VGA Panning
A3,B3,C3	X	X	NoFix	VGA Timing
A4	X	X	NoFix	DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata

NO.	SPECIFICATION CLARIFICATIONS
C1	82845GV FSB, Memory, and Internal Graphics Frequency Use for QD76 and SL6PU Devices
C2	82845GV FSB, Memory, and Internal Graphics Frequency Use for QD66 and SL6NR Devices

NO.	DOCUMENTATION CHANGES
A1,B1,C1	Remove Note in Graphics Control Register (Device 0), Bit [3]
A2,B2,C2	CAPREG Register Update
A3,B3,C3	RID Register Update

Specification Changes

C1 82845GV Adds DDR333 Capability

Reference the *Intel® 845G/845GL/845GV Chipset Datasheet*, document number 290746-002, for the following changes:

1. The "82845G GMCH Features" list on page 11, in the bullet "System Memory Controller (SDR and DDR), for "Double Data Rate (DDR) SDRAM Configuration", add a line which says "DDR333 unregistered, 184-pin non-ECC DDR SDRAM DIMMS can be used with the 82845GV chipset".

2. Section 1.4.2, System Memory Interface, add a line which says, "DDR333 unregistered, 184-pin non-ECC DDR SDRAM DIMMS can be used with the 82845GV chipset".

3. Section 4.2.1, DDR SDRAM Interface Overview, add a line which says, "DDR333 unregistered, 184-pin non-ECC DDR SDRAM DIMMS can be used with the 82845GV chipset".

C2 82845GV Adds DDR333 Capability Only at FSB 533 MHz

Reference Specification Change C1.

The use of DDR333 unregistered, 184-pin non-ECC DDR SDRAM DIMMS is limited to those 82845GV platforms that have a 533 MHz front side bus speed. DDR333 memory capability cannot be used in 82845GV platforms that have a 400 MHz front side bus speed.

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Errata

A1,B1,C1 GMBUS Protocol

Problem: Under certain environmental conditions, there are design sensitivities in asynchronous clock crossing logic in the 82845G/GL GMBUS implementation. As a result, the 82845G/GL may not correctly complete the protocol transactions to the DVI device.

Implication: A platform will boot normally but there is no display when using non-VGA display devices such as televisions, local non-removable digital flat panels and external user-removable DVI displays.

Workaround: A Video BIOS workaround is available in 82845G/GL VBIOS version 11.4.1 (build #2759).

Status: There are no plans to fix this erratum in silicon. For affected steppings, see the *Summary Table of Changes*.

A2,B2,C2 VGA Panning

Problem: VGA text mode diagnostic and stress test applications that use pixel panning can experience temporary visual anomalies under certain memory configurations. The memory configurations affected are 64-MB technology products that use 2-KB and 4-KB page sizes.

1. Test applications using a single VGA font table with a 32-KB font buffer range could fail. This failure was seen in a diagnostic utility.
2. Test applications using multiple VGA font tables could fail if the first two fonts are from different tables. This failing condition can occur in any memory configuration. This failure was seen in a stress test utility.

Implication: Entire scanlines will appear to flicker in some VGA diagnostic and stress test applications. However, there are no known customer sightings of this erratum. No known end-user applications fail for this erratum.

Workaround: No workaround exists.

Status: This will not be fixed in future steppings. For affected steppings, see the *Summary Table of Changes*.

A3,B3,C3 VGA Timing

Problem: Some VGA applications, running in 40-column modes, that use a non-black border color, may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists. This will not be fixed in future steppings. For affected steppings, see the *Summary Table of Changes*.

A4. DDC Slave Stall during Acknowledge Phase or Short Slave Stall Errata

Problem: Under specific conditions, a slave stall on the DDC interface during the acknowledge phase or a very short slave stall (less than 1 DDC clock) during reads on the DDC interface may cause the stall to be ignored and not seen by the MCH resulting in unpredictable system behavior.

Implication: These issues have only been seen in a synthetic test environment and may result in unpredictable system behavior. No system failures have been observed during normal operation.

Workaround: None

Status: No silicon fix planned. For affected steppings, see the *Summary Table of Changes*.

Specification Clarifications

C1 82845GV Front Side Bus, Memory, and Internal Graphics Frequency Use Model for QD76 and SL6PU Devices

The following table provides information on the supported front side bus speed, the memory speed, and the internal graphics speed combinations that can be used with the 82845GV Q-Spec QD76 and S-Spec SL6PU devices. This is the B1-stepping of the device.

Table Notes:

All numbers are frequency in MHz

FSB = Front Side Bus

DDR = Double Data Rate SDRAM

SDRPC133 = Single Data Rate SDRAM meeting PC133 requirements

IG = Internal Graphics

YES = Combination is supported

N/A = Combination is not applicable

NO = Combination is not supported

	FSB400	FSB533	DDR200	DDR266	DDR333	SDRPC133	IG200	IG266
FSB400	N/A	N/A	NO	YES	NO	NO	NO	YES
FSB533	N/A	N/A	NO	YES	YES	NO	NO	YES
DDR200	NO	NO	N/A	N/A	N/A	N/A	NO	NO
DDR266	YES	YES	N/A	N/A	N/A	N/A	NO	YES
DDR333	NO	YES	N/A	N/A	N/A	N/A	NO	YES
SDRPC133	NO	NO	N/A	N/A	N/A	N/A	NO	NO
IG200	NO	NO	NO	NO	NO	NO	N/A	N/A
IG266	YES	YES	NO	YES	YES	NO	N/A	N/A

C2 82845GV Front Side Bus, Memory, and Internal Graphics Frequency Use Model for QD69 and SL6NR Devices

The following table provides information on the supported front side bus speed, the memory speed, and the internal graphics speed combinations that can be used with the 82845GV Q-Spec QD66 and S-Spec SL6NR devices. This is the A1-stepping of the device.

Table Notes:

All numbers are frequency in MHz

FSB = Front Side Bus

DDR = Double Data Rate SDRAM

SDRPC133 = Single Data Rate SDRAM meeting PC133 requirements

IG = Internal Graphics

YES = Combination is supported

N/A = Combination is not applicable

NO = Combination is not supported

	FSB400	FSB533	DDR200	DDR266	DDR333	SDRPC133	IG200	IG266
FSB400	N/A	N/A	YES	YES	NO	YES	YES	NO
FSB533	N/A	N/A	YES	YES	NO	NO	YES	NO
DDR200	YES	YES	N/A	N/A	N/A	N/A	YES	NO
DDR266	YES	YES	N/A	N/A	N/A	N/A	YES	NO
DDR333	NO	NO	N/A	N/A	N/A	N/A	NO	NO
SDRPC133	YES	NO	N/A	N/A	N/A	N/A	YES	NO
IG200	YES	YES	YES	YES	NO	YES	N/A	N/A
IG266	NO	NO	NO	NO	NO	NO	N/A	N/A

Documentation Changes

A1,B1,C1 Remove Note in Graphics Control Register (Device 0), Bit [3]

Reference *the Intel® 845G/845GL/845GV Chipset Datasheet*, document number 290746-002, section 3.5.1.15, "GC – Graphics Control Register (Device 0)", at address offset 52h.

The Note in the description of bit [3] in this register is not correct. Remove the Note.

A2,B2,C2 CAPREG Register Update

Reference the *Intel® 845G/845GL/845GV Chipset Datasheet*, dated October 2002, document number 290746-002, Section 3.5.1.38 CAPREG – Capability Identification Register (Device 0), at address offset E4h – E8h.

Modify the Part Identifier section of the description in bit [39:28] so that it reads as follows:

Part Identifier.

0E1h = 82845GL with Revision ID of 01h or 03h

0B1h = 82845GV with Revision ID of 01h

211h = 82845GV with Revision ID of 03h

000h = 82845G with Revision ID of 01h

030h = 82845G with Revision ID of 03h

A3,B3,C3 RID Register Update

Reference the *Intel® 845G/845GL/845GV Chipset Datasheet*, dated October 2002, document number 290746-002, Section 3.5.1.5, RID – Revision Identification Register (Device 0), at address offset 08h.

Modify the description in bits [7:0] for the **82845GV GMCH** to include the following:

03h = B1 Stepping