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 Intel® E7500 Chipset

Intel® E7500 Chipset

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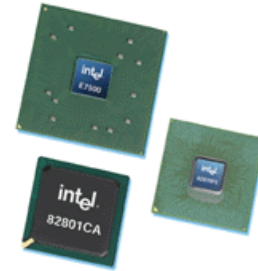
For Embedded Computing

The Intel® E7500 chipset provides a value in high performance chipset technology. The Intel E7500 chipset supports dual processor platforms optimized for the [Intel® Xeon® processor with 512 KB L2 cache](#) and the [Low Voltage Intel® Xeon® processor and Intel NetBurst® microarchitecture](#). The Intel E7500 chipset design delivers maximized system bus, memory, and I/O bandwidth to enhance performance, scalability, and end-user productivity.

The Intel E7500 chipset utilizes a modular design and offers platform implementation flexibility to meet the expanding needs of dual processor (DP) embedded computing applications through three core components:

The E7500 Memory Controller Hub (MCH) is the central hub for all data passing through core system elements such as the single or dual Intel Xeon processors with 512 KB L2 cache via the system bus interface, the memory via memory interface, and both the 64-bit PCI/PCI-X and I/O controller hubs via Intel® Hub Interfaces. The Intel E7500 chipset delivers compelling performance at 3.2 GB/s of bandwidth across the 400 MHz system bus and up to 3.2 GB/s of bandwidth across two high-performance Double Data Rate SDRAM memory channels. To balance the performance offered by the processor and memory interfaces, the MCH allows several high-bandwidth I/O configuration options for a total of 3.2 GB/s of I/O bandwidth. Together, these features deliver balanced, high-throughput system performance.

The 82870P2 64-bit PCI/PCI-X Controller Hub 2 (P64H2) connects to the MCH



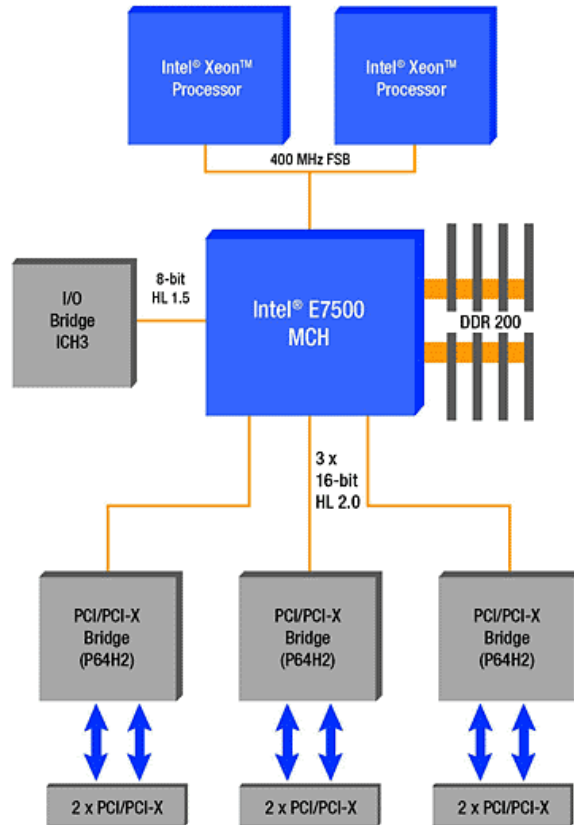
through a point-to-point Hub Interface 2.0 connection. Up to three P64H2 devices can be attached to the MCH, each providing an I/O bandwidth greater than 1 GB/s for a total of 3.2 GB/s of I/O bandwidth. Each P64H2 contains two independent 64-bit PCI-X interfaces and two PCI hot plug controllers, one per PCI-X interface. Each 64-bit PCI-X segment supports multiple PCI-X slots for high-bandwidth connectivity of next-generation components such as Intel® Gigabit Ethernet adapters and Intel® I/O processors.

The 82801CA I/O Controller Hub 3-S (ICH3-S) connects to the MCH through a point-to-point Hub Interface 1.5 connection. The ICH3-S provides legacy I/O interfaces through integrated features including a two-channel Ultra ATA/100 bus master IDE controller and three USB controllers for up to six USB ports. The ICH3-S also offers an integrated System Manageability Bus 2.0 (SMBus 2.0) controller, an integrated LAN controller, as well as AC97 2.2-compliant and PCI 2.2-compliant interfaces.

Features that maximize performance and balance the platform: Dual Intel Xeon processors with 512 KB L2 cache or Low Voltage Intel Xeon processors and a 400 MHz system bus provide up to 3.2 GB/s of available bandwidth. Dual DDR-200 memory channels operate in lock-step to provide up to 3.2 GB/s of memory bandwidth. Three Hub Interface 2.0 connections provide multiple high-bandwidth I/O configuration options, yielding up to 3.2 GB/s of I/O bandwidth.

[Download Product Brief](#) 

Block Diagram



Product Highlights

- Supports one or two Intel® Xeon® processors with 512 KB L2 cache or Low Voltage Intel Xeon processors for embedded computing platforms
- 400 MHz system bus capability
- The P64H2 provide an Intel® Hub Architecture 2.0 connection to the MCH
 - 64-bit PCI/PCI-X Controller Hub-2
- Dual-channel DDR-200 memory interface
- Advanced Platform RASUM

Intel® E7500 Chipset

Product	Product Code	Package
E7500 Memory Controller Hub (MCH)	RGE7500PL	1005 Flip Chip-Ball Grid Array (FC-BGA)
82801CA Integrated Controller Hub (ICH3-S)	FW82801CA	421 Ball Grid Array (BGA)
82870P2 64-bit PCI/PCI-X Controller (P64H2)	RG82870P2	567 Flip Chip-Ball Grid Array (FC-BGA)

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