128Kx32 SRAM MODULE, SMD 5962-93187

FEATURES

- Access Times of 70, 85, 100, 120ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400).
  - 68 lead, 40mm Low Profile CQFP, 3.56mm (0.140") (Package 502).
  - 68 lead, Hermetic CQFP, 22.4mm (0.880 inch) square. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
    - G2 (Package 500), 5.08mm (0.200 inch) high
    - G2U (Package 510), 4.57mm (0.140 inch) high
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS128K32-XG2X - 8 grams typical
  WS128K32-XG2UX - 8 grams typical
  WS128K32-XH1X - 13 grams typical
  WS128K32-XG4TX - 20 grams typical
- All devices are upgradeable to 512Kx32

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	NC	NC	A4	A1
A16	A12	$\overline{WE}_1$	A8	A5	A2
NC	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

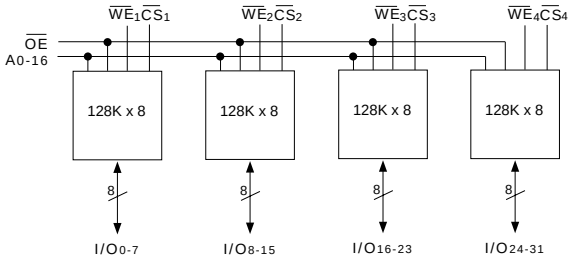
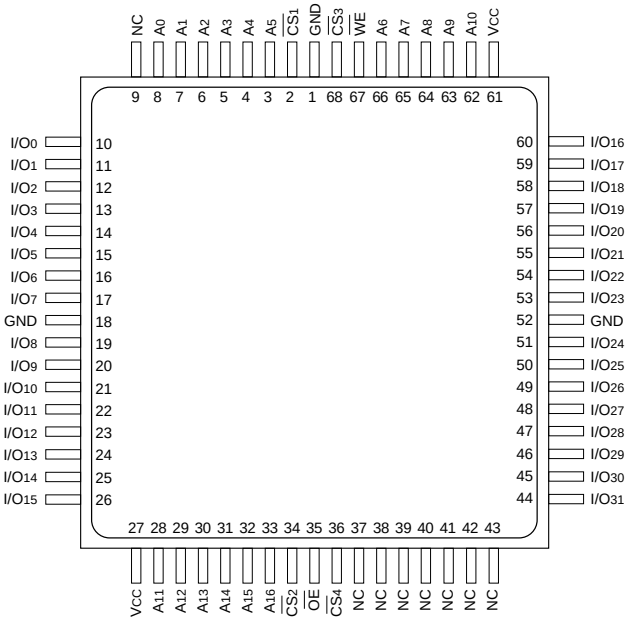


FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

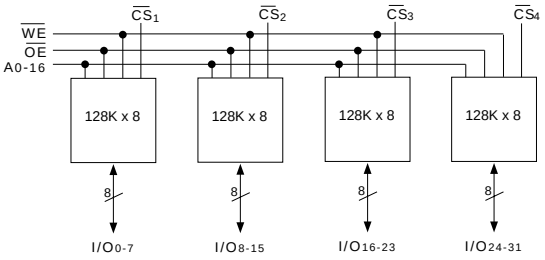
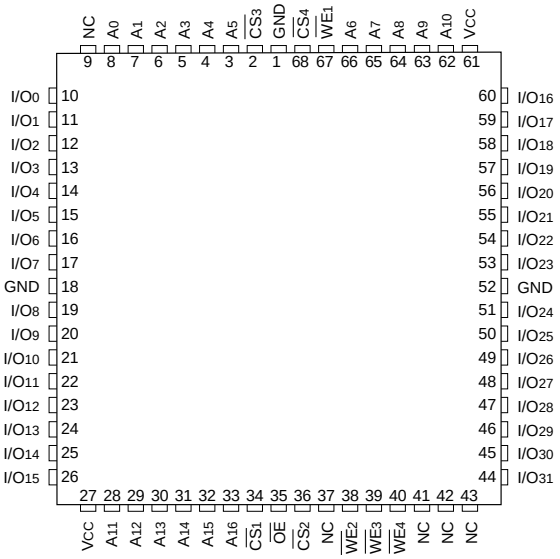
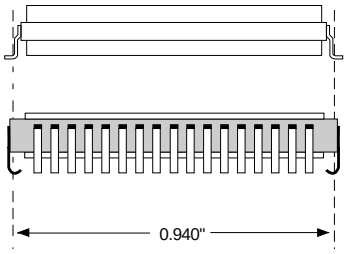


FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2X AND WS128K32-XG2UX

TOP VIEW



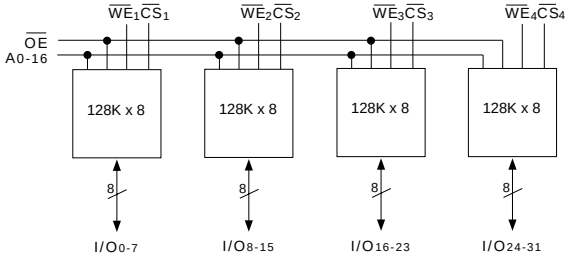


The White 68 lead G2/G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2/G2U has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$1-4	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4			50	
CQFP G2			20	
CQFP G2U			15	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		120		120		120		120	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		5		5		2.4		2.4	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, Vcc = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, Vcc = 4.5	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		80	1600		80	1600		80	1100		80	1100	µA

AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C To +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		45		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

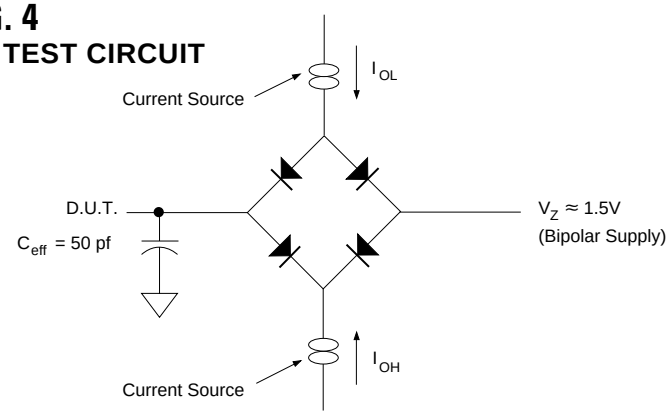
AC CHARACTERISTICS

(V_{CC} = 5.0V, T_A = -55°C To +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		35		40		50		ns
Write Pulse Width	t_{WP}	50		55		70		80		ns
Address Setup Time	t_{AS}	5		5		5		5		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35		35	ns
Data Hold Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 4
AC TEST CIRCUIT

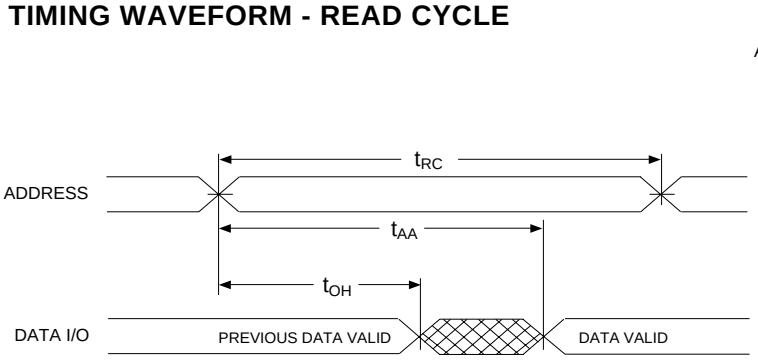


AC TEST CONDITIONS

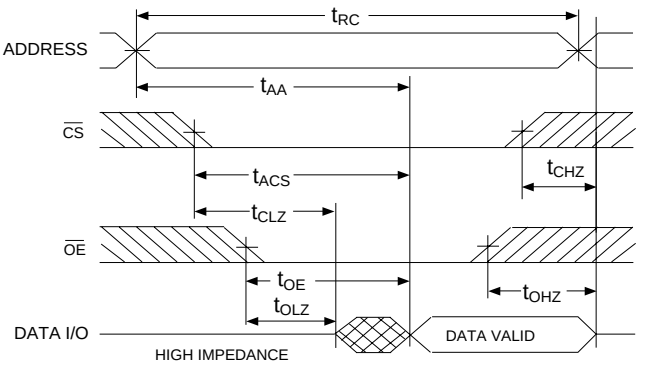
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
TIMING WAVEFORM - READ CYCLE

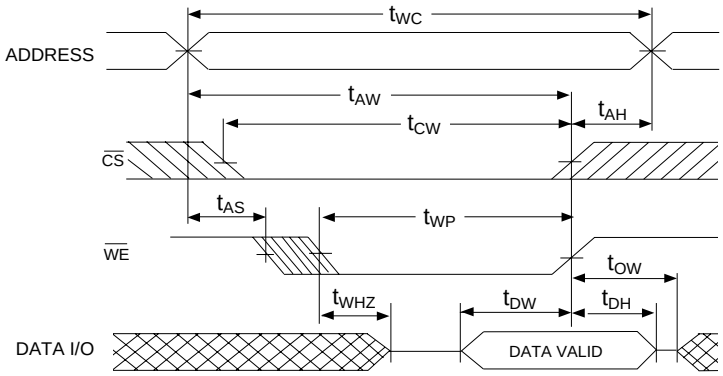


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



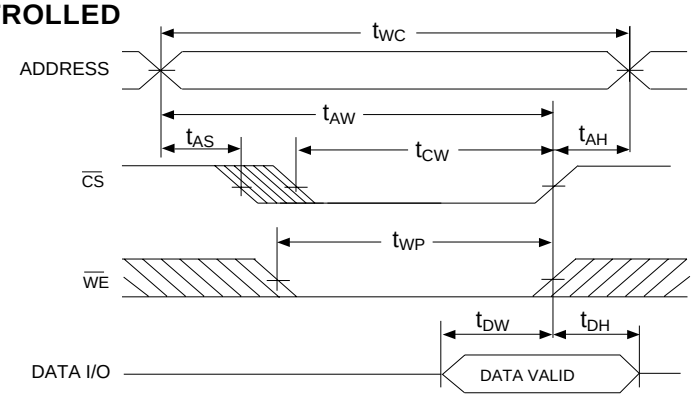
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



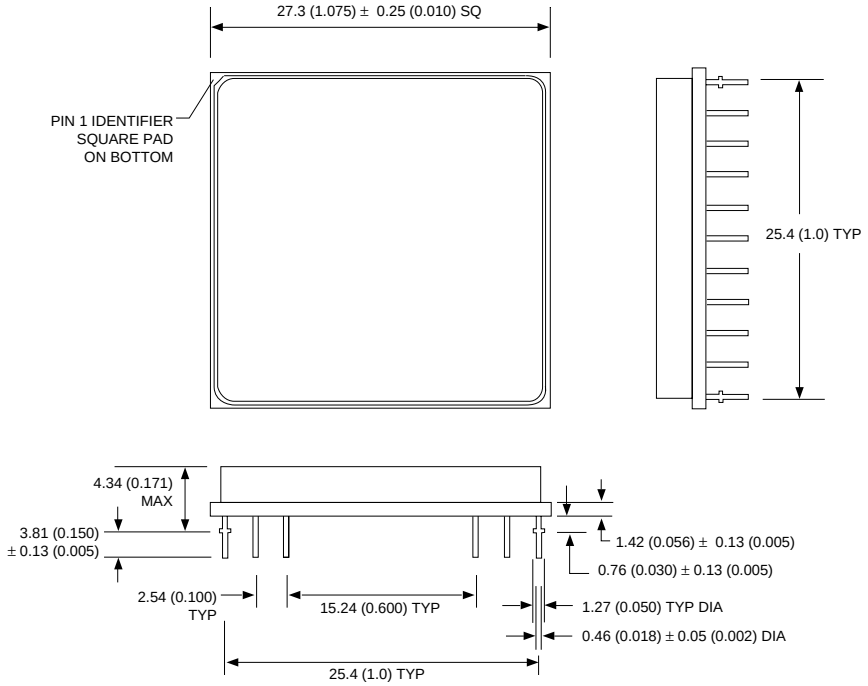
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



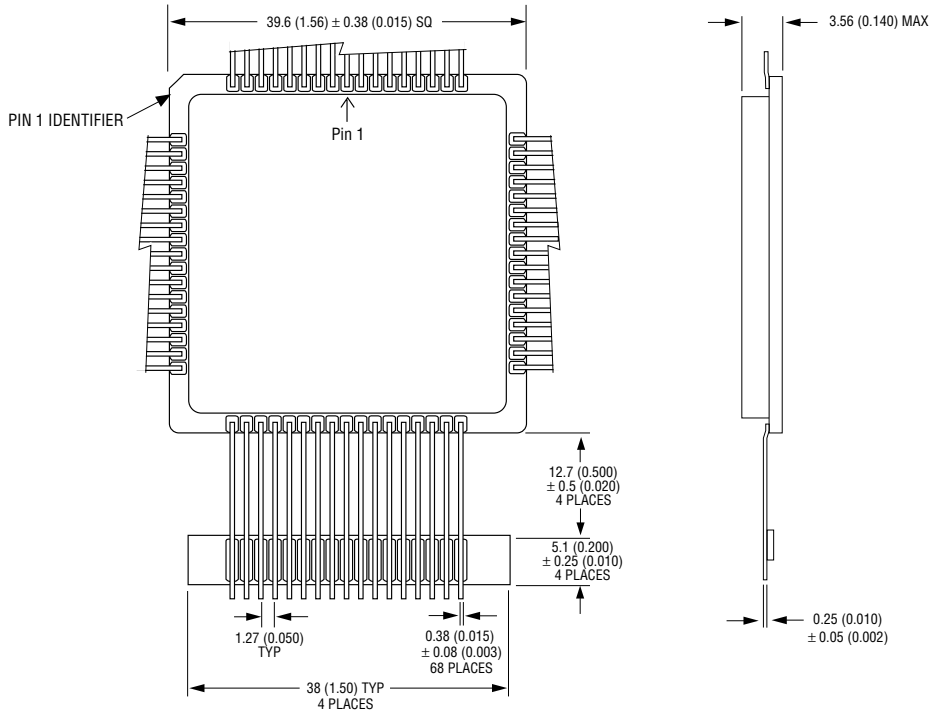
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



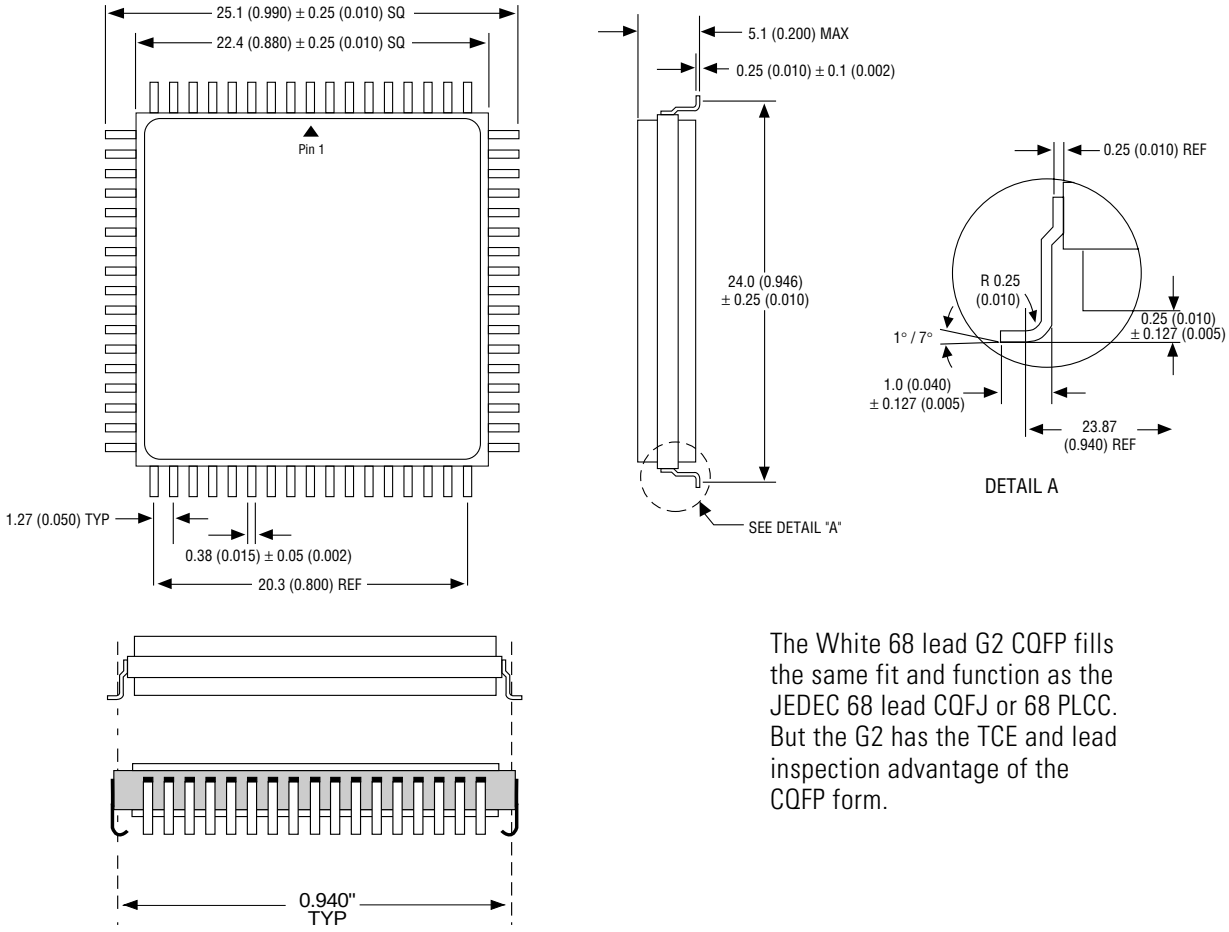
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

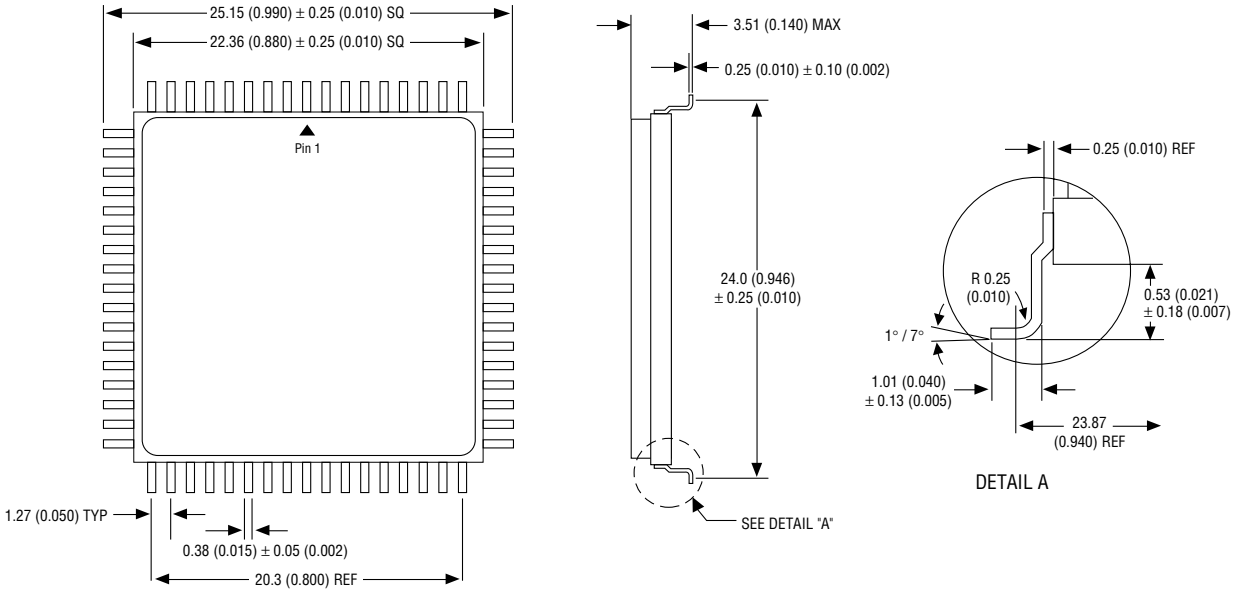
PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)

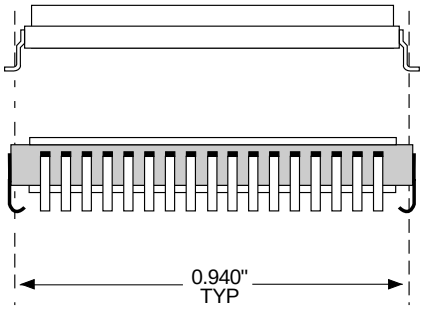


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)





The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 128K 32 X - XXX X X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:
- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:
- H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)
- G2 = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 500)
- G2U = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)
- G4T = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:
- N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

ORGANIZATION, 128Kx32
- User configurable as 256Kx16 or 512Kx8

SRAM

WHITE MICROELECTRONICS

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	120ns	66 pin HIP (H1)	5962-93187 01H5X
128K x 32 SRAM Module	100ns	66 pin HIP (H1)	5962-93187 02H5X
128K x 32 SRAM Module	85ns	66 pin HIP (H1)	5962-93187 03H5X
128K x 32 SRAM Module	70ns	66 pin HIP (H1)	5962-93187 04H5X
128K x 32 SRAM Module	120ns	68 lead CQFP/J (G2)	5962-95595 01HMX
128K x 32 SRAM Module	100ns	68 lead CQFP/J (G2)	5962-95595 02HMX
128K x 32 SRAM Module	85ns	68 lead CQFP/J (G2)	5962-95595 03HMX
128K x 32 SRAM Module	70ns	68 lead CQFP/J (G2)	5962-95595 04HMX
128K x 32 SRAM Module	120ns	68 lead CQFP/J (G2U)	5962-95595 01HNX
128K x 32 SRAM Module	100ns	68 lead CQFP/J (G2U)	5962-95595 02HNX
128K x 32 SRAM Module	85ns	68 lead CQFP/J (G2U)	5962-95595 03HNX
128K x 32 SRAM Module	70ns	68 lead CQFP/J (G2U)	5962-95595 04HNX
128K x 32 SRAM Module	120ns	68 lead CQFP Low Profile (G4T)	5962-95595 01HYX
128K x 32 SRAM Module	100ns	68 lead CQFP Low Profile (G4T)	5962-95595 02HYX
128K x 32 SRAM Module	85ns	68 lead CQFP Low Profile (G4T)	5962-95595 03HYX
128K x 32 SRAM Module	70ns	68 lead CQFP Low Profile (G4T)	5962-95595 04HYX