ISOPRO LOW-POWER TRIPLE-CHANNEL DIGITAL ISOLATOR

Features

- High-speed operation:
  DC to 150 Mbps
- Low propagation delay:
  <10 ns worst case
- Wide Operating Supply Voltage:
  2.70-5.5V
- Ultra low power (typical)
  5 V Operation:
  - < 1.6 mA per channel at 1 Mbps
  - < 1.9 mA per channel at 10 Mbps
  - < 6 mA per channel at 100 Mbps

  2.70 V Operation:
  - < 1.4 mA per channel at 1 Mbps
  - < 1.7 mA per channel at 10 Mbps
  - < 4 mA per channel at 100 Mbps
- Precise timing (typical):
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
- Up to 2500 V_{RMS} isolation
- Transient Immunity: 25 kV/µs
- Tri-state outputs with ENABLE control
- DC correct
- No start-up initialization required
- 15 µs startup time
- High temperature operation:
  125 °C at 150 Mbps
- Wide body and narrow body SOIC-16 packages
- RoHS-compliant

Applications

- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power factor correction systems

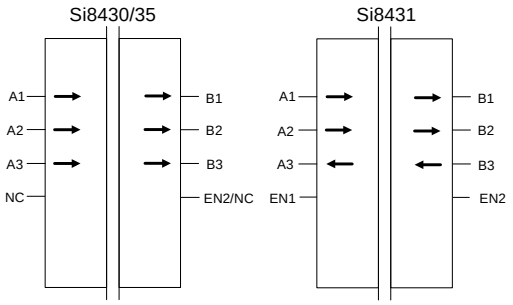
Safety Regulatory Approvals

- UL 1577 recognized
  - 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010 approved
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

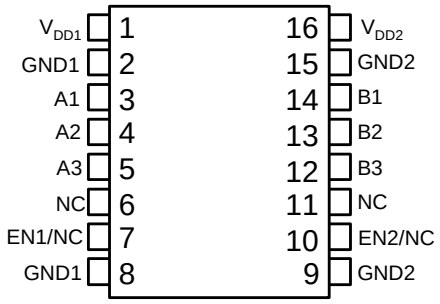
Silicon Lab's family of ultra low power digital isolators are CMOS devices that employ an RF coupler to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These devices are available in 16-pin wide-body and narrow-body SOIC packages. Two speed grade options (1 and 150 Mbps) are available and achieve worst-case propagation delays of less than 10 ns.

Block Diagram



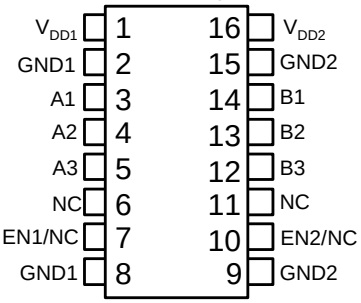
Pin Assignments

Wide Body SOIC



Top View

Narrow Body SOIC



Top View

Patents pending

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at Supply)						
Si8430Ax, Bx and Si8435Bx						
V_{DD1}		All inputs 0 DC	—	1.2	1.8	mA
V_{DD2}		All inputs 0 DC	—	1.9	2.9	
V_{DD1}		All inputs 1 DC	—	4.2	6.3	
V_{DD2}		All inputs 1 DC	—	1.9	2.9	
Si8431Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	2.0	3.0	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.0	4.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8430Ax, Bx						
V_{DD1}			—	2.7	4.1	mA
V_{DD2}			—	2.2	3.3	
Si8431Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.7	4.1	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 1. Electrical Characteristics (Continued)

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			 — —	 2.7 3.0	 4.1 4.2	mA
Si8431Bx V_{DD1} V_{DD2}			 — —	 3.1 3.2	 4.3 4.5	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			 — —	 2.9 14.3	 4.4 17.9	mA
Si8431Bx V_{DD1} V_{DD2}			 — —	 7.0 11.0	 8.8 13.8	mA
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 1. Electrical Characteristics (Continued)

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

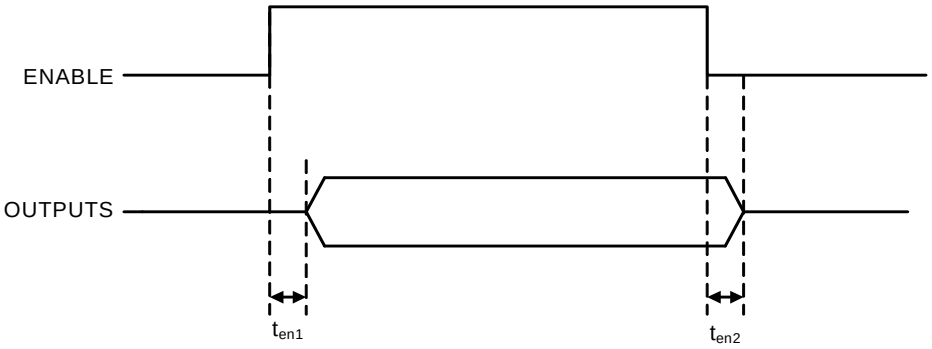


Figure 1. ENABLE Timing Diagram

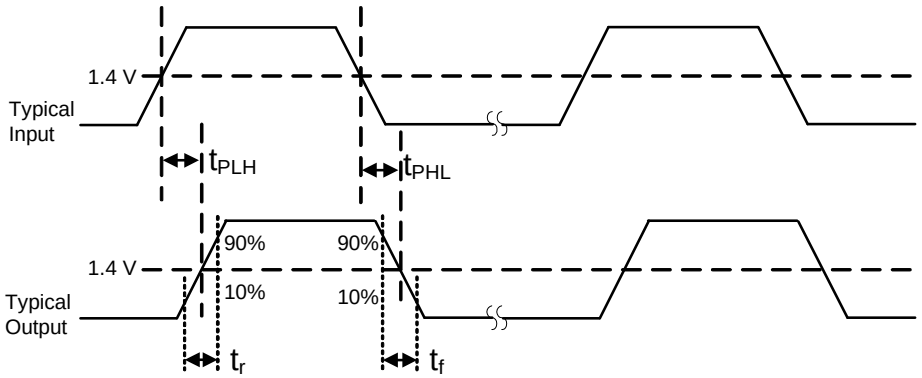


Figure 2. Propagation Delay Timing

Table 2. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8430Ax, Bx and Si8435Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.2 1.9 4.2 1.9	 1.8 2.9 6.3 2.9	mA
Si8431Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.7 2.0 3.7 3.0	 2.6 3.0 5.6 4.5	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8430Ax, Bx V_{DD1} V_{DD2}			 — —	 2.7 2.2	 4.1 3.3	mA
Si8431Ax, Bx V_{DD1} V_{DD2}			 — —	 2.8 2.7	 4.2 4.1	mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			 — —	 2.7 3.0	 4.1 4.2	mA
Si8431Bx V_{DD1} V_{DD2}			 — —	 3.1 3.2	 4.3 4.5	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			 — —	 2.8 10.1	 4.2 12.6	mA
Si8431Bx V_{DD1} V_{DD2}			 — —	 5.5 8.0	 6.9 10.0	mA
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid[3]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[3]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3,4]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8430Ax, Bx and Si8435Bx						
V_{DD1}		All inputs 0 DC	—	1.2	1.8	mA
V_{DD2}		All inputs 0 DC	—	1.9	2.9	
V_{DD1}		All inputs 1 DC	—	4.2	6.3	
V_{DD2}		All inputs 1 DC	—	1.9	2.9	
Si8431Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	2.0	3.0	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.0	4.5	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8430Ax, Bx						
V_{DD1}			—	2.7	4.1	mA
V_{DD2}			—	2.2	3.3	
Si8431Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.7	4.1	

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			— —	2.7 3.0	4.1 4.2	mA
Si8431Bx V_{DD1} V_{DD2}			— —	3.1 3.2	4.3 4.5	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8430Bx, Si8435Bx V_{DD1} V_{DD2}			— —	2.8 8.0	4.2 10	mA
Si8431Bx V_{DD1} V_{DD2}			— —	4.7 6.7	5.9 8.4	mA
Timing Characteristics						
Si843xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 ºC; applies to narrow and wide-body SOIC packages)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si843xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Enable to Data Valid[4]	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State[4]	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[4,5]	t_{SU}		—	15	40	µs

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.
5. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Operating Temperature	T_A	–40	—	125	°C
Supply Voltage (Revision C)[3]	V_{DD1}, V_{DD2}	–0.5	—	5.75	V
Supply Voltage (Revision D)[3]	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "6. Ordering Guide" on page 26 for more information.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125*	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "6. Ordering Guide" on page 26.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0	4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	>175	V
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in "7. Package Outline: 16-Pin Wide Body SOIC" and "9. Package Outline: 16-Pin Narrow Body SOIC". VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic isolation group	Material Group	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	Vpeak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	896	Vpeak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		4000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** This isolator is suitable for basic electrical isolation within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-16	
Case Temperature	T_S		—	—	150	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	220	210	mA
Device Power Dissipation[2]	P_D		—	—	275	275	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 3.
2. The Si843x is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ		Max	Unit
				WB SOIC-16	NB SOIC-16		
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	100	105	—	ºC/W

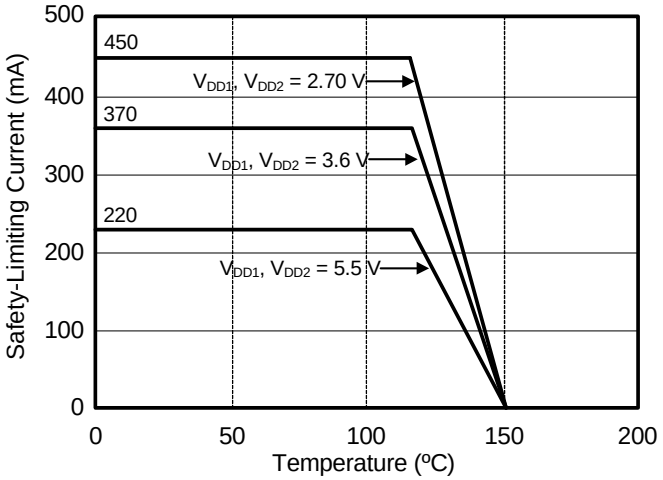


Figure 3. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

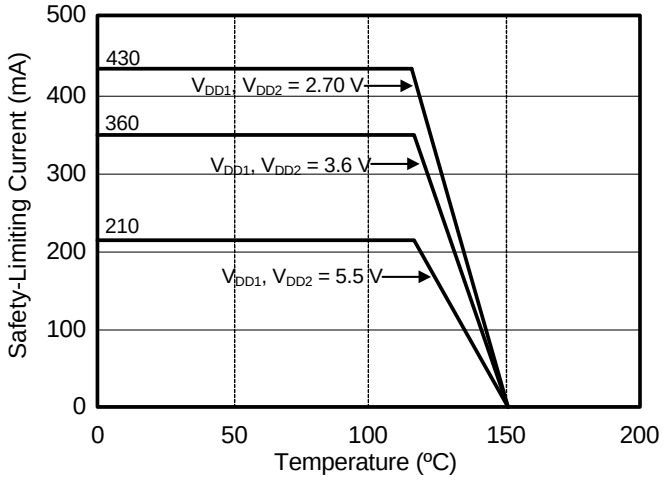


Figure 4. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 12. Si84xx Logic Operation Table

V_I Input[1,2]	EN Input[1,2,3,4]	VDDI State[1,5,6]	VDDO State[1,5,6]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X	L	P	P	Hi-Z or L[7]	Disabled.
X	H or NC	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X	L	UP	P	Hi-Z or L[7]	Disabled.
X	X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z with 1 µs if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si84xx is operating in noisy environments.
4. No Connect (NC) replaces EN1 on Si8430/35. No Connect replaces EN2 on the Si8435. No Connects are not internally connected and can be left floating, tied to VDD, or tied to GND.
5. "Powered" state (P) is defined as 2.70 V < VDD < 5.5 V.
6. "Unpowered" state (UP) is defined as VDD = 0 V.
7. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.

Table 13. Enable Input Truth Table[1]

P/N	EN1[1,2]	EN2[1,2]	Operation
Si8430	—	H	Outputs B1, B2, B3 are enabled and follow input state.
	—	L	Outputs B1, B2, B3 are disabled and Logic Low or in high impedance state.[3]
Si8431	H	X	Output A3 enabled and follows input state.
	L	X	Output A3 disabled and Logic Low or in high impedance state.[3]
	X	H	Outputs B1, B2 are enabled and follow input state.
	X	L	Outputs B1, B2 are disabled and Logic Low or in high impedance state.[3]
Si8435	—	—	Outputs B1, B2, B3 are enabled and follow input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 3 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si84xx is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state is driven to a logic low state when the EN pin is disabled (EN = 0) in Revision C. Revision D outputs go into a high-impedance state when the EN pin is disabled (EN = 0). See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.

2. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 1, 2, and 3 for actual specification limits.

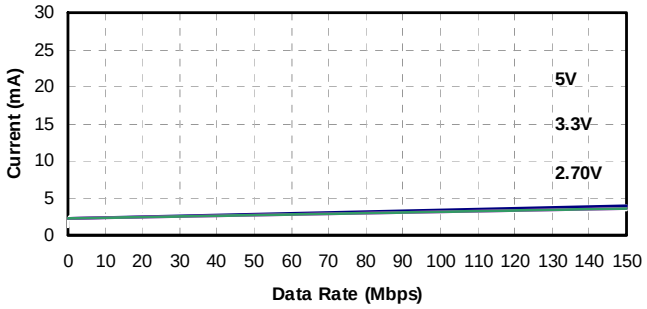


Figure 5. Si8430/35 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

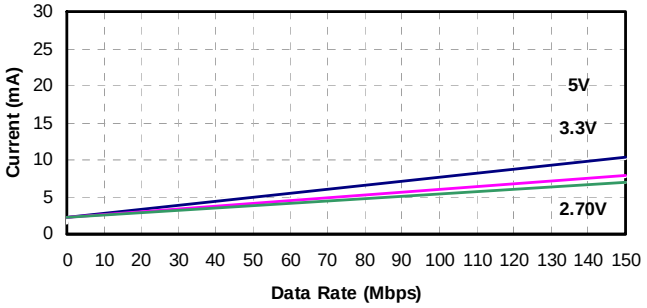


Figure 6. Si8431 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

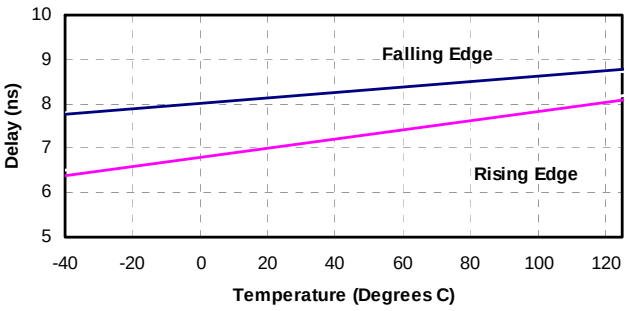


Figure 7. Propagation Delay vs. Temperature

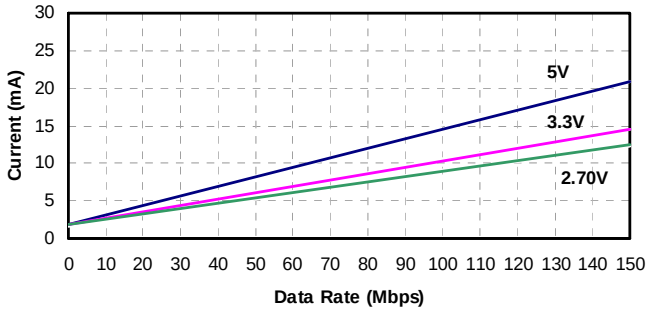


Figure 8. Si8430/35 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

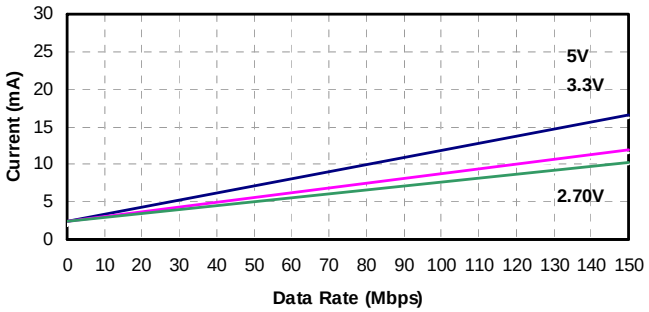


Figure 9. Si8431 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

3. Application Information

3.1. Theory of Operation

The operation of an Si843x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si843x channel is shown in Figure 10.

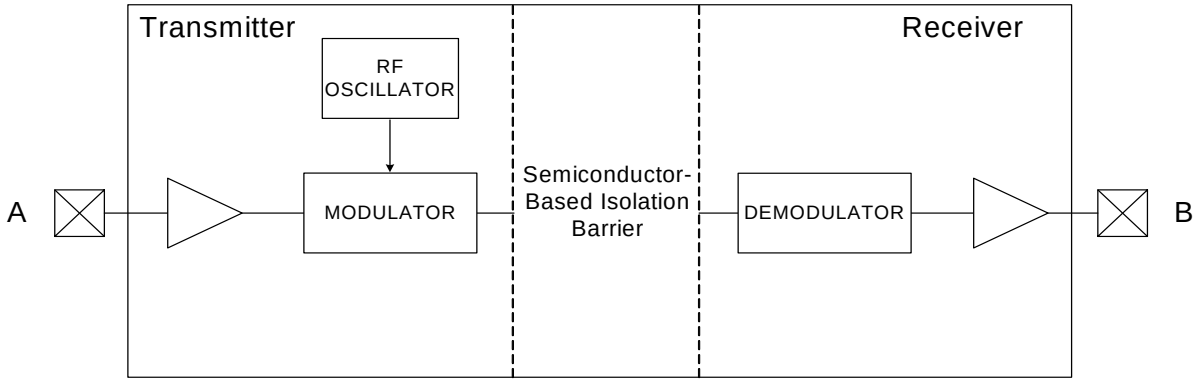


Figure 10. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 11 for more details.

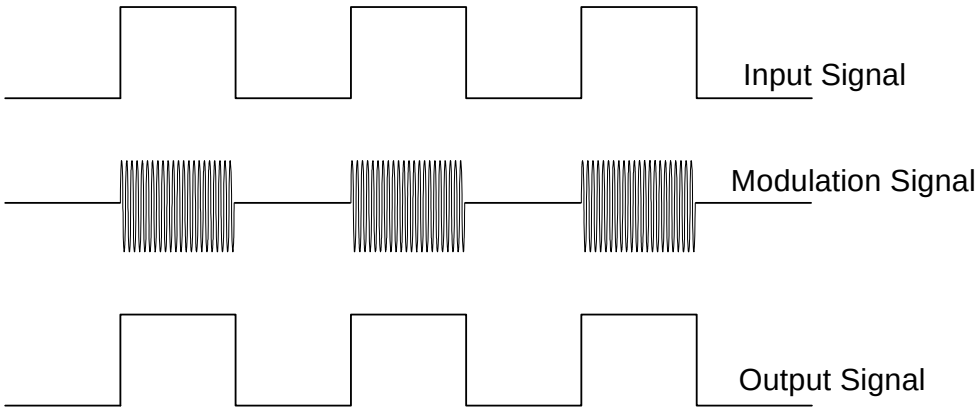


Figure 11. Modulation Scheme

3.2. Eye Diagram

Figure 12 illustrates an eye-diagram taken on an Si8430. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8430 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

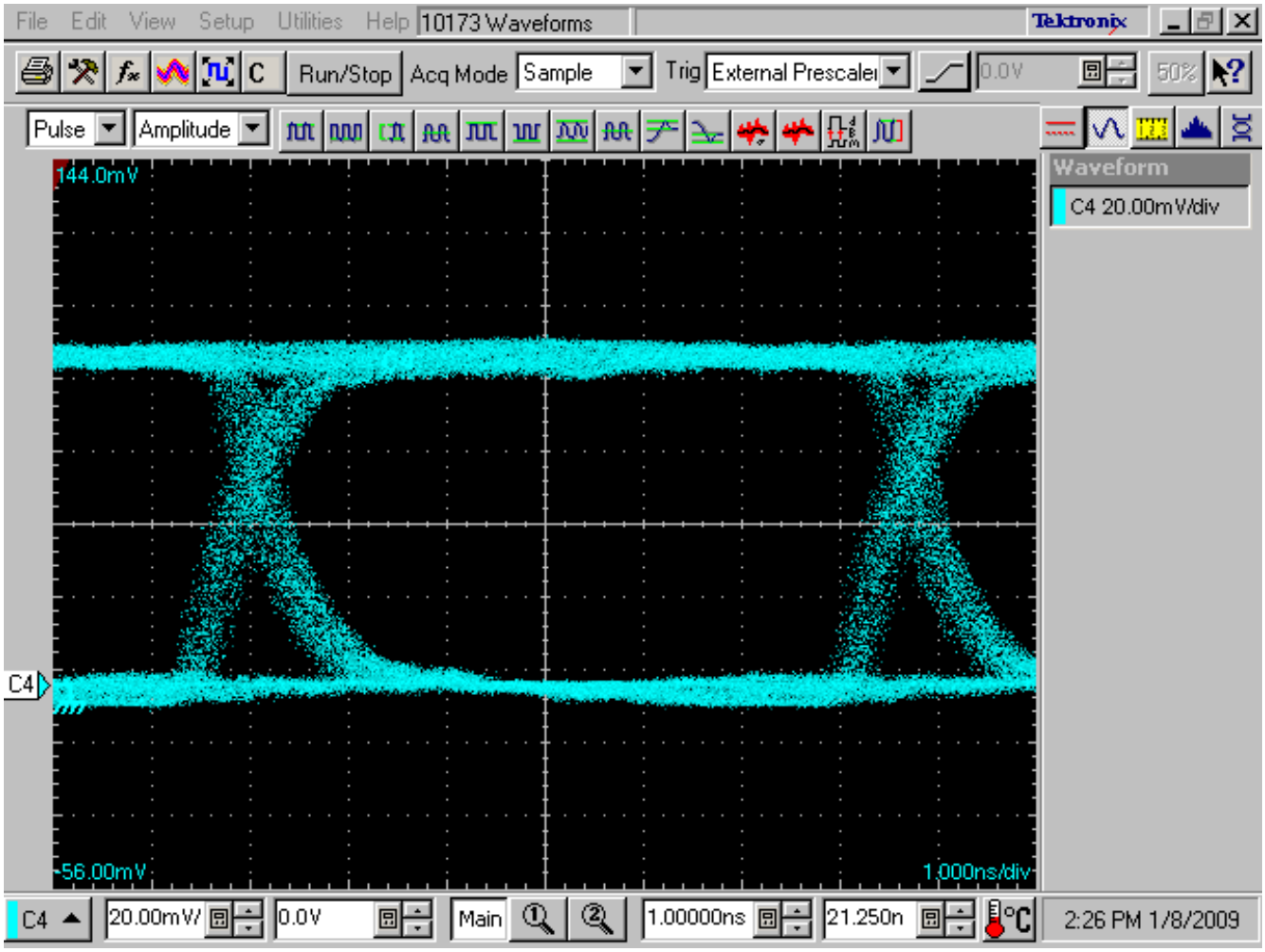


Figure 12. Eye Diagram

3.3. Layout Recommendations

Dielectric isolation is a set of specifications produced by the safety regulatory agencies from around the world that describes the physical construction of electrical equipment that derives power from a high-voltage power system such as 100–240 V_{AC} systems or industrial power systems. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user touchable surfaces of the product. For the IEC relating to products deriving their power from the 100–240 V_{AC} power grids, the minimum test voltage is 2500 V_{AC} (or 3750 V_{DC}—the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the distance through the shortest path through air that an arc may travel.

Figure 13 illustrates the accepted method of providing the proper creepage distance along the surface. For a 120 V_{AC} application, this distance is 3.2 mm, and the narrow-body SOIC package can be used. For a 220–240 V_{AC} application, this distance is 6.4 mm, and a wide-body SOIC package must be used. There must be no copper traces within this 3.2 or 6.4 mm exclusion area, and the surface should have a conformal coating, such as solder resist. The digital isolator chip must straddle this exclusion area.

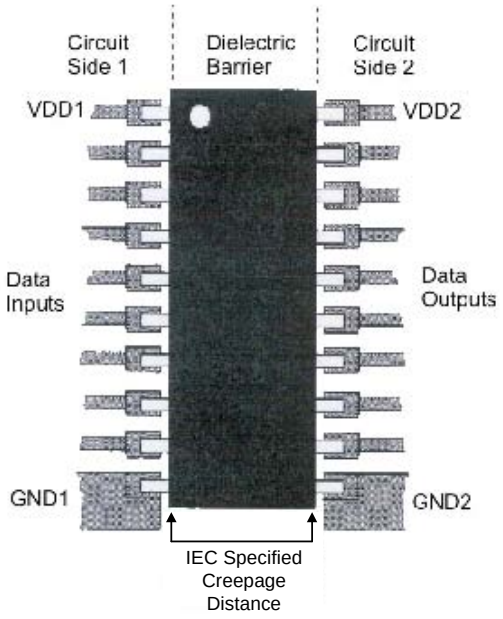


Figure 13. Creepage Distance

3.3.1. Supply Bypass

The Si843x requires a 1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. See "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24 for more details.

3.3.2. Pin Connections

For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground. No connect pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

3.3.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.3.4. RF Radiated Emissions

The Si843x family uses a RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC but, rather, is due to a small amount of RF energy driving the isolated ground planes, which can act as a dipole antenna.

The unshielded Si8430 evaluation board passes FCC Class B (Part 15) requirements. Table 14 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions where all inputs are tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 14. Radiated Emissions

Frequency (MHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
712	29	37	–8
1424	39	54	–15
2136	42	54	–12
2848	43	54	–11
4272	44	54	–10
4984	44	54	–10
5696	44	54	–10

3.3.5. RF, Magnetic, and Common Mode Transient Immunity

The Si84xx families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 25 kV/µs (typical). During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si84xx families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 14, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si843x digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si84xx devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.

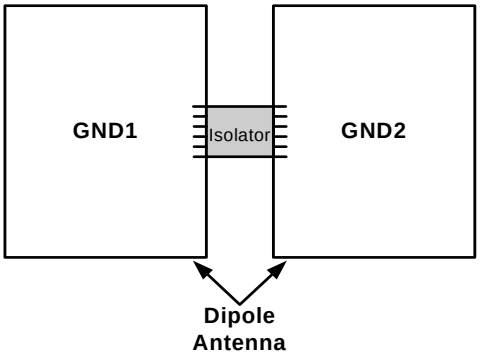


Figure 14. Dipole Antenna

4. Errata and Design Migration Guidelines (Revision C Only)

The following errata apply to Revision C devices only. See "6. Ordering Guide" on page 26 for more details. No errata exist for Revision D devices.

4.1. Enable Pin Causes Outputs to Go Low (Revision C Only)

When using the enable pin (EN1, EN2) function on the ISOpro 3-channel (Si8430/1), the corresponding output pin states (pin = An, Bn, where n can be 1…3) are driven to a logic low (to ground) when the enable pin is disabled (EN1 or EN2 = 0). This functionality is different from the legacy 3-channel (Si8430/1) isolators. On those devices, the isolator outputs go into a high-impedance state (Hi-Z) when the enable pin is disabled (EN1 = 0 or EN2 = 0).

4.1.1. Resolution

The enable pin functionality causing the outputs to go low is supported in production for Revision C of the ISOpro devices. Revision D corrects the enable pin functionality (i.e., the outputs will go into the high-impedance state to match the legacy isolator products). Refer to the Ordering Guide sections of the data sheet(s) for current ordering information.

4.2. Power Supply Bypass Capacitors (Revision C Only)

When using the ISOpro isolators with power supplies $\geq$ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a $\geq$ 4.5 V supply). Although rise time is power supply dependent, $\geq$ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

4.2.1. Resolution

This issue has been corrected with Revision D of the device. Refer to “6. Ordering Guide” for current ordering information.

4.3. Latch Up Immunity (Revision C Only)

ISOpro latch up immunity generally exceeds ± 200 mA per pin. Exceptions: Certain pins provide < 100 mA of latch-up immunity. To increase latch-up immunity on these pins, 100 Ω of equivalent resistance must be included in series with *all* of the pins listed in Table 15. The 100 Ω equivalent resistance can be comprised of the source driver's output resistance and a series termination resistor. The Si8431 is not affected when using power supply voltages (VDD1 and VDD2) $\leq$ 3.5 V.

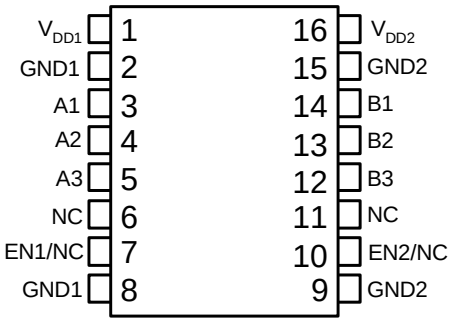
4.3.1. Resolution

This issue has been corrected with Revision D of the device. Refer to “6. Ordering Guide” for current ordering information.

Table 15. Affected Ordering Part Numbers (Revision C Only)

Affected Ordering Part Numbers*	Device Revision	Pin#	Name	Pin Type
SI8430SV-C-IS/IS1, SI8431SV-C-IS/IS1	C	5	A3	Input or Output
		10	EN2	Input
		14	B1	Output
SI8435SV-C-IS/IS1	C	5	A3	Input
		14	B1	Output
***Note:** "SV" = Speed Grade/Isolation Rating (AA, AB, BA, BB).				

5. Pin Descriptions



Top View

Name	SOIC-16 Pin#	Type	Description[1]
V_{DD1}	1	Supply	Side 1 power supply.
GND1	2	Ground	Side 1 ground.
A1	3	Digital Input	Side 1 digital input.
A2	4	Digital Input	Side 1 digital input.
A3	5	Digital I/O	Side 1 digital input or output.
NC	6	NA	No Connect.
EN1/NC[2]	7	Digital Input	Side 1 active high enable. NC on Si8430/35
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
EN2/NC[2]	10	Digital Input	Side 2 active high enable. NC on Si8435.
NC	11	NA	No Connect.
B3	12	Digital I/O	Side 2 digital input or output.
B2	13	Digital Output	Side 2 digital output.
B1	14	Digital Output	Side 2 digital output.
GND2	15	Ground	Side 2 ground.
V_{DD2}	16	Supply	Side 2 power supply.

Notes:

1. For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground.
2. No Connect. These pins are not internally connected. They can be left floating, tied to VDD or tied to GND.

6. Ordering Guide

Revision D devices are recommended for all new designs.

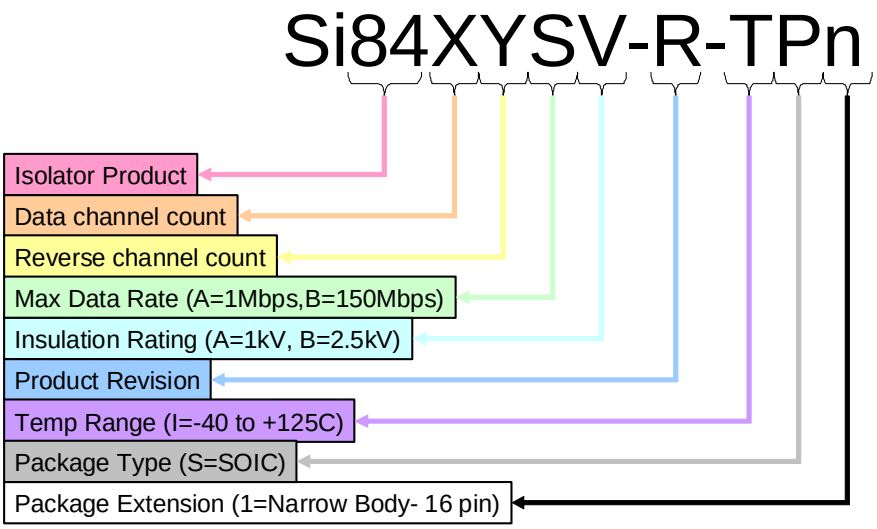


Figure 15. Ordering Part Number (OPN) Convention

Table 16. Ordering Guide for Valid OPNs[1]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
Si8430AB-D-IS	3	0	1	2.5 kVrms	–40 to 125 °C	WB SOIC-16[1]
Si8430BB-D-IS	3	0	150			
Si8431AB-D-IS	2	1	1			
Si8431BB-D-IS	2	1	150			
Si8435BB-D-IS	3	0	150			
Si8430AB-D-IS1	3	0	1	2.5 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8430BB-D-IS1	3	0	150			
Si8431AB-D-IS1	2	1	1			
Si8431BB-D-IS1	2	1	150			
Si8435BB-D-IS1	3	0	150			

Notes:

1. All packages are RoHS-compliant.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages and MSL2A for narrow-body SOIC-16 packages with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. Revision C devices are supported for existing designs, but Revision D is recommended for all new designs.

Table 16. Ordering Guide for Valid OPNs[1] (Continued)

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type
Revision C Devices[2]						
Si8430AB-C-IS[2]	3	0	1	2.5 kVrms	–40 to 125 °C	WB SOIC-16[1]
Si8430BB-C-IS[2]	3	0	150			
Si8431AB-C-IS[2]	2	1	1			
Si8431BB-C-IS[2]	2	1	150			
Si8435BB-C-IS[2]	3	0	150			
Si8430AB-C-IS1[2]	3	0	1	2.5 kVrms	–40 to 125 °C	NB SOIC-16[1]
Si8430BB-C-IS1[2]	3	0	150			
Si8431AB-C-IS1[2]	2	1	1			
Si8431BB-C-IS1[2]	2	1	150			
Si8435BB-C-IS1[2]	3	0	150			

Notes:

1. All packages are RoHS-compliant.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16 packages and MSL2A for narrow-body SOIC-16 packages with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. Revision C devices are supported for existing designs, but Revision D is recommended for all new designs.

7. Package Outline: 16-Pin Wide Body SOIC

Figure 16 illustrates the package details for the Triple-Channel Digital Isolator. Table 17 lists the values for the dimensions shown in the illustration.

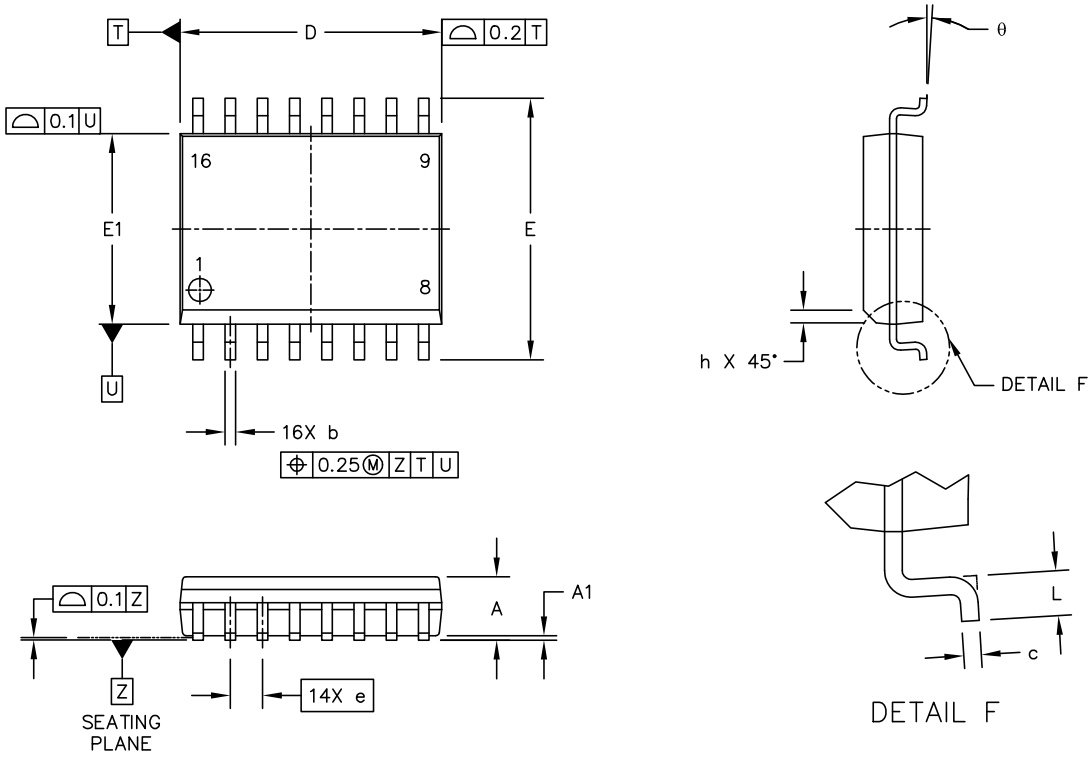


Figure 16. 16-Pin Wide Body SOIC

Table 17. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

8. Landing Pattern: 16-Pin Wide-Body SOIC

Figure 17 illustrates the recommended landing pattern details for the Si843x in a 16-pin wide-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

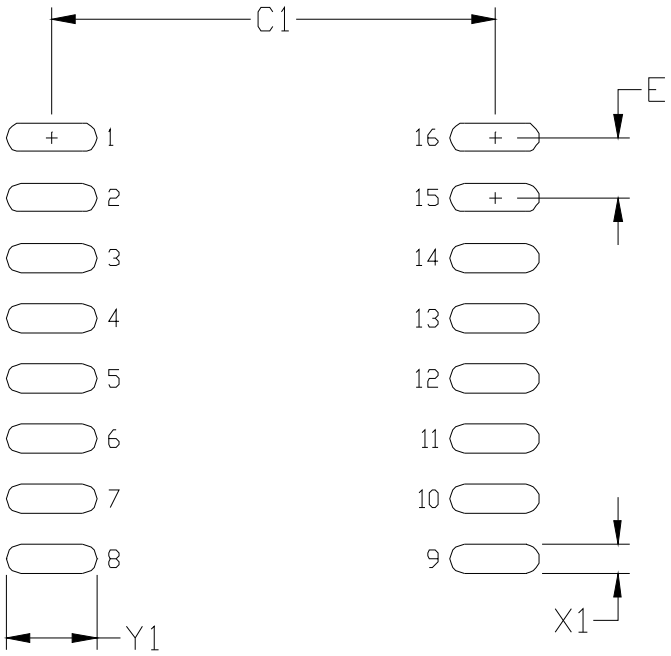


Figure 17. 16-Pin SOIC Land Pattern

Table 18. 16-Pin Wide Body SOIC Landing Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Package Outline: 16-Pin Narrow Body SOIC

Figure 18 illustrates the package details for the Si84xx in a 16-pin narrow-body SOIC (SO-16). Table 19 lists the values for the dimensions shown in the illustration.

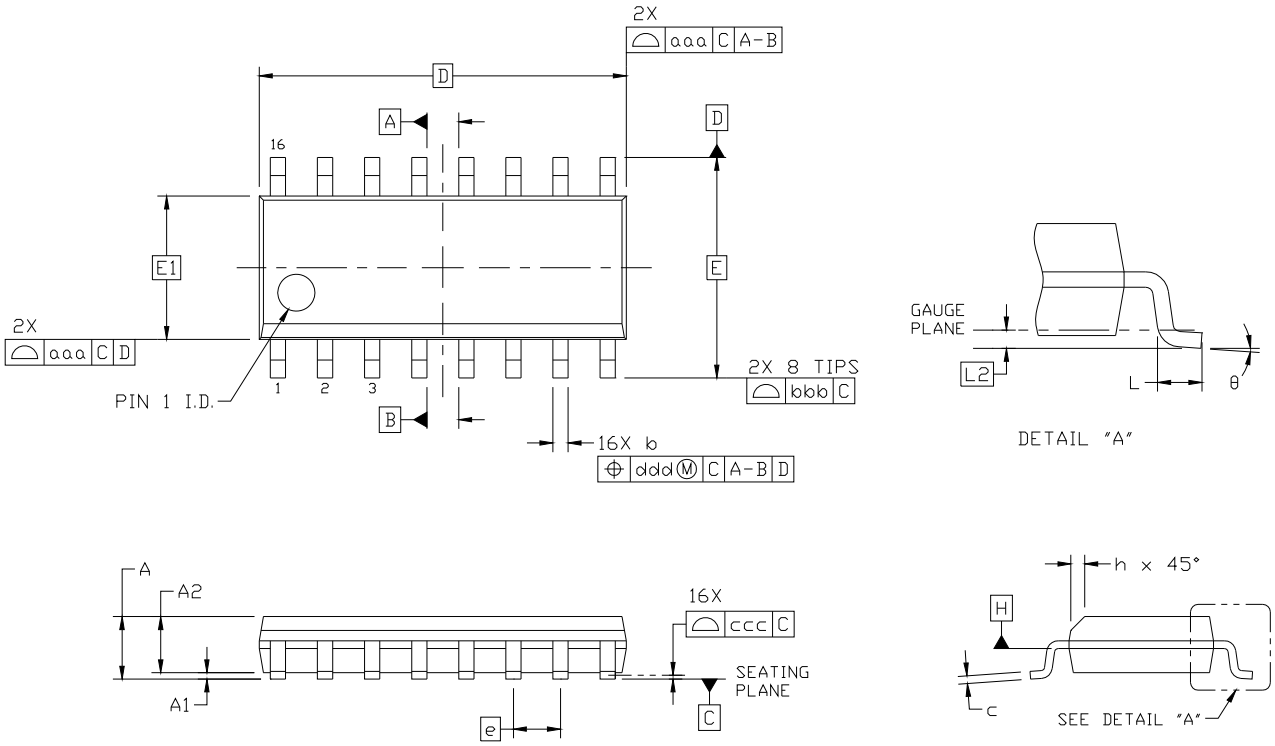


Figure 18. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 19. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 19. Package Diagram Dimensions (Continued)

h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Landing Pattern: 16-Pin Narrow Body SOIC

Figure 19 illustrates the recommended landing pattern details for the Si843x in a 16-pin narrow-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

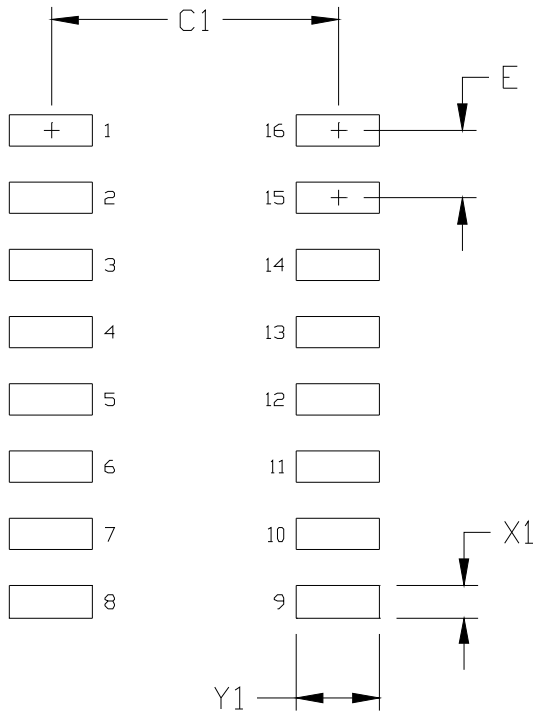


Figure 19. 16-Pin Narrow Body SOIC PCB Landing Pattern

Table 20. 16-Pin Narrow Body SOIC Landing Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Top Marking: 16-Pin Wide Body SOIC

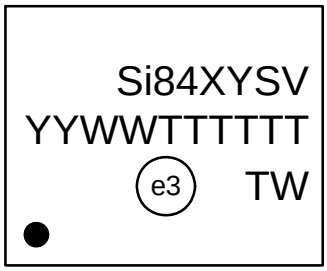


Figure 20. Si8430/31/35 Top Marking

Table 21. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (3, 2, 1) Y = # of reverse channels (1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by Assembly House
	TTTTTT = Mfg Code	Manufacturing Code from Assembly House
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan
***Note:** Si8435 has 0 reverse channels.		

12. Top Marking: 16-Pin Narrow Body SOIC

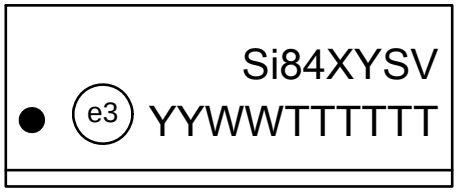


Figure 21. 16-Pin Narrow Body SOIC Top Marking

Table 22. 16-Pin Narrow Body SOIC Top Marking Table

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (3, 2, 1) Y = # of reverse channels (1, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	“e3” Pb-Free Symbol.
***Note:** Si8435 has 0 reverse channels.		

Document Change List

Revision 0.32 to Revision 0.33

- Rev 0.33 is the first revision of this document that applies to the new series of ultra low power isolators featuring pinout and functional compatibility with previous isolator products.
- Updated “1. Electrical Specifications”.
- Updated “6. Ordering Guide”.
- Added “11. Top Marking: 16-Pin Wide Body SOIC”.

Revision 0.33 to Revision 0.34

- Updated all specs to reflect latest silicon.

Revision 0.34 to Revision 0.35

- Updated all specs to reflect latest silicon.
- Added "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24.
- Added "12. Top Marking: 16-Pin Narrow Body SOIC" on page 34.

Revision 0.35 to Revision 1.0

- Updated document to reflect availability of Revision D silicon.
- Updated Tables 1,2, and 3.
  - Updated all supply currents and channel-channel skew.
- Updated Table 4.
  - Updated absolute maximum supply voltage.
- Updated Table 7.
  - Updated clearance and creepage dimensions.
- Updated Table 12.
  - Updated Note 7.
- Updated Table 13.
  - Updated Note 3.
- Updated "4. Errata and Design Migration Guidelines (Revision C Only)" on page 24.
- Updated "6. Ordering Guide" on page 26.

Revision 1.0 to Revision 1.1

- Updated Tables 1, 2, and 3.
  - Updated notes in tables to reflect output impedance of 85 Ω.
  - Updated rise and fall time specifications.
  - Updated CMTI value.

Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "6. Ordering Guide" on page 26.
  - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.