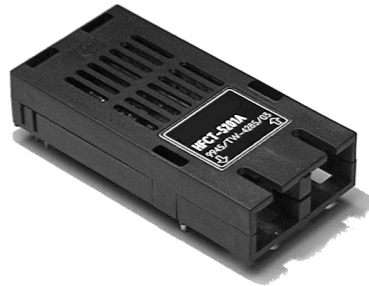


HFCT-5201

155 Mb/s Single Mode Fiber Transceiver for ATM, SONET OC-3/SDH STM-1

Part of the Avago METRAK family

Data Sheet



Description

General

The HFCT-5201 is a 1300 nm laser based transceiver. It provides a very cost-effective solution for medium haul 155 Mb/s data link requirements.

The new multisourced 2 x 9 footprint package style is a variation of the standard 1 x 9 package with an integral Duplex SC connector receptacle. The extra row of 9 pins provides connections for laser bias and optical power monitoring as well as providing transmitter disable function. A block diagram is shown in Figure 1.

Transmitter Section

The transmitter section of the HFCT-5201 consists of a 1300 nm InGaAsP laser in an eyesafe optical subassembly (OSA) which mates to the fiber cable. The laser OSA is driven by a custom, silicon bipolar IC which converts differential input PECL logic signals, ECL referenced to a +5 V supply, into an analog laser drive current.

The laser bias monitor circuit is shown in Figure 2a, the power monitor circuit in Figure 2b.

Receiver Section

The receiver utilizes an InGaAs PIN photodiode mounted together with a silicon bipolar transimpedance preamplifier IC in an OSA. This OSA is connected to a silicon bipolar circuit providing post-amplification quantization, and optical signal detection.

The post amp circuit includes a Signal Detect circuit which provides a PECL logic-high output upon detection of a usable input optical signal level. Signal Detect is a basic fiber failure indicator. This single-ended PECL output is designed to drive a standard PECL input.

Features

- 1300 nm Single mode transceiver for links up to 15 Km
- Compliant with ATM forum 155 Mb/s physical layer specification AF-PHY-0046.000
- Compliant with specifications proposed to ANSI T1E1.2 committee for inclusion in T1.646-1995 Broadband ISDN and T1E1.2/96-002 SONET network to customer installation interface standards
- Compliant with specifications proposed to ANSI T1X1.5 committee for inclusion in T1.105.06 SONET physical layer specifications standard
- Multisourced 2 x 9 pin-out package style derived from 1 x 9 pin-out industry standard package style
- Integral duplex SC connector receptacle compliant with TIA/IA and IEC standards
- Laser bias monitor, power monitor and transmitter disable functions compliant with SONET objectives
- Two Temperature Ranges:
0°C - +70°C HFCT-5201B/D -40°C - +85°C
HFCT-5201A/C
- Single +5 V power supply operation and PECL logic interfaces
- Wave solder and aqueous wash process compatible
- Manufactured in an ISO 9001 certified facility
- Considerable EMI margin to FCC Class B

Applications

- ATM 155 Mb/s links
- SONET OC-3/SDH STM-1 interconnections

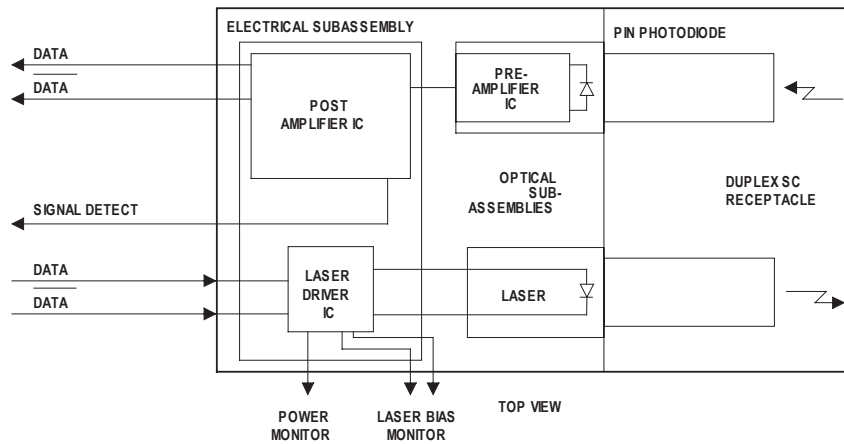


Figure 1. Block Diagram

Receiver Signal Detect

As the input optical power is decreased, Signal Detect will switch from high to low (de-assert point) somewhere between sensitivity and the no light input level. As the input optical power is increased from very low levels, Signal Detect will switch back from low to high (assert point). The assert level will be at least 0.5 dB higher than the de-assert level.

Transceiver Specified for Wide Temperature Range Operation

The HFCT-5201 is specified for operation over normal commercial temperature range of 0° to +70°C (HFCT-5201B/D) or the extended temperature range of -40° to +85°C (HFCT-5201A/C) in an airflow of 2 m/s.

Other Members of Avago SC Duplex

155 Mb/s Product Family

- HFCT-5205, 5103, 5215, 1300 nm single mode transceivers for links up to 40 km. The part is based on the 1 x 9 industry standard package and has an integral duplex SC connector receptacle
- XMT5370155, 1300 nm laser-based transmitter in pigtailed package for 2 km and 15 km links with SMF cables
- XMT5170155, 1300 nm laser-based transmitter in pigtailed package for 40 km links with SMF cables

Applications Information

Typical BER Performance of Receiver versus Input Optical Power Level

The HFCT-5201 transceiver can be operated at Bit-Error-Rate conditions other than the required BER = 1 x 10⁻¹⁰

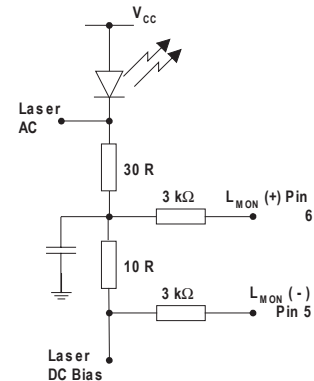


Figure 2a. Laser Bias Monitor

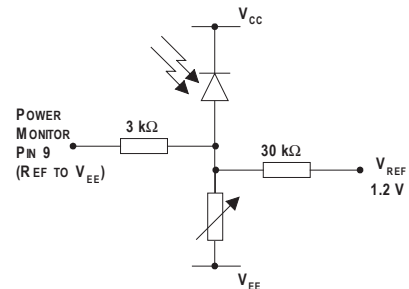


Figure 2b. Power Monitor Circuit

¹⁰ of the ATM Forum 155.52 Mb/s Physical Layer Standard. The typical trade-off of BER versus Relative Input Optical Power is shown in Figure 3. The Relative Input Optical Power in dB is referenced to the Input Optical Power parameter value in the Receiver Optical Characteristics table. For BER conditions better than 1 x 10⁻¹⁰, more input signal is needed (+dB).

Recommended Circuit Schematic

In order to ensure proper functionality of the HFCT-5201 a recommended circuit is provided in Figure 4. When designing the circuit interface, there are a few fundamental guidelines to follow. For example, in the Recommended Circuit Schematic figure the differential data lines should be treated as 50 ohm Microstrip or stripline transmission lines. This will help to minimize the parasitic inductance and capacitance effects. Proper termination of the differential data signals will prevent reflections and ringing which would compromise the signal fidelity and generate unwanted electrical noise. Locate termination at the received signal end of the transmission line. The length of these lines should be kept short and of equal length. For the high speed signal lines, differential signals should be used, not single-ended signals, and these differential signals need to be loaded symmetrically to prevent unbalanced currents from flowing which will cause distortion in the signal.

Maintain a solid, low inductance ground plane for returning signal currents to the power supply. Multilayer

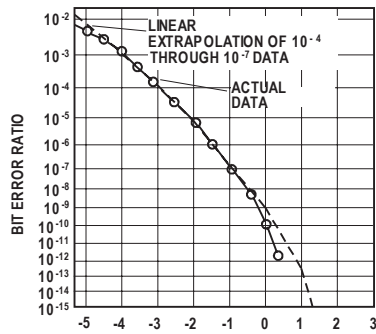


Figure 3. Relative Input Optical Power - dBm. Avg.

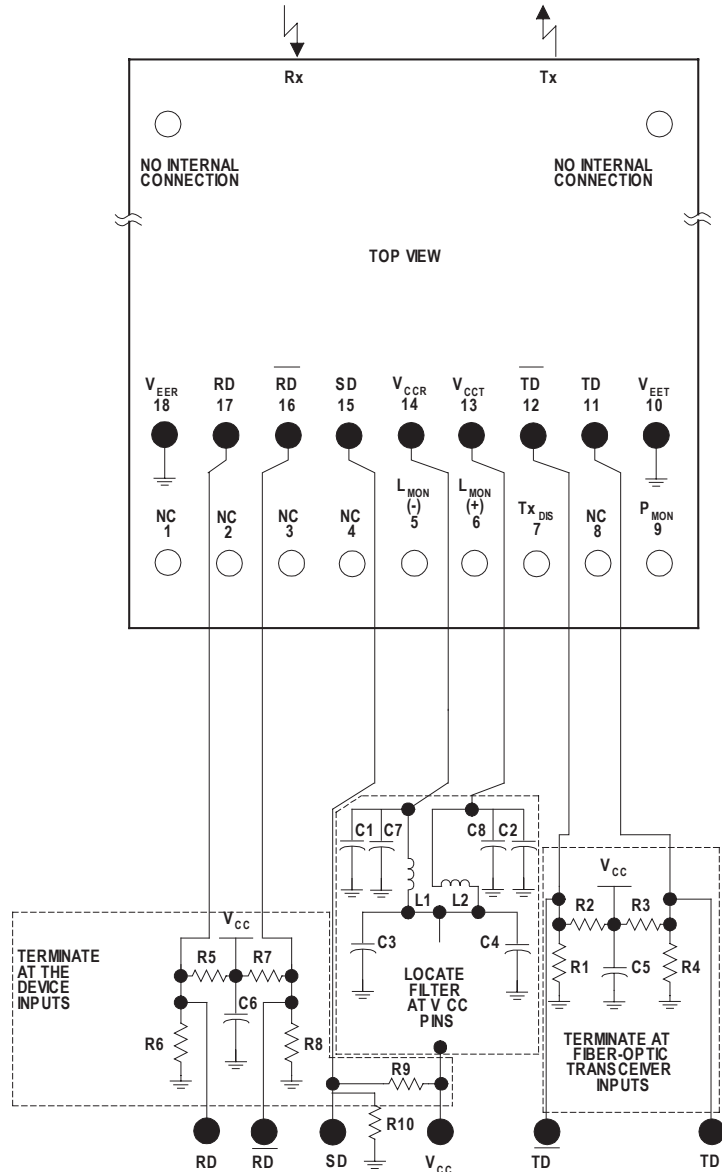
plane printed circuit board is best for distribution of V_{CC} , returning ground currents, forming transmission lines and shielding. Also, it is important to suppress noise from influencing the fiber-optic transceiver performance, especially the receiver circuit. Proper power supply filtering of V_{CC} for this transceiver is accomplished by using the recommended separate filter circuits shown in Figure 4, the Recommended Circuit Schematic diagram for the transmitter and receiver sections. These filter circuits suppress V_{CC} noise of 100 mV peak-to-peak or less over a broad frequency range. This prevents receiver sensitivity degradation due to V_{CC} noise. It is recommended that surface-mount components be used. Use tantalum capacitors for the 10 μ F capacitors and monolithic, ceramic bypass capacitors for the 0.1 μ F capacitors. Also, it is recommended that a surface-mount coil inductor of 3.3 μ H be used. Ferrite beads can be used to replace the coil inductors when using quieter V_{CC} supplies, but a coil inductor is recommended over a ferrite bead. Coils with a low, series dc resistance (<0.7 ohms) and high, self-resonating frequency are recommended. All power supply components need to be placed physically next to the V_{CC} pins of the receiver and transmitter. Use a good, uniform ground plane with a minimum number of holes to provide a low-inductance ground current return for the power supply currents.

Evaluation Circuit Boards

Evaluation circuit boards implementing this recommended circuit design are available from Avago's Application Engineering staff. Contact your local Avago sales representative to arrange for access to one if needed.

Operation in -5.2 V Designs

For applications that require -5.2 V dc power supply level for true ECL logic circuits, the HFCT-5201 transceiver can be operated with a $V_{CC} = 0$ V dc and a $V_{EE} = -5.2$ V dc. This transceiver is not specified with an operating, negative power supply voltage. The potential compromises that can occur with use of -5.2 V dc power are that the absolute voltage states for V_{OH} and V_{OL} will be changed slightly



NOTES:
 THE SPLIT-LOAD TERMINATIONS FOR PECL SIGNALS NEED TO BE LOCATED AT THE INPUT OF DEVICES RECEIVING THOSE PECL SIGNALS.
 $R1 = R4 = R6 = R8 = R10 = 130 \Omega$
 $R2 = R3 = R5 = R7 = R9 = 82 \Omega$
 $C1 = C2 = 10 \mu F$
 $C3 = C4 = C7 = C8 = 100 \text{ nF}$
 $C5 = C6 = 0.1 \mu F$
 $L1 = L2 = 3.3 \mu H$ COIL.

Figure 4. Recommended Circuit Schematic

due to the 0.2 V difference in supply levels. Also, noise immunity may be compromised for the HFCT-5201 transceiver because the ground plane is now the V_{CC} supply point. The suggested power supply filter circuit shown in Figure 4, Recommended Circuit Schematic, should be located in the V_{EE} paths at the transceiver supply pins. Direct coupling of the differential data signals can be done between the HFCT-5201 transceiver and the standard ECL circuits.

Recommended Solder and Wash Process

The HFCT-5201 is compatible with industry standard wave or hand solder processes.

HFCT-5201 Process Plug

The HFCT-5201 transceiver is supplied with a process plug for protection of the optical ports with the Duplex SC connector receptacle. This process plug prevents contamination during wave solder and aqueous rinse as well as during handling, shipping or storage. It is made of high-temperature, molded, sealing material.

Recommended Solder Fluxes and Cleaning/Degreasing Chemicals

Solder fluxes used with the HFCT-5201 fiber-optic transceiver should be water-soluble, organic solder fluxes. Some recommended solder fluxes are Lonco 3355-11 from London Chemical West, Inc. of Burbank, CA, and 100 Flux from Alpha- metals of Jersey City, NJ.

Recommended cleaning and degreasing chemicals for

the HFCT-5201 are alcohol's (methyl, isopropyl, isobutyl), aliphatics (hexane, heptane) and other chemicals, such as soap solution or naphtha. Do not use partially halogenated hydrocarbons for cleaning/degreasing. Examples of chemicals to avoid are 1.1.1. trichloroethane, ketones (such as MEK), acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride or N-methylpyrrolidone.

Regulatory Compliance

The HFCT-5201 is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table 1 for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFCT-5201 has been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these HFCT-5201 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests without a chassis enclosure.

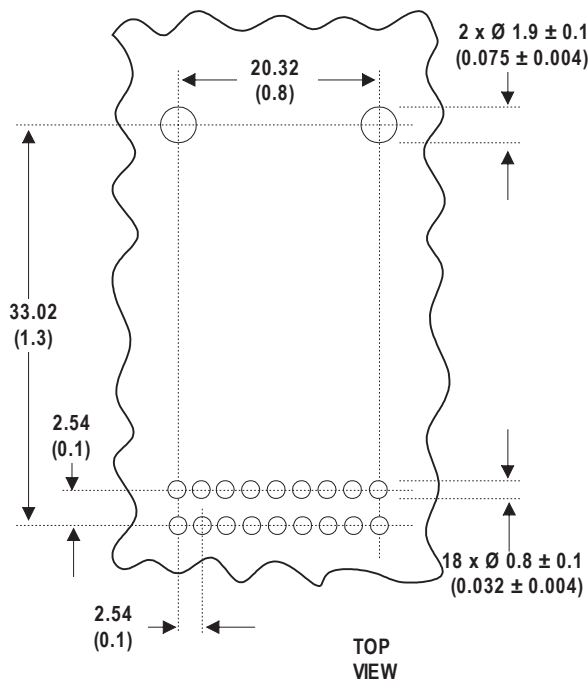
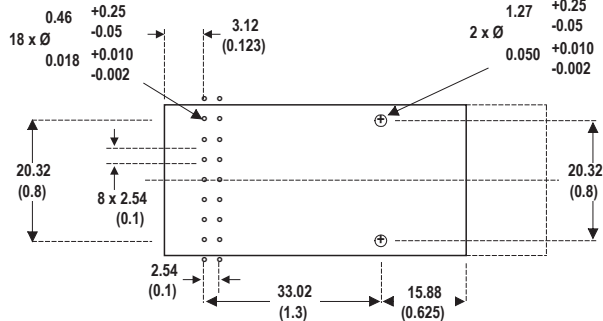


Figure 5. Recommended Board Layout Hole Pattern



Note: SOLDER POSTS AND ELECTRICAL PINS ARE TIN/LEAD PLATED.

DIMENSIONS IN MILLIMETERS (INCHES).

Figure 6. Package Outline Drawing and Pinout

Regulatory Compliance

The HFCT-5201 is intended to enable commercial system designers to develop equipment that complies with the various regulations governing certification of Information Technology Equipment. See the Regulatory Compliance Table 1 for details. Additional information is available from your Avago sales representative.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches and floor mats in ESD controlled areas.

Table 1. Regulatory Compliance - Typical Performance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883 Method 3015	Class 1 (>1000 V)
Electrostatic Discharge (ESD) to the Duplex SC Receptacle	Variation of IEC 61000-4-2	15 kV Air Discharge
Electromagnetic Interference (EMI)	FCC Class B	Typically provide 11 dB margin to FCC Class B when tested in a GTEM cell with the transceiver mounted to a circuit card without a chassis enclosure at frequencies up to 1 GHz. Margins above 1 GHz are dependent on customer board and chassis designs.
Immunity	Variation of IEC 61000-4-3	Typically show no measurable effect from a 10 V/m field swept from 27 MHz to 1 GHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.
Eye Safety	IEC 60825-1 CDRH Class 1	TUV Bauart License: 933/510018/02 CDRH Accession Number: 9521220-31

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the duplex SC connector is exposed to the outside of the equipment chassis it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan.

The HFCT-5201 has been characterized without a chassis enclosure to demonstrate the robustness of the part's integral shielding. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests with no chassis enclosure.

Immunity

Equipment utilizing these HFCT-5201 transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers, with their integral shields, have been characterized without the benefit of a normal equipment chassis enclosure and the results are reported below. Performance of a system containing these transceivers within a well designed chassis is expected to be better than the results of these tests without a chassis enclosure.

Performance Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T _S	-40	+85	°C	
Operating Temperature - HFCT-5201 A/C	-	-40	+85	°C	1
Operating Temperature - HFCT-5201 B/D	-	0	+70	°C	1
Lead Soldering Temperature/Time	-	-	+260/10	°C/s	
Output Current (other outputs)	I _{OUT}	0	30	mA	
Input Voltage	-	GND	V _{CC}	V	
Power Supply Voltage	-	0	+6	V	

Operating Environment

Parameter	Symbol	Minimum	Maximum	Units	Notes
Power Supply Voltage ECL Operation	V _{CC}	-4.95	-5.45	V	
Power Supply Voltage PECL Operation	V _{CC}	+4.75	+5.25	V	
Ambient Operating Temperature - HFCT-5201 A/C	T _{OP}	-40	+85	°C	1
Ambient Operating Temperature - HFCT-5201 B/D	T _{OP}	0	+70	°C	1

Transmitter Section

(Ambient Operating Temperature, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Output Center Wavelength	λ _{ce}	1261	-	1360		
Output Spectral Width (RMS)	Δλ	-	-	7.7	nm	
Average Optical Output Power	P _O	-15	-	-8	dBm	2
Extinction Ratio	E _R	8.2	-	-	dB	
Bias Monitor	-	-	0.1	-	mA/mV	3
Rear Facet Monitor	-	-	V _{EE} +1.2	-	V	
Tx Disable	TX _{DIS}	V _{CC} -3.2	-	V _{CC}	V	
Power Supply Current	I _{CC}	-	140	-	mA	4
Output Eye	Compliant with Bellcore TR-NWT-000253 and ITU recommendation G957					

Receiver Section

(Ambient Operating Temperature, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Receiver Sensitivity	-	-31	-	-	dBm	5
Maximum Input Power	-	-7	-	-	dBm	
Alarm ON	-	-45	-	-31	dBm	
Hysteresis	-	0.5	-	4.0	dB	
Power Supply Current	I _{CC}	-	-	100	mA	6
Data Outputs	ECL/PECL					
Alarm Output	ECL/PECL					

Notes:

- 2 m/s air flow required.
- Output power is power coupled into a single mode fiber.
- Common mode signal 2.5 V nominal.
- The power supply current varies with temperature. Maximum current is specified at V_{CC} = Maximum@ maximum temperature (not including terminations) and end of life.
- Minimum sensitivity and saturation levels for a 2²³-1 PRBS with 72 ones and 72 zeros inserted. (ITU recommendation G.958).
- The current excludes the output load current.

Table 2. Pin Out Table

Pin	Symbol	Functional Description
Mounting Studs		The mounting studs are provided for transceiver mechanical attachment to the circuit board. They are embedded in the non-conductive plastic housing and are not connected to the transceiver internal circuit. They should be soldered into plated-through holes on the printed circuit board.
1	N/C	
2	N/C	
3	N/C	
4	N/C	
5	L _{MON(-)}	Laser Bias Monitor (-) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
6	L _{MON(+)}	Laser Bias Monitor (+) This analog current is monitored by measuring the voltage drop across a 10 ohm resistor placed between high impedance resistors connected to pins 5 and 6 internal to the transceiver.
7	TX _{DIS}	Transmitter Disable Transmitter Output Disabled: $V_{CCT} - 1.5V \leq V_7 \leq V_{CCT}$ Transmitter Output Uncertain: $V_{CCT} - 4.2V \leq V_7 \leq V_{CCT} - 1.5V$ Transmitter Output Enabled: $V_{EET} \leq V_7 \leq V_{CCT} - 4.2V$ or open circuit
8	N/C	
9	P _{MON}	Power Monitor The analog voltage measured at this high impedance output provides an indication of whether the optical power output of the Laser Diode is operating within the normal specified power output range per the following relationships: High Light Indication: $V_9 \geq V_{EET} + 1.7V$ Normal Operation: $V_9 \approx V_{EET} + 1.2V$ Low Light Indication: $V_9 \leq V_{EET} + 0.7V$
10	V _{EET}	Transmitter Signal Ground Directly connect this pin to the transmitter signal ground plane.
11	TD+	Transmitter Data In Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
12	TD-	Transmitter Data In Bar Terminate this high-speed, differential Transmitter Data input with standard PECL techniques at the transmitter input pin.
13	V _{CCT}	Transmitter Power Supply Provide +5 V dc via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the V _{CCT} pin.
14	V _{CCR}	Receiver Power Supply Provide +5 V dc via the recommended receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the V _{CCR} pin.
15	SD	Signal Detect Normal input optical levels to the receiver result in a logic "1" output. Low input optical levels to the receiver result in a fault indication shown by a logic "0" output. Signal Detect is a single-ended, low-power, PECL output. For low power applications a 10kΩ termination resistor may be connected to V _{EE} to achieve PECL output levels. This Signal Detect output can be used to drive a PECL input on an upstream circuit, such as, Signal Detect input and Loss of Signal-bar input.
16	RD-	Receiver Data Out Bar Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
17	RD+	Receiver Data Out Terminate this high-speed, differential, PECL output with standard PECL techniques at the follow-on device input pin.
18	V _{EER}	Receiver Signal Ground Directly connect this pin to receiver signal ground plane.

Ordering Information

Temperature Range 0°C to +70°C

HFCT-5201B	Black Case
HFCT-5201D	Blue Case

Temperature Range -40°C to +85°C

HFCT-5201A	Black Case
HFCT-5201C	Blue Case

Supporting Documentation

Application Note 1098
Characterization Report
Interim Reliability Data Sheet