Intel® TXN17431 (0850) 10.3 Gbps 850 nm Optical Transceiver Compliant with XENPAK MSA

Datasheet

Product Features

- 10BASE-SR 10.3 Gbps Optical Transceiver, IEEE 802.3ae Compliant
- Available for 10.3 Gpbs Ethernet Bit Rate (up to 300 m multi-mode fiber) Applications
- XENPAK Multisource Agreement (MSA) Compliant Form Factor and Pin Configuration
- XAUI Data Interface via standard 70-Pin Connector
- Faceplate, Z-Axis Hot-Plug Capability
- Digital Management Interface (MDIO) Compatible with the IEEE Standard and XENPAK MSA
- Class 1 Laser Safety Product
- IEC/UL 60950-1 Safety Certified
- Designed and verified as RoHS compliant
- China RoHS compliant with 30-year EFUP

Applications

- 10 Gigabit Ethernet equipment, high density data-center applications, including:
  - — Enterprises Switches
  - — Optical Router
  - — Enterprise Stackable Switches
  - — Optical Test Equipment

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Revision History

Date	Revision	Description
2-Nov-2007	005	Updated Section 10.0, “Regulatory Compliance” on page 40 and Section 11.0, “Ordering Information” on page 43. Change bars indicate areas of change.
27-Sep-2007	004	Updated “Regulatory Compliance”.
12-Jul-2005	003	Modified “Optical Specifications — Transmitter”; changed Transmitter and Dispersion Penalty to Transmiter Dispersion Penalty and removed TDP; added table note. Modified “Optical Specifications — Receiver”: Removed “Receiver Sensitivity.”
26-May-2005	002	Updated Part Number and MM Number in “Ordering Information” and “Addendum for Cisco Systems Only”.
29-Apr-2005	001	Initial release.

Related Hardware and Documents

Part Number	Description
TXNEB17431	**XENPAK Evaluation board:** Provides access to all XAUI interfaces, control, and monitor signals.

1.0 Introduction

The Intel® TXN17431 (0850) Optical Transceiver is a 10.3 Gbps 850 nm Optical Transceiver compliant with the XENPAK Multisource Agreement (MSA). The TXN17431 Optical Transceiver provides an IEEE 802.3ae 2002-compliant 10GBASE-SR interface between the photonic physical layer and the electrical section layer.

The TXN17431 Optical Transceiver is comprised of an optical transmitter and receiver pair integrated with XAUI-to-serial conversion. PCS, PMA, and PMD functions are included.

Note: Unless otherwise noted, the Intel® TXN17431 (0850) 10.3 Gbps 850 nm Optical Transceiver Compliant with XENPAK MSA will be called the TXN17431 Optical Transceiver throughout the remainder of this document.

The TXN17431 Optical Transceiver transmitter section decodes four 8B/10B-encoded channels running at 3.125 Gbps for Ethernet from a XAUI parallel data bus, performs a 64B/66B scrambling and multiplexes the results into a 10.3125 Gbps optical signal launched into a multi-mode optical fibre using an 850 nm Vertical Cavity Surface Emitting Laser (VCSEL).

The TXN17431 Optical Transceiver receiver section de-multiplexes a single 10.3 Gbps (Ethernet) optical signal and converts it back to four channels of 3.125 Mbps (Ethernet) XAUI. The receiver includes a photodiode, transimpedance amplifier, clock recovery, decision circuit, and de-multiplexer. The receiver operates over an 850 nm band for 10GBASE-SR.

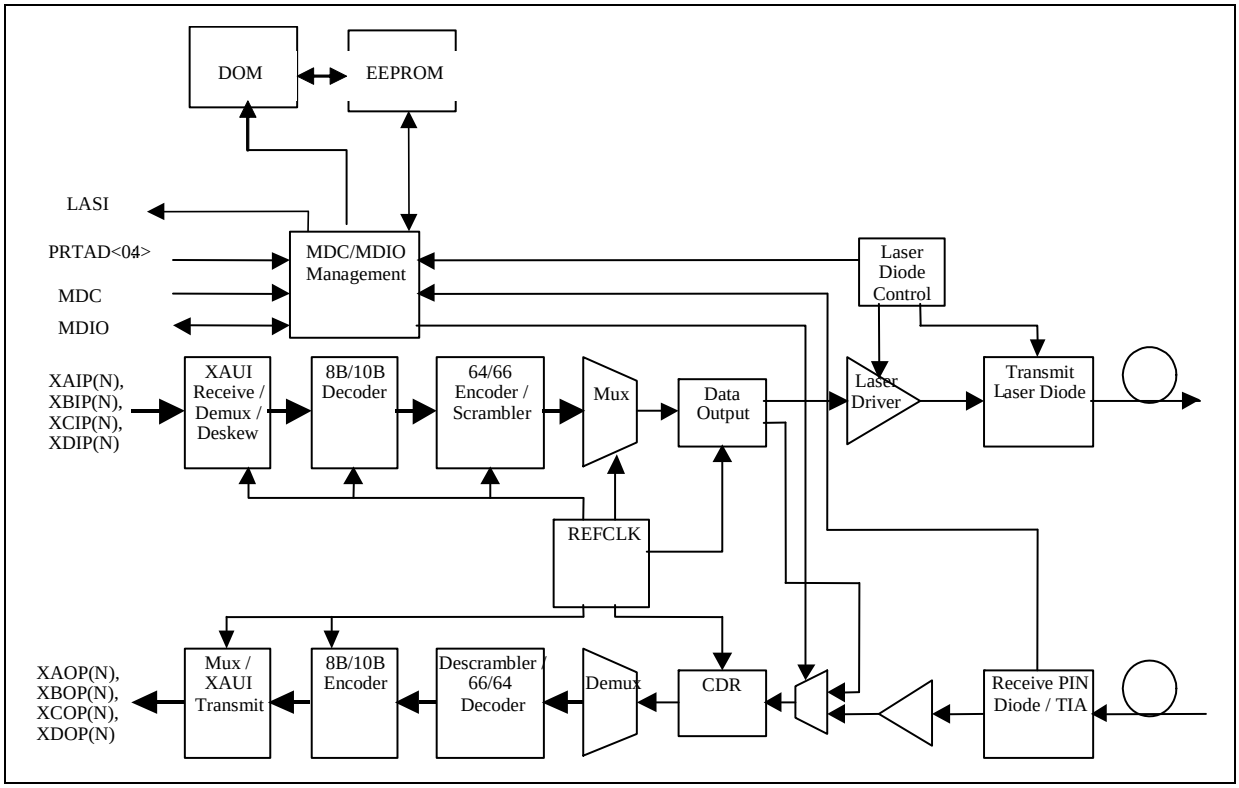
Figure 1 illustrates the TXN17431 Optical Transceiver block diagram.

The TXN17431 Optical Transceiver is assembled in a XENPAK MSA-compatible 4.8 in. L × 1.4 in. W × 0.7 in. H package. The heat sink is designed for a 50 °C ambient temperature with 200 linear feet-per-minute airflow. A XENPAK MSA-compliant, 70-pin, board edge connector provides/supplies the electrical interface. Optical connections are made with standard SC-UPC optical connectors.

The TXN17431 Optical Transceiver is designed for link spans up to 300 m and uses an 850 nm Transistor Outline (TO)-can laser source.

An IEEE 802.3ae version 5 and XENPAK MSA-compliant Management Data Interface (MDIO) with Digital Optical Monitoring (DOM) support is included.

Figure 1. Block Diagram



2.0 Ratings

Table 1 lists the absolute maximum ratings for the TXN17431 Optical Transceiver. Table 2 lists the required power supplies. Minimum and maximum values listed in Table 3 through Table 6 apply over the recommended operating conditions specified in Table 2.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Case operating temperature range	T_C	0	+70	°C
Case storage temperature range	T_S	40	+85	°C
Positive supply voltage (+3.3 V)	$V_{3.3}+$	0	+3.6	V
Positive supply voltage (+1.8 V APS)	$V_{1.8}+$	0	+2.0	V
Positive supply voltage (+5 V)	V_5+	0	5.5	V
Relative humidity (non-condensing)	RH	–	85	%
Receiver input power	–	–	-1	dBm

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Power Supply Characteristics (10GBASE-SR)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Positive supply voltage (+5.0 V)	V_5+	4.75	5.0	5.25	V
Positive supply current drain (+5.0 V)	I_5+	–		0.22	A
Positive supply voltage (+3.3 V)	$V_{3.3}$+	+3.135	+3.3	+3.465	V
Positive supply current drain (+3.3 V)	$I_{3.3}$+			0.6	A
Positive supply voltage (+1.8 V) APS	$V_{1.8}$+	+1.728	+1.8	+1.872	V
Positive supply current drain (+1.8 V) APS	$I_{1.8}$+	–	–	0.50	A
Negative Voltage due to transient current for all supplies	V_{tran}	–	–	-0.3	V
Total Power Dissipation	Pdiss	–	–	6	W

NOTE: Case operating temperature = 0 °C to 70 °C.

3.0 Optical Specifications

The TXN17431 Optical Transceiver is designed for applications consistent with IEEE 802.3ae version 5.0 recommendations for 10GBASE-SR. Table 3 through Table 6 list the transmitter, link, and receiver specifications.

Table 3. Optical Specifications — Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Wavelength	λ	840	–	860	nm
Signaling Speed (nominal)	–	–	10.3125	–	GBd
Signaling Speed Variation from nominal	–	-100	–	100	ppm
Average Launch Power (Meets Class 1 safety limits)	–	-7.3	–	-1	dBm
Average Launch Power of Off Tx	–	–	–	-30	dBm
Minimum OMA[1]	–	–	see Table 4	–	
Transmitter Dispersion Penalty[3]	–	–	–	3.9	dBm
Extinction Ratio	r_e	3	–	–	dB
RIN12OMA (maximum)	RIN	–	–	-128	dB/Hz
RMS Spectral Width	–	–	–	0.45	nm
Optical Return Loss	ORLT	–	–	12	dB
Eye Mask of Optical Output	Compliant with IEEE 802.3ae 2002 specifications				
Encircled Flux	See Note 2				

1. Per triple trade-off curves for 10G BASE-SR.
2. The encircled flux at 19 μm shall be greater than or equal to 86% and the encircled flux at 4.5 μm shall be less than or equal to 30% when measured into type A1a (50/125 μm multi-mode) fiber per TIA-455-203.
3. Transmitter Dispersion Penalty was tested using the two worst-case links from Table 52-6 in IEEE 802.3ae.

Table 4. Minimum OMA (dBm) as a Function of Center Wavelength and Spectral Width

Center Wavelength (nm)	RMS Spectral Width (nm)								
	Up to 0.05	0.05 to 0.1	0.1 to 0.15	0.15 to 0.2	0.2 to 0.25	0.25 to 0.3	0.3 to 0.35	0.35 to 0.4	0.4 to 0.45
840 to 842	-4.2	-4.2	-4.1	-4.1	-3.9	-3.8	-3.5	-3.2	-2.8
842 to 844	-4.2	-4.2	-4.2	-4.1	-3.9	-3.8	-3.6	-3.3	-2.9
844 to 846	-4.2	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
846 to 848	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-2.9
848 to 850	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.3	-3.0
850 to 852	-4.3	-4.2	-4.2	-4.1	-4.0	-3.8	-3.6	-3.4	-3.0
852 to 854	-4.3	-4.2	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
854 to 856	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.4	-3.1
856 to 858	-4.3	-4.3	-4.2	-4.1	-4.0	-3.9	-3.7	-3.5	-3.1
858 to 860	-4.3	-4.3	-4.2	-4.2	-4.1	-3.9	-3.7	-3.5	-3.2

Table 5. Optical Specifications — Link

Parameter	62.5 µm MMF		50 µm MMF			Unit
Modal bandwidth as measured at 850 nm	160	200	400	500	2000	MHz.km
Power budget	7.3	7.3	7.3	7.3	7.3	dB
Link distance	26	33	66	82	300	meter
Link overall optical return loss	12	12	12	12	12	dB

Table 6. Optical Specifications — Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit
Average receive power (maximum)	–	–	–	-1.0	dBm
Stressed receiver sensitivity (OMA)[1]	PRS_{OMA}	–	–	-7.5	dBm
Receiver reflectance	–	–	–	-12	dB
Center wavelength	λ	840	850	860	nm
Signaling Speed Nominal	–	–	10.3125, 10.51875	–	GBd
Signaling Speed Variation from nominal	–	–	–	100	ppm
Receive Electrical 3 dB upper cutoff frequency	–	–	–	12.3	GHz

1. Measured with 3.5 dB vertical eye closure penalty and 0.3UI pk-pk stressed eye jitter.

4.0 Control and Monitoring Functions

The TXN17431 Optical Transceiver provides digital control and monitoring functions as listed in Table 7.

Table 7. Digital Control and Monitoring Signals

Function	Pin Name	Pin #	Description	Interface
Management data interface	MDIO	17	Digital interface provides access to management data as specified in IEEE 802.3ae XAUI interface specifications and XENPAK MSA	1.2 V CMOS compatible
Management data clock	MDC	18	Clock for management data interface	1.2 V CMOS compatible
Input pins for setting module port address	PRTAD	19–23	Allows the MDIO address to be set	1.2 V CMOS compatible
Link alarm status interrupt	LASI	9	Logic low indicates status interrupt triggered, logic high indicates normal operation	Open drain compatible 10–22 k pull-up on host 1.2 V CMOS compatible
Transmitter on/off	TX ON/OFF	12	Turns off laser. Optical output power with laser turned off is less than -30 dBm.	Open drain compatible 14.7 k pull-up on transceiver 1.2 V CMOS compatible
Module reset	RESET	10	Logic high for normal operation, logic low for reset	Open drain compatible 14.7 K pull-up on transceiver 1.2 V CMOS compatible
Module detect	MOD DETECT	14	Indicates presence of module	Connected to signal ground inside module through 1 KΩ resistor
Adaptive power supply	APS	7-8 28–29	Adaptive power supply input	The device requires 1.8V at these pins.
APS sense connection	APS_SENSE	27	Adaptive power supply voltage select pin	This pin is a direct sense of the APS voltage on pins 7–8 and 28–29 at an internal point
APS configuration	APS_SET	25	Feedback input for APS	This pin will be connected to the ground inside module to direct an adaptive power supply to provide 1.8 V.

5.0 Data Output / Input Configuration

The TXN17431 Optical Transceiver is fully compliant with IEEE 802.3ae standards for XAUI data format. Table 8 lists the I/O configuration. Table 9 lists the complete pinout for the TXN17431 Optical Transceiver.

Table 8. Data Input/Output Configuration (Sheet 1 of 2)

Pin Name	In/Out	Description	Logic
TX LANE0+ TX LANE0-	In	Transmitter XAUI input differential pair—Lane 0	Compliant with IEEE 802.3ae clause 47
TX LANE1+ TX LANE1-	In	Transmitter XAUI input differential pair—Lane 1	Compliant with IEEE 802.3ae clause 47
TX LANE2+ TX LANE2-	In	Transmitter XAUI input differential pair—Lane 2	Compliant with IEEE 802.3ae clause 47
TX LANE3+ TX LANE3-	In	Transmitter XAUI input differential pair—Lane 3	Compliant with IEEE 802.3ae clause 47
RX LANE0+ RX LANE0-	Out	Receiver XAUI output differential pair—Lane 0	Compliant with IEEE 802.3ae clause 47

Table 8. Data Input/Output Configuration (Sheet 2 of 2)

Pin Name	In/Out	Description	Logic
RX LANE1+ RX LANE1-	Out	Receiver XAUI output differential pair—Lane 1	Compliant with IEEE 802.3ae clause 47
RX LANE2+ RX LANE2-	Out	Receiver XAUI output differential pair—Lane 2	Compliant with IEEE 802.3ae clause 47
RX LANE3+ RX LANE3-	Out	Receiver XAUI output differential pair—Lane 3	Compliant with IEEE 802.3ae clause 47

Table 9. Pin Configuration (Sheet 1 of 3)

Pin #	Name	In/Out	Function	Notes
1	GND	–	Electrical ground	1
2	GND	–	Electrical ground	1
3	GND	–	Electrical ground	1
4	5.0 V	–	Power	2
5	3.3 V	–	Power	2
6	3.3 V	–	Power	2
7	APS	I	Adaptive power supply input. The Intel® TXN17431(0850) 10.3 Gbps 850 nm Optical Transceiver uses 1.8 V	–
8	APS	I	Adaptive power supply input. The Intel® TXN17431(0850) 10.3 Gbps 850 nm Optical Transceiver uses 1.8 V	–
9	LASI	O	Link alarm status interrupt	–
10	RESET	I	Module reset	–
11	NC	–	Vendor specific, do not connect	–
12	TX ON/OFF	I	Transmitter shutoff	–
13	NC	–	Vendor specific, do not connect	–
14	MOD DETECT	O	Indicates presence of module	–
15	I^2C_CLK	I	Clock line for I^2C bus (Do not connect)	–
16	I^2C_DATA	I	Data line for I^2C bus (Do not connect)	–
17	MDIO	I/O	Management data interface	–
18	MDC	I	Clock for management data interface	–
19	PRTAD4	I	Port address bit 4	–
20	PRTAD3	I	Port address bit 3	–
21	PRTAD2	I	Port address bit 2	–
22	PRTAD1	I	Port address bit 1	–
23	PRTAD0	I	Port address bit 0	–
24	NC	–	Vendor specific, do not connect	–
25	APS_SET	I	This pin is connected to ground inside the module through a 0 Ω resistor for 1.8 V APS SENSE pin	–
26	NC	–	No Connect	–
27	APS SENSE	I	This pin is a direct sense of the APS voltage	–

1. Ground connections are common for transmit and receive.
2. VCC contacts are each rated at 0.5 A.

Table 9. Pin Configuration (Sheet 2 of 3)

Pin #	Name	In/Out	Function	Notes
28	APS	I	Adaptive power supply input. The TXN17431 Optical Transceiver uses 1.8 V.	–
29	APS	I	Adaptive power supply input. The TXN17431 Optical Transceiver uses 1.8 V.	–
30	3.3 V	–	Power	2
31	3.3 V	–	Power	2
32	5.0 V	–	Power	2
33	GND	–	Electrical ground	1
34	GND	–	Electrical ground	1
35	GND	–	Electrical ground	1
36	GND	–	Electrical ground	1
37	GND	–	Electrical ground	1
38	NC	–	No connect	–
39	NC	–	No connect	–
40	GND	–	Electrical ground	1
41	RX LANE0+	O	Module XAUI output lane 0+	–
42	RX LANE0-	O	Module XAUI output lane 0-	–
43	GND	–	Electrical ground	1
44	RX LANE1+	O	Module XAUI output lane 1+	–
45	RX LANE1-	O	Module XAUI output lane 1-	–
46	GND	–	Electrical ground	1
47	RX LANE2+	O	Module XAUI output lane 2+	–
48	RX LANE2-	O	Module XAUI output lane 2-	–
49	GND	–	Electrical ground	1
50	RX LANE3+	O	Module XAUI output lane 3+	–
51	RX LANE3-	O	Module XAUI output lane 3-	–
52	GND	–	Electrical ground	1
53	GND	–	Electrical ground	1
54	GND	–	Electrical ground	1
55	TX LANE0+	I	Module XAUI input lane 0+	–
56	TX LANE0-	I	Module XAUI input lane 0-	–
57	GND	–	Electrical ground	1
58	TX LANE1+	I	Module XAUI input lane 1+	–
59	TX LANE1-	I	Module XAUI input lane 1-	–
60	GND	–	Electrical ground	1
61	TX LANE2+	I	Module XAUI input lane 2+	–
62	TX LANE2-	I	Module XAUI input lane 2-	–
63	GND	–	Electrical ground	1
64	TX LANE3+	I	Module XAUI input lane 3+	–
65	TX LANE3-	I	Module XAUI input lane 3-	–

1. Ground connections are common for transmit and receive.
2. VCC contacts are each rated at 0.5 A.

Table 9. Pin Configuration (Sheet 3 of 3)

Pin #	Name	In/Out	Function	Notes
66	GND	–	Electrical ground	1
67	NC	–	No connect	–
68	NC	–	No connect	–
69	GND	–	Electrical ground	1
70	GND	–	Electrical ground	1

1. Ground connections are common for transmit and receive.
2. VCC contacts are each rated at 0.5 A.

6.0 MDIO Interface

The TXN17431 Optical Transceiver supports the management data input/output (MDIO) interface as defined by IEEE 802.3ae Clause 45 and XENPAK MSA. This interface consists of the following:

- A two-wire physical interface
- A frame format
- An MDIO register set
- A timing relationship for reads and writes to the MDIO registers

6.1 MDIO Physical Interface

The two wires of the physical interface are the management data clock (MDC) and the MDIO. The MDC is an input clock signal to synchronize the MDIO data stream. The minimum clock period required is 400 ns with a minimum high pulse level and low pulse level at each 160 ns.

The MDIO data stream is a serial bi-directional signal to send control and receive management status information. Please refer to the frame format section for exact bit transferring sequence.

6.2 MDIO Access Frame Format

The MDIO read and write operations use indirect register addressing. Thus, register addresses need to be pre-written as a setup for a subsequent read or write operation. A possible operation sequence uses the ADDRESS frame to reference the register location and then performs address incrementing (READ INC) for subsequent reads.

Note: A single read only or write only does not automatically increment the address.

Table 10. MDIO Frame Format

Transaction Type	PRE[1]	ST[2]	Opcode[3]	PRTAD[4]	DID[5]	TA[6]	AD[7]	IDLE[8]
ADDRESS	1...1	00	00	PRTAD[4:0]	DID[4:0]	10	AD[15:0]	Z
WRITE	1...1	00	01	PRTAD[4:0]	DID[4:0]	10	AD[15:0]	Z
READ	1...1	00	11	PRTAD[4:0]	DID[4:0]	Z0	AD[15:0]	Z
READ INC	1...1	00	10	PRTAD[4:0]	DID[4:0]	Z0	AD[15:0]	Z

1. **Preamble (PRE):** A pattern of 32 logic one bits used for clock and data synchronization.
2. **Start of Frame (ST):** Two bit logic 0 ensures transitions from default logic one to zero.
3. **Opcode:** Indicates the MDIO transaction type. "00" indicates register addressing command, "01" indicates write data to register command, "11" indicates read data from register command, "10" indicates read data return and address increment.
4. **PRTAD:** A 5-bit port address set through PRTAD[4:0] pins at the connector level.
5. **DID:** Device address is 5 bits but only valid combinations are "00001" for accessing PMA/PMD, "00011" for accessing PCS and "00100" for accessing PHY XS.
6. **TA:** Two bit time spacing between the addressing and data fields to avoid contention during a read transaction.
7. **AD:** This address/data field is 16 bits; the most significant bit is transmitted/received first.
8. **IDLE:** MDIO high impedance state will disable all three state drivers.

6.3 MDIO Register Set

This section provides information on the location and functionality of the TXN17431 Optical Transceiver Registers. The MDIO Register set is divided into the following five register sections:

- "PMA/PMD Control Registers (Device ID = 1h)" on page 17
  Physical Medium Attachment/Physical Medium Dependent (PMA/PMD) control
- "PCS Control Registers (Device ID = 3h)" on page 22
  Physical Coding Sublayer (PCS) control
- "PHY_XS Control Registers (Device ID = 4h)" on page 26
  XGMII Extender Sublayer (PHY XGXS) control
- "XENPAK NVR Registers and NVR EEPROM Description" on page 30
- "XENPAK DOM/LASI Control and Status Registers" on page 31

Unique device IDs address the various registers.

Abbreviations under the register Access column are described as follows:

Abbreviation	Register Access Description
RO	**Read only register:** Writes are ignored
R/W	**Read and write register:** Reads and writes are allowed with the proper read/write sequence
RO, LL	**Read only register:** The latched low bit is reset to high by a read unless the input low state is present
R/W, SC	**Self clearing read/write register:** The bit clears itself after transaction
RO, LH	**Read only register:** Latched high bit is reset to low by a read unless the input high state is present

6.3.1 Register Set

Table 11 through Table 15 list the five register sets for the TXN17431 Optical Transceiver Register sets.

Table 11. PMA/PMD Control Register Set: Device ID = 1h

Address	Register Name	Reference
0h	"PMA/PMD Control 1 Register (DID = 1h, Address = 0h)"	Table 16 on page 17
1h	"PMA/PMD Status 1 Register (DID = 1h, Address = 1h)"	Table 17 on page 18
4h	"PMA/PMD Speed Ability Register (DID = 1h, Address = 4h)"	Table 19 on page 18
5h	"PMA/PMD Devices in Package Register (DID = 1h, Address = 5h)"	Table 20 on page 19
7h	"PMA/PMD Control 2 Register (DID = 1h, Address = 7h)"	Table 21 on page 19
8h	"PMA/PMD Status 2 Register (DID = 1h, Address = 8h)"	Table 22 on page 20
9h	"PMD Transmit Disable Register (DID = 1h, Address = 9h)"	Table 23 on page 20
ah	"PMD Receive Signal OK Register (DID = 1h, Address = ah)"	Table 24 on page 20
eh	"Package Identifier OUI Register (DID = 1h, Address = eh)"	Table 25 on page 20
fh	"Package Identifier OUI Register (DID = 1h, Address = fh)"	Table 26 on page 21
c001h	"PMA Network Loopback Register (DID = 1h, Address = c001h)"	Table 26 on page 21
c003h	"EEPROM Control Register (DID = 1h, Address = c003h)"	Table 27 on page 21
c004h	"EEPROM Checksum Register (DID = 1h, Address = c004h)"	Table 28 on page 22

Table 12. PCS Control Register Set: Device ID = 3h

Address	Register Name	Reference
0h	"PCS Control 1 Register (DID = 3h, Address = 0h)"	Table 29 on page 22
1h	"PCS Status 1 Register (DID = 3h, Address = 1h)"	Table 30 on page 22
4h	"PCS Speed Ability Register (DID = 3h, Address = 4h)"	Table 31 on page 23
5h	"PCS Devices in Package Register (DID = 3h, Address = 5h)"	Table 32 on page 23
7h	"PCS Control 2 Register (DID = 3h, Address = 7h)"	Table 33 on page 23
22h-25h	"10GBASE-R PCS Jitter Test Pattern Seed A Registers (DID = 3h, Address = 22h to 25h)"	Table 37 on page 24
29h	"10GBASE-R PCS Jitter Test Pattern Seed B Registers (DID = 3h, Address = 26h to 29h)"	Table 38 on page 25
2bh	"10GBASE-R PCS Jitter Test Counter Register (DID = 3h, Address = 2bh)"	Table 40 on page 25
c006h	"Fiber PRBS Mode Register (DID = 3h, Address = c006h)"	Table 42 on page 26

Table 13. PHY_XS Control Register Set: Device ID = 4h (Sheet 1 of 2)

Address	Register Name	Reference
0h	"PHY_XS Control 1 Register (DID = 4h, Address = 0h)"	Table 43 on page 26
1h	"PHY_XS Status 1 Register (DID = 4h, Address = 1h)"	Table 44 on page 27
8h	"PHY_XS Status 2 Register (DID = 4h, Address = 8h)"	Table 47 on page 27
18h	"PHY_XS Lane Status Register (DID = 4h, Address = 18h)"	Table 48 on page 28
19h	"PHY_XS Test Control Register (DID = 4h, Address = 19h)"	Table 49 on page 28
c000h	"PHY_XS Control 2 Register (DID = 4h, Address = c000h)"	Table 50 on page 28

Table 13. PHY_XS Control Register Set: Device ID = 4h (Sheet 2 of 2)

Address	Register Name	Reference
c001h	"PHY_XS XAUI PRBS Status Register (DID = 4h, Address = c001h)"	Table 51 on page 29
c002h	"PHY_XS Rate Adjust Register (DID = 4h, Address = c002h)"	Table 52 on page 29
c008h	"PHY_XS Receive Code Violation Counter Register (DID = 4h, Address = c008h)"	Table 53 on page 30

Table 14. XENPAK NVR Register Set and NVR EEPROM Description

Address	Register Name	Reference
8000h	"PMA/PMD EEPROM Control Register (DID = 1h, Address = 8000h)"	Table 54 on page 30
8106h	"EEPROM Registers (DID = 1h, from Address = 8007h to Address = 8106h)"	Table 55 on page 30
1h	"EEPROM Register Mapping Information (DID = 1h)"	Table 56 on page 31

Table 15. XENPAK DOM/LASI Control and Status Register Set

Address	Register Name	Reference
9000h	"RX_ALARM Enable Register (DID = 1h, Address = 9000h)"	Table 57 on page 31
9001h	"TXALARM Enable Register (DID = 1h, Address = 9001h)"	Table 58 on page 32
9002h	"LASI Control Register (DID = 1h, Address = 9002h)"	Table 59 on page 32
9003h	"RXALARM Status Register (DID = 1h, Address = 9003h)"	Table 60 on page 32
9004h	"TXALARM Status Register (DID = 1h, Address = 9004h)"	Table 61 on page 33
9005h	"LASI Status Register (DID = 1h, Address = 9005h)"	Table 62 on page 33
9006h	"DOM Tx_flag Control Register (DID = 1h, Address = 9006h)"	Table 63 on page 34
9007h	"DOM Rx_flag Control Register (DID = 1, Address = 9007h)"	Table 64 on page 34
A000h-A069h, A072h-A0FFh	"DOM Registers (DID = 1, Address = A000h to A069h, A072h to A0FFh)"	Table 65 on page 34
A070h	"DOM – Tx_flag Status Register (DID = 1, Address = A070h)"	Table 66 on page 34
A071h	"DOM – Rx_flag Status Register (DID = 1, Address = A071h)"	Table 67 on page 35
A100h	"DOM Command and Status Register (DID = 1, Address = A100h)"	Table 68 on page 35

6.3.2 PMA/PMD Control Registers (Device ID = 1h)

Using MDIO to access registers listed in Section 6.3.2 monitors and controls the PMA and PMD portion of the TXN17431 Optical Transceiver (see Table 16 through Table 28).

Table 16. PMA/PMD Control 1 Register (DID = 1h, Address = 0h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15	PMA/PMD reset	0 = Normal operation 1 = Reset	R/W, SC
14	Reserved	–	–
13	Speed selection	0 = Ignored 1 = Operation at 10 Gbps and above	R/W
12	Reserved	–	–

Table 16. PMA/PMD Control 1 Register (DID = 1h, Address = 0h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
11	Low power	0 = Normal operation (default) 1 = Low power mode	R/W
10:7	Reserved	–	–
6	Speed selection	1 = Operation at 10 Gbps and above (writes ignored)	R/W
5	Speed selection	1 = Ignored; 0 = operation at 10 Gbps and above (writes ignored)	R/W
4	Speed selection	0 = Operation at 10 Gbps and above (writes ignored) 1 = Ignored	R/W
3	Speed selection	1 = Ignored; 0 = operation at 10 Gbps and above (writes ignored)	R/W
2	Speed Selection	0 = Operation at 10 Gbps and above (writes ignored) 1 = Ignored	R/W
1	Reserved	–	R/W
0	PMA loopback	0 = Disable PMA loopback 1 = Enable PMA loopback	R/W

Table 17. PMA/PMD Status 1 Register (DID = 1h, Address = 1h)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Local PMA/PMD fault	0 = No PMA/PMD fault detected 1 = PMA/PMD fault detected	RO
6:3	Reserved	–	–
2	Receive link status	0 = PMA not locked to receive signal 1 = PMA locked to receive signal	RO,LL
1	Low power capability	0 = PMA/PMD does not support low power mode 1 = PMA/PMD supports low power mode	RO
0	Reserved	–	–

Table 18. PMA/PMD Speed Ability Register (DID = 1h, Address = 4h)

Bit	Functionality	Description	Access
15:1	Reserved	–	–
0	Speed ability	1 = PMA/PMD capable of operating at 10 Gbps (default)	RO

Table 19. PMA/PMD Devices in Package Register (DID = 1h, Address = 5h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15:6	Reserved	–	–
5	DTE_XS presence	0 = DTE_XS not present in package	RO
4	PHY_XS presence	1 = PHY_XS present in package	RO
3	PCS_presence	1 = PCS present in package	RO

Table 19. PMA/PMD Devices in Package Register (DID = 1h, Address = 5h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
2	WIS_presence	0 = WIS not present in package	RO
1	PMA/PMD presence	1 = PMA/PMD present in package	RO
0	Clause 22 registers presence	0 = IEEE clause 22 registers not present in package	RO

Table 20. PMA/PMD Control 2 Register (DID = 1h, Address = 7h)

Bit	Functionality	Description	Access
15:3	Reserved	–	–
2:0	PMA/PMD type	110 = indicates 10GBASE-LR PMA/PMD Type 101 = indicates 10GBASE-ER PMA/PMD Type 111 = indicates 10GBASE-SR PMA/PMD Type (default)	RO

Table 21. PMA/PMD Status 2 Register (DID = 1h, Address = 8h)

Bit	Functionality	Description	Access
15	Device present	1 = Default	RO
14	Device present	0 = Default	RO
13	Transmit fault detectability	1 = Default, indicate PMA/PMD has ability to detect transmit fault	RO
12	Receive fault detectability	1 = Default, indicate PMA/PMD has ability to detect receive fault	RO
11	Transmit fault	0 = No transmit local fault detected 1 = Transmit local fault detected	RO, LH
10	Receive fault	0 = No receive local fault detected 1 = Receiver local fault detected	RO,LH
9	Reserved	–	–
8	PMD transmit disable ability	1 = Default	RO
7	10GBASE-SR ability	1 = Default	RO
6	10GBASE-LR ability	0 = Default	RO
5	10GBASE-ER ability	0 = Default	RO
4	10GBASE-LX4 ability	0 = Default	RO
3	10GBASE-SW ability	0 = Default	RO
2	10GBASE-LW ability	0 = Default	RO
1	10GBASE-EW ability	0 = Default	RO
0	PMA loopback ability	1 = Default	RO

Table 22. PMD Transmit Disable Register (DID = 1h, Address = 9h)

Bit	Functionality	Description	Access
15:5	Reserved	–	–
4	PMD transmit disable lane 3	0 = Default (no PMD lane 3 support)	RO
3	PMD transmit disable lane 2	0 = Default (no PMD lane 2 support)	RO
2	PMD transmit disable lane 1	0 = Default (no PMD lane 1 support)	RO
1	PMD transmit disable lane 0	0 = Default (no PMD lane 0 support)	RO
0	Global PMD transmit disable	0 = Transmitter enable 1 = Transmitter disable	R/W

Table 23. PMD Receive Signal OK Register (DID = 1h, Address = ah)

Bit	Functionality	Description	Access
15:5	Reserved	–	–
4	PMD receive signal OK lane 3	0 = Default, no PMD lane 3 support	RO
3	PMD receive signal OK lane 2	0 = Default, no PMD lane 2 support	RO
2	PMD receive signal OK lane 1	0 = Default, no PMD lane 1 support	RO
1	PMD receive signal OK lane 0	0 = Default, no PMD lane 0 support	RO
0	Global PMD receive signal OK	0 = Signal not OK on receive 1 = Signal OK on receive	RO

Table 24. Package Identifier OUI Register (DID = 1h, Address = eh)

Bit	Functionality	Description	Access
15:8	EEPROM register 44	Package identifier OUI byte (pre-programmed), also mapped to 1.8033H.7:0	RO
7:0	EEPROM register 43	Package identifier OUI byte (pre-programmed), also mapped to 1.8032H7:0	RO

Table 25. Package Identifier OUI Register (DID = 1h, Address = fh)

Bit	Functionality	Description	Access
15:8	EEPROM register 46	Package identifier OUI byte (pre-programmed), also mapped to 1.8035H.7:0	RO
7:0	EEPROM register 45	Package identifier OUI byte (pre-programmed), also mapped to 1.8034H.7:0	RO

Table 26. PMA Network Loopback Register (DID = 1h, Address = c001h)

Bit	Functionality	Description	Access
15:11	Reserved	–	–
10	RxLOSB_I override	0 = No override (default) 1 = RXLOSB_I override	R/W
9	Network loopback data out enable	0 = Received data at RxXAUI when in network loopback mode (default) 1 = Transmit all idles at RxXAUI when in network loopback mode	R/W
8:5	Reserved	–	–
4	Network loopback enable	0 = Disable network loopback 1 = Enable network loopback	R/W
3	Reserved	–	RO
2	erefmon	1 = EREFCLK present	RO
1	sync_err	1 = Recovered clock rate error	RO,LH
0	txlock	1 = Fiber transmit PLL in lock	RO

Table 27. EEPROM Control Register (DID = 1h, Address = c003h)

Bit	Functionality	Description	Access
15	Reserved	–	–
14	EEPROM test mode frequency	0 = 37 kHz (default) 1 = High frequency test mode	R/W
13	EEPROM detected	1 = EEPROM detected	RO
12	EEPROM error	1 = EEPROM error (clear on read)	RO, LH
11	EEPROM active	1 = EEPROM access in progress	RO
10:8	Reserved	–	–
7	EEPROM checksum OK	1 = OK (clear on read)	RO, LH
6	Reserved	–	–
5:4	EEPROM burst read size	00 = 1 byte 01 = 8 bytes 10 = 16 bytes 11 = 256 bytes (default)	R/W
3:2	Reserved	–	–
1:0	EEPROM burst write size	00 = 1 byte 01 = 8 bytes (default) 10 = 16 bytes 11 = 1 byte	R/W

Table 28. EEPROM Checksum Register (DID = 1h, Address = c004h)

Bit	Functionality	Description	Access
15:8	EEPROM calculated checksum	Checksum value calculated over EEPROM addresses 0-99	RO
7:4	Reserved	–	–
3:2	DOM 256 byte write burst size	00 = 1 byte 01 = 8 bytes (default) 10 = 16 byte 11 = 1 byte	R/W
1:0	DOM Write Command	00 = Reserved 01 = Reserved 10 = Reserved 11 = Write 256 bytes	R/W

6.3.3 PCS Control Registers (Device ID = 3h)

Using MDIO to access registers listed in Section 6.3.3 will monitor and control the TXN17431 Optical Transceiver Physical Coding Sublayer (PCS) portion (see Table 29 through Table 42).

Table 29. PCS Control 1 Register (DID = 3h, Address = 0h)

Bit	Functionality	Description	Access
15	PCS 64/66 reset	0 = Normal operation 1 = Reset	R/W, SC
14	PCS loopback	0 = Disable PCS loopback 1 = Enable PCS loopback mode	R/W
13	Speed selection	1 = Operation at 10 Gbps and above (default)	RO
12	Reserved	Value always 0, write ignored	R/W
11	Low power	0 = Normal operation 1 = Low power mode	R/W
10:7	Reserved	–	–
6	Speed selection	1 = Operation at 10 Gbps and above (default)	RO
5	Speed selection	0 = Operation at 10 Gbps and above (default)	RO
4	Speed selection	0 = Operation at 10 Gbps and above (default)	RO
3	Speed selection	0 = Operation at 10 Gbps and above (default)	RO
2	Speed selection	0 = Operation at 10 Gbps and above (default)	RO
1:0	Reserved	–	–

Table 30. PCS Status 1 Register (DID = 3h, Address = 1h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Local fault condition detected	0 = No fault detected 1 = Fault detected	RO
6:3	Reserved	–	–

Table 30. PCS Status 1 Register (DID = 3h, Address = 1h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
2	PCS receive link status	0 = PCS receive link status down 1 = PCS receive link status up	RO,LL
1	Low power ability	0 = PCS does not support low power mode 1 = PCS supports low power mode	RO
0	Reserved	–	–

Table 31. PCS Speed Ability Register (DID = 3h, Address = 4h)

Bit	Functionality	Description	Access
15:1	Reserved	–	–
0	10 G capable	1 = PCS capable of operating at 10 G (default)	RO

Table 32. PCS Devices in Package Register (DID = 3h, Address = 5h)

Bit	Functionality	Description	Access
15:6	Reserved	–	–
5	DTE_XS presence	0 = DTE_XS not present in package	RO
4	PHY_XS presence	1 = PHY_XS present in package	RO
3	PCS_presence	1 = PCS present in package	RO
2	WIS_presence	0 = WIS not present in package	RO
1	PMA/PMD presence	1 = PMA/PMD present in package	RO
0	Clause 22 registers presence	0 = IEEE clause 22 registers not present in package	RO

Table 33. PCS Control 2 Register (DID = 3h, Address = 7h)

Bit	Functionality	Description	Access
15:2	Reserved	–	–
1	PCS type selection	0 = Select 10GBASE-R PCS type	R/W
0	PCS type selection	0 = Select 10GBASE-R PCS type	R/W

Table 34. 10 G PCS Status 2 Register (DID = 3h, Address = 8h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15	Device present	1 = Default	RO
14	Device present	0 = Default	RO
13:12	Reserved	–	–
11	Transmit local fault detect	0 = No fault detected 1 = PCS transmit local fault detected	RO, LH
10	Receive local fault detect	0 = No fault detected 1 = PCS receive local fault detected	RO,LH
9:3	Reserved	–	–

Table 34. 10 G PCS Status 2 Register (DID = 3h, Address = 8h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
2	10GBASE-W PCS capable	0 = Default (10GBASE-W PCS not supported)	RO
1	10GBASE-X PCS capable	0 = Default (10GBASE-X PCS not supported)	RO
0	10GBASE-R PCS capable	1 = Default (10GBASE-R PCS supported)	RO

Table 35. 10GBASE-R PCS Status 1 Register (DID = 3h, Address = 20h)

Bit	Functionality	Description	Access
15:13	Reserved	–	–
12	Receive link status	0 = 10GBASE-R PCS Receive link down 1 = 10GBASE-R PCS Receive link up	RO
11:3	Reserved	–	–
2	PRBS31 test mode support	0 = PRBS mode not supported 1 = PRBS mode supported;	RO
1	10GBASE-R PCS high BER	0 = 10GBASE-R PCS not reporting high BER 1 = 10GBASE-R PCS reporting high BER	RO
0	10GBASE-R PCS block lock	0 = 10GBASE-R PCS not locked to received blocks 1 = 10GBASE-R PCS locked to received blocks	RO

Table 36. 10GBASE-R PCS Status Register 2 (DID = 3h, Address = 21h)

Bit	Functionality	Description	Access
15	Latched block lock	0 = 10GBASE-R PCS does not have block lock 1 = 10GBASE-R PCS has block lock	RO,LL
14	Latched high BER	0 = 10GBASE-R PCS has not reported high BER 1 = 10GBASE-R PCS has reported high BER	RO,LH
13:8	BER counter	BER Counter in binary (MSB at bit 13, LSB at bit 8)	RO,NR
7:0	Errored blocks counter (MSB)	Errored blocks counter in binary (MSB at bit 7, LSB at bit 0)	RO,NR

Table 37. 10GBASE-R PCS Jitter Test Pattern Seed A Registers (DID = 3h, Address = 22h to 25h)

Bit	Functionality	Description	Access
15:0 (22h)	Bit 15 to Bit 0	Jitter Test Pattern (bit 15 to Bit 0) Reg A0	R/W
15:0 (23h)	Bit 31 to Bit 16	Jitter Test Pattern (bit 31 to bit 16) Reg A1	R/W
15:0 (24h)	Bit 47 to Bit 32	Jitter Test Pattern (bit 47 to Bit 32) Reg A2	R/W
15:10 (24h)	Reserved	–	R/W
9:0 (24h)	Bit 57 to Bit 48	Jitter Test Pattern (bit 57 to bit 48) Reg A3	R/W

Table 38. 10GBASE-R PCS Jitter Test Pattern Seed B Registers (DID = 3h, Address = 26h to 29h)

Bit	Functionality	Description	Access
15:0 (26h)	Bit 15 to Bit 0	Jitter Test Pattern (bit 15 to Bit 0) Reg B0	R/W
15:0 (27h)	Bit 31 to Bit 16	Jitter Test Pattern (bit 31 to bit 16) Reg B1	R/W
15:0 (28h)	Bit 47 to Bit 32	Jitter Test Pattern (bit 47 to Bit 32) Reg B2	R/W
15:10 (29h)	Reserved	–	R/W
9:0 (29h)	Bit 57 to Bit 48	Jitter Test Pattern (bit 57 to bit 48) Reg B3	R/W

Table 39. 10GBASE-R PCS Test Control Register (DID = 3h, Address = 2ah)

Bit	Functionality	Description	Access
15:6	Reserved	–	–
5	Receive PRBS31 checker enable	0 = Not enabled (default) 1 = Enable Rx PRBS31 checker	R/W
4	Transmit PRBS31 generator enable	0 = Not enabled (default) 1 = Enable Tx PRBS31	R/W
3	Transmit jitter test pattern enable	0 = Disable transmit jitter test 1 = Enable transmit jitter test	R/W
2	Receive jitter test pattern enable	0 = Disable receive jitter test 1 = Enable receive jitter test	R/W
1	Jitter test pattern data select	0 = Pseudo random test pattern 1 = Square wave test pattern	R/W
0	Jitter test pattern select	0 = LF data pattern 1 = Zeros data pattern	R/W

Table 40. 10GBASE-R PCS Jitter Test Counter Register (DID = 3h, Address = 2bh)

Bit	Functionality	Description	Access
15:0	Jitter test error counter	Jitter test error count (MSB at bit 15, LSB at bit 0)	RO, NR

Table 41. 10GBASE-R PCS Test Register (DID = 3h, Address = c000h)

Bit	Functionality	Description	Access
15	BER Test Complete	1 = BER Test Completed	RO/LH
14	BER Test in Progress	1 = BER Test in Progress	RO
13	Reserved	–	RO
12	BER TEST Enable	0 = Disabled (default) 1 = Enabled	R/W
11:6	Reserved	–	RO
5	PCS loopback data out enable	0 = Transmit square wave (00ffh) when in PCS loopback mode 1 = Transmit data at output when in PCS loopback mode	R/W
4	Reset transmit PCS	0 = Reset 1 = Not reset (default) not self clearing	R/W
3	Reset receive PCS	0 = Reset 1 = Not reset (default) not self clearing	R/W
2	Transmit scrambler bypass	0 = No operation 1 = Bypass activated	R/W
1	Receive descrambler bypass	0 = No operation 1 = Bypass activated	R/W
0	64/66 encoder error	0 = No error detected 1 = Error detected	RO,LH

Table 42. Fiber PRBS Mode Register (DID = 3h, Address = c006h)

Bit	Functionality	Description	Access
15:8	Fiber PRBS error count	Bit 15 = MSB Bit 8 = LSB	RO
6:0	Receive frame offset	–	RO

6.3.4 PHY_XS Control Registers (Device ID = 4h)

Using MDIO to access registers listed in Section 6.3.4 will monitor and control the PHY XGMII Extender Sublayer portion of the TXN17431 Optical Transceiver (see Table 43 through Table 53).

Table 43. PHY_XS Control 1 Register (DID = 4h, Address = 0h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15	Reset	0 = Normal operation 1 = Reset	R/W, SC
14	PHY_XS loopback enable	0 = No loopback enable 1 = Enable PHY_XS loopback	R/W
13	Speed selection	1 = Operation at 10 Gbps and above	RO
12	Reserved	–	–
11	Power down	0 = Do not power down 1 = Power down	RW
10:7	Reserved	–	–
6	Speed selection	1 = Operation at 10 Gbps and above	RO

Table 43. PHY_XS Control 1 Register (DID = 4h, Address = 0h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
5	Speed selection	0 = Operation at 10 Gbps and above	RO
4	Speed selection	0 = Operation at 10 Gbps and above	RO
3	Speed selection	0 = Operation at 10 Gbps and above	RO
2	Speed selection	0 = Operation at 10 Gbps and above	RO
1:0	Reserved	–	–

Table 44. PHY_XS Status 1 Register (DID = 4h, Address = 1h)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Local fault	0 = No fault condition 1 = Fault condition detected	RO
6:3	Reserved	–	–
2	Transmit link status	0 = Transmit link down 1 = Transmit link up	RO, LL
1	Power down capability	0 = No capability to power down 1 = Ability to power down	RO
0	Reserved	–	–

Table 45. PHY_XS Speed Ability Register (DID = 4h, Address = 4h)

Bit	Functionality	Description	Access
15:1	Reserved	–	–
0	Speed ability	1 = PHY_XS capable of operating at 10 Gbps	RO

Table 46. PHY_XS Devices in Package Register (DID = 4h, Address = 5h)

Bit	Functionality	Description	Access
15:6	Reserved	–	–
5	DTE_XS presence	0 = DTE_XS not present in package	RO
4	PHY_XS presence	1 = PHY_XS present in package	RO
3	PCS_presence	1 = PCS present in package	RO
2	WIS_presence	0 = WIS not present in package	RO
1	PMA/PMD presence	1 = PMA/PMD present in package	RO
0	Clause 22 registers presence	0 = IEEE clause 22 registers not present in package	RO

Table 47. PHY_XS Status 2 Register (DID = 4h, Address = 8h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15	Device present	1 = Device responding at this address (default)	RO
14	Device present	0 = Device responding at this address (default)	RO
13:12	Reserved	–	–

Table 47. PHY_XS Status 2 Register (DID = 4h, Address = 8h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
11	Transmit local fault detect	0 = No fault detected 1 = Transmit local fault detected	RO, LH
10	Receive local fault detect	0 = No fault detected 1 = Receive local fault detected	RO, LH
9:0	Reserved	–	–

Table 48. PHY_XS Lane Status Register (DID = 4h, Address = 18h)

Bit	Functionality	Description	Access
15:13	Reserved	–	–
12	XGXS transmit lane alignment	0 = Lanes no aligned 1 = Lanes aligned	RO
11	PHY_XS pattern testing ability	0 = Capable of PHY_XS pattern testing	RO
10	PHY_XS loopback ability	1 = Capable of PHY_XS loopback ability	RO
9:4	Reserved	–	–
3	Lane 3 synchronization	0 = Lane not in synch 1 = Lane in synch	RO
2	Lane 2 synchronization	0 = Lane not in synch 1 = Lane in synch	RO
1	Lane 1 synchronization	0 = Lane not in synch 1 = Lane in synch	RO
0	Lane 0 synchronization	0 = Lane not in synch 1 = Lane in synch	RO

Table 49. PHY_XS Test Control Register (DID = 4h, Address = 19h)

Bit	Functionality	Description	Access
15:3	Reserved	–	–
2	XGXS test pattern enable	0 = Disable 1 = Enable	R/W
1:0	Test pattern select	00 = High speed 01 = Low speed 10 = Mixed speed 11 = Reserved	R/W

Table 50. PHY_XS Control 2 Register (DID = 4h, Address = c000h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15	XAUI system loopback data out enable	0 = Transmit all ones when in PHY_XS loopback mode 1 = Transmit data at TXOUT when in PHY_XS loopback mode	R/W
14	XAUI system loopback	1 = Enable loopback (transmit -> receive path)	R/W
13	XAUI PRBS enable	0 = Not enabled 1 = Enable PRBS	R/W
12	XAUI Analog Monitor Point Control	0 = XAUI lane 3 recovered clock 1 = XAUI lane 3 recovered data	R/W
11:8	Reserved	–	–

Table 50. PHY_XS Control 2 Register (DID = 4h, Address = c000h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
7	Lane 3 lock	0 = Lane 3 not in lock 1 = Lane 3 in lock	RO
6	Lane 2 lock	0 = Lane 2 not in lock 1 = Lane 2 in lock	RO
5	Lane 1 lock	0 = Lane 1 not in lock 1 = Lane 1 in lock	RO
4	Lane 0 lock	0 = Lane 0 not in lock 1 = Lane 0 in lock	RO
3	Receive path XAUI PLL lock	0 = PLL not locked 1 = PLL locked	RO
2	Reserved	–	–
1	Receive XGXS reset	0 = Reset 1 = Not reset (default) not self clearing	R/W
0	Transmit XGXS reset	0 = Reset 1 = Not reset (default) not self clearing	R/W

Table 51. PHY_XS XAUI PRBS Status Register (DID = 4h, Address = c001h)

Bit	Functionality	Description	Access
15:4	Reserved	–	–
3	XAUI lane 3 PRBS error	0 = No error detected 1 = Error detected (cleared on read)	RO, LH
2	XAUI lane 2 PRBS error	0 = No error detected 1 = Error detected (cleared on read)	RO, LH
1	XAUI lane 1 PRBS error	0 = No error detected 1 = Error detected (cleared on read)	RO, LH
0	XAUI lane 0 PRBS error	0 = No error detected 1 = Error detected (cleared on read)	RO, LH

Table 52. PHY_XS Rate Adjust Register (DID = 4h, Address = c002h)

Bit	Functionality	Description	Access
15:10	Reserved	–	–
9	XGXS transmit rate adjust overflow	1 = Overflow	RO, LH
8	XGXS transmit rate adjust underflow	1 = Underflow	RO, LH
7	XGXS receive rate adjust overflow	1 = Overflow	RO, LH
6	XGXS receive rate adjust underflow	1 = Underflow	RO,LH
5:0	Reserved	–	–

Table 53. PHY_XS Receive Code Violation Counter Register (DID = 4h, Address = c008h)

Bit	Functionality	Description	Access
15:0	PHY_XS receive code violation counter	Bit 15 = MSB Bit 0 = LSB; clear on read	RO, NR

6.3.5 XENPAK NVR Registers and NVR EEPROM Description

Table 54 through Table 56 provide the XENPAK NVR Registers and NVR EEPROM Register description.

Table 54. PMA/PMD EEPROM Control Register (DID = 1h, Address = 8000h)

Bit	Functionality	Description	Access
15:8	EEPROM address for single byte write/read	EEPROM register number	RW
7:6	Reserved	–	–
5	R/W command	0 = Read mode 1 = Write mode	R/W
4	Reserved	–	–
3:2	Command status	00 = No command 01 = Previous command 10 = Reserved 11 = Previous command failed	RO, LH
1:0	EEPROM command	00 = Reserved 01 = Reserved 10 = Read or write one byte 11 = Read or write 256 bytes	R/W

A total of 256 registers are mapped into this address range. Table 55 lists an example of how each 16 bits are arranged.

Table 55. EEPROM Registers (DID = 1h, from Address = 8007h to Address = 8106h)

Bit	Functionality	Description	Access
Address = 8007h			
15:8	Reserved	–	RO
7:0	EEPROM register 0	Bit 7 is MSB, Bit 0 is LSB	RO
Address = 8106h			
15:8	Reserved	–	RO
7:0	EEPROM register 255	Bit 7 is MSB, Bit 0 is LSB	RO

The TXN17431 Optical Transceiver has an EEPROM with 256 register locations. Out of the 256 register locations, 48 registers are designated as customer writable areas and four registers are for package identifier OUI. The remaining registers are for internal operation.

The customer writable EEPROM area is accessed through the standard MDIO read/write interface per IEEE 802.3ae clause 45. Data must first be written into the corresponding MDIO registers designated as a customer writable area. The MDIO data is then transferred to the EEPROM through transactions in 1.C003 and 1.8000 (EEPROM control registers).

Table 56. EEPROM Register Mapping Information (DID = 1h)

EEPROM Register # (dec.)	MDIO Address (hex.)	Description	Access
0	8007	First register used for checksum calculation	RO
6	800d	Customer field address	RO
7	800e	Vendor field address	RO
17	8018	10GBASE type	RO
43	8032	Package identifier OUI (mapped to MDIO 1.14 lower byte)	RO
44	8033	Package identifier OUI (mapped to MDIO 1.14 upper byte)	RO
45	8034	Package identifier OUI (mapped to MDIO 1.15 lower byte)	RO
46	8035	Package identifier OUI (mapped to MDIO 1.15 upper byte)	RO
82	8059	Default last lower protected EEPROM register	RO
115	807A	DOM capability bits 2:0 are DOM device address LSB, bit 6 indicate if DOM is implemented	RO
116	807B	DOM control/status	RO
117	807C	Last register used for checksum calculation	RO
118	807D	Basic field checksum value	RO
119	807e	Start of customer writable area	R/W
166	80ad	End of customer writable area	R/W
167 to 255	80ae to 8106	Reserved	–

6.3.6 XENPAK DOM/LASI Control and Status Registers

Table 57 through Table 68 cover the XENPAK DOM/LASI Control and Status Registers.

Table 57. RX_ALARM Enable Register (DID = 1h, Address = 9000h)

Bit	Functionality	Description	Access
15:7	Reserved	–	R/W
6	PHY_XS receive buffer over/underflow error enable	0 = Disable (default) 1 = Enable	R/W
5	Reserved	–	–
4	PMA/PMD receive local fault enable	0 = Disable 1 = Enable (default)	R/W
3	PCS receive local fault enable	0 = Disable 1 = Enable (default)	R/W
2	PCS receive code violation enable	0 = Disable (default) 1 = Enable	R/W
1	Rx_flag enable	0 = Disable (default) 1 = Enable	R/W
0	PHY_XS receive local fault enable	0 = Disable 1 = Enable (default)	R/W

Table 58. TXALARM Enable Register (DID = 1h, Address = 9001h)

Bit	Functionality	Description	Access
15:11	Reserved	–	–
10	PHY XS Code Violation Error Enable	0 = Disable (default) 1 = Enable	R/W
9:7	Reserved	–	–
6	Transmitter fault enable	0 = Disable 1 = Enable (default)	R/W
5	Transmitter loss of lock enable	0 = Disable (default) 1 = Enable	R/W
4	PMA/PMD transmit local fault enable	0 = Disable 1 = Enable (default)	R/W
3	PCS transmit local fault enable	0 = Disable 1 = Enable (default)	R/W
2	PCS buffer over/ underflow error enable	0 = Disable (default) 1 = Enable	R/W
1	tx_flag enable	0 = Disable (default) 1 = Enable	R/W
0	PHY_XS transmit local fault enable	0 = Disable 1 = Enable (default)	R/W

Table 59. LASI Control Register (DID = 1h, Address = 9002h)

Bit	Functionality	Description	Access
15:7	Reserved	–	R/W
6	Monitor 3.3 V_IN supply too low enable	0 = Disable (default) 1 = Enable	R/W
5	3.3 V	0 = Disable (default) 1 = Enable	R/W
4	1.8 V low detect enable	0 = Disable (default) 1 = Enable	R/W
3	LASI test data enable	0 = Disable (default) 1 = Enable	R/W
2	RX_ALARM enable	0 = Disable (default) 1 = Enable	R/W
1	TX_ALARM enable	0 = Disable (default) 1 = Enable	R/W
0	Link status alarm enable	0 = Disable (default) 1 = Enable	R/W

Table 60. RXALARM Status Register (DID = 1h, Address = 9003h) (Sheet 1 of 2)

Bit	Functionality	Description	Access
15:7	Reserved	–	R/W
6	PHY_XS receive buffer over/underflow value error	0 = No error detected 1 = Error detected	RO, LH
5	Reserved	–	R/W
4	PMA/PMD receive local fault	0 = No fault detected 1 = Fault detected	RO, LH

Table 60. RXALARM Status Register (DID = 1h, Address = 9003h) (Sheet 2 of 2)

Bit	Functionality	Description	Access
3	PCS receive local fault	0 = No fault detected 1 = Fault detected	RO, LH
2	PCS receive code violation	0 = No violation 1 = Violation detected	RO, LH
1	Rx_flag	0 = No error detected 1 = Error detected	RO, LH
0	PHY_XS receive local fault	0 = No error detected 1 = Error detected	RO, LH

Table 61. TXALARM Status Register (DID = 1h, Address = 9004h)

Bit	Functionality	Description	Access
15:11	Reserved	–	–
10	PHY XS Code Violation Error Enable	0 = Disable (default) 1 = Enable	RO, LH
9:7	Reserved	–	–
6	Transmit fault	0 = No fault detected 1 = Fault detected	RO, LH
5	Transmitter loss of lock	0 = No loss of lock 1 = Loss of lock	RO, LH
4	PMA/PMD transmit local fault	0 = No fault detected 1 = Fault detected	RO, LH
3	PCS transmit local fault	0 = No fault detected 1 = Fault detected	RO, LH
2	PCS buffer over/ underflow error	0 = No flow error detected 1 = Flow error detected	RO, LH
1	tx_flag	0 = No error detected 1 = Error detected	RO,LH
0	PHY_XS transmit local fault	0 = No fault detected 1 = Fault detected	RO

Table 62. LASI Status Register (DID = 1h, Address = 9005h)

Bit	Functionality	Description	Access
15:7	Reserved	–	RO
6	Monitor 3.3 V_IN supply too low	0 = No alarm 1 = 3.3 V supply too low	RO, LH
5	3.3 V supply too low	0 = No alarm 1 = 3.3 V supply too low	RO, LH
4	1.8 V supply too low	0 = No alarm 1 = 1.8 V supply too low	RO, LH
3	LASI test data	–	R/W
2	RXALARM status	0 = No alarm 1 = RX_ALARM condition	RO
1	TXALARM status	0 = No alarm 1 = TX_ALARM condition	RO
0	Link status change	0 = No status change 1 = Status change	RO,LH

Table 63. DOM Tx_flag Control Register (DID = 1h, Address = 9006h)

Bit	Functionality	Description	Access
15:8	Reserved	–	R/W
7	Temp High Alarm Enable	0 = Disabled (default) 1 = Enabled	R/W
6	Temp Low Alarm Enable	0 = Disabled (default) 1 = Enabled	R/W
5:4	Reserved	–	R/W
3	Laser Bias current high alarm enable	0 = Disabled (default) 1 = Enabled	R/W
2	Laser Bias current low alarm enable	0 = Disabled (default) 1 = Enabled	R/W
1	Laser Output power high alarm enable	0 = Disabled (default) 1 = Enabled	R/W
0	Laser output power low alarm enable	0 = Disabled (default) 1 = Enabled	R/W

Table 64. DOM Rx_flag Control Register (DID = 1, Address = 9007h)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Rx Optical Power High Alarm Enable	0 = Disable (default) 1 = Enable	R/W
6	Rx Optical Power Low Alarm Enable	0 = Disable (default) 1 = Enable	R/W
5:0	Reserved	–	R/W

Table 65. DOM Registers (DID = 1, Address = A000h to A069h, A072h to A0FFh)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7:0	MSB bit 7 to LSB bit 0	–	–

Table 66. DOM – Tx_flag Status Register (DID = 1, Address = A070h)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Temp High Alarm	–	RO
6	Temp Low Alarm	–	RO
5:4	Reserved	–	RO
3	Laser Bias Current High Alarm	–	RO
2	Laser Bias Current Low Alarm	–	RO
1	Laser Output Power High Alarm	–	RO
0	Laser Output Power Low Alarm	–	RO

Table 67. DOM – Rx_flag Status Register (DID = 1, Address = A071h)

Bit	Functionality	Description	Access
15:8	Reserved	–	–
7	Rx Optical Power High Alarm	–	RO
6	Rx Optical Power Low Alarm	–	RO
5:0	Reserved	–	RO

Table 68. DOM Command and Status Register (DID = 1, Address = A100h)

Bit	Functionality	Description	Access
15:14	Reserved	–	RO
13:12	DOM Write Command Status	00 = Idle, no command 01 = Command completed 10 = Command in progress 11 = Previous command failed	RO, LH
11:4	Reserved	–	RO
3:2	DOM Command Status	00 = Idle, no command 01 = Command completed 10 = Command in progress 11 = Previous command failed	RO, LH
1:0	DOM Update commands	00 = Write, single DOM update (default) 01 = Write, slow periodic update 10 = Write, inter periodic update 11 = Write, fast periodic update	R/W

7.0 Digital Optical Monitoring

The TXN17431 Optical Transceiver supports Digital Optical Monitoring (DOM) according to the XENPAK MSA 1.0b specification. This feature allows diagnostic monitoring of the transmitter and receiver optical power, bias current, transceiver operating temperature and state. The threshold alarm can be set appropriately to trigger LASI.

There are 256 8-bit registers resident in MDIO register space 1.A000h to 1.A0FFh that support DOM. These registers store the digitized value of analog temperature/bias current measurements, warning and threshold values, and control/status settings. A DOM agent (microcontroller on board) loads these registers upon reset and polls these registers periodically for status checks. Layout of DOM registers can be found in Table 55 “EEPROM Registers (DID = 1h, from Address = 8007h to Address = 8106h)” on page 30 through Table 59 “LASI Control Register (DID = 1h, Address = 9002h)” on page 32, and also in XENPAK MSA 1.0b, Tables 27-28.

The following two flag values (ref 1.9006h and 1.9007h) trigger LASI alarms when DOM fault conditions occur:

- **Rx_flag:** Register 1.A071h contains bits to indicate the receiver Fault Status. Register 1.9007h selects the fault conditions in register 1.A071 to be reported via the Rx Flag bit (1.A071 AND 1.9007). The logic OR of any of the selected fault conditions is then reflected by Rx Flag.
- **Tx_flag.** Register 1.A070h contains bits to indicate the transmitter Fault Status. Register 1.9006h selects the fault conditions in register 1.A071 to be reported via

the Rx Flag bit (1.A070 AND 1.9006). The logic OR of any of the selected fault conditions is then reflected by Tx flag.

These two flag values are fed directly to RX_ALARM and TX_ALARM, respectively. LASI is asserted when either RX_ALARM or TX_ALARM is set and enabled.

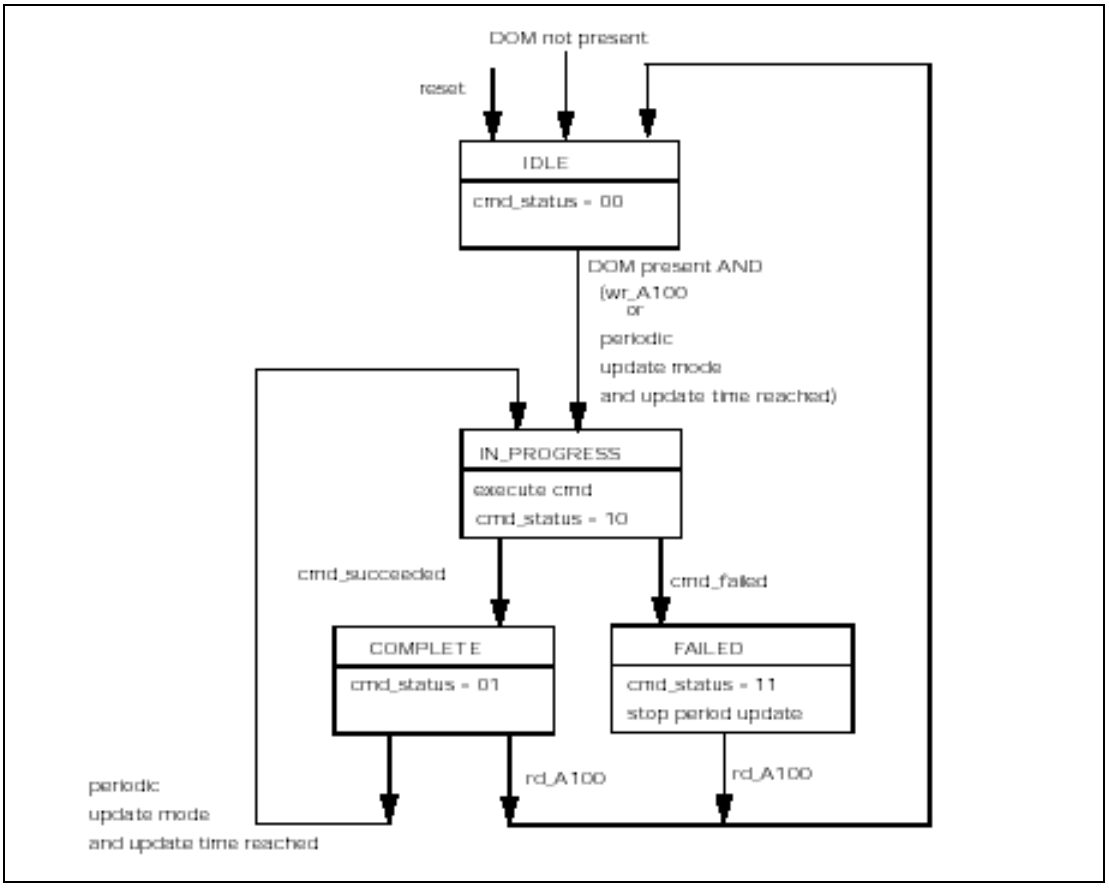
The DOM register update rate can be set by register 1.A100.1:0 contents. Writing a "00" to these bits initiates a single upload of DOM registers. The DOM registers periodically update if these bits are set to any other state (see Table 69).

Table 69. DOM Update Rates (DID = 1, Address = A100h)

Bits (1:0)	Description
00	Initiate a single update of MDIO DOM registers; default update interval value
01	Periodic update of MDIO DOM registers every 60 seconds
10	Periodic update of MDIO DOM registers every 10 seconds
11	Periodic update of MDIO DOM registers every 1 second

If a DOM update is requested while a Non Volatile Register (NVR) read or write is in progress, the NVR transaction is allowed to complete and the DOM update begins. While the DOM update is pending, the DOM command register (1.A100h) indicates a transaction in progress. The same applies if an NVR transaction is requested while a DOM update is in progress. While an NVR or DOM update is queued, the associated command register is put in the command-in-progress state. Figure 2 shows a state diagram.

Figure 2. DOM Access State Diagram



8.0 Loopback Capability

The TXN17431 Optical Transceiver features five loopback modes for diagnostic and test purposes. This feature is enabled and configured by writing appropriate values to the MDIO registers (see Table 70).

Table 70. Loopback Capability (Sheet 1 of 2)

Loopback Type	Loopback Control Register	Data Output Enable Register	Data Path Output (Data Output Enable Register = 0 and Loopback Control Register Enabled)	Data Path Output (Data Output Enable Register = 1 and Loopback Control Register Enabled)
PMA loopback (transmit -> receive)	DID = 1h, Address = 0h, Bit 0	None	Loopback transmit data	NA
PCS loopback (transmit -> receive)	DID = 3, Address = 0h, Bit 14	DID = 3h, Address = c000h, Bit 5	0F0F	Loopback transmit data

Table 70. Loopback Capability (Sheet 2 of 2)

Loopback Type	Loopback Control Register	Data Output Enable Register	Data Path Output (Data Output Enable Register = 0 and Loopback Control Register Enabled)	Data Path Output (Data Output Enable Register = 1 and Loopback Control Register Enabled)
PHY_XS loopback (receive -> transmit)	DID = 4h, Address = 0h, Bit 14	None	Receive data at RxXAUI	None
PHY_XS system loopback (transmit -> receive)	DID = 4h, Address = c000h, Bit 14	DID = 4h, Address = c000h, Bit 15	ffffh at TXOUT	Transmit data
PMA network loopback (receive -> transmit)	DID = 1h, Address = c001h, Bit 4	DID = 1h, Address = c001h, Bit 9	Received data at RxXAUI	Transmit all idles at RxXAUI

Typically, data from the transmit path is rerouted to the receive path when the loopback mode is enabled. However, for PCS loopback and PHY_XS loopback, you can observe a fixed data pattern (listed in Table 70 as bypassed path output) instead of the looped back data by setting the Data Output Enable Register to logic 0.

In PMA network loopback mode, the recovered and re-timed 10 G signal, (that is, the receiving signal) is looped back to the transmitter output. The receive path XAUI output data is XAUI idle codes. If the Data Output Enable Register is asserted, the output is received data instead of idle codes.

Note: Enabling more than one loopback path is invalid and should not be part of normal operation.

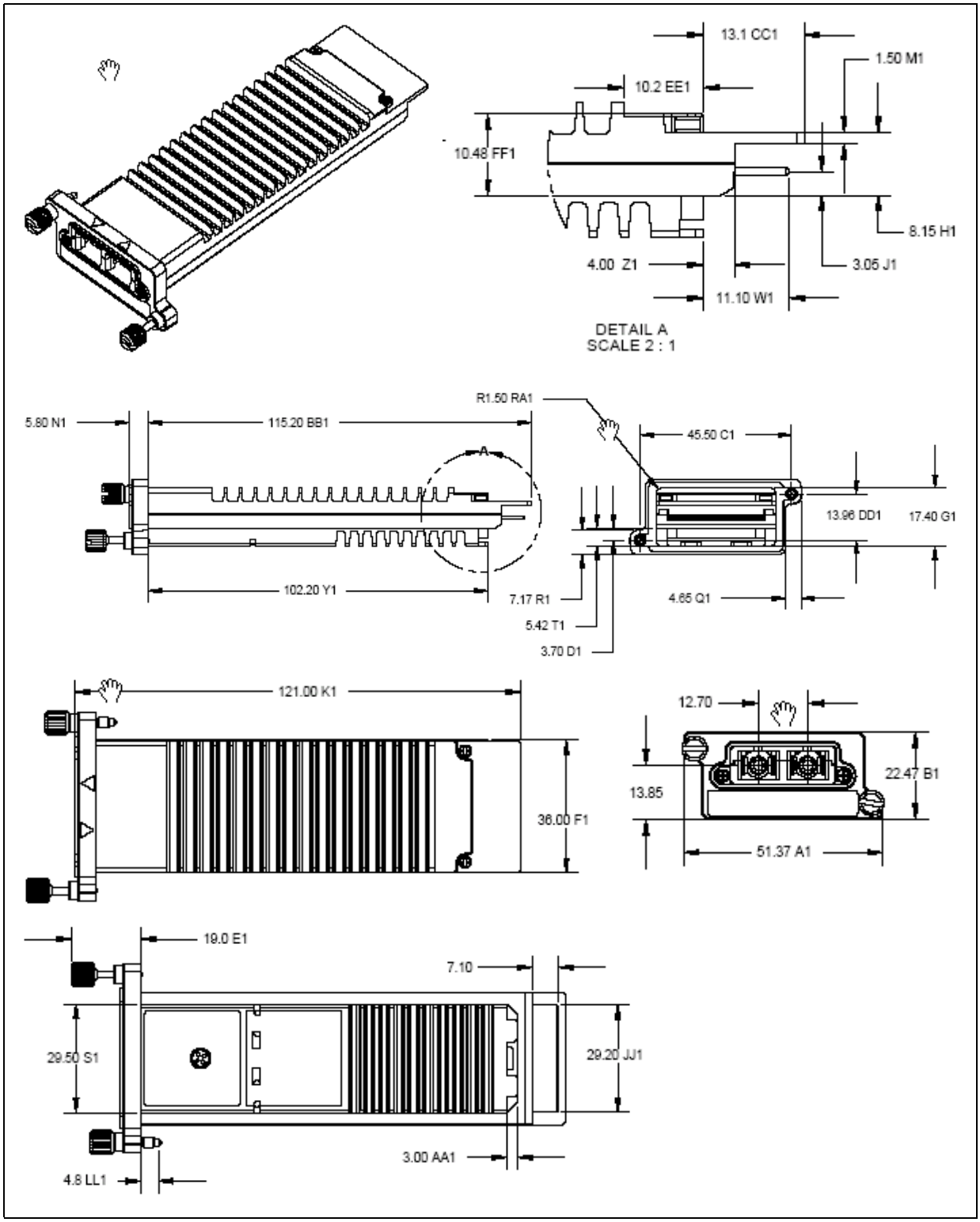
9.0 Mechanical Layout and Configuration

The TXN17431 Optical Transceiver comes standard with an integrated heat sink designed for nominal operation of the module at 200 linear feet per minute (lfm) of 50 °C ambient temperature airflow. These conditions produce a worst-case 70 °C case temperature, which keeps the optical and electrical components within their specified operating temperature requirements.

Warning: Do not use an “Aqueous Wash” with the TXN17431 Optical Transceiver.

Figure 3 shows the form factor and dimensions of the TXN17431 Optical Transceiver.

Figure 3. Mechanical Outline for a Heat Sink



10.0 Regulatory Compliance

This section discusses the following topics:

10.1 Electromagnetic Compatibility Compliance

Table 71 lists emissions and immunity regulations with which the Intel® TXN17431 (0850) Optical Transceiver complies when tested in a representative chassis.

Table 71. Electromagnetic Compatibility Compliance

Requirement	Regulation	Performance Level
Electromagnetic interference (EMI)	• FCC rules, Part 15, subpart B • EN 55022	Meets Class B limits with a minimum 6 dB margin
Electrostatic discharge (ESD)	JEDEC JESD22-A114-B Human Body Model	± 400 V contact discharge to connector electrical pins
	EN 61000-4-2	• ±15 kV air discharge • ± 8 kV contact discharge to face plate
Radio frequency electromagnetic field (Radiated immunity)	EN 61000-4-3	10 V/m from 80 MHz to 1G Hz with no degradation of performance or loss of function

10.2 Safety Compliance

Table 72 lists and describes the relevant safety regulations with which the Intel® TXN17431 (0850) Optical Transceiver complies.

Table 72. Safety Compliance (Sheet 1 of 2)

Requirement	Regulation	Title
Product Safety	UL 60950-1CSA C22.2 No. 60950-1-03	Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada)
	EN 60950-1 +A11	Information Technology Equipment – Safety - Part 1: General Requirements (European Union)
	IEC 60950-1	Information Technology Equipment – Safety - Part 1: General Requirements (International)
	GR-63-CORE Section 4.2, Clause 4.2.3.1	Compliant with the fire resistance requirements of Telcordia Technologies Generic Requirements GR-63-CORE document for discrete electronic components.

Table 72. Safety Compliance (Sheet 2 of 2)

Requirement	Regulation	Title
Laser Safety	21CFR1040.10	Code of Federal Regulations Title 21 Chapter I Subchapter J – Radiological Health Part 1040: Performance Standards for Light-Emitting Products
	EN 60825-1 +A1 +A2	Safety of Laser Products - Part 1: Equipment Classification, Requirements and User's Guide
	IEC 60825-1 +A1 +A2	Safety of Laser Products - Part 1: Equipment Classification, Requirements and User's Guide
	EN 60825-2	Safety of Laser Products - Part 2: Safety of Optical Fiber Communication Systems
	IEC 60825-2	Safety of Laser Products - Part 2: Safety of Optical Fiber Communication Systems

10.3 Compliance with Restriction of Hazardous Substances

This product complies with the European Union directive for Restriction of Hazardous Substances (RoHS) – *Restriction on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment*, Directive 2002/95/EC plus amendments.

However, certain discrete components do contain lead (a RoHS-restricted substance) in amounts that exceed threshold concentration levels. This product uses the following applicable RoHS technology exemptions:

- Lead in optical and filter glass
- Lead in glass of electronic components
- Lead in electronic ceramic parts
- Lead in solders for servers, storage and storage array systems, network infrastructure equipment for switching, signaling, transmission, as well as network management for telecommunications

Note: RoHS implementation details are subject to change.

10.4 Product Certification Markings and Compliance Statements

Table 73 lists the Intel® TXN17431 (0850) Optical Transceiver product certification markings and compliance statements.

Table 73. Product Certification Markings and Compliance Statements

Origin and Description	Markings and Compliance Statements
Markings	
CE mark. The CE (Conformité Européene*) mark indicates compliance to the European Union Low Voltage directive (73/23/EEC).	
TÜV Rheinland type approval mark for components and subassemblies for the European Union. The Technischer Überwachungsverein* (TÜV – German for "Technical Inspection Association") Rheinland type approval mark is for components and subassemblies for the European Union. Where space does not permit, the smaller alternate TÜV mark (see the next row in this table) may be used.	
TÜV Rheinland type approval mark for components and subassemblies for the European Union – *Alternate*. This alternate mark may be used where space constraints exist that do not permit use of the TUV Rheinland mark in the previous row of this table.	Alternate TÜV mark: 
UL Recognized Component mark for the USA and Canada.	
China Environmental Friendly Use Period (EFUP) mark, where 30 in the marking denotes 30 years. The number provided as the EFUP is provided solely to comply with applicable laws of the People's Republic of China. It does not create any warranties or liabilities on behalf of Intel Corporation to customers.	
Compliance Statements	
USA Food and Drug Administration (FDA), Center for Devices and Radiological Health compliance statement.	Complies with 21CFR 1040.10 except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001.
USA FDA, Center for Devices and Radiological Health compliance statement – *Alternate*. Use the alternate statement listed, as needed.	Alternate FDA compliance statement: Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated July 26, 2001.

10.5 Management Methods on Control of Pollution from Electronic Information Products (a.k.a. China RoHS)

关于符合中国《电子信息产品污染控制管理办法》的声明

Table 74. Hazardous Substances Table

产品中有毒有害物质的名称及含量

部件名称 (Parts)	有毒有害物质或元素 (Hazardous Substance)					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
集成光电器件 Integrated optical circuit board assembly	×	○	○	○	○	○
金属盒件 Metal enclosure	○	○	○	○	○	○

○：表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T 11363-2006标准规定的限量要求以下。

○： Indicates that this hazardous substance contained in all homogeneous materials of this part is below the limit requirement in SJ/T 11363-2006.

×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T 11363-2006标准规定的限量要求。

×： Indicates that this hazardous substance contained in at least one of the homogeneous materials of this part is above the limit requirement in SJ/T 11363-2006.

对销售之日的所售产品，本表显示我公司供应链的电子信息产品可能包含这些物质。注意：在所售产品中可能会也可能不会含有所有所列的部件。

This table shows where these substances may be found in the supply chain of our electronic information products, as of the date of sale of the enclosed product. Note that some of the component types listed above may or may not be a part of the enclosed product.

除非另外特别的标注，此标志为针对所涉及产品的环保使用期限标志. 此环保使用期限只适用于产品在产品手册中所规定的条件下工作.

The Environment-Friendly Use Period (EFUP) for all enclosed products and their parts are per the symbol shown here, unless otherwise marked. The Environment-Friendly Use Period is valid only when the product is operated under the conditions defined in the product manual.

11.0 Ordering Information

Specify the complete TXN17431 Optical Transceiver part number defined in Table 75 when ordering.

Table 75. Ordering Information

Part Number	MM Number	Description
TXN174310850F16 (obsolete, replaced by TXN174310850F36)	872628	300 m, 850 nm Serial, 10.3 Gbps Ethernet Optical Transceiver Compliant with XENPAK MSA, manufactured in Malaysia.
TXN174310850F36	891472	300 m, 850 nm Serial, 10.3 Gbps Ethernet Optical Transceiver Compliant with XENPAK MSA, manufactured in Thailand.

12.0 Acronyms

Table 76. Acronyms

Acronym	Meaning
CDR	Clock and Data Recovery
DFB	Distributed Feedback
DOM	Digital Optical Monitoring
EEPROM	Electrically Erasable Programmable Read Only Memory
IEEE	Institute of Electrical and Electronics Engineers
LASI	Link Alarm Status Interrupt
MDIO	Management Data Input/Output
PCS	Physical Coding Sublayer (PCS)
MSA	Multisouorce Agreement
NVR	Non Volatile Register
PMA	Physical Medium Attachment (PMA)
PMD	Physical Medium Dependent (PMD)
SC-UPC	Snap-on Connector with Ultra-Physical Contact
SerDes	Serializer-Deserializer
TO	Transmitter Optical
XAUI	10 Gigabit Attachment Unit Interface

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