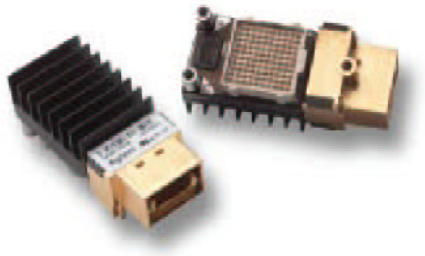
AFBR-732BWZ/BEWZ/BEHWZ and AFBR-742BZ/BEZ/BEHZ

Ultra Short Link Pluggable Parallel Fiber Optic Modules, Transmitter and Receiver

Data Sheet



Description

The AFBR-732BWZ transmitter and AFBR-742BZ receiver are high performance fiber optic modules for parallel optical data communication applications. These 12-channel devices, operating up to 2.5Gbd per channel, provide a cost effective solution for short-reach applications requiring up to 30 Gb/s aggregate bandwidth. These modules are designed to operate on multimode fiber systems at a nominal wavelength of 850 nm. They incorporate high performance, highly reliable, short wavelength optical devices coupled with proven circuit technology to provide long life and consistent service.

The AFBR-732BWZ transmitter module incorporates a 12- channel VCSEL (Vertical Cavity Surface Emitting Laser) array together with a custom 12-channel laser driver integrated circuit providing IEC-60825 and CDRH Class 1M laser eye safety.

The AFBR-742BZ receiver module contains a 12-channel PIN photodiode array coupled with a custom preamplifier / post amplifier integrated circuit.

Operating from a single +3.3 V power supply, both modules provide LVTTL or LVCMOS control interfaces and Current Mode Logic (CML) compatible data interfaces to simplify external circuitry.

The transmitter and receiver devices are housed in MTP®/ MPO receptacled packages. Electrical connections to the devices are achieved by means of a pluggable 10 x 10 connector array.

Features

- RoHS Compliant
- Low cost per Gb/s
- High package density per Gb/s
- 3.3 volt power supply for low power consumption
- 850 nm VCSEL array source
- 12 independent channels per module
- Separate transmitter and receiver modules
- 2.5 Gbd data rate per channel
- Standard MTP® (MPO) ribbon fiber connector interface
- Pluggable package
- 50/125 micron multimode fiber operation:
  Distance up to 50 m with 50um,
  500 MHz.km fiber at 2.5 Gbd
- Data I/O is CML compatible
- Control I/O is LVTTL compatible
- Manufactured in an ISO 9002 certified facility

Applications

- Proprietary Ultra short link interconnects

Ordering Information

The AFBR-732BWZ and AFBR-742BZ products are available for production orders through the Avago Component Field Sales office.

AFBR-732BWZ No EMI Nose Shield, with Heatsink

AFBR-742BZ No EMI Nose Shield, with Heatsink

AFBR-732BEWZ With EMI Nose Shield, with Heatsink

AFBR-742BEZ With EMI Nose Shield, with Heatsink

AFBR-732BEHWZ With EMI Nose Shield, No Heatsink

AFBR-742BEHZ With EMI Nose Shield, No Heatsink

Design Summary:

Design for low-cost, high-volume manufacturing

Avago's parallel optics solution combines twelve 2.5 Gb/s channels into discrete transmitter and receiver modules providing a maximum aggregate data rate of 30 Gb/s. Moreover, these modules employ a heat sink for thermal management when used on high-density cards, have excellent EMI performance, and interface with the industry standard MTP®/MPO connector systems. They provide the most cost-effective high- density (Gb/s per inch) solutions for high-data capacity applications. See Figure 1 for the transmitter and Figure 2 for the receiver block diagrams.

The AFBR-732BWZ transmitter and the AFBR-742BZ receiver modules provide very closely spaced, high-speed parallel data channels. Within these modules there will be some level of cross talk between channels. The cross talk within the modules will be exhibited as additional data jitter or sensitivity reduction compared to single-channel performance. Avago Technologies' jitter and sensitivity specifications include cross talk penalties and thus represent real, achievable module performance.

Functional Description, Transmitter Section

The transmitter section, Figure 1, uses a 12-channel 850 nm VCSEL array as the optical source and a diffractive optical lens array to launch the beam of light into the fiber. The package and connector system are designed to allow repeatable coupling into standard 12-fiber ribbon cable. In addition, this module has been designed to be compliant with IEC 60825 Class 1M eye safety requirements.

The optical output is controlled by a custom IC, which provides proper laser drive parameters and monitors drive current to ensure eye safety. An EEPROM and state machine are programmed to provide both ac and dc current drive to the laser to ensure correct modulation, eye diagram over variations of temperature and power supply voltages.

Functional Description, Receiver Section

The receiver section, Figure 2, contains a 12-channel AlGaAs/ GaAs photodetector array, transimpedance preamplifier, filter, gain stages to amplify and buffer the signal, and a quantizer to shape the signal.

The Signal Detect function is designed to sense the proper optical output signal on each of the 12 channels. If loss of signal is detected on an individual channel, that channel output is squelched.

Packaging

The flexible electronic subassembly was designed to allow high-volume assembly and test of the VCSEL, PIN photo diode and supporting electronics prior to final assembly.

Regulatory Compliance

The overall equipment design into which the parallel optics module is mounted will determine the certification level. The module performance is offered as a figure of merit to assist the designer in considering their use in the equipment design.

Organization Recognition

See the Regulatory Compliance Table for a listing of the standards, standards associations and testing laboratories applicable to this product.

Electrostatic Discharge (ESD)

There are two design cases in which immunity to ESD damage is important.

The first case is during handling of the module prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the module parts. To the extent that the MTP® (MPO) connector receptacle is exposed to the outside of the equipment chassis it may be subject to system level ESD test criteria that the equipment is intended to meet.

See the Regulatory Compliance Table for further details.

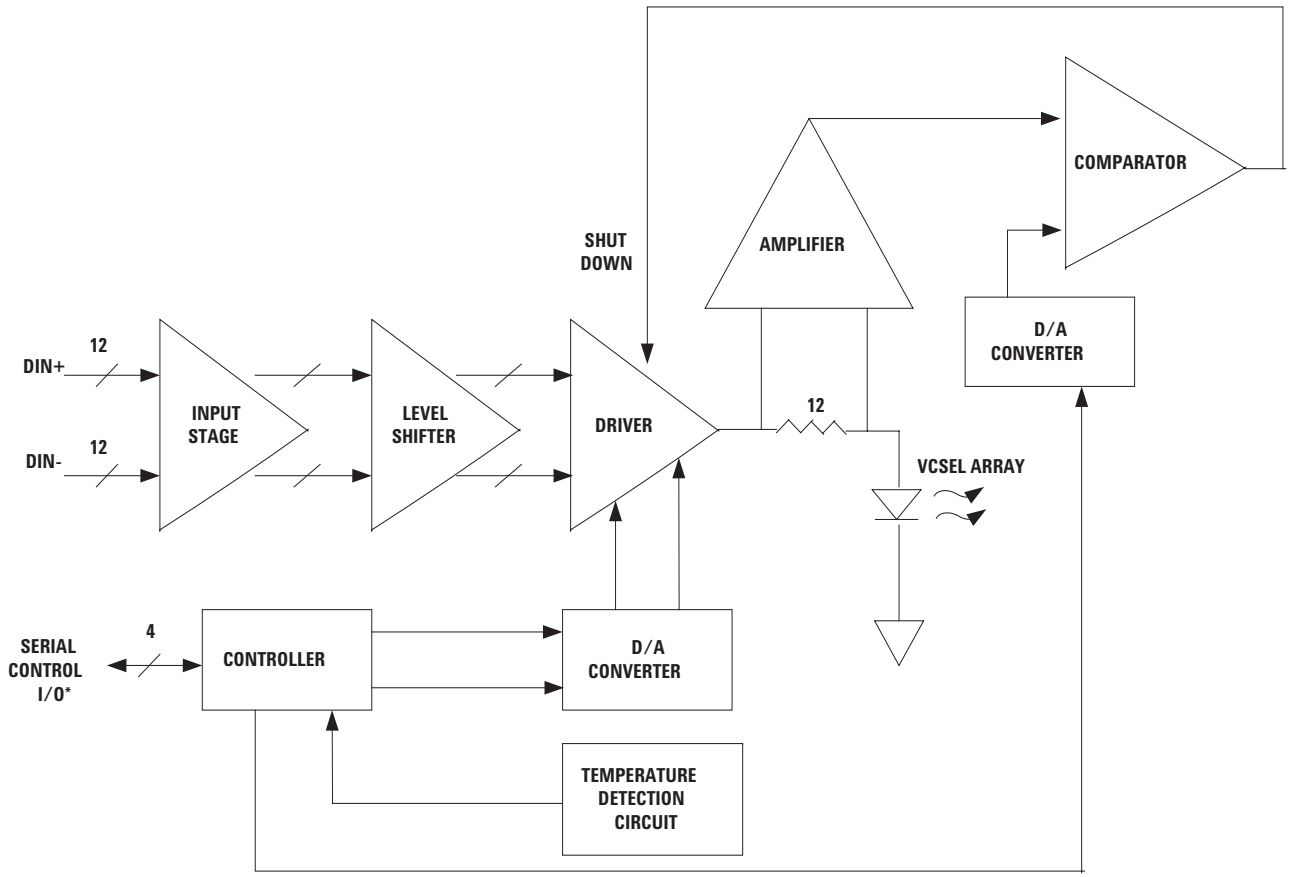


Figure 1. Transmitter block diagram(each channel).
* TX_EN, TX_DIS, RESET-, FAULT-

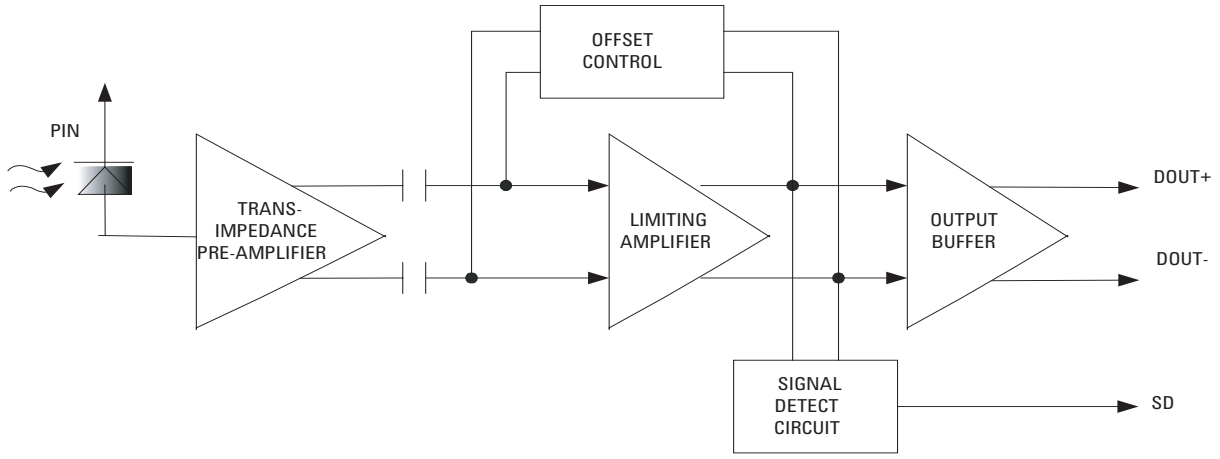


Figure 2. Receiver block diagram (each channel).

Electromagnetic Interference (EMI)

Many equipment designs using these high-data-rate modules will be required to meet the requirements of the FCC in the United States, CENELEC in Europe and VCCI in Japan. These modules, with their shielded design, perform to the levels detailed in the Regulatory Compliance Table. The performance detailed in the Regulatory Compliance Table is intended to assist the equipment designer in the management of the overall equipment EMI performance. However, system margins are dependent on the customer board and chassis design.

Immunity

Equipment using these modules will be subject to radio frequency electromagnetic fields in some environments. These modules have good immunity due to their shielded designs. See the Regulatory Compliance Table for further detail.

Eye Safety

These 850 nm VCSEL-based modules provide eye safety by design. The AFBR-732BWZ has been registered with CDRH and certified by TUV as a Class 1M device under Amendment 2 of IEC 60825-1. See the Regulatory Compliance Table for further detail. If Class 1M exposure is possible, a safety-warning label should be placed on the product stating the following:

LASER RADIATION
DO NOT VIEW DIRECTLY WITH OPTICAL INSTRUMENTS
CLASS 1M LASER PRODUCT

Connector Cleaning

The optical connector used is the MTP® (MPO). The optical ports have recessed optics that are visible through the nose of the ports. The provided port plug should be installed any time a fiber cable is not connected. The port plug ensures the optics remain clean and no cleaning should be necessary. In the event the optics become contaminated, forced nitrogen or clean dry air at less than 20 psi is the recommended cleaning agent. The optical port features, including guide pins, preclude use of any solid instrument. Liquids are not advised due to potential damage.

Process Plug

Each parallel optics module is supplied with an inserted process plug for protection of the optical ports within the MTP® (MPO) connector receptacle.

Handling Precautions

The AFBR-732BWZ and AFBR-742BZ can be damaged by current surges and overvoltage conditions. Power supply transient precautions should be taken.

Application of wave soldering, reflow soldering and/or aqueous wash processes with the parallel optic device on board is not recommended as damage may occur.

Normal handling precautions for electrostatic sensitive devices should be taken (see ESD section).

The AFBR-732BWZ is a Class 1M laser product.
DO NOT VIEW RADIATION DIRECTLY WITH OPTICAL INSTRUMENTS.

Absolute Maximum Ratings [1,2]

Parameter	Symbol	Min.	Max.	Unit	Reference
Storage Temperature (non-operating)	T_S	–40	100	°C	1
Case Temperature (operating)	T_C		90	°C	1, 2, 4
Supply Voltage	V_{CC}	–0.5	4.6	V	1, 2
Data/Control Signal Input Voltage	V_I	–0.5	V_{CC} + 0.5	V	1
Transmitter Differential Data Input Voltage	$\|V_D\|$		2	V	1, 3
Output Current (dc)	I_D		25	mA	1
Relative Humidity (non-condensing)	RH	5	95	%	1

Notes:
1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. See Reliability Data Sheet for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.
3. This is the maximum voltage that can be applied across the Transmitter Differential Data Inputs without damaging the input circuit.
4. Case Temperature is measured as indicated in Figure 3.

Recommended Operating Conditions [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Case Temperature	T_C	0	40	80	°C	2, Figs. 3, 4
Supply Voltage	V_{CC}	3.135	3.3	3.465	V	Figs. 5, 6, 12
Signaling Rate per Channel		1		2.5	Gbd	3
Data Input Differential Peak-to-Peak Voltage Swing	ΔV_{DINP-P}	175		1400	mV_{P-P}	4, Figs. 7, 8
Control Input Voltage High	V_{IH}	2.0		V_{CC}	V	
Control Input Voltage Low	V_{IL}	V_{EE}		0.8	V	
Power Supply Noise for Transmitter and Receiver	N_P			200	mV_{P-P}	5, Figs. 5, 6
Transmitter/Receiver Data I/O Coupling Capacitors	C_{AC}		0.1		µF	Fig. 7
Receiver Differential Data Output Load	R_{DL}		100		Ω	Fig. 7

Notes:
1. Recommended Operating Conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance.
2. Case Temperature is measured as indicated in Figure 3. A +55 °C, 1 m/s, parallel to the printed circuit board, air flow at the module or equivalent cooling is required. See Figure 4.
3. The receiver has a lower cut off frequency near 100 kHz.
4. Data inputs are CML compatible. Coupling capacitors are required to block DC. $\Delta V_{DINP-P} = \Delta V_{DINH} - \Delta V_{DINL}$, where ΔV_{DINH} = High State Differential Data Input Voltage and ΔV_{DINL} = Low State Differential Data Input Voltage.
5. Power Supply Noise is defined for the supply, VCC, over the frequency range from 500 Hz to 2500 MHz, with the recommended power supply filter in place, at the supply side of the recommended filter. See Figures 5 and 6 for recommended power supply filters.

Electrical Characteristics

Transmitter Electrical Characteristics

(T_C = 0 °C to +80 °C, V_{CC} = 3.3 V ± 5%, Typical T_C = +40 °C, V_{CC} = 3.3 V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Reference (Conditions)
Supply Current		I_{CCT}		364	415	mA	Fig. 6
Power Dissipation		P_{DIST}		1.2	1.45	W	
Differential Input Impedance		Z_{in}	80	100	120	Ω	1, Fig. 7, 11
FAULT Assert Time		T_{OFF}		200	250	µs	Fig. 13
RESET Assert Time		T_{OFF}		5	7.5	µs	Fig. 14
RESET De-assert Time		T_{ON}		55	100	ms	Fig. 14
Transmit Enable (TX_EN) Assert Time		T_{ON}		55	100	ms	Fig. 15
Transmit Enable (TX_EN) De-assert Time		T_{OFF}		5	7.5	µs	2, Fig. 15
Transmit Disable (TX_DIS) Assert Time		T_{OFF}		5	7.5	µs	Fig. 15
Transmit Disable (TX_DIS) De-assert Time		T_{ON}		55	100	ms	Fig. 15
Power On Initiation Time		T_{INT}		60	100	ms	Fig. 12
Control I/Os (TX_EN, TX_DIS FAULT, RESET) Compatible	|Input Current High |	$\|I_{IH}\|$			0.5	mA	(2.0 V ≤ VIH ≤ V_{CC})
	| Input Current Lo w|	$\|I_{IL}\|$			0.5	mA	(V_{EE} ≤ V_{IL} ≤ 0.8 V)
	Output Voltage Low	V_{OL}	V_{EE}		0.4	V	(I_{OL} = 4.0 mA)
	Output Voltage High	V_{OH}	2.5	3.3	V_{CC}	V	(I_{OH} = –0.5 mA)

Notes:

1. Differential impedance is measured between $D_{IN+}$and $D_{IN–}$ over the range 4 MHz to 2 GHz.
2. When the control signal Transmitter Enable, Tx_EN, is used to disable the transmitter, Tx_EN must be taken to a logic low-state level (VIL) for one millisecond or longer. Similarly, if the control signal Transmitter Disable, Tx_DIS, is used, then Tx_DIS must be taken to a logic high- state level (VIH) for one millisecond or longer.

Receiver Electrical Characteristics

(T_C = 0 °C to +80 °C, V_{CC} = 3.3 V ± 5%, Typical T_C = +40 °C, V_{CC} = 3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference (Conditions)
Supply Current	I_{CCR}		400	445	mA	1, Fig. 5
Power Dissipation	P_{DISR}		1.3	1.55	W	
Differential Output Impedance	Z_{OUT}	80	100	120	Ω	2, Fig. 8, 10
Data Output Differential Peak-to-Peak Voltage Swing	$\Delta V_{D\text{-}OUTP\text{-}P}$	450	600	750	$mV_{P\text{-}P}$	3, Figs. 7, 8
Inter-channel Skew			100	150	ps	4
Differential Data Output Rise/Fall Time	t_r/t_f		110	150	ps	5
Signal Detect						
Assert Time (OFF-to-ON)	t_{SDA}		170		µs	6
De-assert Time (ON-to-OFF)	t_{SDD}		190		µs	7
Control I/O						
Output Voltage LowLVTTL & LVCMOS	V_{OL}	V_{EE}	3.1	0.4	V	(I_{OL} = 4.0 mA)
Output Voltage HighCompatible	V_{OH}	2.5		V_{CC}	V	(I_{OH} = -0.5 mA)

Notes:

1. $I_{CC}R$ is the dc supply current, dependent upon the number of active channels, where the Data Outputs are ac coupled with capacitors between the outputs and any resistive terminations. See Figure 7 for recommended termination.
2. Measured over the range 4 MHz to 2 GHz.
3. $\Delta V_{DOUTP\text{-}P} = \Delta V_{DOUTH} - \Delta V_{DOUTL}$, where ΔV_{DOUTH} = High State Differential Data Output Voltage and ΔV_{DOUTL} = Low State Differential Data Output Voltage. ΔV_{DOUTH} and $\Delta V_{DOUTL} = V_{DOUT+} - V_{DOUT-}$, measured with a 100 Ω differential load connected with the recommended coupling capacitors and with a 2500 MBd, 8B10B serial encoded data pattern.
4. Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals. Input power at –10 dBm.
5. Rise and Fall Times are measured between the 20% and 80% levels using a 500 MHz square wave signal.
6. The Signal Detect output will change from logic "0" (Low) to "1" (High) within the specified assert time for a step transition in optical input power from the de-asserted condition to the specified asserted optical power level on all 12 channels.
7. The Signal Detect output will change from logic "1" (High) to "0" (Low) within the specified de-assert time for a step transition in optical input power from the specified asserted optical power level to the de-asserted condition on any 1 channel.

Optical Characteristics

Transmitter Optical Characteristics

(T_C = 0 °C to +80 °C, V_{CC} = 3.3 V ± 5%, Typical T_C = +40 °C, V_{CC} = 3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power	P_{OUT}			–1	dBm avg.	1
Output Optical Power – Off State	$P_{OUT\ DIS}$			–30	dBm avg.	
Optical Modulation Amplitude	OMA	-9.84			dBm	
Center Wavelength	λ_C	830	850	860	nm	
Spectral Width – rms	σ		0.4	0.85	nm rms	
Rise/Fall Time	t_r/t_f		50	150	ps	2
Inter-channel Skew			110	200	ps	3
Relative Intensity Noise	RIN			–124	dB/Hz	
Jitter Contribution						
Deterministic	DJ			80	ps_{p-p}	4
Total	TJ			162	ps_{p-p}	5

Notes:

1. The specified optical output power, measured at the output of a short test cable, will be compliant with IEC 60825-1 Amendment 2, Class 1 Accessible Emission Limits, AEL, and the output power of the module without an attached cable will be compliant with the IEC 60825-1 Amendment 2, Class 1M AEL. See discussion in the Regulatory Compliance section.
2. These are unfiltered 20-80% value measured with optical-electrical converter with 12 GHz bandwidth. To increase accuracy of measurement owning to laser overshoot and ringing, a filtered rise/fall time measurement is adopted with a 2.5Gbps (1.875 GHz bandwidth) 4th Bessel Thompson filter. A max spec of 150 ps for unfiltered waveform is equivalent to a max spec 242 ps for filtered waveform.
3. Inter-channel Skew is defined for the condition of equal amplitude, zero ps skew input signals.
4. Deterministic Jitter (DJ) is defined as the combination of Duty Cycle Distortion (Pulse-Width Distortion) and Data Dependent Jitter. Deterministic Jitter is measured at the 50% signal threshold level using a 2.5 GBd K28.5, or equivalent, test pattern with zero skew between the differential data input signals.
5. Total Jitter (TJ) includes Deterministic Jitter and Random Jitter (RJ). Total Jitter is specified at a BER of 10^{-12} for the same 2.5 GBd test pattern as for DJ.

Receiver Optical Characteristics

(T_C = 0 °C to +80 °C, V_{CC} = 3.3 V ± 5%, Typical T_C = +40 °C, V_{CC} = 3.3 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Sensitivity (OMA)	$P_{IN\ MIN}$			-13	dBm	1
Input Optical Power Saturation (OMA)	$P_{IN\ MAX}$	–1.22			dBm	2
Operating Center Wavelength	λ_C	830		860	nm	
Stressed Receiver Sensitivity (OMA)				-11.8	dBm	3
Stressed Receiver Eye Opening		120			ps	4
Return Loss		12	19		dB	5
Signal Detect						
Asserted (OMA)	P_A			-15	dBm	6
De-asserted (OMA)	P_D	-35	-21		dBm	
Hysteresis	P_A-P_D	0.5	2		dB	

Notes:

1. Sensitivity is defined as the OMA necessary to produce a BER of 10^{-12} at the center of the Baud interval using a 2.5 GBd Pseudo Random Bit Sequence of length 2^7 – 1 (PRBS), or equivalent, test pattern. For this parameter, input power is equivalent to that provided by an ideal source, i.e., a source with RIN and switching attributes that do not degrade the sensitivity measurement. All channels not under test are operating receiving data with an average input power up to 6 dB above $P_{IN\ MIN}$.
2. Saturation is defined as the OMA that produces at the center of the output swing a receiver output eye width less than 120 ps where BER < 10^{-12} using a 2.5 GBd Pseudo Random Bit Sequence of length 2^7 –1 (PRBS), or equivalent, test pattern.
3. Stressed receiver sensitivity is defined as the average input power necessary to produce a BER < 10^{-12} at the center of the Baud interval using a 2.5 GBd Pseudo Random Bit Sequence of length 2^7 – 1 (PRBS), or equivalent, test pattern. For this parameter, input power is conditioned with 2.5 dB Inter-Symbol Interference, ISI, (min), 120 ps Total Jitter, TJ (min). All channels not under test are operating receiving data with an average input power up to 6 dB above $P_{IN\ MIN}$.
4. Stressed receiver eye opening is defined as the receiver output eye width where BER < 10^{-12} at the center of the output swing using a 2.5 GBd Pseudo Random Bit Sequence of length 2^7 – 1 (PRBS), or equivalent, test pattern. For this parameter, input power is an average input optical power of –10.4 dBm and conditioned with 1.2 dB ISI (min), 120 ps TJ (min), All channels not under test are operating receiving data with an average input power up to 6 dB above $P_{IN\ MIN}$.
5. Return loss is defined as the ratio, in dB, of the received optical power to the optical power reflected back down the fiber.
6. Signal Detect assertion requires all optical inputs to exhibit a minimum -15 dBm OMA. All channels not under test are operating with PRBS 7 serial encoded patterns, asynchronous with the channel under test, and an average input power up to 6 dB higher than $P_{IN\ MIN}$.

Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pads	JEDEC Human Body Model (HBM) (JESD22-A114-B)	Transmitter Module > 1000 V Receiver Module > 2000 V
	JEDEC Machine Model (MM)	Transmitter Module > 50 V Receiver Module > 200 V
Electrostatic Discharge (ESD) to the Connector Receptacle	Variation of IEC 61000-4-2	Typically withstands at leasr 6 kV air discharge (with module biased) without damage.
Electromagnetic Interference (EMI)	FCC Part 15 CENELEC EN55022 (CISPR 22A) VCCI Class 1	Typically pass with 10 dB margin. Actual performance dependent on enclosure design.
Immunity	Variation of IEC 61000-4-3	Typically minimal effect from a 10 v/m field swept from 80 MHz to 1 GHz applied to the module without a chassis enclosure.
Laser Eye Safety and Equipment Type Testing	IEC 60825-1 Amendment 2 CFR 21 Section 1040	P_{OUT}: IEC AEL & US FDA CRDH Class 1M CDRH Accession Number: 9720151-22 TUV Certficate Number: E2171095.04
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment including Electrical Business Equipment	UL File Number: E173874
RoHS Complaince		Less than 1000ppm of Cadmium, lead, mercury, hexavalent chromium, polybrominated biphenyls, and polybrominated biphenyl ethers

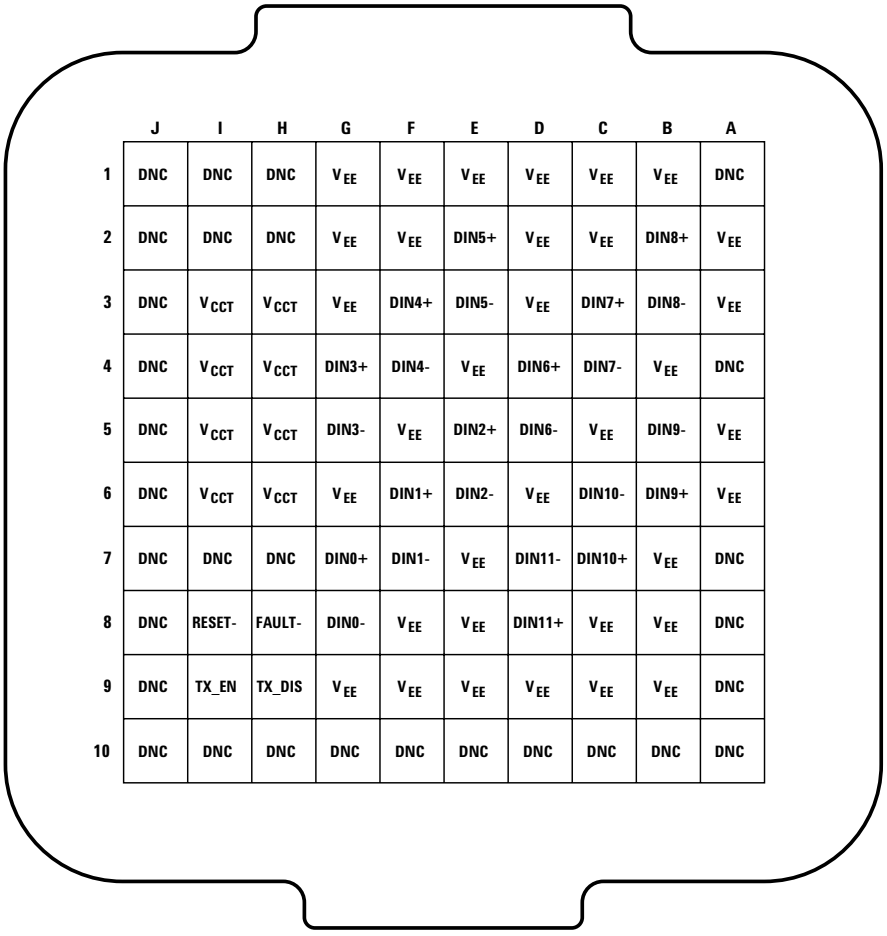
Table 1. Transmitter Module Pad Description

Symbol	Functional Description
V_{EE}	Transmitter Signal Common. All voltages are referenced to this potential unless otherwise indicated. Directly connect these pads to transmitter signal ground plane.
$V_{CC}T$	Transmitter Power Supply. Use recommended power supply filter circuit in Figure 6.
DIN0+ through DIN11+	Transmitter Data In+ for channels 0 through 11, respectively. Differential termination and self bias are included, see Figure 11.
DIN0– through DIN11–	Transmitter Data In- for channels 0 through 11, respectively. Differential termination and self bias are included; see Figure 11.
TX_EN	TX Enable. Active high. Internal pull-up High = VCSEL array is enabled if TX_DIS is inactive (Low). Low = VCSEL array is off. TX_EN must be taken to a logic low state level (V_{OL}) for 1 ms or longer.
TX_DIS	TX Disable. Active high. Internal pull-down Low = VCSEL array is enabled if TX_EN is active (High). High = VCSEL array is off. TX_DIS must be taken to a logic High state level (V_{OH}) for 1 ms or longer.
RESET-	Transmitter RESET- input. Active low. Internal pull-up. Low = Resets logic functions, clears FAULT- signal, VCSEL array is off. high = Normal operation. See Figure 14.
FAULT-	Transmitter FAULT- output. Active low. Low (logic "0") results from a VCSEL over-current condition, out of temperature range, or EEPROM calibration data corruption condition detected for any VCSEL. An asserted (logic "0") FAULT- disables the VCSEL array and is cleared by RESET- or power cycling $V_{CC}T$ FAULT- is a single ended LVTTL compatible output.
DNC	Do not connect to any electrical potential.

Table 2. Receiver Module Pad Description

Symbol	Functional Description
V_{EE}	Receiver Signal Common. All voltages are referenced to this potential unless otherwise indicated. Directly connect these pads to receiver signal ground plane.
$V_{CC}R$	Receiver Power Supply. Use recommended power supply filter circuit in Figure 5.
V_{PP}	Not required for Avago product. Pads not internally connected
DOUT0+ through DOUT11+	Receiver Data Out+ for channels 0 through 11, respectively. Terminate these high-speed differential CML outputs with standard CML techniques at the inputs of the receiving device. Individual data outputs will be squelched for insufficient input signal level.
DOUT0– through DOUT11–	Receiver Data Out- for channel 0 through 11, respectively. Terminate these high-speed differential CML outputs with standard CML techniques at the inputs of the receiving device. Individual data outputs will be squelched for insufficient input signal level.
SD	Signal Detect. Normal optical input levels to all channels results in a logic "1" output, V_{OH}, asserted. Low input optical levels to any channel results in a fault condition indicated by a logic "0" output, V_{OL}, de-asserted. SD is a single-ended LVTTL compatible output.
RX_EN	Receiver output enable. Active high (logic "1"), internal pull-up. Low (logic "0") = receiver outputs disabled, all outputs are high (logic "1").
SQ_EN	Squelch enable input. Active high (logic "1"), internal pull-up. Low (logic "0") = squelch disabled. When SQ_EN is high and SD is low, corresponding outputs are squelched.
EN_SD	Enable Signal Detect. Active high (logic "1"), internal pull-up. Low (logic "0") = Signal detect output forced active high.
DNC	Do not connect to any electrical potential.

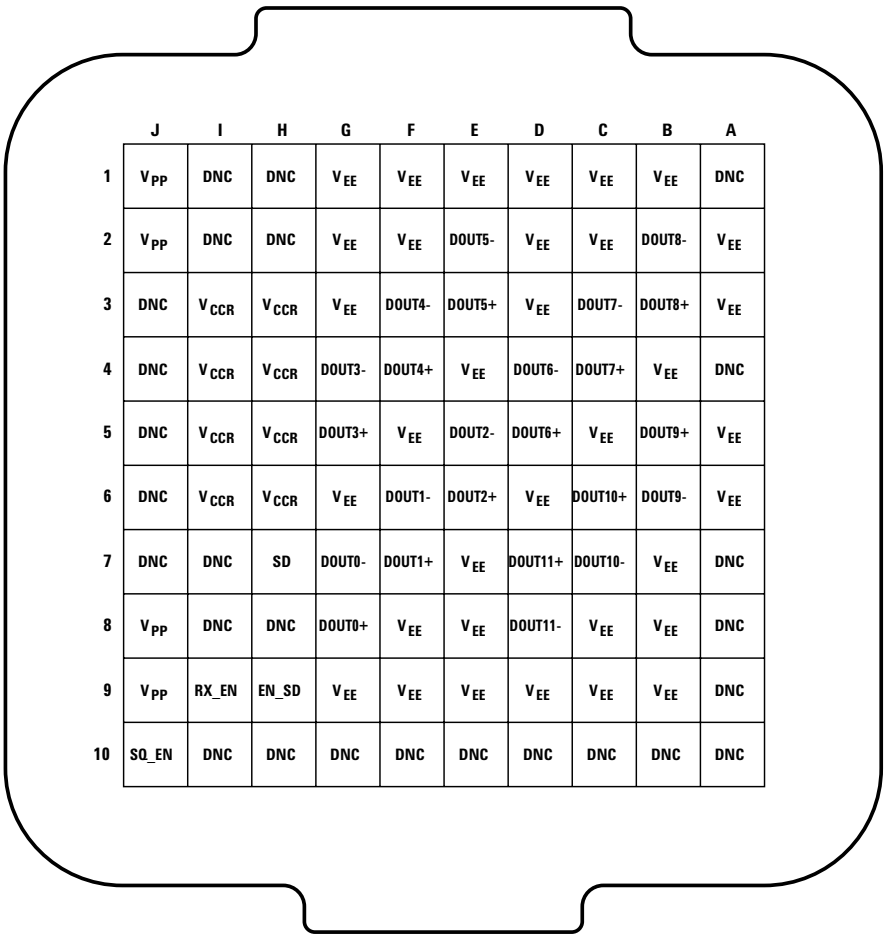
TRANSMITTER MODULE PAD ASSIGNMENT
(TOWARD MTP® CONNECTOR)



	J	I	H	G	F	E	D	C	B	A
1	DNC	DNC	DNC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
2	DNC	DNC	DNC	V_{EE}	V_{EE}	DIN5+	V_{EE}	V_{EE}	DIN8+	V_{EE}
3	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN4+	DIN5-	V_{EE}	DIN7+	DIN8-	V_{EE}
4	DNC	V_{CCT}	V_{CCT}	DIN3+	DIN4-	V_{EE}	DIN6+	DIN7-	V_{EE}	DNC
5	DNC	V_{CCT}	V_{CCT}	DIN3-	V_{EE}	DIN2+	DIN6-	V_{EE}	DIN9-	V_{EE}
6	DNC	V_{CCT}	V_{CCT}	V_{EE}	DIN1+	DIN2-	V_{EE}	DIN10-	DIN9+	V_{EE}
7	DNC	DNC	DNC	DIN0+	DIN1-	V_{EE}	DIN11-	DIN10+	V_{EE}	DNC
8	DNC	RESET-	FAULT-	DIN0-	V_{EE}	V_{EE}	DIN11+	V_{EE}	V_{EE}	DNC
9	DNC	TX_EN	TX_DIS	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
10	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

TOP VIEW (PCB LAYOUT)
(10 x 10 ARRAY)

RECEIVER MODULE PAD ASSIGNMENT
(TOWARD MTP® CONNECTOR)



	J	I	H	G	F	E	D	C	B	A
1	V_{PP}	DNC	DNC	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
2	V_{PP}	DNC	DNC	V_{EE}	V_{EE}	DOUT5-	V_{EE}	V_{EE}	DOUT8-	V_{EE}
3	DNC	V_{CCR}	V_{CCR}	V_{EE}	DOUT4-	DOUT5+	V_{EE}	DOUT7-	DOUT8+	V_{EE}
4	DNC	V_{CCR}	V_{CCR}	DOUT3-	DOUT4+	V_{EE}	DOUT6-	DOUT7+	V_{EE}	DNC
5	DNC	V_{CCR}	V_{CCR}	DOUT3+	V_{EE}	DOUT2-	DOUT6+	V_{EE}	DOUT9+	V_{EE}
6	DNC	V_{CCR}	V_{CCR}	V_{EE}	DOUT1-	DOUT2+	V_{EE}	DOUT10+	DOUT9-	V_{EE}
7	DNC	DNC	SD	DOUT0-	DOUT1+	V_{EE}	DOUT11+	DOUT10-	V_{EE}	DNC
8	V_{PP}	DNC	DNC	DOUT0+	V_{EE}	V_{EE}	DOUT11-	V_{EE}	V_{EE}	DNC
9	V_{PP}	RX_EN	EN_SD	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	V_{EE}	DNC
10	SQ_EN	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC	DNC

TOP VIEW (PCB LAYOUT)
(10 x 10 ARRAY)

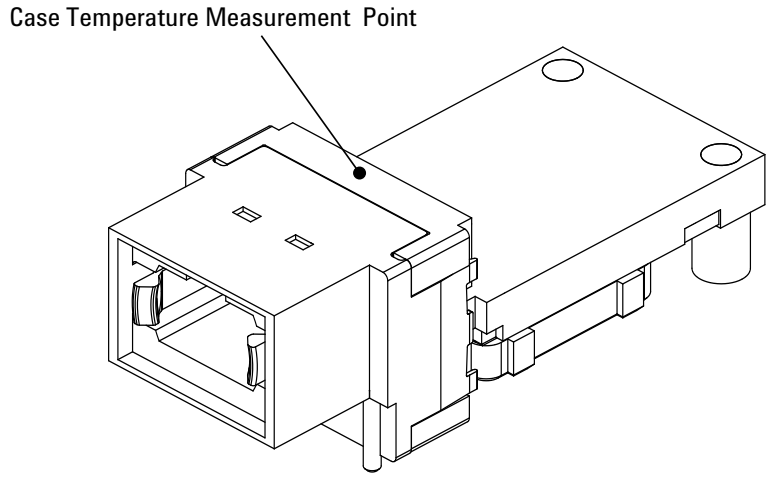


Figure 3. Case temperature measurement. (label and heatsink removed for clarity)

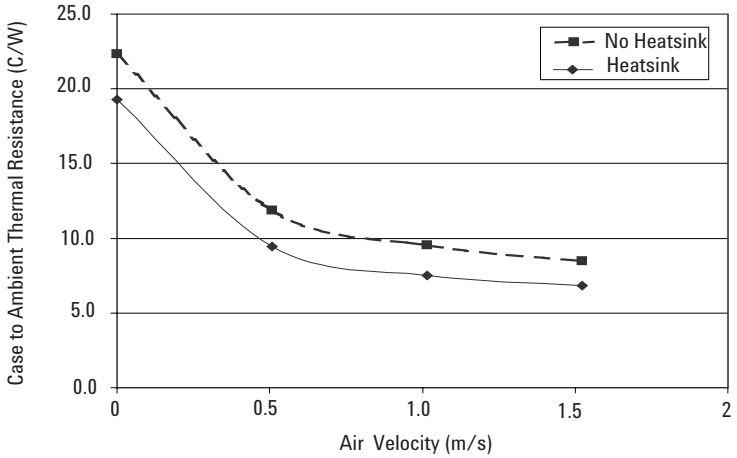
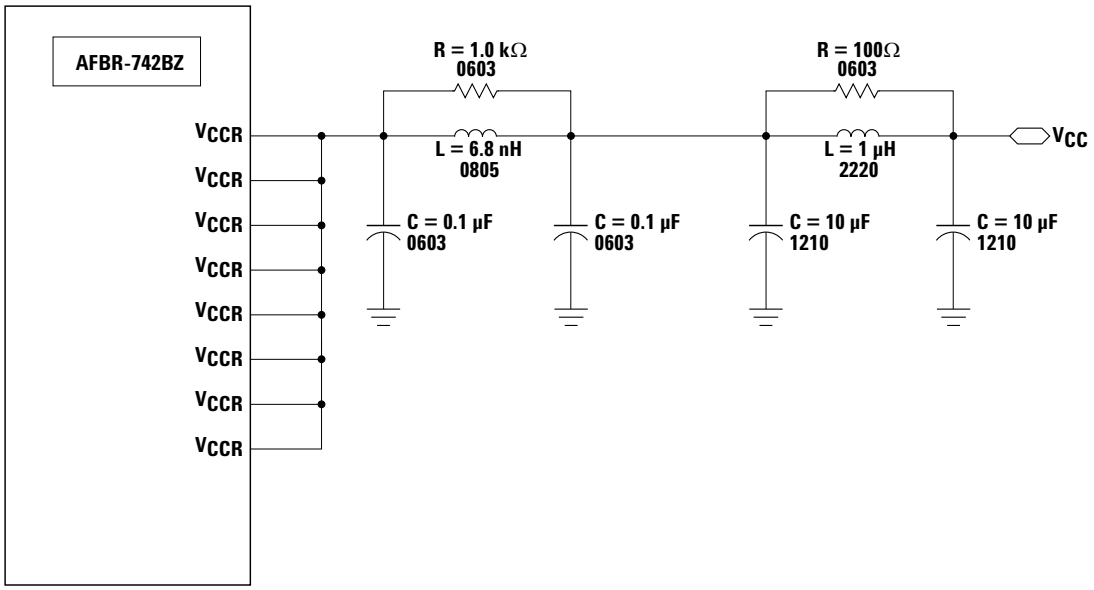


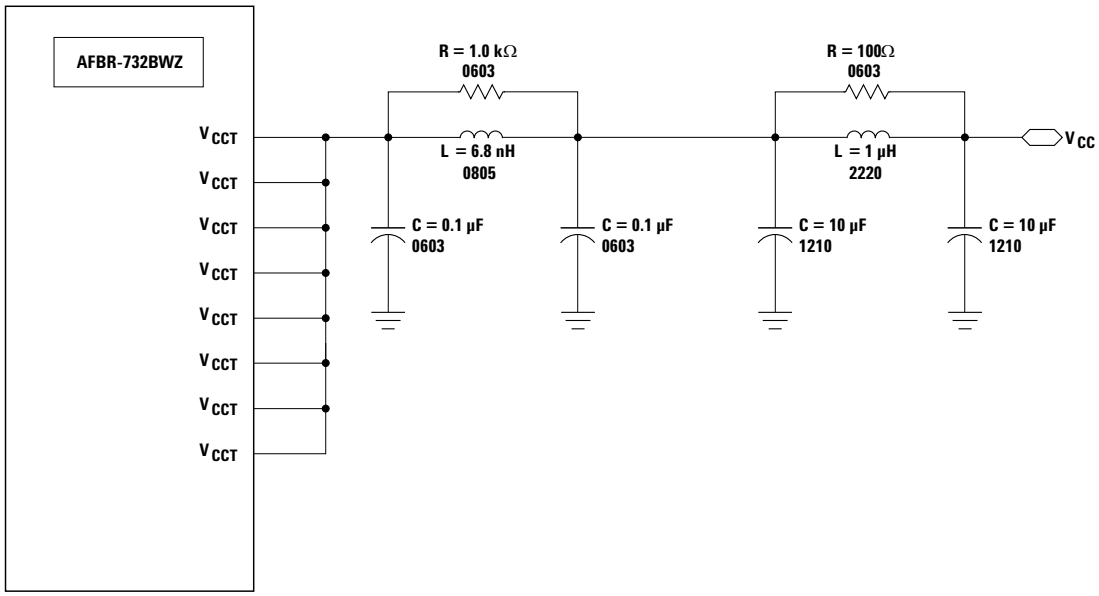
Figure 4. Case to Ambient thermal resistance (C/W) versus air velocity (sea level)



NOTE:

1. V_{CC} IS DEFINED BY 3.135 < V_{CC} < 3.465 VOLTS AND THE POWER SUPPLY FILTER HAS < 50 mV DROP ACROSS IT RESULTING IN 3.085 < V_{CCR} < 3.415 VOLTS.

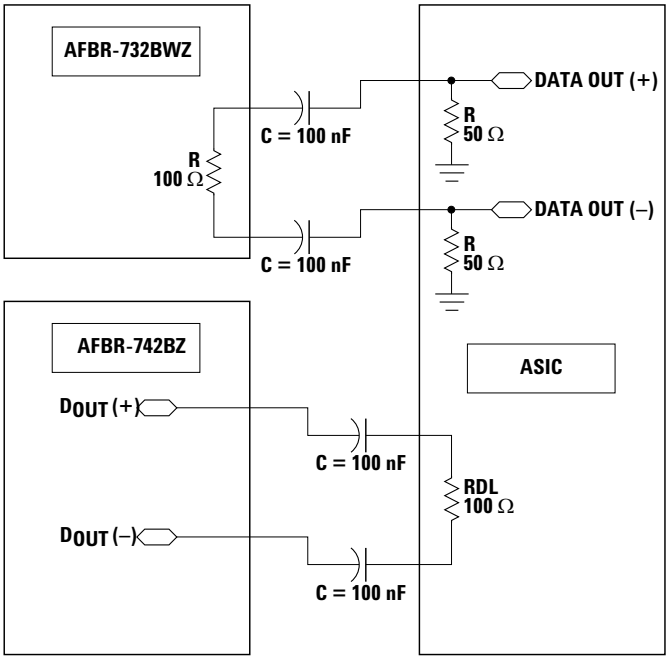
Figure 5. Recommended receiver power supply filter.



NOTE:

V_{CC} IS DEFINED BY 3.135 < V_{CC} < 3.465 VOLTS AND THE POWER SUPPLY FILTER HAS < 50 mV DROP ACROSS IT RESULTING IN 3.085 < V_{CCT} < 3.415 VOLTS.

Figure 6. Recommended transmitter power supply filter.



UNUSED RECEIVER CHANNEL OUTPUTS MUST BE TERMINATED.

NOTE:
AC COUPLING CAPACITORS SHOULD BE USED TO CONNECT DATA OUTPUTS TO DATA INPUTS BETWEEN THE AFBR-732BWZ, AFBR-742BZ, AND HOST BOARD ICs (e.g., ASIC) WITH EITHER 50WSINGLE-ENDED OR 100Ω DIFFERENTIAL TERMINATIONS AS SHOWN. THE CAPACITORS' VALUES CAN BE REDUCED FROM 100 nF (0603 SIZE) IF THE DATA RATE AND RUN LENGTH ARE LIMITED.

Figure 7. Recommended ac coupling and data signal termination.

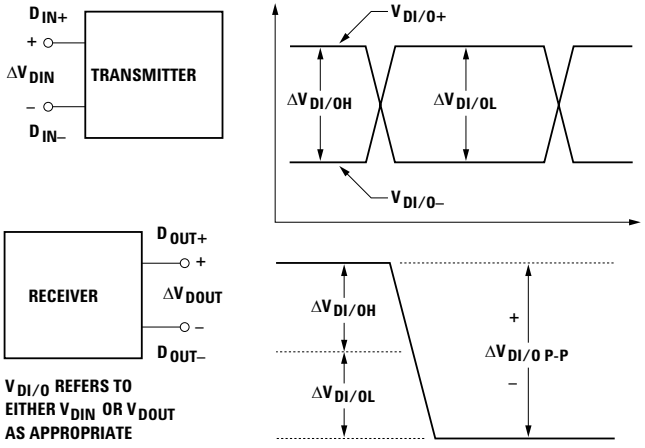
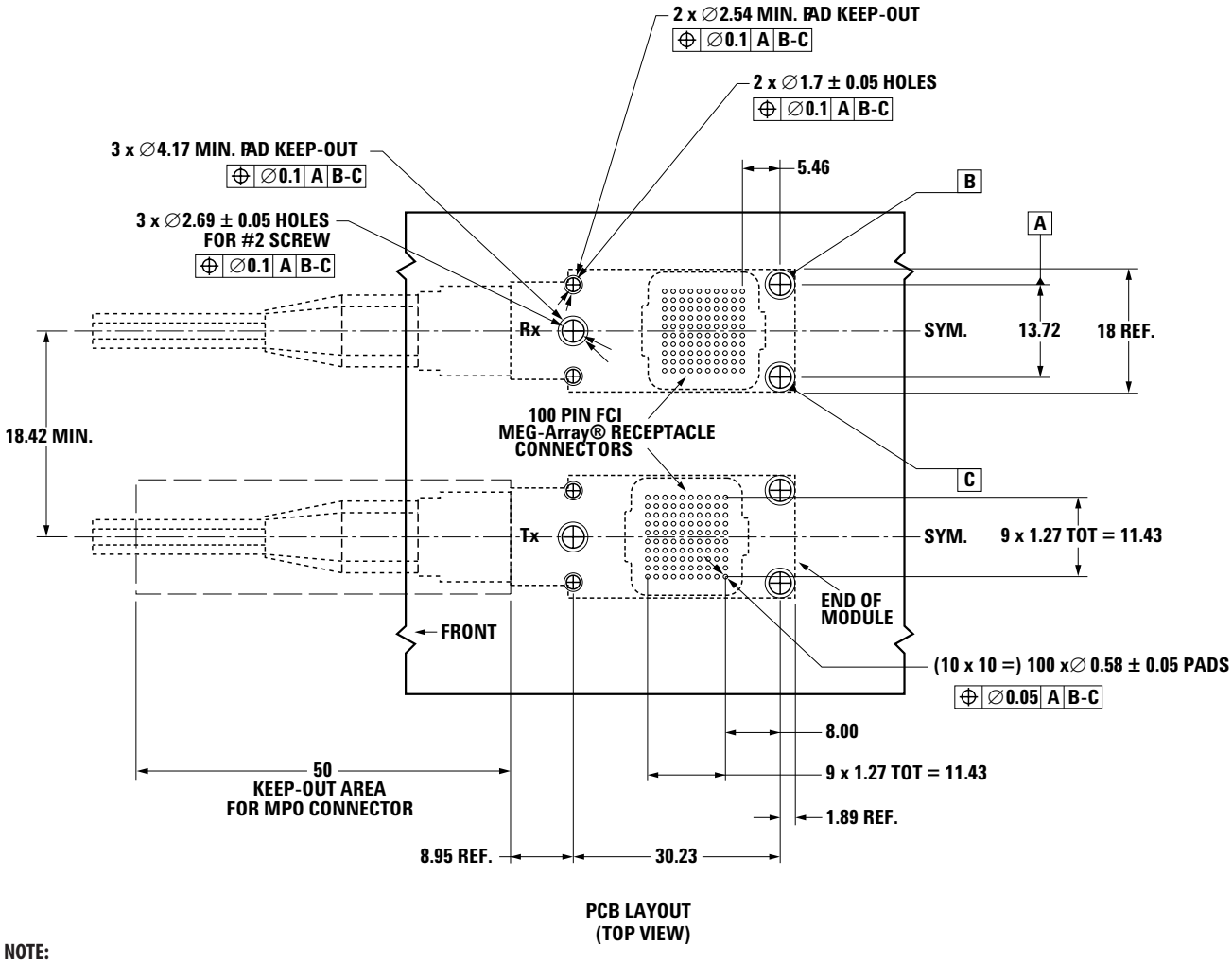


Figure 8. Differential signals.



PCB LAYOUT
(TOP VIEW)

NOTE:

The host electrical connector attached to the PCB must be a 100-position FCI Meg-Array plug (FCI PN: 84512-102) or equivalent.

Figure 9. Package board footprint (dimensions in mm). PCB top view.

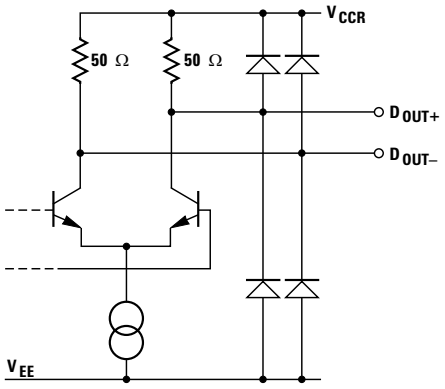


Figure 10. Rx data output equivalent circuit.

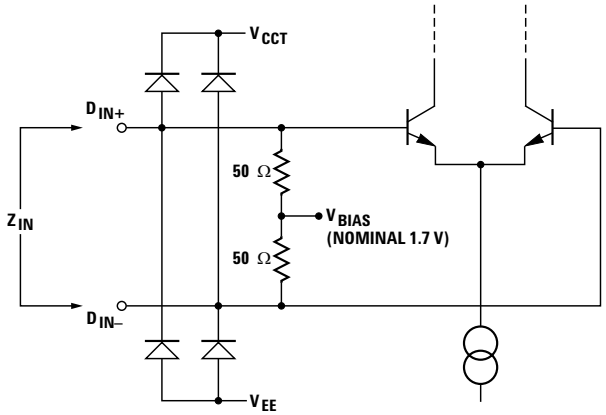


Figure 11. Tx data input equivalent circuit.

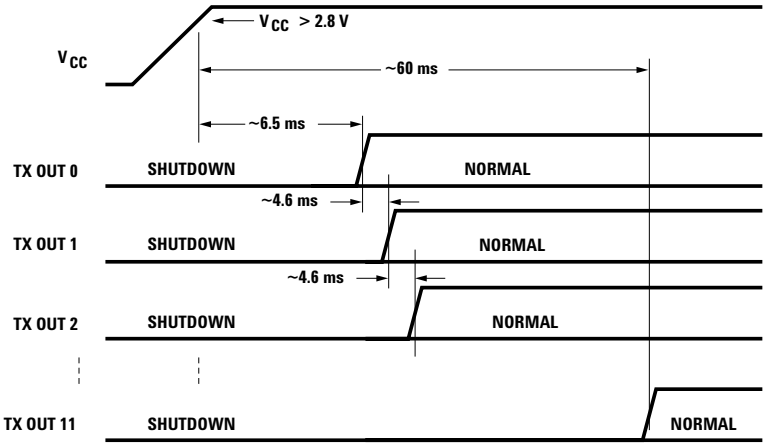


Figure 12. Typical transmitter power-up sequence.

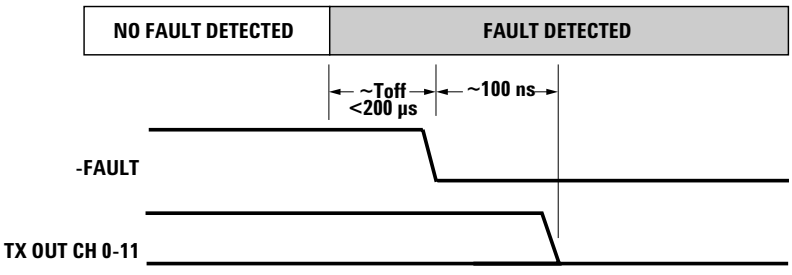


Figure 13. Transmitter FAULT signal timing diagram.

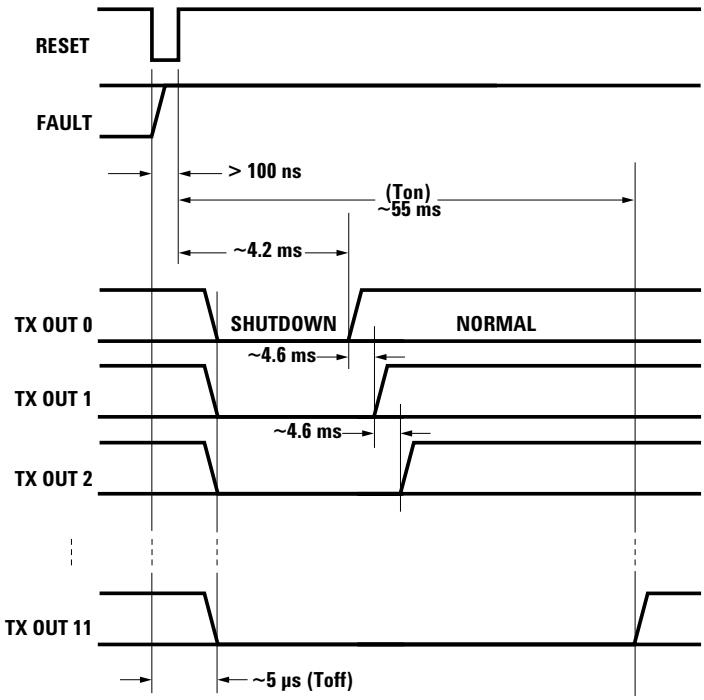


Figure 14. Transmitter RESET timing diagram.

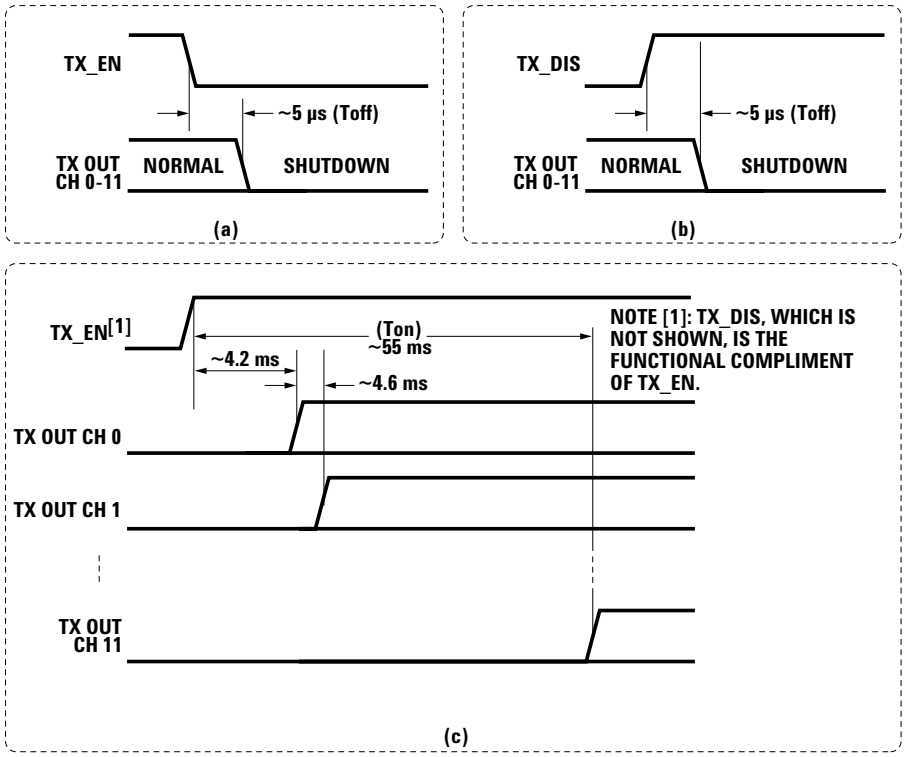
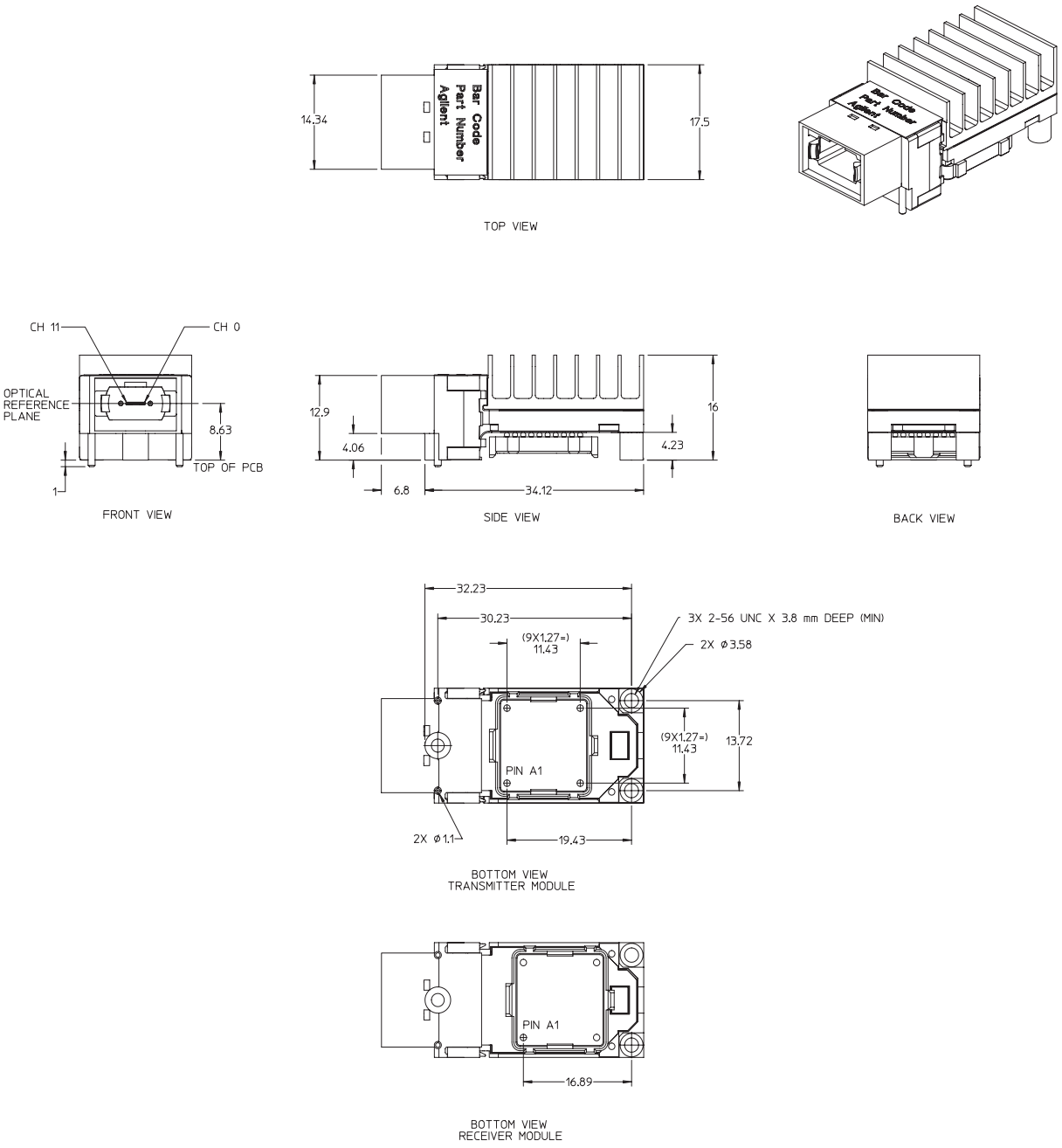


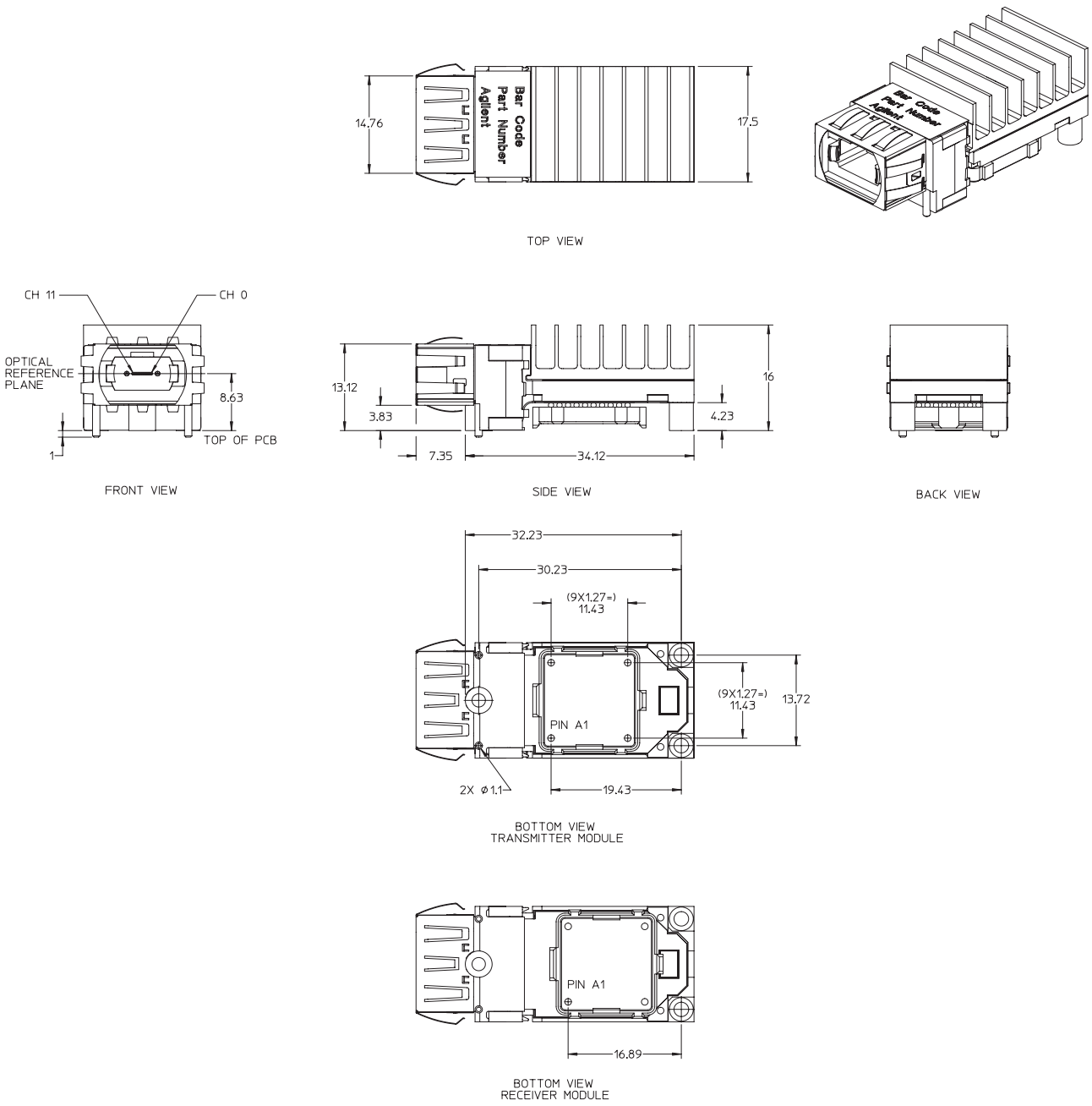
Figure 15. Transmitter TX_EN and TX_DIS timing diagram.

Module Outline



Notes:
1. Module supplied with port process plug.
2. Module mass approximately 20 grams.

Figure 16. Package outline for AFBR-732BWZ and AFBR-742BZ (dimensions in mm).



Notes:
1. Module supplied with port process plug.
2. Module mass approximately 20 grams.

Figure 17. Package Outline for AFBR-732BEWZ and AFBR-742BEZ (dimensions in mm)

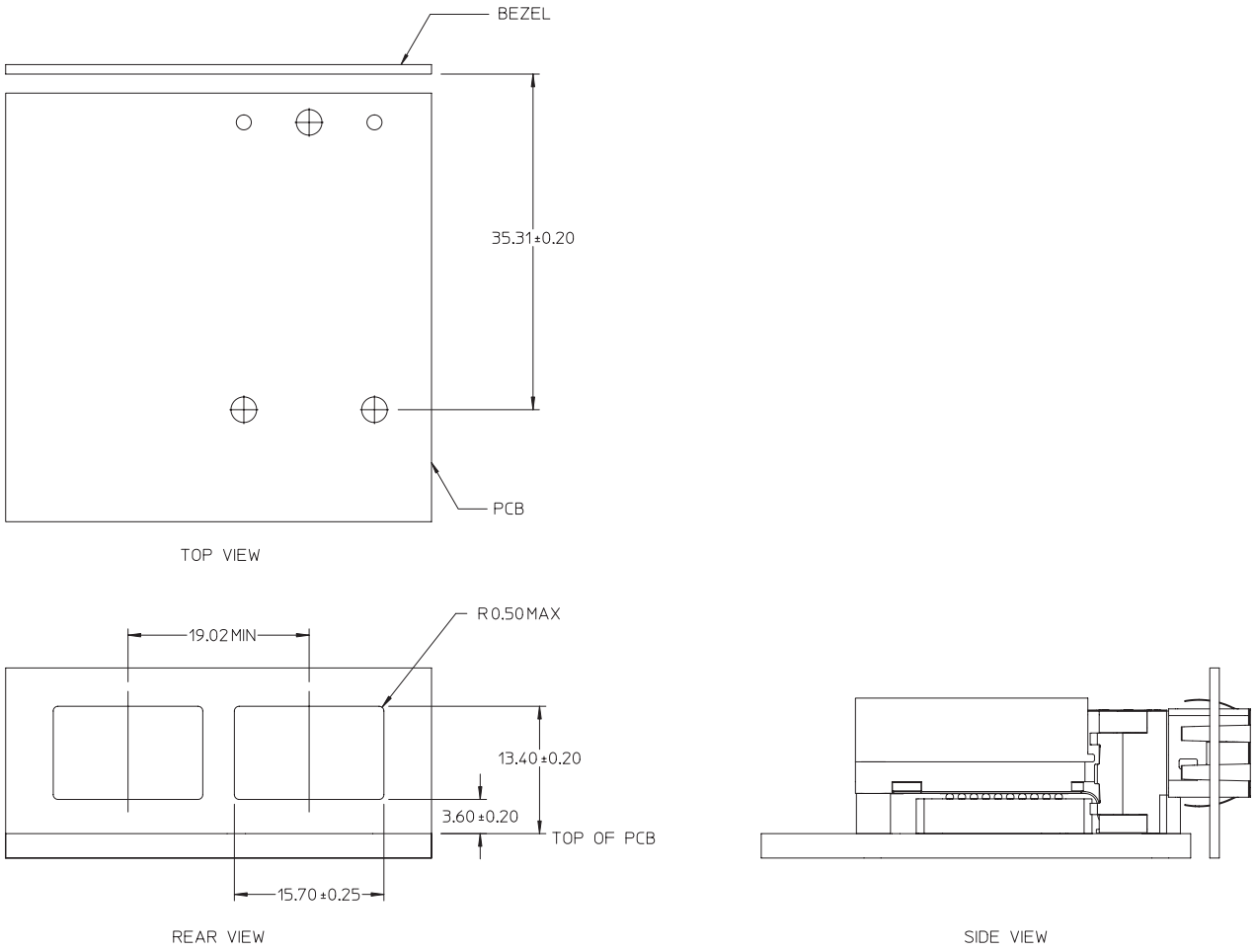


Figure 18. Host Frontplate Layout (dimensions in mm)

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