an Intel company

2.5 Gbit/s Retiming Laser Driver GD16578

General Description

The GD16578 is a high performance low power 2.5 Gbit/s Laser Driver with optional on chip retiming of data.

The GD16578 is designed to meet and exceed ITU-T STM-16 or SONET OC-48 fiberoptic communication systems requirements.

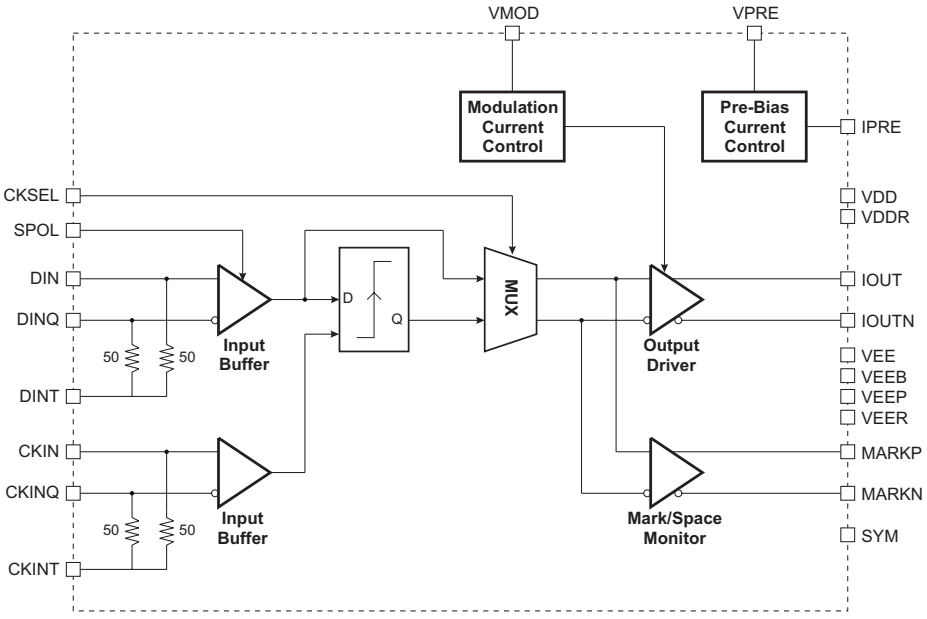
The GD16578 is designed to sink a Modulation Current into the IOUT pin and a Pre-Bias Current into the IPRE pin. The Modulation Current is adjustable up to 200 mA by means of the pin VMOD. The Pre-Bias Current may be adjusted up to 60 mA by means of the VPRE pin.

Retiming of the data signal connected to the pins DIN, DINQ is made by means of a DFF clocked by an external clock signal at the data rate fed to the pins CKIN and CKINQ.

A Mark-Space monitor is available on the pins MARKP and MARKN. Together with the symmetry adjustment pin (SYM) this may be used to control the mark space ratio of the output signal.

The GD16578 can operate on a single +5 V supply or a single -5.2 V supply.

The circuit is available in a thermally enhanced 32-pin TQFP plastic package.



Features

- Complies with ITU-T STM-16 and SONET OC-48 standards.
- Intended for driving a 25 Ω load, e.g. a laser diode or Mach Zender modulator with 25 Ω input impedance.
- Clocked or non-clocked operation.
- Large modulation current adjustment range from 70 mA to 200 mA.
- Output voltage over / under shoot less than ±5 % respectively ±10 %.
- Rise / fall times less than 100 ps.
- Laser diode pre-bias adjustable up to 60 mA.
- Mark-Space monitor.
- Symmetry adjustment
- Internal 50 Ω termination of data and clock inputs.
- Power dissipation: 1 W (typ.). (excluding Modulation Current and Pre-bias Current).
- 32 pin thermally enhanced TQFP plastic package.

Applications

- Tele Communication:
  - SDH STM-16
  - SONET OC-48
- Data Communication.
- Electro Absorption laser driver.
- Direct Modulation laser driver.
- Mach Zender modulator driver.

Functional Details

GD16578 is a 2.5 Gbit/s laser driver with an optional retiming of the data signal. It is capable of driving high power laser diodes, typically having input impedance of 25 Ω, at a maximum modulation current of 200 mA and a maximum pre-bias current of 60 mA.

Data (DIN, DINQ) is input to GD16578 and retimed within a DFF clocked by an external clock (CKIN, CKINQ). Optionally the retiming may be bypassed controlled by a select pin (CKSEL).

Both the differential data (DIN, DINQ) and clock inputs (CKIN, CKINQ) are internally terminated to 50 Ω. Termination is made with a 50 Ω resistor from the two differential inputs to a common pin called DINT and CKINT respectively. Each of these termination pins is DC biased internally via 750 Ω to -1.3 V, hence there is no need for external bias network. The input sensitivity when driven with a single ended signal is better than 150 mV on both clock and data inputs.

The GD16578 can be used e.g. to boost the output from the GD16553 MUX. This differential output can be DC coupled to the GD16578 input. A signal of 200 mV_{PP} at a common mode level of -100 mV has been observed to provide good performance.

The output pin (IOUT) is an open collector output designed for driving external loads with 25 Ω characteristic impedance. Because of the nature of an open collector the output therefore may be regarded as a current switch, with infinite output impedance. The characteristic impedance through the package is approximately 25 Ω. Optimum performance of GD16578 therefore is achieved if the output is terminated into a 25 Ω impedance.

The output modulation current is controlled by the pin VMOD and can be controlled in the range from 0 mA to 200 mA, however the specifications is only valid in the range from 70 mA to 200 mA. The output voltage swing across the external load may be varied accordingly. The modulation current control on pin VMOD is implemented as a current mirror and therefore sinks a current proportional to the modulation current. The current sink into the VMOD pin is approximately 1/210 of the modulation current.

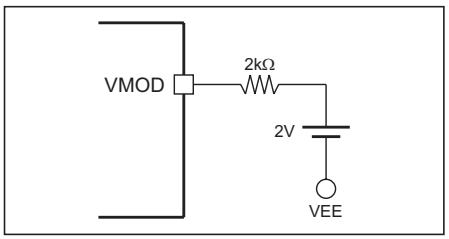


Figure 2. *Equivalent schematic of the VMOD input*

When DC coupled the output swing will be limited by the specification for the minimum voltage of V_{DD} -3 V on the IOUT and IOUTN pins. Since 120 mA into 25 Ω gives 3 V swing it will not be possible to terminate the output with a 25 Ω load to V_{DD}.

If more than 120 mA modulation current is required, either the load (i.e. the laser) must be supplied from a positive supply voltage, or AC coupling with a bias tee must be used (see Figure 3).

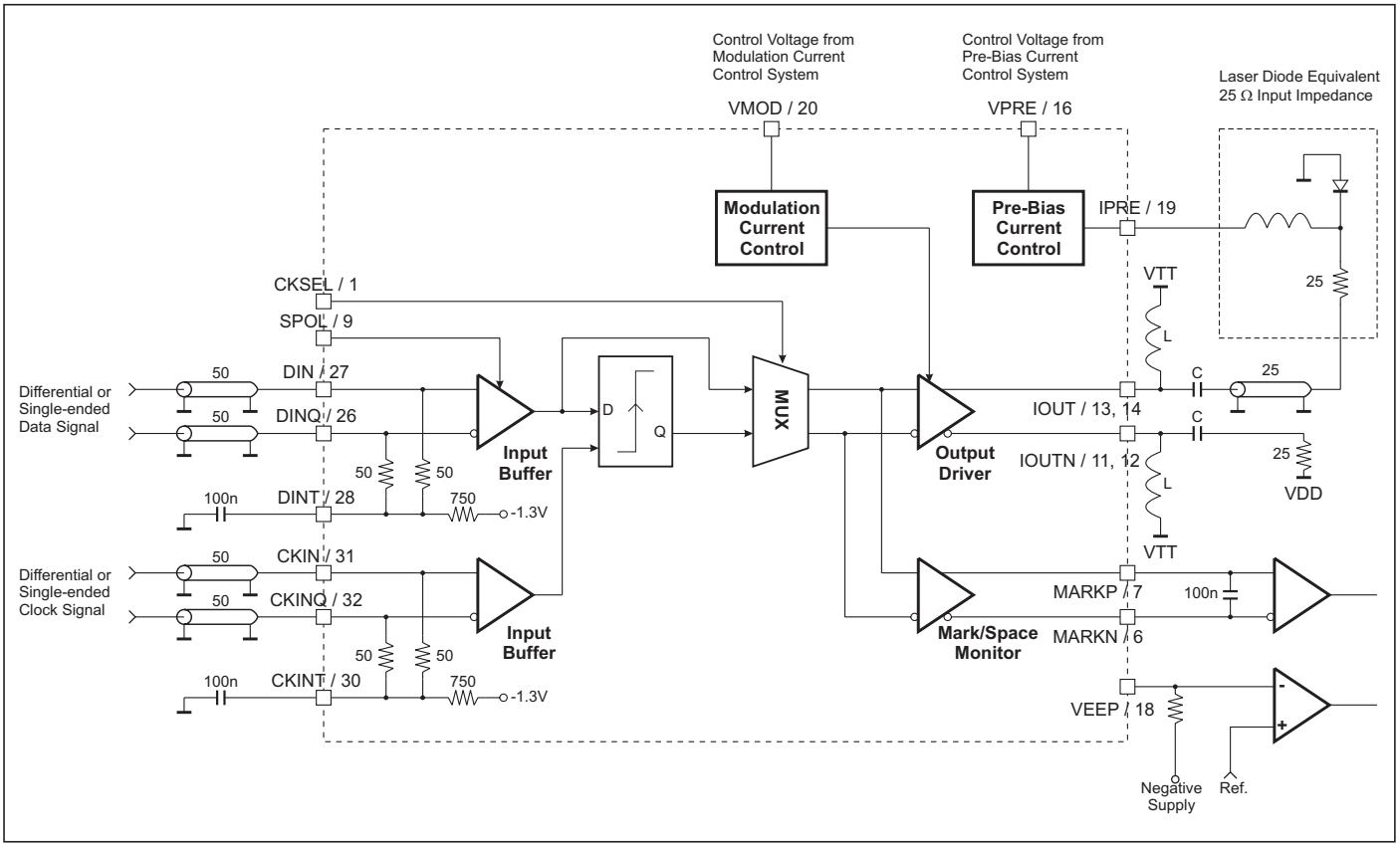


Figure 1. *Application Diagram*

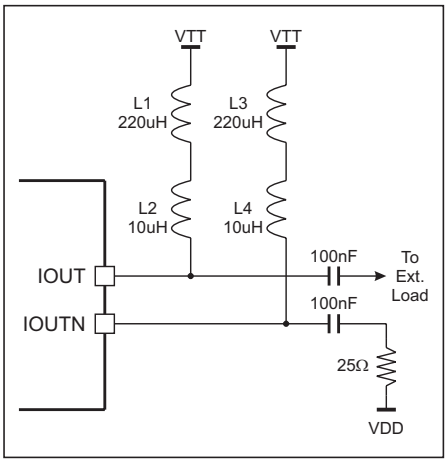


Figure 3. *AC Coupled Output*

For high modulation currents it may be necessary to use a positive supply for the bias tee, depending on the resistance in the bias coils. Measurements with the set-up in Figure 3 with bias coils with 7 Ω resistance show that a positive supply is required for modulation current above approximately 150 mA, and a voltage V_{TT} = +1,0 V is sufficient to give 200 mA with V_{EE} = –5.2 V supply. Less negative V_{EE} voltage must be compensated by correspondingly higher V_{TT} supply.

In the configuration shown in Figure 3 two coils in series are used for each branch of the output for effective blocking of high and low frequencies. Low frequency ciols generally have high parasitic parallel capacitance.

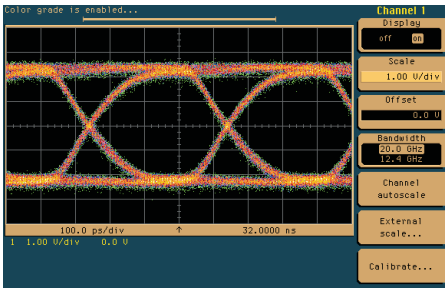


Figure 4. *Output waveform at 200 mA, -4.7 V supply, AC coupled load.*

The pre-bias current is controlled by the pin VPRE and can be controlled from 0 mA to 60 mA. The pre-bias current control on pin VPRE is implemented as a current mirror and therefore sinks a current proportional to the pre-bias current. The current sink into the VPRE pin is approximately 3/500 of the pre-bias current.

An important parameter for laser drivers is voltage overshoot on the output pin (IOUT), because it determines the extinction ratio. GD16578 has been designed with special emphasis on achieving a very small voltage overshoot. For GD16578 the voltage overshoot is less than 5 % across the full modulation current range, when driving a 25 Ω load. Similarly the voltage undershoot is less than 10 %.

A mark-space monitor is provided through the pins MARKP and MARKN. These may be connected as shown in the application diagram below, with a capacitor across the two outputs and a comparator (or Op-amp) to determine the mark density. Symmetry input (SYM) is available which may be used to control the mark-space ratio.

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DIN DINQ	27 26	AC IN	Data inputs. Internally terminated in 50 Ω to DINT.
DINT	28	ANL IN	Termination voltage for DIN and DINQ. Internally biased to -1.3 V with 750 Ω.
CKIN CKINQ	31 32	AC IN	Clock inputs. Internally terminated in 50 Ω to CKINT. Data is sampled on the positive going edge of the clock (CKIN).
CKINT	30	ANL IN	Termination voltage for CKIN and CKINQ. Internally biased to -1.3 V with 750 Ω.
IOUT IOUTN	13, 14 11, 12	OPEN COLLECTOR	Laser Driver Output (2.5 Gbit/s). IOUT and IOUTN sink a modulation current, which is controlled by the pin VMOD. The polarity of the output depends on the settings of SPOL, see below.
IPRE	19	OPEN COLLECTOR	Pre-bias current output. IPRE sinks a current, which is controlled by the pin VPRE.
VMOD	20	ANL IN	Modulation current control input. The control system is made as a current mirror. VMOD sinks a current proportional to the modulation current. This current is approximately 1/210 times “The modulation current”.
VPRE	16	ANL IN	Pre-bias current control input. The control system is made as a current mirror. VPRE sinks a current proportional to the pre-bias current. This current is approximately 3/500 times “The pre-bias current”.
CKSEL	1	ECL IN	When CKSEL is low data is retimed. Otherwise data is bypassed the retiming. May be connected to rails.
SPOL	9	ECL IN	Data polarity select pin. When SPOL is high, a high level on DIN will cause the IOUT output to sink current, i.e. causing the voltage on IOUT to be low. SPOL is internally pulled to VDD with a 5 k resistor. May be connected to rails.
SYM	24	ANL IN	SYM controls the mark-space ratio of the output. Decreasing the voltage of the SYM pin decreases the pulse width of a current high into the IOUT pin. When SYM is left open the output crossover will be 50%.
MARKP MARKN	7 6	ANL OUT	Mark-space monitor outputs. High impedance CML outputs. The output voltage of the MARKP pin is the same polarity as the voltage on the IOUT pin.
VDD	2, 3, 4, 10, 15	PWR	Ground pins for laser driver part.
VDDR	29	PWR	Ground pin for retiming part.
VEE	5, 8, 23	PWR	Negative supply pins for laser driver part. Package back is VEE.
VEEB	17	PWR	Negative supply pin for pre-bias circuitry.
VEEP	18	PWR	Negative supply pin for output driver.
VEER	25	PWR	Negative supply pin for retiming part.
NC	21, 22		Not Connected.
Heat sink	Package back		Connected to VEE.

Package Pinout

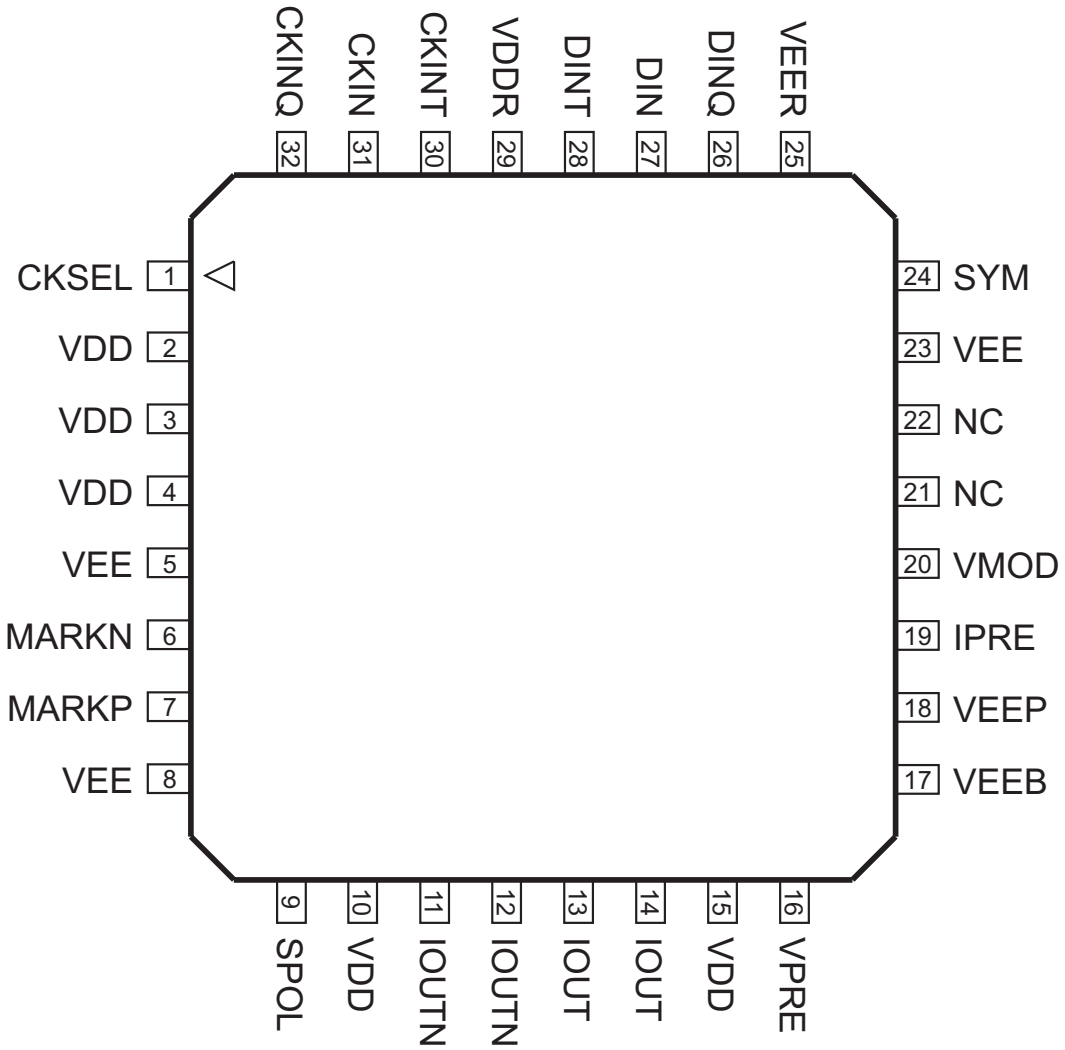


Figure 5. *Package 32 TQFP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Power Supply		-6		0	V
V_O	Applied Voltage (All Outputs)		V_{EE} -0.5		0.5	V
$V_{O\ IOUT/N}$	Applied Voltage IOUT and IOUTN		V_{EE} -0.5		3	V
V_I	Applied Voltage (All Inputs)		V_{EE} -0.5		0.5	V
$I_{I\ AC\ IN}$	Input Current (AC IN)		-1		1	mA
$I_{I\ VMOD}$	Input Current (VMOD)		-2		0.1	mA
$I_{I\ VPRE}$	Input Current (VPRE)	Note 1	-1		1	mA
T_O	Operating Temperature	Case	-40		+110	°C
T_S	Storage Temperature		-65		+125	°C

Note 1: Voltage and/or current should be externally limited to specified range.

DC Characteristics

T_{CASE} = –40 °C to 85 °C, appropriate heat sinking may be required. Device is DC-tested in the temperature range 0 °C to 85 °C, specifications from -40 °C to 0 °C are guaranteed by design, and evaluated during the engineering test.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Power Supply		–5.5		-4.7	V
I_{EE}	Negative Supply Current	V_{EE} = -5.2 V I_{OUT} = 0 A I_{PRE} = 0 A		160	180	mA
P_{DISS}	Power Dissipation	V_{EE} = –5.0 V, I_{OUT} = 0 A, I_{PRE} = 0 A, Note 4		1		W
V_{pp} AN IN	Peak–peak Voltage when Input is Driven Single ended.	V_{VTH} = –1.3 V	150		800	mV
V_C AN IN	Common Mode Voltage Range for Data and Clock Inputs		-1.5		-0.5	V
V_{IH} ECL	ECL Input HI Voltage		-1.1		0	V
V_{IL} ECL	ECL Input LO Voltage		V_{EE}		-1.5	V
V VMOD	Voltage Range for VMOD		V_{EE}		V_{DD}	V
I VMOD	Sink Current into Pin VMOD		-1.3		0	mA
V_{IN} NN	Input Voltage Range for VPRE and SYM		V_{EE}		V_{DD}	V
I_{SINK} NN	Sink Current into pin VPRE and SYM		–1		0	mA
V_{IN} SYM	Input Voltage Range for SYM		V_{EE}		V_{DD}	V
I_{LEAK} SYM	Leakage Current for SYM		–1		1	mA
I_{LEAK} CKSEL,SPOL	Leakage Current for CKSEL and SPOL	-2 < V_I < -0.7	–1		1	mA
V_{LO} MARK	Low Output Voltage for Mark-Space Monitor			–2.0		V
R_O MARK	Output Impedance for Mark-Space Monitor			4.0		kΩ
V_O IPRE	IPRE Output Voltage		–3.0			V
I IPRE	IPRE Current		–60		0	mA
V_O IOUT	IOUT Output Voltage	Note 1	–3.0			V
$I_{Mod,HI}$ IOUT	IOUT High Modulation Current	Note 1, 2	-200		0	mA
$I_{Mod,LO}$ IOUT	IOUT Low Modulation Current	Note 1, 3	-6		1	mA
$I_{OUT}/I_{(VMOD)}$	Modulation Control Current to Modulation Current Gain		200	210	220	

Note 1: R_{LOAD} = 25 Ω to V_{DD} +2 V connected to pin IOUT and IOUTN. Sink current is controlled by the VMOD pin, and may be adjusted in the range as specified. Notice that high modulation current means that the output voltage level is low.
Note 2: The AC parameters are only specified in the range from -200 mA to -70 mA.
Note 3: This is a leakage current. Maximum leakage current is present at max modulation current (i.e. at 200 mA modulation current). The leakage current decreases for smaller modulation currents.
Note 4: Please observe that the heat dissipation in the GD16578 is the sum of contributions from the modulation current, the pre-bias current, and the device's own power consumption. Furthermore, the GD16578's own power consumption depends on the modulation current. Please refer to Figure 6 and example on page 7 .

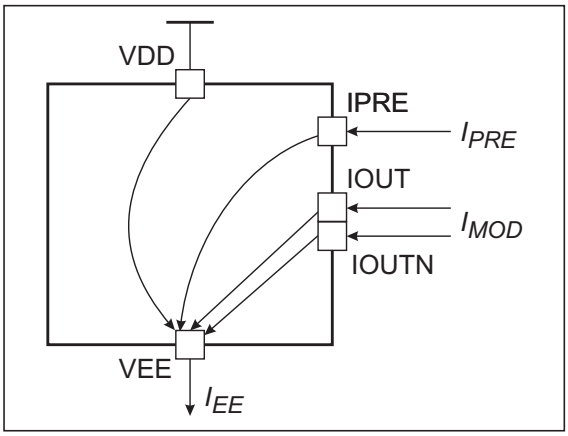


Figure 6. *Equivalent of power dissipation*

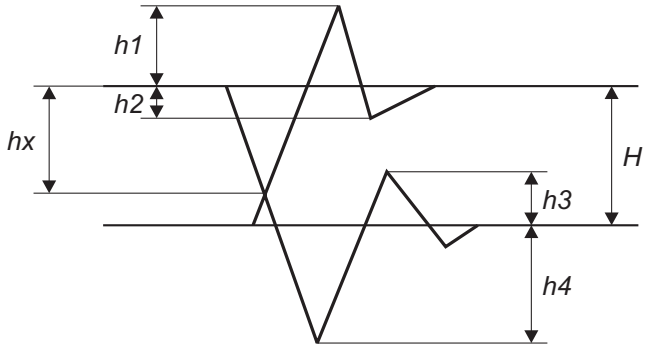
Example:
With V_{EE} = -5,2 V, I_{PRE} = 50 mA from a 25 Ω load to 0 V, and I_{MOD} = 200 mA from bias coils (≈ 0 Ω) connected to 0 V, and a base consumption for the device itself at 160 mA + 0.1 × I_{MOD} the total power equals

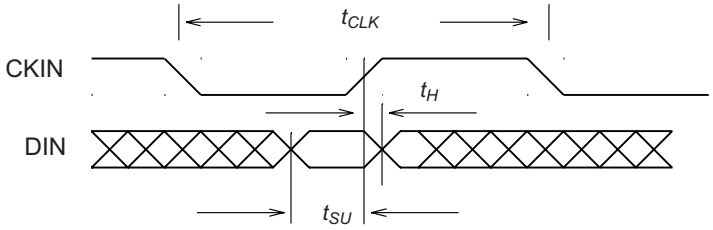
- Prebias:
  (5.2V - (25 Ω × 50 mA)) × 50 mA ≈ 0.2 W
- Modulation current:
  5.2 V × 200 mA ≈ 1.04 W
- Own consumption:
  5.2 V × (160 + 0.1 × 200 mA) » 0.94 W
- This amounts to a total of:
  2.2 W.

Please observe that the heat sink is connected to VEE to obtain best thermal contact between die and heat sink of the package.

AC Characteristics

T_{CASE} = -40 °C to +85 °C, appropriate heat sinking may be required. Device is AC-tested in the temperature range 0 °C to 85 °C, specifications from -40 °C to 0 °C are guaranteed by design, and evaluated during the engineering test.

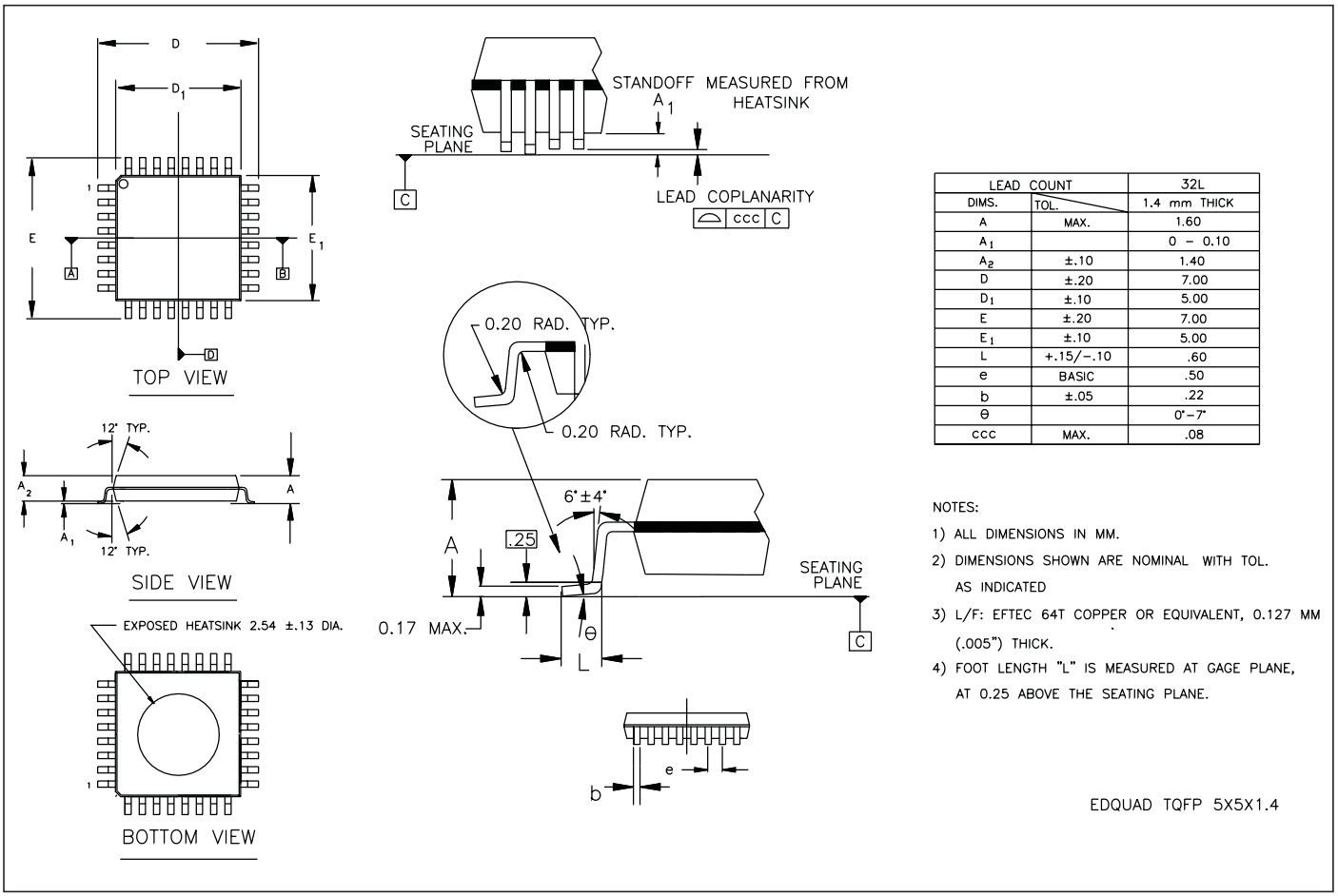




Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
f_{MAX} OUT	Data Output Frequency		2700			Mbit/s
J_{pp} OUT	Added Output Jitter	Note 1, 2, 3			30	ps
t_{RISE} OUT	Output Rise Time	Note 1, 2			125	ps
t_{FALL} OUT	Output Fall Time	Note 1, 2			125	ps
t_{PM}	Phase Margin Clock to Data	Note 2, 4	300			ps
t_{SU}	Data Set-up Time	Note 2, 4	60	30		ps
t_H	Data Hold Time	Note 2, 4	20	5		ps
Δ_{CROSS_OVER}	Output Cross Over Control Range, Δhx/H	Note 1, 2	± 30			%
h1	Ringing h1/H	Note 2, 4			5	%
h2	Ringing h2/H	Note 2, 4			5	%
h3	Ringing h3/H	Note 2, 4			10	%
h4	Ringing h4/H	Note 2, 4			10	%

Note 1: I_{LD} = 140 mA. Rise/Fall times at 20 – 80 % of HI/LO voltage levels.
Note 2: Measured in GIGA evaluation board GD90571. IOUT and IOUTN are terminated to 25 Ω and DC terminated to V_{DD} through a biastee.
Note 3: Added jitter. Measured as a peak-peak jitter value on a sampling oscilloscope in 60 s period. Measured with the data re-timing enabled, and using the retiming clock signal as trigger for the oscilloscope.
Note 4: I_{LD} = 70 mA. Engineering test has shown that this is the worst case corner.

Package Outline



LEAD COUNT		32L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	7.00
D_1	±.10	5.00
E	±.20	7.00
E_1	±.10	5.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ccc	MAX.	.08

Figure 7. *Package 32 pin TQFP EQUAD.*

Device Marking

Figure 8. *Device Marking. Top View.*

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order Number:	Package Type:	Case Temperature Range:
GD16578-32BA	**FAGD1657832BA**	32L TQFP EDQUAD	-40..85 °C

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