TDA9975A

Triple 10-bit video converter and HDMI receiver interface with digital processing

Rev. 01 — 17 March 2008 Product short data sheet

1. General description

The TDA9975A is a combination of an analog video interface and a High-Definition Multimedia Interface (HDMI) receiver. The analog video interface comprises three 10-bit video converters, each converter having triple inputs. The HDMI receiver has two inputs and an embedded High-bandwidth Digital Content Protection (HDCP) keys memory.

The IC converts a YUV (YP_BP_R) analog signal into a YUV (YC_BC_R) or RGB digital signal or converts an RGB analog signal into a RGB or YUV (YC_BC_R) digital signal with a sampling rate up to 81 Msample/s.

The IC supports analog TV resolutions from 480i (720 × 480i at 60 Hz) and 576i (720 × 576i at 50 Hz) to HDTV (up to 1920 × 1080i at 50/60 Hz) and analog PC resolutions from VGA (640 × 480p at 60 Hz) to XGA (1024 × 768p at 75 Hz).

The IC can also convert an HDMI stream (with or without HDCP) into a RGB or YUV (YC_BC_R) digital signal with a sampling rate up to 81 Msample/s.

The YC_BC_R digital output signal can be 4 : 4 : 4 or 4 : 2 : 2 semi-planar format following the ITU-R BT.601 standard or 4 : 2 : 2 ITU-R BT.656 format.

All settings are controllable via the I^2C-bus.

2. Features

- Triple 10-bit Analog-to-Digital Converter (ADC)
- Three independent analog video sources, up to 81 Msample/s
- Two independent HDMI inputs, up to 81 Msample/s
- Analog video sources or HDMI inputs selectable via the I^2C-bus
- Integrated analog composite sync slicer for Sync-On-Green (SOG) or Sync-On-Y (SOY) signal
- Integrated sync separator with automatic detection
- Frame and field detection for interlaced video signal
- Sync timing measurement for format recognition on analog and HDMI inputs
- Three clamps for programming a 10-bit clamping code from 0 to +767 in steps of 1 LSB for RGB and YP_BP_R signals
- Three programmable video gain amplifiers to enable full-scale resolution to be reached
- Amplifier bandwidth of 100 MHz
- Low gain variation with temperature

- PLL controllable via the I^2C-bus, to generate the ADCs, formatter and output clocks which can be locked into a line frequency from 15 kHz to 70 kHz
- Programmable clock phase adjustment in 64-steps to 256-steps for precise sample timing control
- High-bandwidth Digital Content Protection (HDCP); key set in embedded One Time Programmable (OTP) non-volatile memory
- Programmable color space conversion of RGB or YUV input signal into YUV or RGB
- Output format RGB 4 : 4 : 4, YC_BC_R 4 : 4 : 4, YC_BC_R 4 : 2 : 2 semi-planar following the ITU-R BT.601 standard or YC_BC_R 4 : 2 : 2 ITU-R BT.656
- 8-bit, 10-bit or 12-bit output formats selectable via the I^2C-bus
- Integrated downsampling-by-two with selectable filters on the C_B and C_R channels for 4 : 2 : 2 mode
- Internal video and audio pattern generator
- IC controllable via the I^2C-bus; 5 V tolerant and bit rate up to 400 kbit/s
- TTL inputs 5 V tolerant
- LV-TTL outputs
- Power-down mode
- 1.8 V and 3.3 V power supplies
- Lead-free packages

3. Applications

- YUV or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-end TV

4. Quick reference data

Table 1. Quick reference data

$V_{DDA(3V3)}$ = 3.15 V to 3.45 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDI(3V3)}$ = 3.0 V to 3.6 V; $V_{DDO(3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(1V8)}$ = 1.65 V to 1.95 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.3 V; $V_{DDA(1V8)}$ = $V_{DDH(1V8)}$ = $V_{DDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		3.15	3.3	3.45	V
$V_{DDA(1V8)}$	analog supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDH(1V8)}$	HDMI supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDI(3V3)}$	input supply voltage (3.3 V)		3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.65	1.8	1.95	V
$V_{DDO(3V3)}$	output supply voltage (3.3 V)		3.0	3.3	3.6	V

Table 1. Quick reference data *...continued*

$V_{DDA(3V3)}$ = 3.15 V to 3.45 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDI(3V3)}$ = 3.0 V to 3.6 V; $V_{DDO(3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(1V8)}$ = 1.65 V to 1.95 V; $V_{DDH(1V8)}$ = 1.65 V to 1.95 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDI(3V3)}$ = $V_{DDO(3V3)}$ = 3.3 V; $V_{DDA(1V8)}$ = $V_{DDH(1V8)}$ = $V_{DDC(1V8)}$ = 1.8 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P	power dissipation	analog interface; f_s = 81 Msample/s; ADCs current at 100 %	-	1030	-	mW
		HDMI interface; f_s = 78.25 Msample/s	-	680	-	mW
P_{pd}	power dissipation in Power-down mode	powered-up: I^2C-bus, activity detection and HDCP memory	-	40	-	mW
ADCs						
f_s	sampling frequency		12	-	81	MHz
Clock timing input: pin VCLK						
$f_{clk(max)}$	maximum clock frequency	analog interface	-	-	81	MHz
		HDMI interface	-	-	81	MHz
Digital inputs: pins RXA0+, RXA0−, RXA1+, RXA1−, RXA2+, RXA2−, RXAC+, RXAC−, RXB0+, RXB0−, RXB1+, RXB1−, RXB2+, RXB2−, RXBC+ and RXBC−						
$f_{clk(RX)(max)}$	maximum receiver clock frequency		-	-	81	MHz

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9975AHS	SQFP208	plastic shrink quad flat package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT316-1
TDA9975AEL	LBGA256	plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1.05 mm	SOT740-1

5.1 Ordering options

Table 3. Survey of type numbers

Extended type number	Sampling frequency (Msample/s)	Application
TDA9975AHS/8/C1xx	81	customer specific version
TDA9975AEL/8/C1xx	81	customer specific version

6. Block diagram

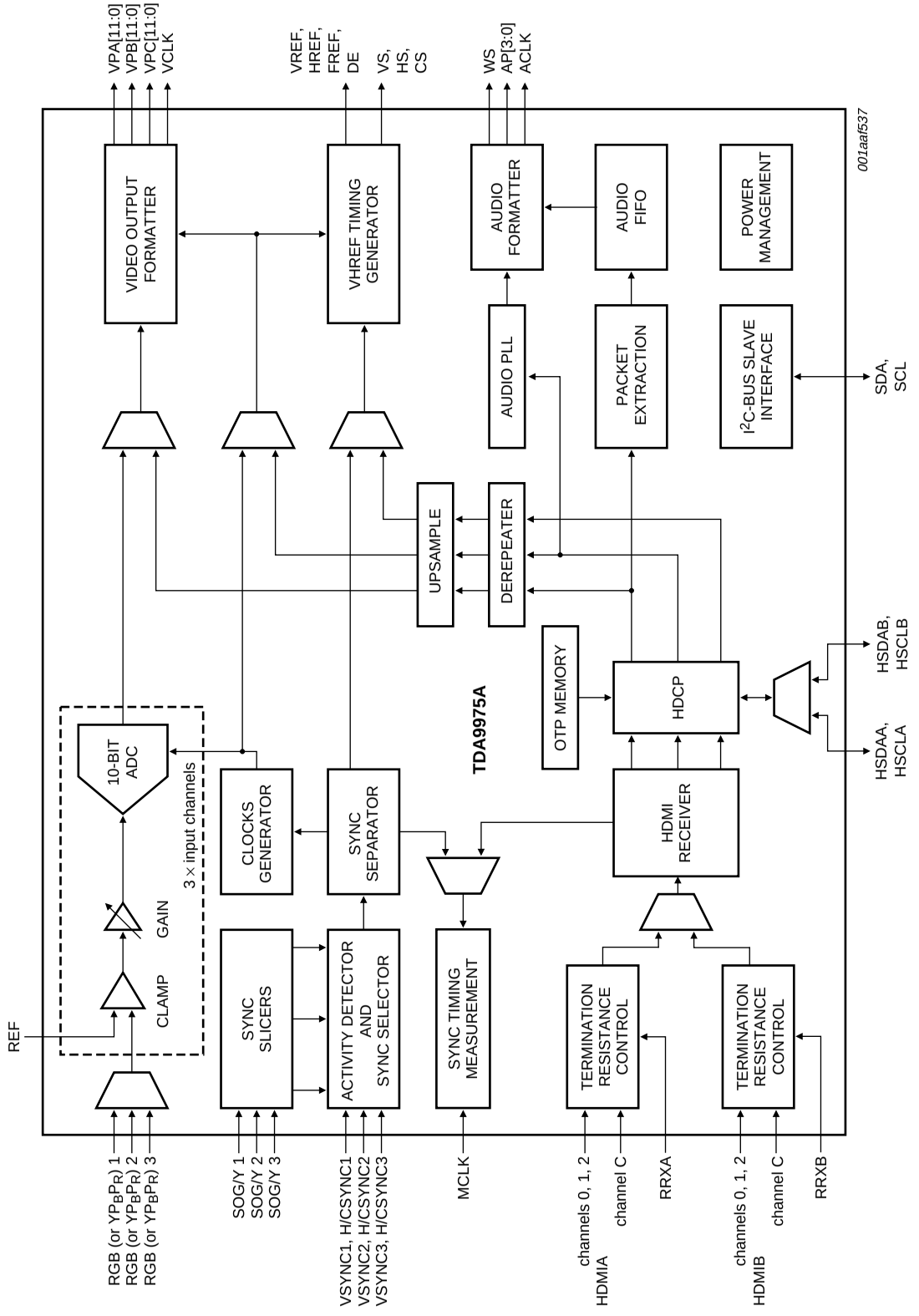

Fig 1. Block diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDx(3V3)}$	supply voltage on all 3.3 V pins		–0.5	+4.6	V
$V_{DDx(1V8)}$	supply voltage on all 1.8 V pins		–0.5	+2.5	V
ΔV_{DD}	supply voltage difference		–0.5	+0.5	V
I_O	output current		-	35	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	125	°C
V_{esd}	electrostatic discharge voltage	human body model	–2000	+2000	V

8. Abbreviations

Table 5. Abbreviations

Acronym	Description
ADC	Analog Digital Converter
HDCP	High-bandwidth Digital Content Protection
HDTV	High-Definition Television
LV-TTL	Low Voltage Transistor-Transistor Logic
PLL	Phase-Locked Loop
RGB	Red Green Blue
TTL	Transistor-Transistor Logic
VGA	Video Graphics Array
XGA	eXtended Graphics Array
YUV	color space used by the NTSC and PAL video systems

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA9975A_SDS_1	20080317	Product short data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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