CY7C130, CY7C130A
CY7C131, CY7C131A

1K x 8 Dual-Port Static RAM

Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1K x 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power: I_{CC} = 110 mA (maximum)
- Fully asynchronous operation
- Automatic power down
- Master CY7C130/130A/CY7C131/131A easily expands data bus width to 16 or more bits using slave CY7C140/CY7C141
- $\overline{BUSY}$ output flag on CY7C130/130A/CY7C131/131A; $\overline{BUSY}$ input on CY7C140/CY7C141
- $\overline{INT}$ flag for port-to-port communication
- Available in 48-pin DIP (CY7C130/130A/140), 52-pin PLCC, 52-pin TQFP
- Pb-free packages available

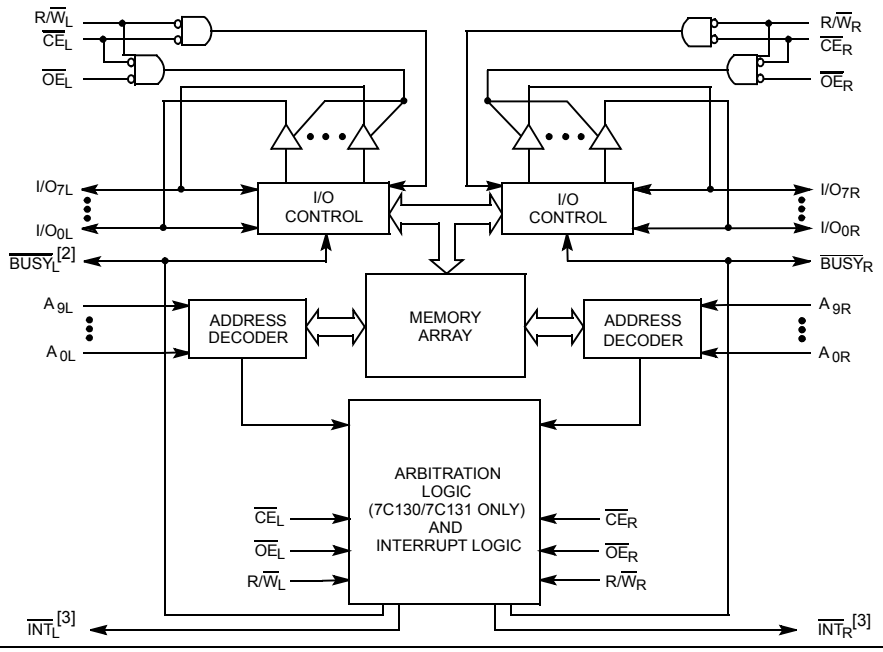
Functional Description

The CY7C130/130A/CY7C131/131A/CY7C140[1] and CY7C141 are high speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/130A/ CY7C131/131A can be used as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multi-processor designs.

Each port has independent control pins; chip enable ($\overline{CE}$), write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port, $\overline{BUSY}$ and $\overline{INT}$. $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{INT}$ is an interrupt flag indicating that data is placed in a unique location (3FF for the left port and 3FE for the right port). An automatic power down feature is controlled independently on each port by the chip enable ($\overline{CE}$) pins.

The CY7C130/130A and CY7C140 are available in 48-pin DIP. The CY7C131/131A and CY7C141 are available in 52-pin PLCC, 52-pin Pb-free PLCC, 52-pin PQFP, and 52-pin Pb-free PQFP.

Logic Block Diagram



Notes
1. CY7C130 and CY7C130A are functionally identical; CY7C131 and CY7C131A are functionally identical.
2. CY7C130/130A/CY7C131/131A (Master): $\overline{BUSY}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{BUSY}$ is input.
3. Open drain outputs: pull-up resistor required.

Pin Configurations

Figure 1. Pin Diagram - DIP (Top View)

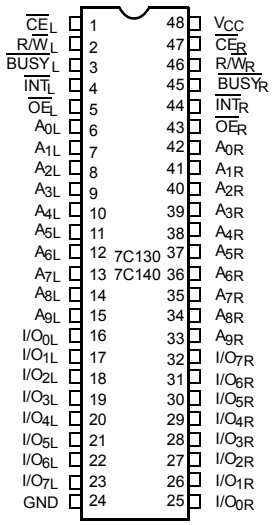


Figure 2. Pin Diagram - PLCC (Top View)

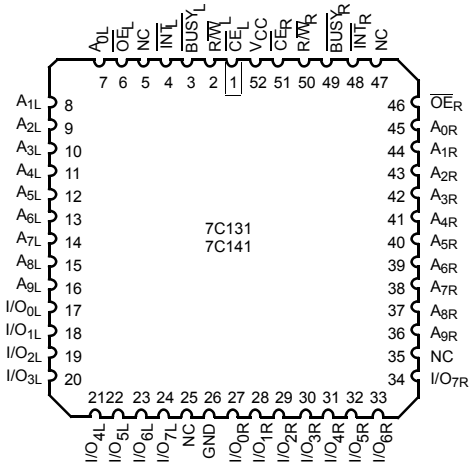
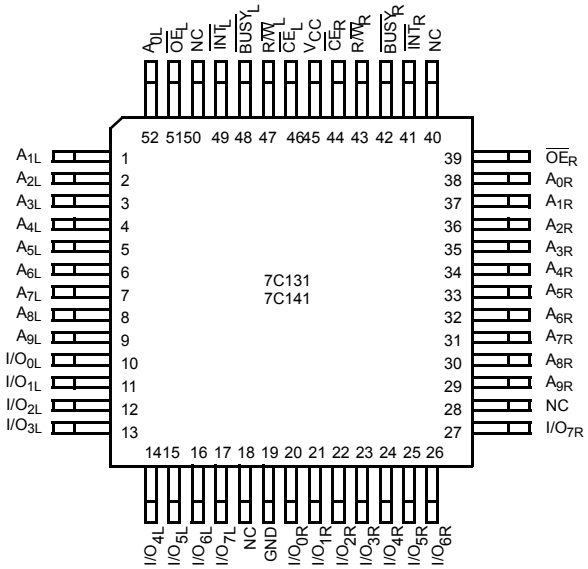


Figure 3. Pin Diagram - PQFP (Top View)



Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–$A_{11/12L}$	A_{0R}–$A_{11/12R}$	Address
I/O_{0L}–$I/O_{15/17L}$	I/O_{0R}–$I/O_{15/17R}$	Data Bus Input/Output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground

Selection Guide

Parameter		7C131-15[4] 7C131A-15 7C141-15	7C131-25[4] 7C141-25	7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55	Unit
Maximum Access Time		15	25	30	35	45	55	ns
Maximum Operating Current	Com'l/Ind	190	170	170	120	120	110	mA
Maximum Standby Current	Com'l/Ind	75	65	65	45	45	35	mA

Shaded areas contain preliminary information.

Note
4. 15 and 25 ns version available only in PLCC/PQFP packages.

Maximum Ratings[5]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24).....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .....–0.5V to +7.0V

DC Input Voltage .....–3.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%
Military[6]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7C131-15[4] 7C131A-15 7C141-15		7C130-30[4] 7C130A-30 7C131-25,30 7C140-30 7C141-25,30		7C130-35,45 7C131-35,45 7C140-35,45 7C141-35,45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[8]			0.5		0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[9, 10]	V_{CC} = Max, V_{OUT} = GND			–350		–350		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	CE = V_{IL}, Outputs Open, f = f_{MAX}[11]	Com'l		190		170		120		110	mA
I_{SB1}	Standby Current Both Ports, TTL Inputs	CE_L and CE_R ≥ V_{IH}, f = f_{MAX}[11]	Com'l		75		65		45		35	mA
I_{SB2}	Standby Current One Port, TTL Inputs	CE_L or CE_R ≥ V_{IH}, Active Port Outputs Open f = f_{MAX}[11]	Com'l		135		115		90		75	mA
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports CE_L and CE_R ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15		15		15	mA
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port CE_L or CE_R ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[11]	Com'l		125		105		85		70	mA

Shaded areas contain preliminary information.

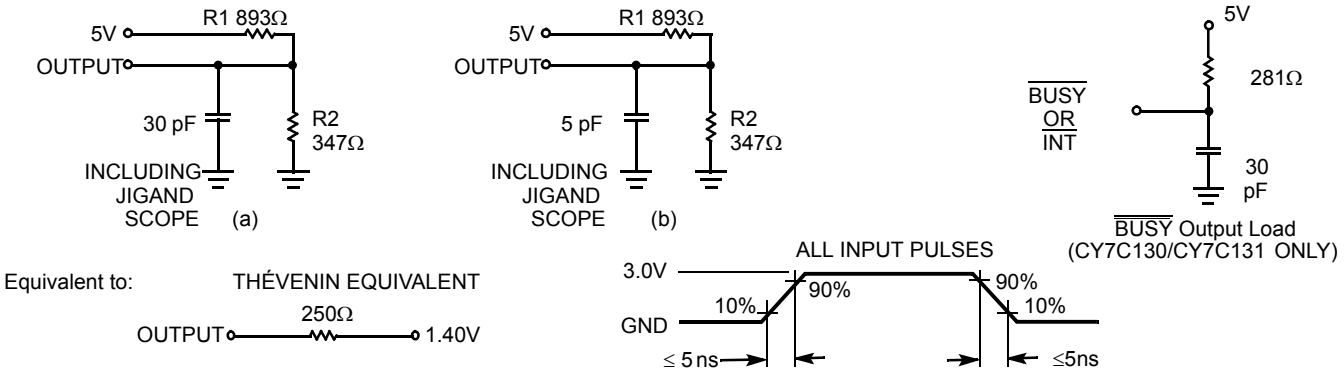
Notes

5. The voltage on any input or I/O pin cannot exceed the power pin during power up.
6. T_A is the "instant on" case temperature
7. See the last page of this specification for Group A subgroup testing information.
8. BUSY and INT pins only.
9. Duration of the short circuit should not exceed 30 seconds.
10. This parameter is guaranteed but not tested.
11. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{RC}$ and using AC Test Waveforms input levels of GND to 3V.

Capacitance[10]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		10	pF

Figure 4. AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[7, 12]

Parameter	Description	7C131-15[4] 7C131A-15 7C141-15		7C130-25[4] 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read Cycle Time	15		25		30		ns
t_{AA}	Address to Data Valid[13]		15		25		30	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[13]		15		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[13]		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10, 14, 15]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10, 14, 15]		10		15		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10, 14, 15]	3		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[10, 14, 15]		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up[10]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down[10]		15		25		25	ns
Write Cycle[16]								
t_{WC}	Write Cycle Time	15		25		30		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		25		ns
t_{AW}	Address Setup to Write End	12		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Setup to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		25		ns
t_{SD}	Data Setup to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[15]		10		15		15	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[15]	0		0		0		ns

Shaded areas contain preliminary information.

Notes
12. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30 pF load capacitance.
13. AC Test Conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
14. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
15. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
16. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and R/$\overline{W}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[7, 12] (continued)

Parameter	Description	7C131-15[4] 7C131A-15 7C141-15		7C130-25[4] 7C131-25 7C140-25 7C141-25		7C130-30 7C130A-30 7C131-30 7C140-30 7C141-30		Unit
		Min	Max	Min	Max	Min	Max	
Busy/Interrupt Timing								
t_{BLA}	BUSY LOW from Address Match		15		20		20	ns
t_{BHA}	BUSY HIGH from Address Mismatch[17]		15		20		20	ns
t_{BLC}	BUSY LOW from CE LOW		15		20		20	ns
t_{BHC}	BUSY HIGH from CE HIGH[17]		15		20		20	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[18]	R/W LOW after BUSY LOW	0		0		0		ns
t_{WH}	R/W HIGH after BUSY HIGH	13		20		30		ns
t_{BDD}	BUSY HIGH to Valid Data		15		25		30	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 19		Note 19		Note 19	ns
t_{WDD}	Write Pulse to Data Delay		Note 19		Note 19		Note 19	ns
Interrupt Timing								
t_{WINS}	R/W to INTERRUPT Set Time		15		25		25	ns
t_{EINS}	CE to INTERRUPT Set Time		15		25		25	ns
t_{INS}	Address to INTERRUPT Set Time		15		25		25	ns
t_{OINR}	OE to INTERRUPT Reset Time[17]		15		25		25	ns
t_{EINR}	CE to INTERRUPT Reset Time[17]		15		25		25	ns
t_{INR}	Address to INTERRUPT Reset Time[17]		15		25		25	ns

Shaded areas contain preliminary information.

Notes
17. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
18. CY7C140/CY7C141 only.
19. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    BUSY on Port B goes HIGH.
    Port B's address is toggled.
    CE for Port B is toggled.
    R/W for Port B is toggled during valid read.

Switching Characteristics Over the Operating Range[7,12]

Parameter	Description	7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid[13]		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[13]		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[13]		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[10, 14, 15]	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[10, 14, 15]		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10, 14, 15]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[10, 14, 15]		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up[10]	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down[10]		35		35		35	ns
Write Cycle[16]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		35		40		ns
t_{AW}	Address Setup to Write End	30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Setup to Write Start	0		0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	25		30		30		ns
t_{SD}	Data Setup to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z[15]		20		20		25	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z[15]	0		0		0		ns
Busy/Interrupt Timing								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[17]		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[17]		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		ns
t_{WB}[18]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 19		Note 19		Note 19	ns
t_{WDD}	Write Pulse to Data Delay		Note 19		Note 19		Note 19	ns
Interrupt Timing								
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[17]		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[17]		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[17]		25		35		45	ns

Switching Waveforms

Figure 5. Read Cycle No. 1[20, 21]

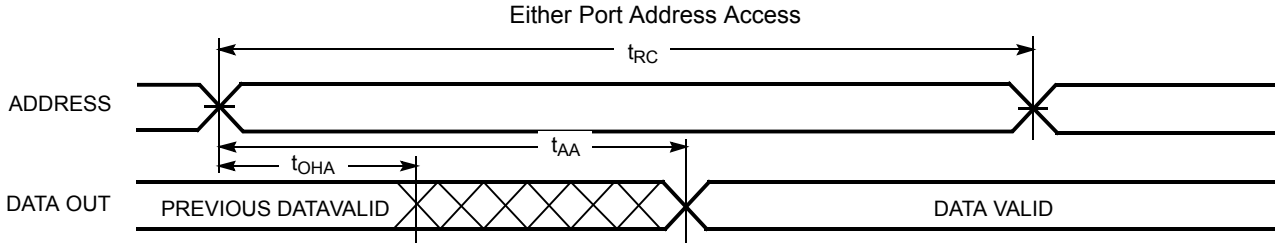


Figure 6. Read Cycle No. 2[20, 22]

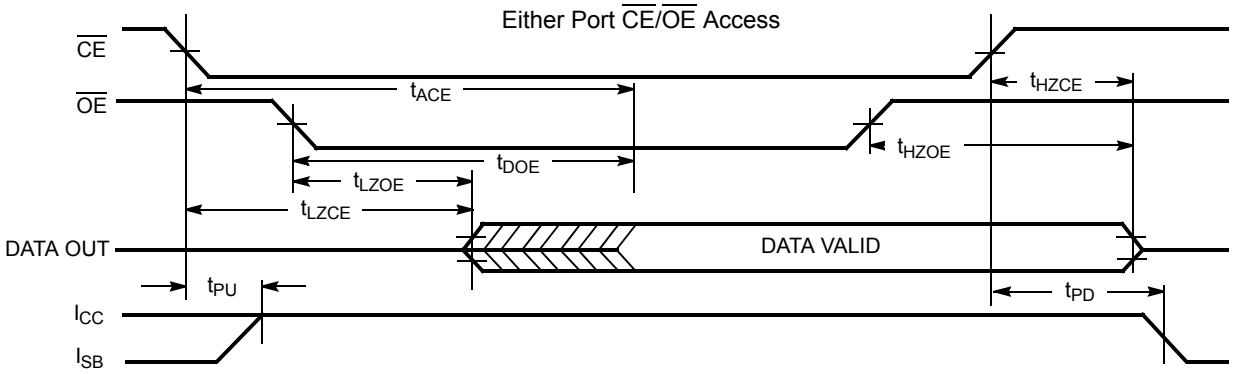
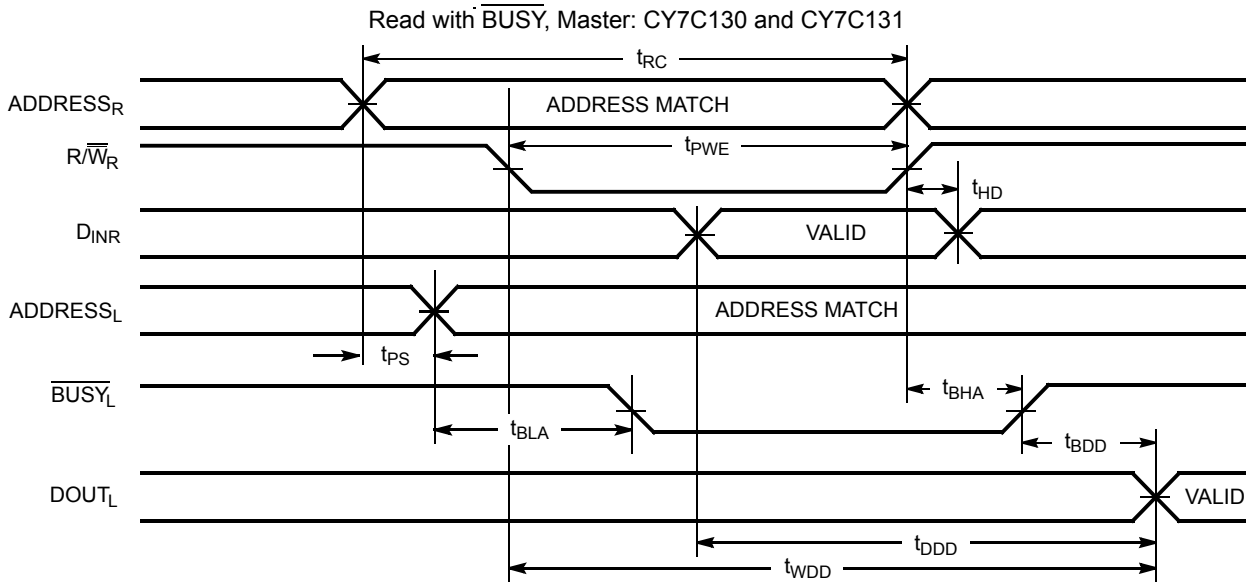


Figure 7. Read Cycle No. 3[21]



Notes
20. R/W is HIGH for read cycle.
21. Device is continuously selected, CE = V_{IL} and OE = V_{IL}.
22. Address valid prior to or coincident with CE transition LOW.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 (OE Three-States Data I/Os—Either Port[16, 23]

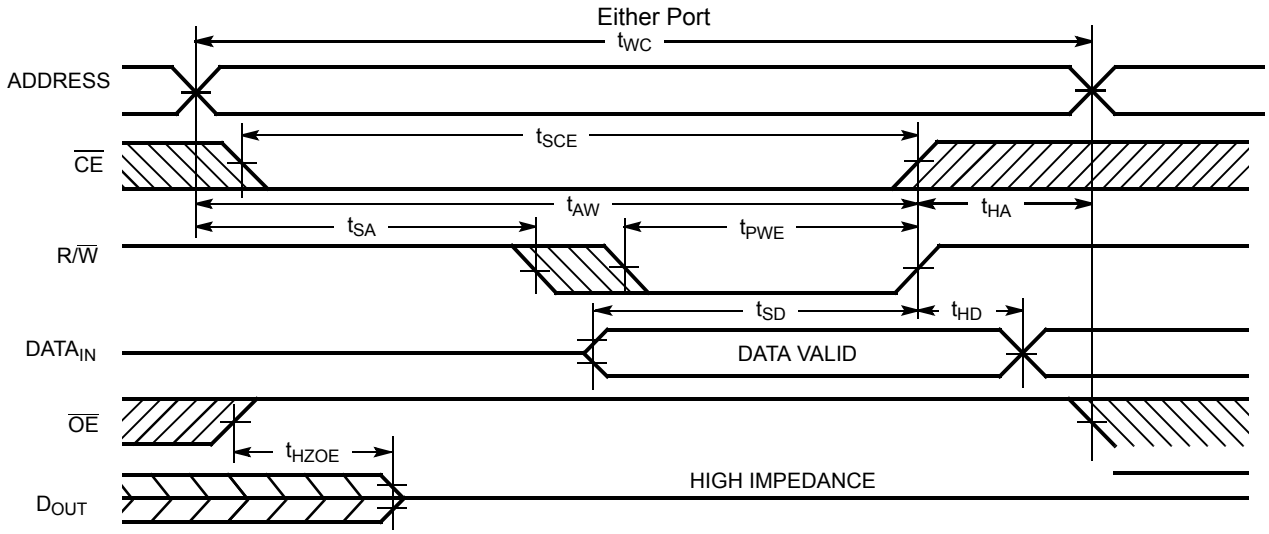
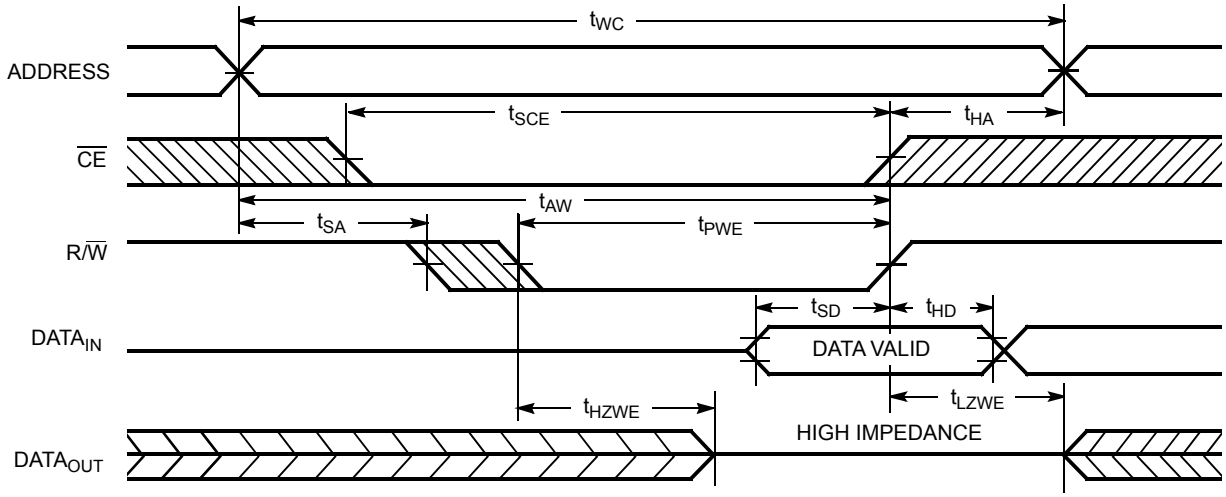


Figure 9. Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os—Either Port)[17, 24]



Notes
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.
24. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 10. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

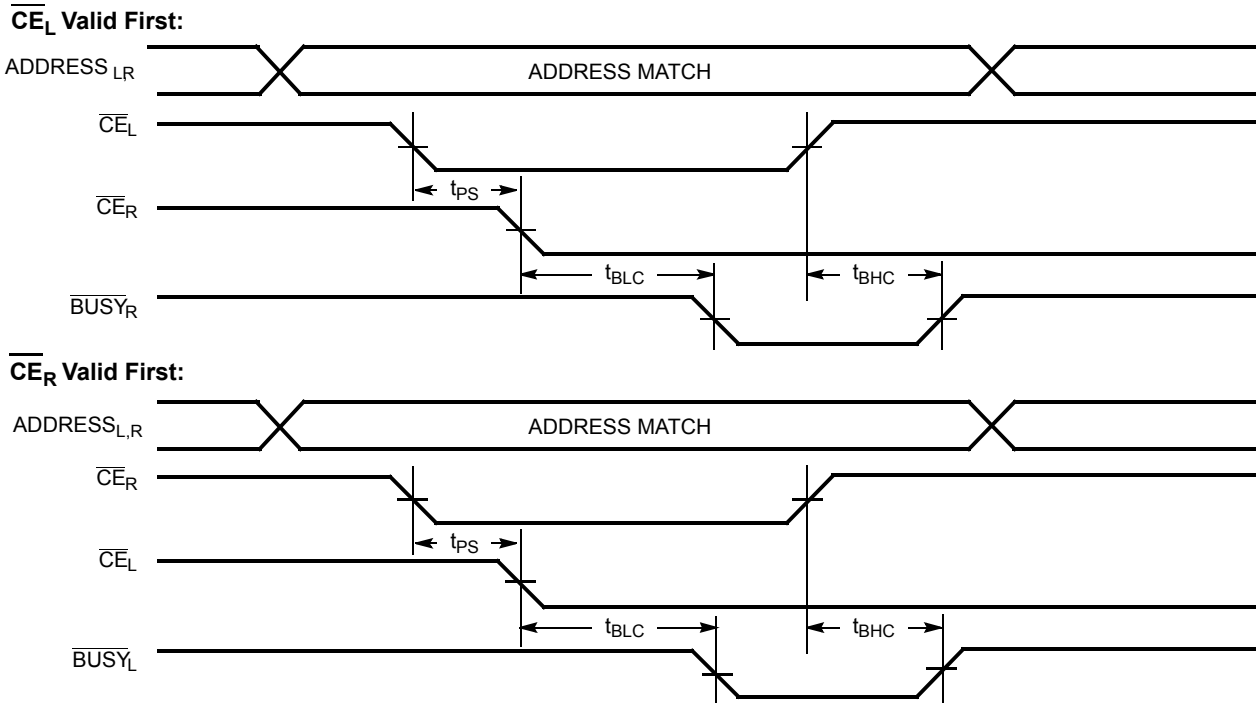
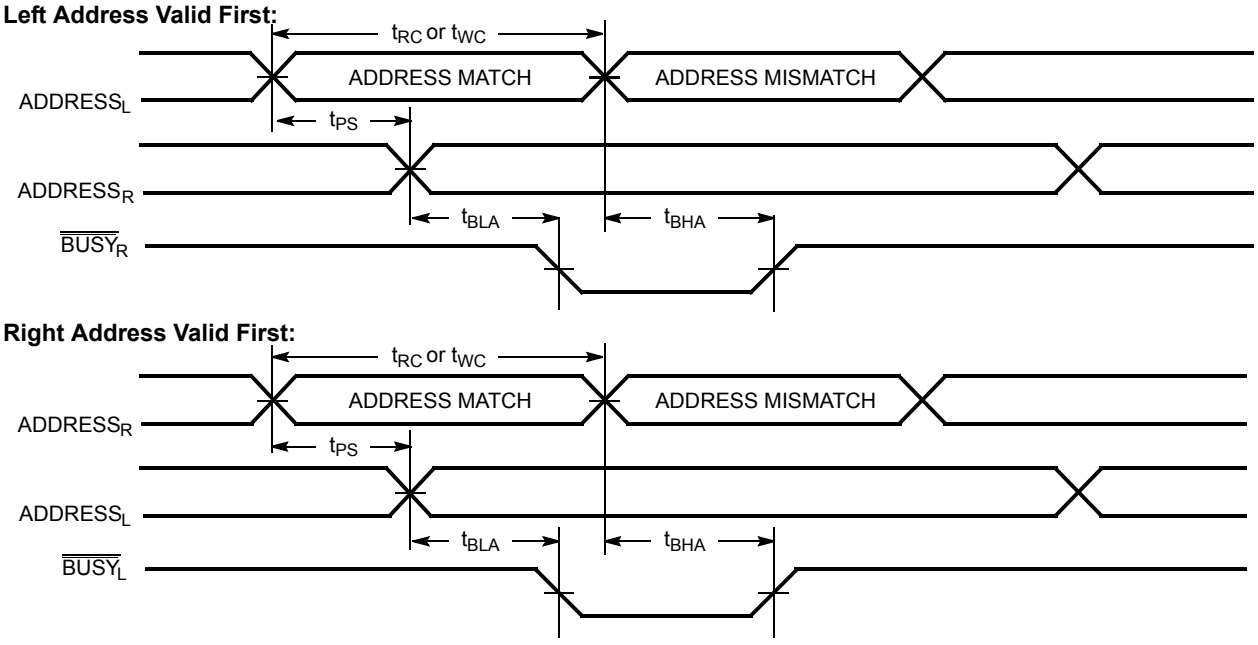


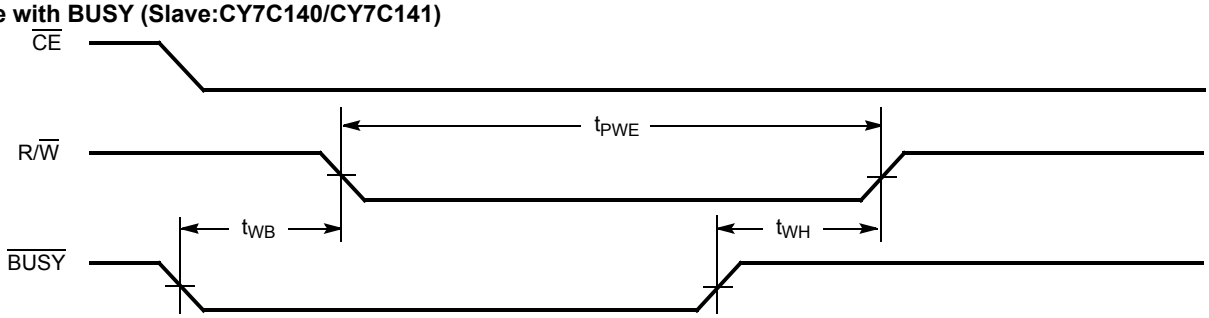
Figure 11. Busy Timing Diagram No. 2 (Address Arbitration)



Switching Waveforms (continued)

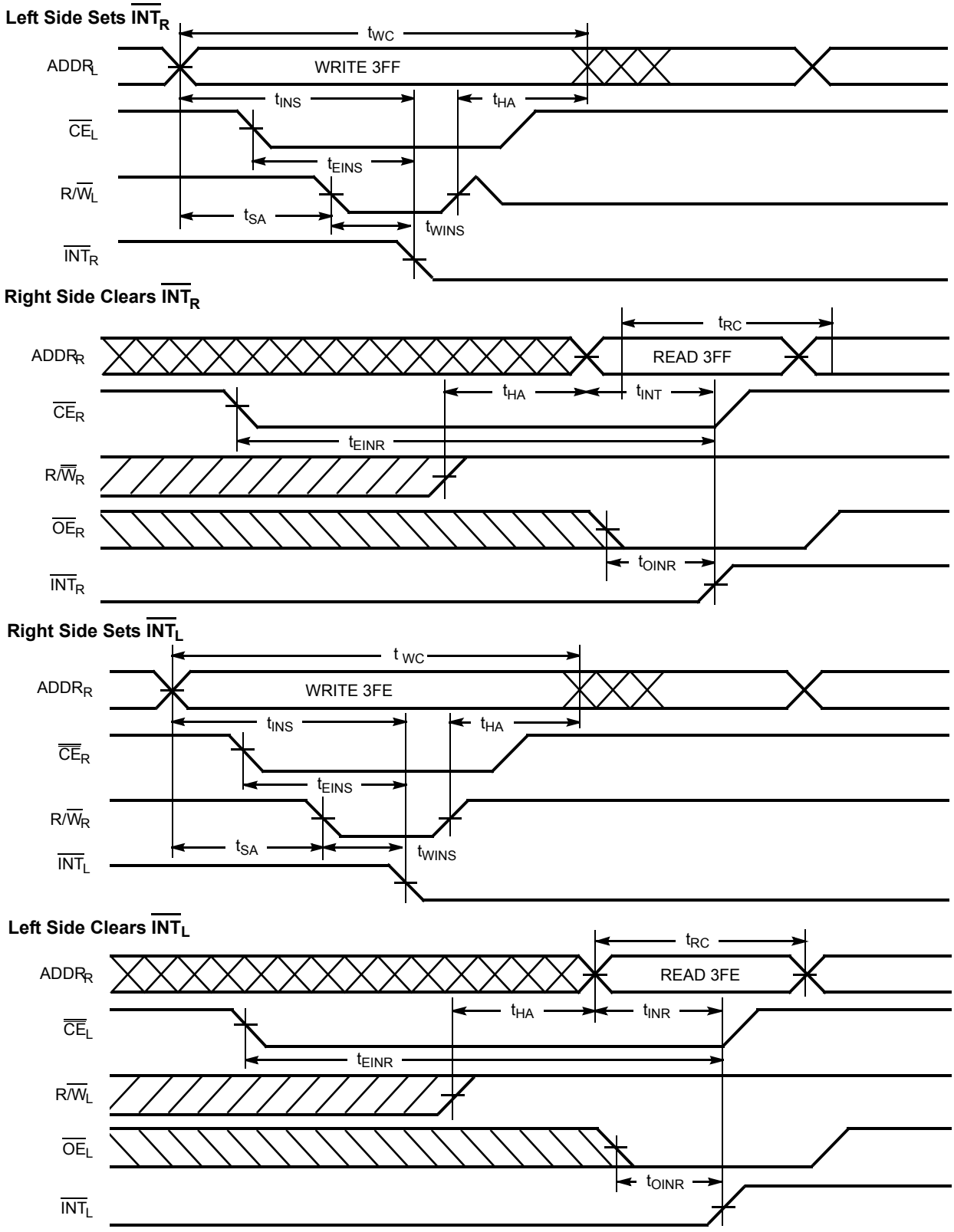
Figure 12. Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (Slave:CY7C140/CY7C141)



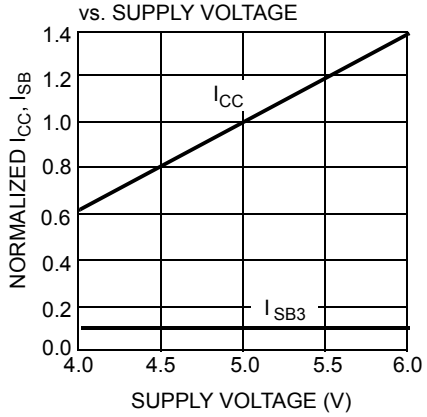
Switching Waveforms (continued)

Figure 13. Interrupt Timing Diagrams

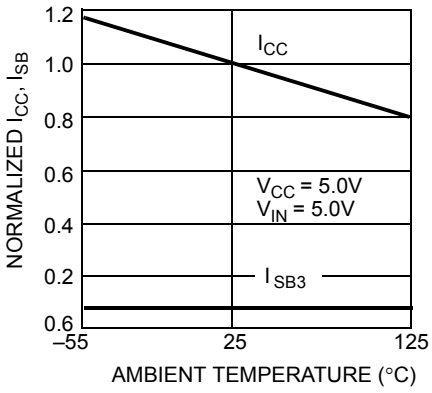


Typical DC and AC Characteristics

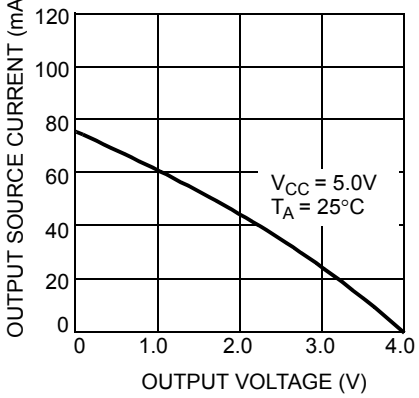
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



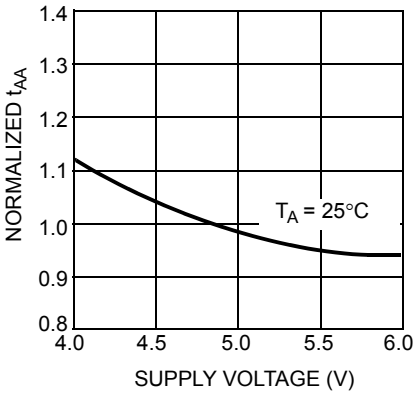
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



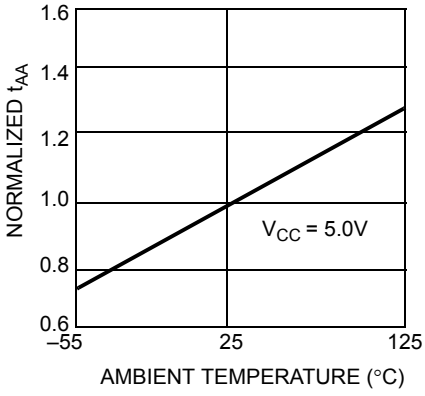
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



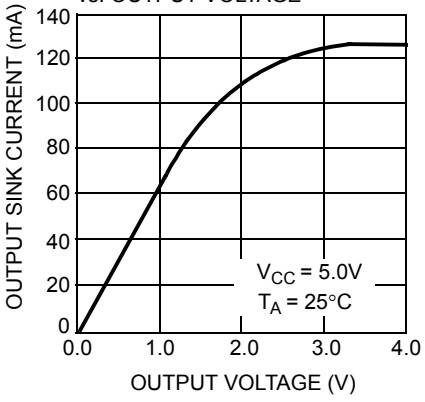
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



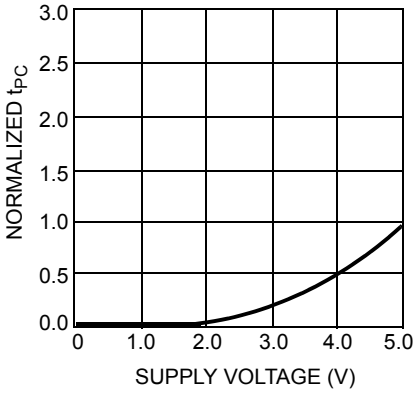
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



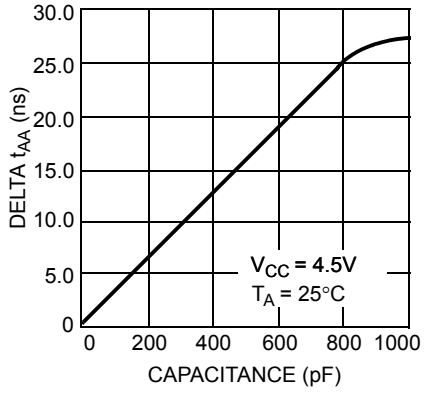
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



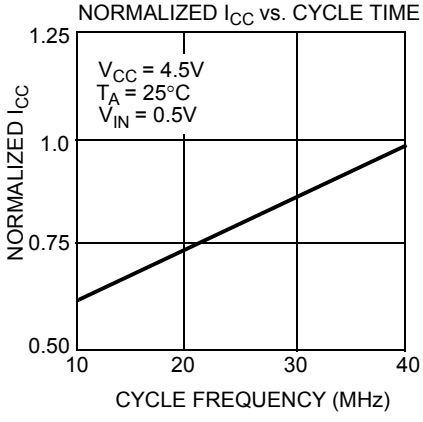
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



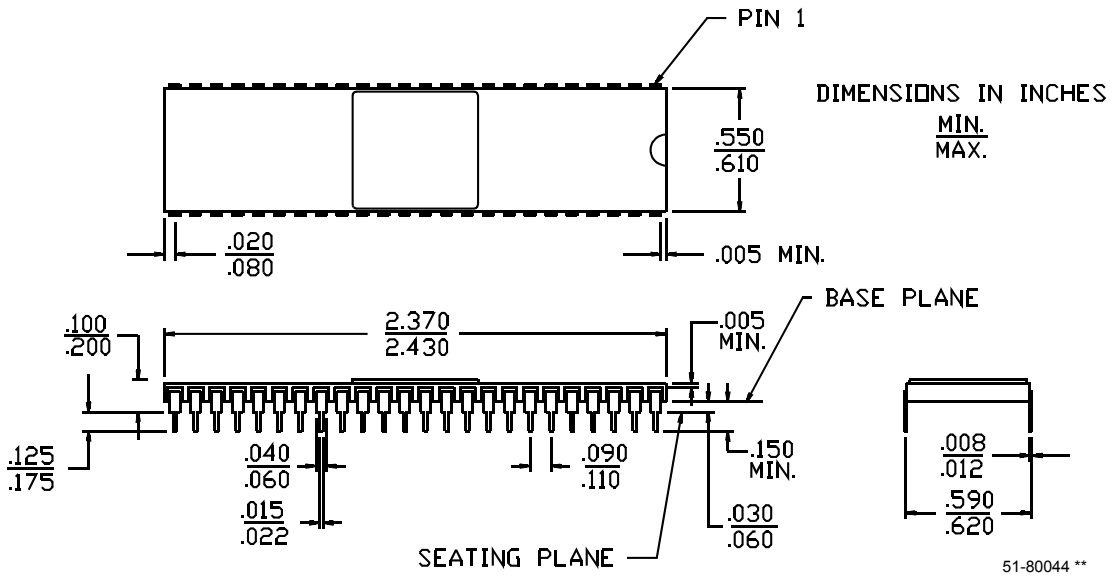
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY7C130-55PC	P25	48-Pin (600 Mil) Molded DIP	Commercial
15	CY7C131A-15JXI	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	Industrial
	CY7C131-15NXI	N52	52-Pin Pb-Free Plastic Quad Flatpack	
25	CY7C131-25JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	Commercial
	CY7C131-25NC	N52	52-Pin Plastic Quad Flatpack	
	CY7C131-25NXC	N52	52-Pin Pb-Free Plastic Quad Flatpack	
55	CY7C131-55JC	J69	52-Pin Plastic Leaded Chip Carrier	Commercial
	CY7C131-55JXC	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	
	CY7C131-55NXC	N52	52-Pin Pb-Free Plastic Quad Flatpack	
	CY7C131-55JXI	J69	52-Pin Pb-Free Plastic Leaded Chip Carrier	Industrial
	CY7C131-55NXI	N52	52-Pin Pb-Free Plastic Quad Flatpack	

Package Diagrams

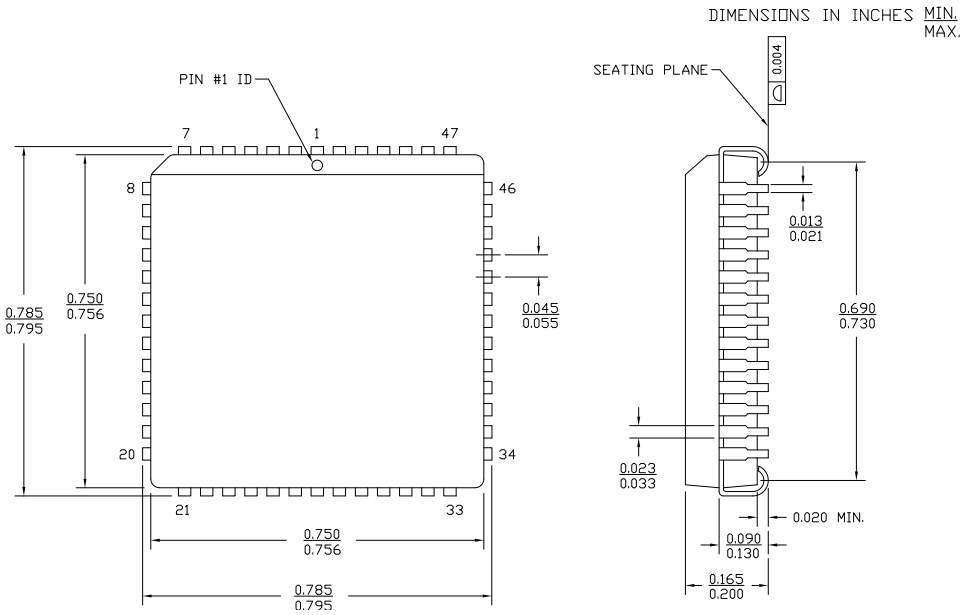
Figure 14. 48-Pin (600 Mil) Sidebraze DIP D26

MIL-STD-1835 D-14 Config. C



Package Diagrams (continued)

Figure 15. 52-Pin Pb-Free Plastic Leaded Chip Carrier J69



51-85004 *B

Package Diagrams (continued)

Figure 16. 48-Pin (600 Mil) Molded DIP P25

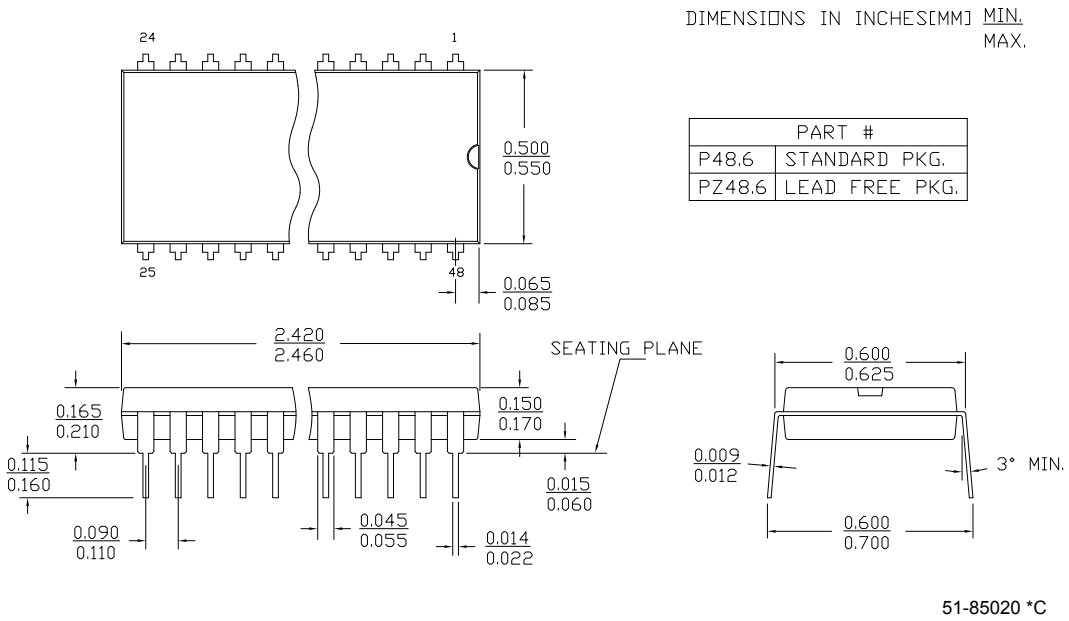
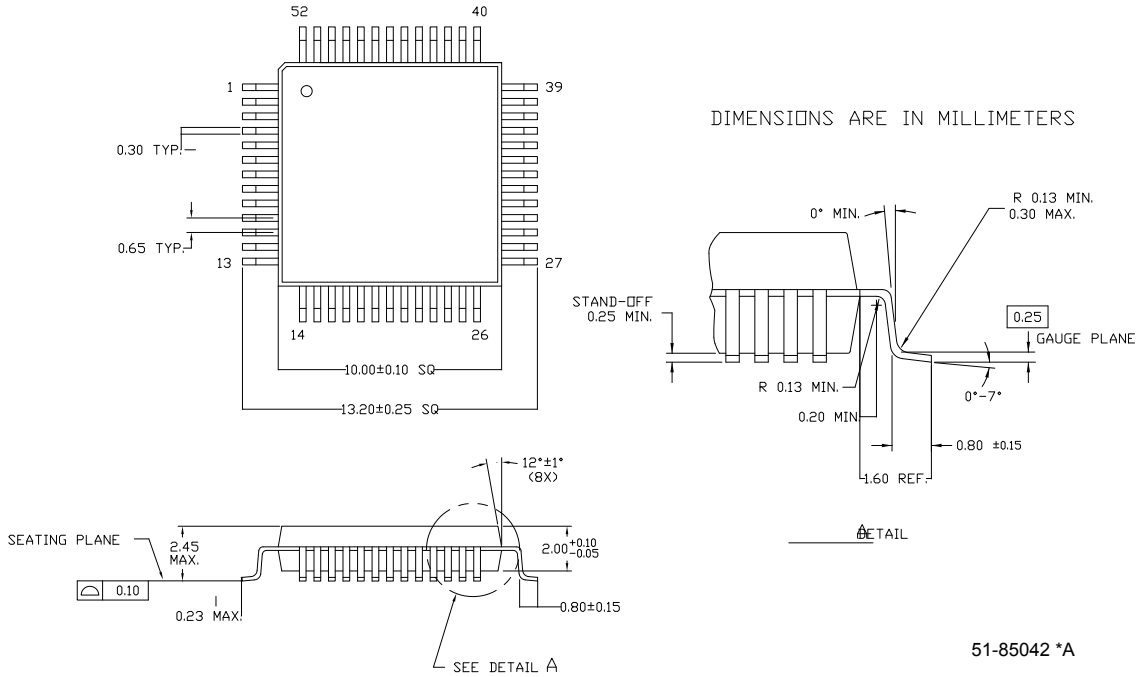


Figure 17. 52-Pin Pb-Free Plastic Quad Flatpack N52



Document History Page

Document Title: CY7C130/CY7C130A/CY7C131/CY7C131A 1K x 8 Dual-Port Static RAM Document Number: 38-06002				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110169	SZV	09/29/01	Change from Spec number: 38-00027 to 38-06002
*A	122255	RBI	12/26/02	Power up requirements added to Maximum Ratings Information
*B	236751	YDT	See ECN	Removed cross information from features section
*C	325936	RUY	See ECN	Added pin definitions table, 52-pin PQFP package diagram and Pb-free information
*D	393153	YIM	See ECN	Added CY7C131-15JI to ordering information Added Pb-Free parts to ordering information: CY7C131-15JXI
*E	2623540	VKN/PYRS	12/17/08	Added CY7C130A and CY7C131A parts Removed military information Updated ordering information table
*F	2897217	RAME	03/22/2010	Updated Ordering Information Updated Package Diagrams

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