128K x 24 Three Megabit 3.3V CMOS Static RAM

IDT7MMV4101

Features

- **High density 3 megabit 3.3V static RAM**
- **Low profile 119 lead, 14mm x 22mm BGA (Ball Grid Array)**
- **Fast RAM access times: 10,12,15ns**
- **Single 3.3V power supply**
- **Multiple Vcc & GND pins for maximum noise immunity**
- **Inputs/outputs directly LVTTL compatible**
- **Commercial (0° C to +70° C) Industrial (-40° C to +85° C) temperature options**
  - *Commercial: 10 / 12 / 15 ns*
  - *Industrial: 12 / 15 ns*

Description

The IDT7MMV4101 is a three megabit static RAM constructed on an multilayer laminate substrate using three 3.3V, 128K x 8 (IDT71V124) static RAMS encapsulated in a Ball Grid Array (BGA).

The IDT7MMV4101 is packaged in a plastic BGA. The BGA configuration allows 119 leads to be placed on a package 14mm by 22mm. At a maximum of 3.5mm high, this low-profile surface mount package is ideal for ultra dense systems.

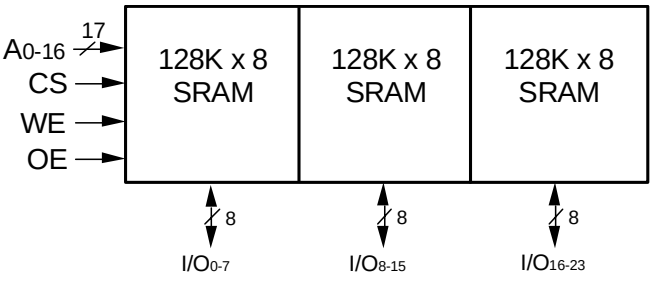
All inputs and outputs of the IDT7MMV4101 are LVTTL compatible and operate from a single 3.3V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Pin Names

I/O_{0-23}	Data Inputs/Outputs
A_{0-16}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground
NC	No Connect

4083 tbl 01

Functional Block Diagram



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Pin Configuration

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
7	NC	NC	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	NC	I/O6	I/O7	I/O8	I/O9	I/O10	I/O11	NC	NC
6	A4	A8	NC	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	NC	A12	A16
5	A3	A7	NC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	NC	A11	A15
4	A2	CS	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	NC	WE	OE
3	A1	A6	NC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	NC	A10	A14
2	A0	A5	NC	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	GND	VCC	NC	A9	A13
1	NC	NC	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	NC	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	NC	NC

Top View

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JANUARY 2003

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	20	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	10	pF

4083 tbl 02

NOTE:
1. This parameter is guaranteed by design but not tested.

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Outputs Disabled	L	H	H	High-Z	Active

4083 tbl 04

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}[1]	Supply Voltage	3.15	3.3	3.6	V
V_{CC}[2]	Supply Voltage	3.0	3.3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3[4]	V
V_{IL}	Input Low Voltage	-0.3[3]	—	0.8	V

4083 tbl 03

NOTES:
1. For 7MMV4101S10BG only.
2. For all speed grades except 7MMV4101S10BG.
3. V_{IL} (min) = –1.5V for pulse width less than 5ns, once per cycle.
4. V_{IH} (max) = V_{CC} + 1.5V for pulse width less than 5ns, once per cycle.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial	Industrial	Unit
V_{CC}	Supply Voltage Relative to GND	-0.5 to +4.6	-0.5 to +4.6	V
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to V_{CC}+0.5	-0.5 to V_{CC}+0.5	V
T_A	Operating Temperature	0 to +70	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-10 to +85	°C
T_{STG}	Storage Temperature	-55 to +125	-55 to +125	°C
I_{OUT}	DC Output Current	50	50	mA

4083 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (V_{CC} = 3.3V ±10%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC},	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

4083 tbl 06

Symbol	Parameter	Test Condition	-10[1] Max.	-12 Max.	-15 Max.	Unit
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Outputs Open	295	275	255	mA
I_{SB}	Standby Power Supply Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, f = f_{MAX}, Outputs Open	95	85	85	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V, f =0 $V_{IN} > V_{CC}$ - 0.2V or < 0.2V	10	10	10	mA

4083 tbl 07

NOTES:
1. Commercial temperature only, Vcc = -5% to +10%.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

4083 tbl 08

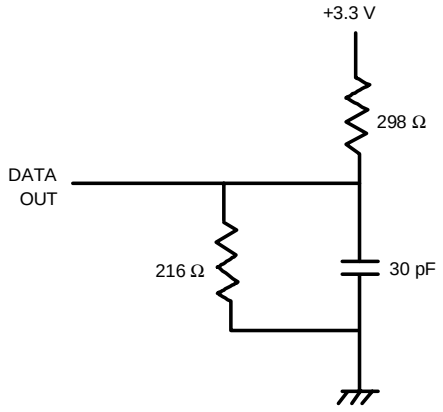

Figure 1. Output Load

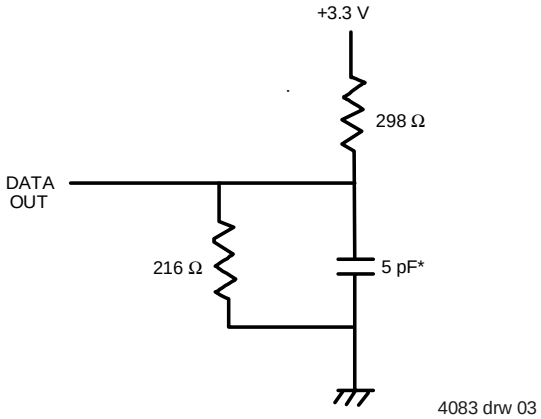

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Figure 2. Output Load
(for t_{OLZ}, t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})
*** Includes scope and jig.**

AC Electrical Characteristics (2)

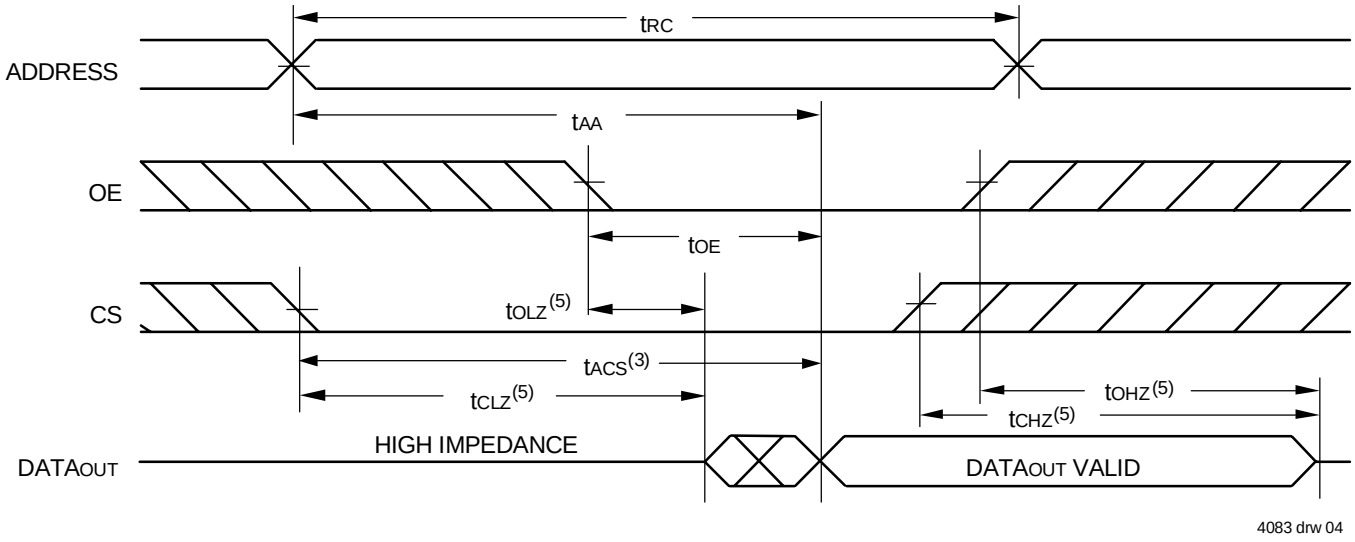
(Vcc = 3.3V ±10%)

Symbol	Parameter	-10(3)		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	4	—	6	—	7	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	5	—	6	—	7	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	8	—	10	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	10	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	5	—	5	—	5	ns
t_{DW}	Data to Write Time Overlap	6	—	6	—	7	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	3	—	3	—	3	—	ns

4083 tbl 09

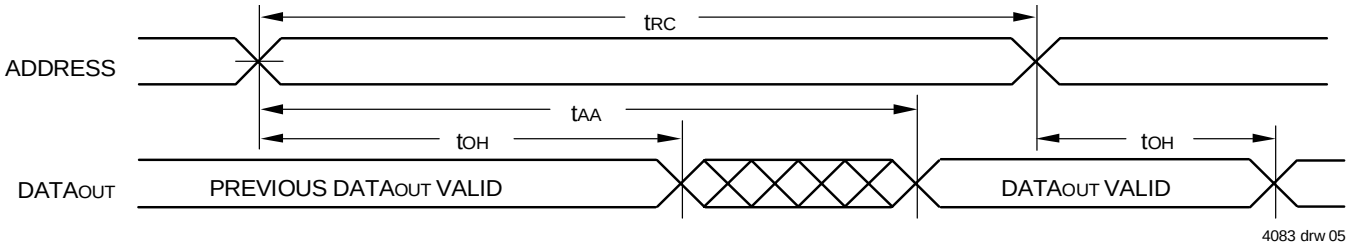
NOTES:
1. This parameter is guaranteed by design but not tested.
2. These specifications are for the individual 71V124 Static RAMs.
3. Commercial temperature only, Vcc = -5% to +10%.

Timing Waveform of Read Cycle No. 1(1)



4083 drw 04

Timing Waveform of Read Cycle No. 2(1,2,4)



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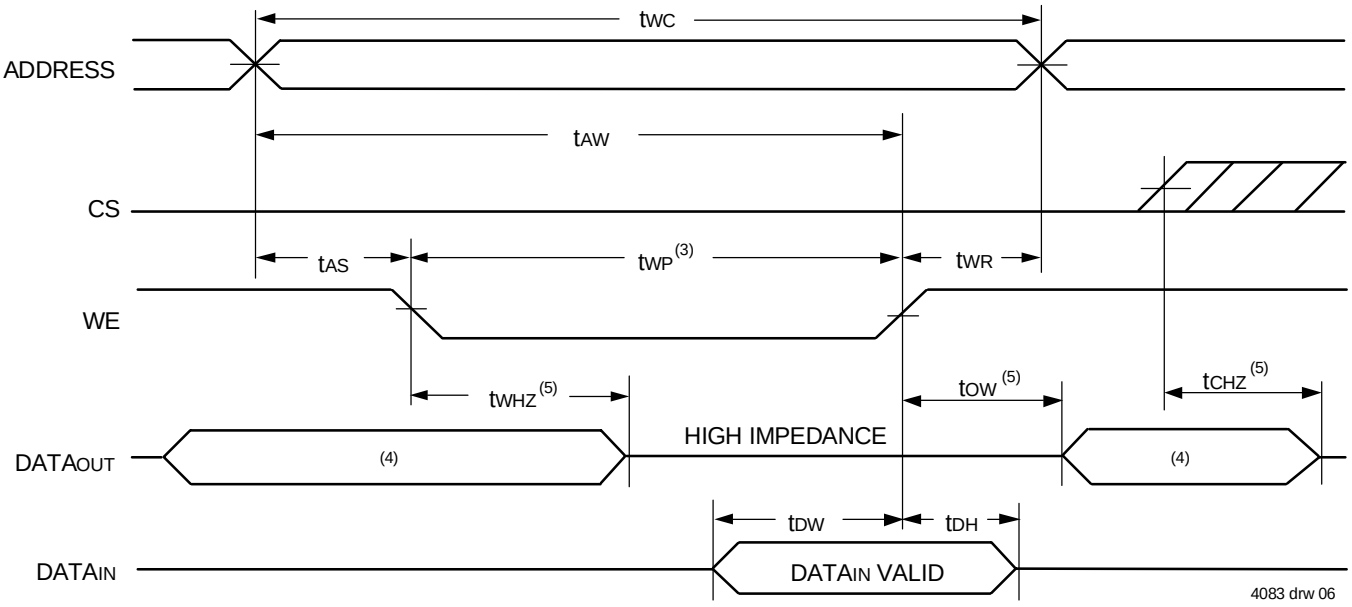
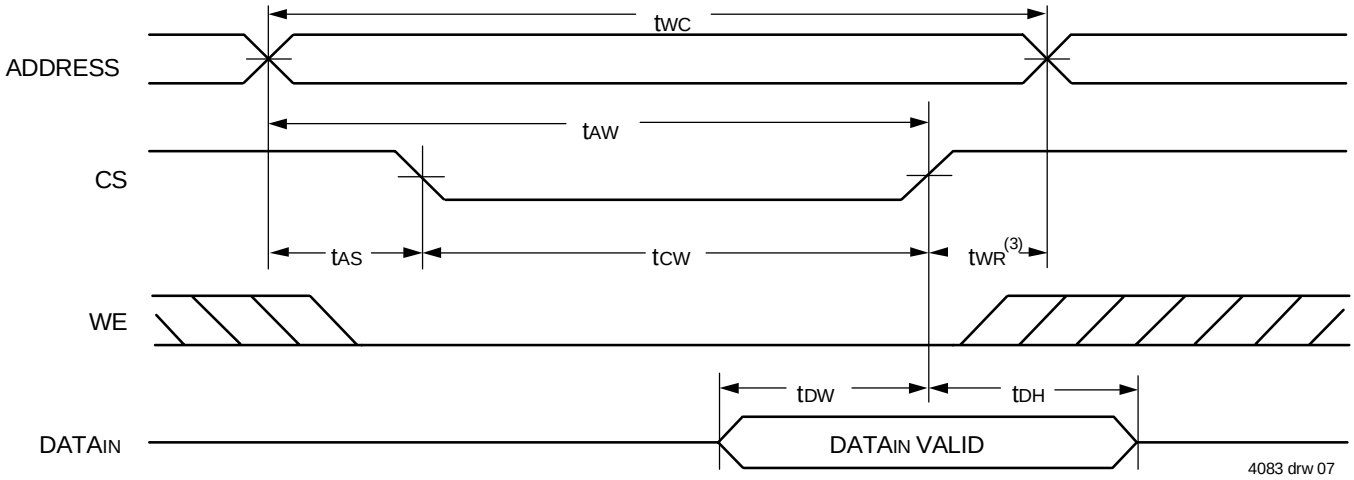
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,4,5)



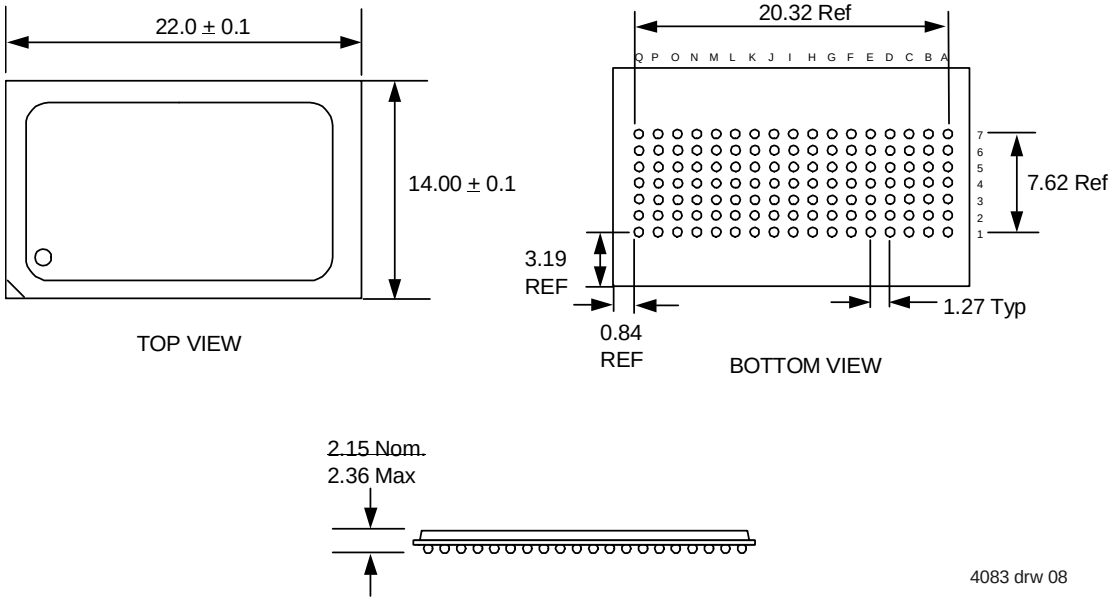
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1, 4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the t_{CW} write period.
5. Transition is measured ±200mV from steady state.

Package Dimensions



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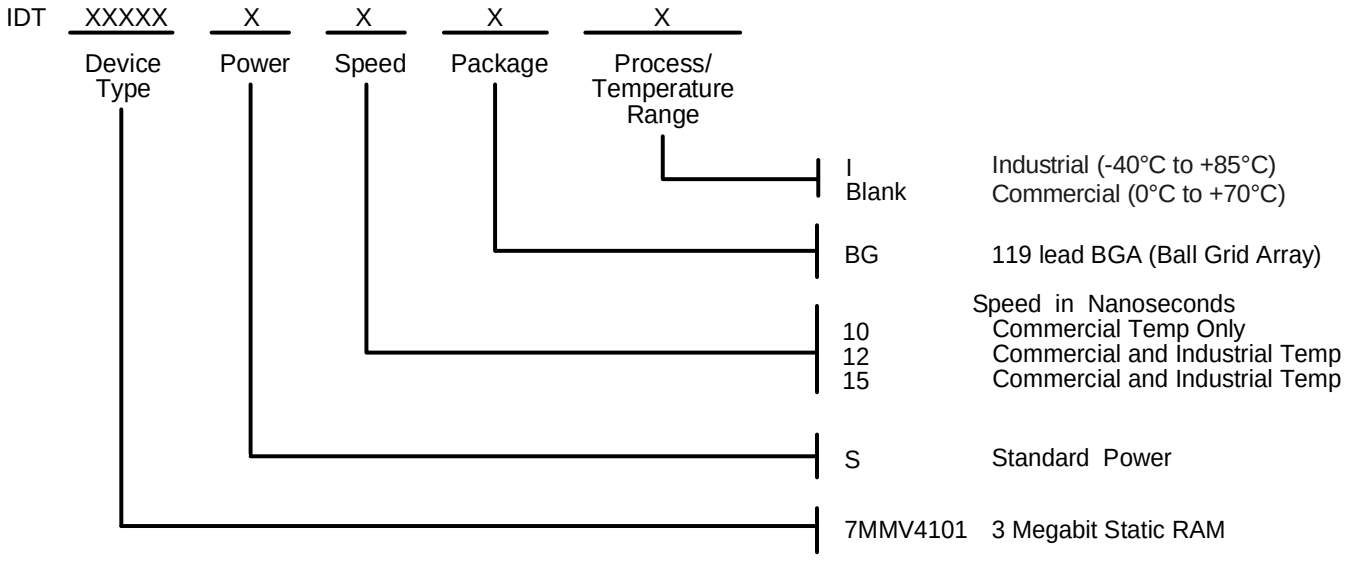
NOTES:
1. All dimensions are in mm.

Ordering Information



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Datasheet History

09/18/00		Add datasheet history
	Pg. 2	Reduce I_{CC}, I_{SB}, and I_{SB1} to reflect K step die shrink
01/07/03		Changed datasheet from Prelininary to final release

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