

## HIGH SPEED 1K X 8 DUAL-PORT STATIC SRAM

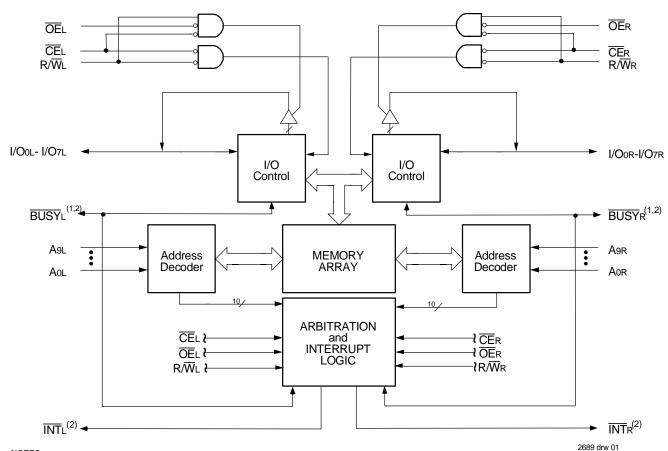
## IDT7130SA/LA IDT7140SA/LA

### **Features**

- High-speed access
  - Commercial: 20/25/35/55/100ns (max.)
  - Industrial: 25/55/100ns (max.)
  - Military: 25/35/55/100ns (max.)
- Low-power operation
  - IDT7130/IDT7140SA
    - Active: 550mW (typ.)
    - Standby: 5mW (typ.)
  - IDT7130/IDT7140LA
    - Active: 550mW (typ.)
    - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-ormore-bits using SLAVE IDT7140

- On-chip port arbitration logic (IDT7130 Only)
- ◆ BUSY output flag on IDT7130; BUSY input on IDT7140
- INT flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation-2V data retention (LA only)
- ◆ TTL-compatible, single 5V ±10% power supply
- ◆ Military product compliant to MIL-PRF-38535 QML
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in 48-pin DIP, LCC and Ceramic Flatpack, 52-pin PLCC, and 64-pin STQFP and TQFP
- Green parts available, see ordering information

## Functional Block Diagram



#### NOTES

- IDT7130 (MASTER): BUSY is open drain output and requires pullup resistor. IDT7140 (SLAVE): BUSY is input.
- 2. Open drain output: requires pullup resistor.

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### Description

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

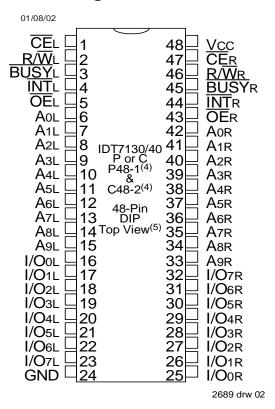
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by  $\overline{\text{CE}}$ , permits the on chip circuitry

of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance tech-nology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, flatpacks, 52-pin PLCC, and 64-pin TQFP and STQFP. Military grade products are manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Pin Configurations<sup>(1,2,3)</sup>



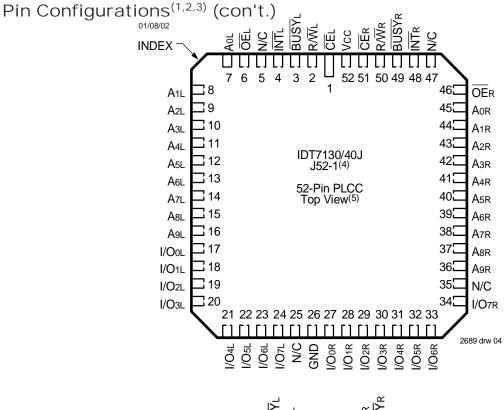
#### NOTES:

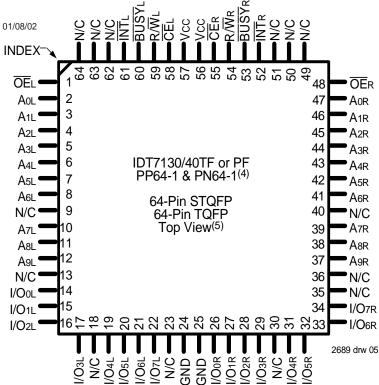
- All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- P48-1 package body is approximately .55 in x .61 in x .19 in. C48-2 package body is approximately .62 in x 2.43 in x .15 in. L48-1 package body is approximately .57 in x .57 in x .68 in. F48-1 package body is approximately .75 in x .75 in x .11 in.
- 4. This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.

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#### NOTES:

- 1. All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- J52-1 package body is approximately .75 in x .75 in x .17 in. PP64-1 package body is approximately 10 mm x 10 mm x 1.4mm. PN64-1 package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.

## Absolute Maximum Ratings(1)

	<u> </u>					
Symbol	Rating	Commercial & Industrial	Military	Unit		
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	>		
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	۰C		
Tstg	Storage Temperature	-65 to +150	-65 to +150	°C		
ЮИТ	DC Output Current	50	50	mA		

#### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may
  cause permanent damage to the device. This is a stress rating only and functional
  operation of the device at these or any other conditions above those indicated in
  the operational sections of the specification is not implied. Exposure to absolute
  maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

## Capacitance (TA = +25°C, f = 1.0MHz)

STQFP and TQFP Packages Only

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
Соит	Output Capacitance	Vout = 3dV	10	pF

### NOTES: 2689 tbl 05

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

# Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
Vн	Input High Voltage	2.2		6.0(2)	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	_	0.8	V

#### NOTES

- 1. VIL (min.)  $\geq$  -1.5V for pulse width less than 10ns.
- 2. VTERM must not exceed Vcc + 10%.

# Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%

#### S:

1. This is the parameter Ta. This is the "instant on" case temperature.

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

			7130SA 7140SA		7130LA 7140LA		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
lu	Input Leakage Current <sup>(1)</sup>	Vcc = 5.5V, $VIN = 0V$ to $Vcc$	_	10	_	5	μA
llo	Output Leakage Current <sup>(1)</sup>	$\frac{V_{CC}}{CE}$ = VIH, VOUT = 0V to VCC	_	10	-	5	μA
Vol	Output Low Voltage (I/Oo-I/O7)	IoL = 4mA	_	0.4	_	0.4	V
Vol	Open Drain O <u>utput</u> Low Voltage (BUSY, INT)	IOL = 16mA		0.5	_	0.5	V
Voh	Output High Voltage	IOH = -4mA	2.4	_	2.4	_	V

#### NOTE:

1. At Vcc ≤ 2.0V leakages are undefined.

2689 tbl 04

2689 tbl 02

2689 tbl 03

# DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range $^{(1,5)}$ (Vcc = 5.0V $\pm$ 10%)

					7140	X20 <sup>©</sup> X20 <sup>©</sup> I Only	7140 Com'	0X25 0X25 I, Ind litary	7140	0X35 0X35 m'l litary	
Symbol	Parameter	Test Condition	Versi	on	Тур.	Max.	Тур.	Max.	Тур.	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CEL and CER = VIL, Outputs Disabled f = fMAX <sup>(3)</sup>	COM'L	SA LA	110 110	250 200	110 110	220 170	110 110	165 120	mA
	(Bull Folis Active)	I = IMAX**/	MIL & IND	SA LA	_	_	110 110	280 220	110 110	230 170	
ISB1	Standby Current (Both Ports - TTL	$\overline{\text{CE}}_L$ and $\overline{\text{CE}}_R$ = VIH $f = \text{fMAX}^{(3)}$	COM'L	SA LA	30 30	65 45	30 30	65 45	25 25	65 45	mA
	Level Inputs)		MIL & IND	SA LA	-		30 30	80 60	25 25	80 60	
ISB2	Standby Current (One Port - TTL	$\overline{CE}$ 'B" = VIL and $\overline{CE}$ 'B" = VIH <sup>(6)</sup> Active Port OutputsDisabled,	COM'L	SA LA	65 65	165 125	65 65	150 115	50 50	125 90	mA
	Level Inputs)	f=fmax <sup>(3)</sup>	MIL & IND	SA LA	11	11	65 65	160 125	50 50	150 115	
ISB3	Full Standby Current (Both Ports -	CEL and CER ≥ Vcc - 0.2V,	COM'L	SA LA	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	30 10	mA
	CMOS Level Inputs)	$V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$ , $f = 0^{(4)}$	MIL & IND	SA LA	_		1.0 0.2	30 10		_	
ISB4	Full Standby Current (One Port -	<u>CE</u> "A" ≤ 0.2V and <u>CE</u> "B" ≥ VCC - 0.2V <sup>(6)</sup>	COM'L	SA LA	60 60	155 115	60 60	145 105	45 45	110 85	mA
	CMOS Level Inputs)	$V$ IN $\geq \overline{V}$ CC - 0.2V or $V$ IN $\leq$ 0.2V Active Port Outputs Disabled, $f = f$ Max $^{(3)}$	MIL & IND	SA LA	-		60 60	155 115	45 45	145 105	

2689 tbl 06a

					7140 Com	0X55 0X55 'I, Ind litary	7140 Com	X100 X100 II, Ind litary		
Symbol	Parameter	Test Condition	Versi	on	Тур.	Max.	Тур.	Max.	Unit	
Icc	Dynamic Operating Current (Both Ports Active)	CEL and CER = VIL, Outputs Disabled $f = fMAX^{(3)}$	COM'L	SA LA	110 110	155 110	110 110	155 110	mA	
	(Boill Poils Active)	I = IMAX <sup>e</sup> /	MIL & IND	SA LA	110 110	190 140	110 110	190 140		
ISB1	Standby Current (Both Ports - TTL Level Inputs)	and $\overline{CE}_R = V_{IH}$ $MAX^{(3)}$	COM'L	SA LA	20 20	65 35	20 20	55 35	mA	
Level inputs)		MIL & IND	SA LA	20 20	65 45	20 20	65 45			
ISB2	Standby Current (One Port - TTL Active Port Outputs Disabled,	COM'L	SA LA	40 40	110 75	40 40	110 75	mA		
	Level Inputs)	f=[MAX <sup>(3)</sup>	MIL & IND	SA LA	40 40	125 90	40 40	125 90		
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	CEL and CER > Vcc - 0.2V,	COM'L	SA LA	1.0 0.2	15 4	1.0 0.2	15 4	mA	
	CMOS Level Inputs) $V_{\text{IN}} \ge V_{\text{CC}} - 0.2V$ or $V_{\text{IN}} \le 0.2V$ , $f = 0^{(4)}$		MIL & IND	SA LA	1.0 0.2	30 10	1.0 0.2	30 10		
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$ 'A" $\leq 0.2V$ and $\overline{CE}$ 'B" $\geq VCC - 0.2V^{(6)}$	COM'L	SA LA	40 40	100 70	40 40	95 70	mA	
	Civios Level Inpuis)	$V$ IN $\geq V$ CC - 0.2 $V$ or $V$ IN $\leq$ 0.2 $V$ Active Port Outputs Disabled, $f = f$ IMAX $^{(S)}$	MIL & IND	SA LA	40 40	110 85	40 40	110 80		

#### NOTES

2689 tbl 06b

- 1. 'X' in part numbers indicates power rating (SA or LA).
- 2. PLCC, TQFP and STQFP packages only.
- 3. At f = fmax, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tcyc, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- 4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
- 5. Vcc = 5V, Ta=+25°C for Typ and is not production tested. Vcc DC = 100 mA (Typ)
- 6. Port "A" may be either left or right port. Port "B" is opposite from port "A".

Data Retention Characteristics (LA Version Only)

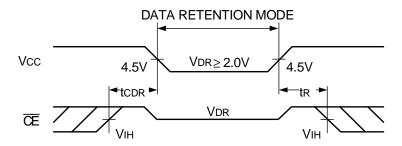
		7130LA/7140LA					
Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit	
VDR	Vcc for Data Retention			2.0	_	_	V
ICCDR	Data Retention Current		MIL. & IND.	_	100	4000	μΑ
		$Vcc = 2.0V$ , $\overline{CE} \ge Vcc -0.2V$	COM'L.	_	100	1500	
tcdr <sup>(3)</sup>	Chip Deselect to Data Retention Time	$Vin \ge Vcc -0.2V$ or $Vin \le 0.2V$		0	_	_	ns
tR <sup>(3)</sup>	Operation Recovery Time			trc(2)	-	_	ns

#### 2689 tbl 07

#### NOTES:

- 1. Vcc = 2V, TA = +25°C, and is not production tested.
- 2. trc = Read Cycle Time
- 3. This parameter is guaranteed but not production tested.

## **Data Retention Waveform**



2692 drw 06

### **AC Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

2689 tbl 08

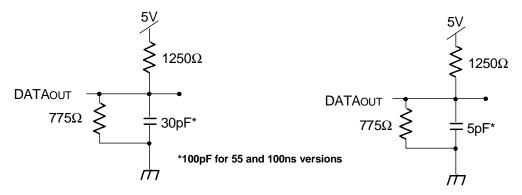


Figure 1. Output Test Load

Figure 2. Output Test Load (for thz, tLz, twz, and tow) \* including scope and jig

2689 drw 07

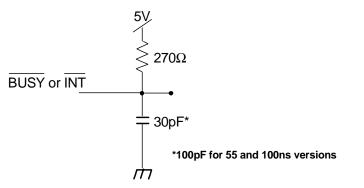


Figure 3. BUSY and INT AC Output Test Load

# AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(3)</sup>

		7130X20 <sup>(2)</sup> 7140X20 <sup>(2)</sup> Com'l Only		7130X25 7140X25 Com'l, Ind & Military		7130X35 7140X35 Com'l & Military			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	
READ CYCLE									
trc	Read Cycle Time	20		25	-	35	_	ns	
taa	Address Access Time	-	20	_	25	_	35	ns	
tace	Chip Enable Access Time	-	20	-	25		35	ns	
taoe	Output Enable Access Time	-	11		12		20	ns	
tон	Output Hold from Address Change	3	1	3	1	3	-	ns	
tLZ	Output Low-Z Time <sup>(1,4)</sup>	0		0	1	0	-	ns	
tHZ	Output High-Z Time <sup>(1,4)</sup>	_	10	_	10	_	15	ns	
<b>t</b> PU	Chip Enable to Power Up Time <sup>(4)</sup>	0		0		0	_	ns	
tPD	Chip Disable to Power Down Time <sup>(4)</sup>	_	20	_	25	_	35	ns	

2689 tbl 09a

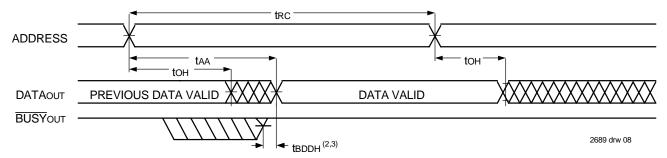
		7130X55 7140X55 Com'l, Ind & Military		7130X100 7140X100 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
READ CYCLE						
trc	Read Cycle Time	55	_	100	١	ns
taa	Address Access Time	_	55	1	100	ns
tace	Chip Enable Access Time	_	55	1	100	ns
taoe	Output Enable Access Time	_	25	_	40	ns
toн	Output Hold from Address Change	3	-	10	1	ns
tLZ	Output Low-Z Time <sup>(1,4)</sup>	5	-	5	1	ns
tHZ	Output High-Z Time <sup>(1,4)</sup>	_	25	_	40	ns
tpu	Chip Enable to Power Up Time (4)	0	_	0	_	ns
tpD	Chip Disable to Power Down Time <sup>(4)</sup>	_	50		50	ns

#### NOTES:

- 1. Transition is measured 0mV from Low or High-impedance voltage Output Test Load (Figure 2).
- 2. PLCC, TQFP and STQFP packages only.
- 3. 'X' in part numbers indicates power rating (SA or LA).
- 4. This parameter is guaranteed by device characterization, but is not production tested.

2689 tbl 09b

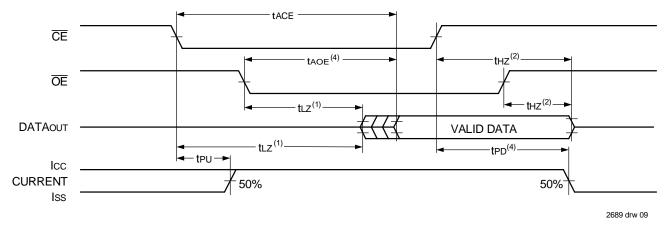
# Timing Waveform of Read Cycle No. 1, Either Side<sup>(1)</sup>



#### NOTES:

- 1.  $R/\overline{W} = V_{IH}$ ,  $\overline{CE} = V_{IL}$ , and is  $\overline{OE} = V_{IL}$ . Address is valid prior to the coincidental with  $\overline{CE}$  transition LOW.
- 2. tbbb delay is required only in the case where the opposite port is completing a write operation to the same the address location. For simultaneous read operations, BUSY has no relationship to valid output data.
- 3. Start of valid data depends on which timing becomes effective last tage, tage, tage, tage, tage, tage.

# Timing Waveform of Read Cycle No. 2, Either Side (3)



#### NOTES

- 1. Timing depends on which signal is asserted last,  $\overline{\text{OE}}$  or  $\overline{\text{CE}}$ .
- 2. Timing depends on which signal is deaserted first,  $\overline{\text{OE}}$  or  $\overline{\text{CE}}$ .
- 3.  $R/\overline{W} = V_{IH}$  and  $\overline{OE} = V_{IL}$ , and the address is valid prior to or coincidental with  $\overline{CE}$  transition LOW.
- 4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

# AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(5)</sup>

		7130X20 <sup>(2)</sup> 7140X20 <sup>(2)</sup> Com'l Only		7130X25 7140X25 Com'l, Ind & Military		7130X35 7140X35 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLI								
twc	Write Cycle Time <sup>(3)</sup>	20	_	25	-	35	_	ns
tew	Chip Enable to End-of-Write	15	_	20	_	30	_	ns
taw	Address Valid to End-of-Write	15	-	20	_	30	_	ns
tas	Address Set-up Time	0	1	0	-	0	-	ns
twp	Write Pulse Width <sup>(4)</sup>	15	1	15	-	25	-	ns
twr	Write Recovery Time	0	-	0	_	0	_	ns
tow	Data Valid to End-of-Write	10	-	12	_	15	_	ns
tHZ	Output High-Z Time <sup>(1)</sup>	_	10		10	_	15	ns
toн	Data Hold Time	0	_	0		0	_	ns
twz	Write Enable to Output in High-Z <sup>(1)</sup>	_	10		10	_	15	ns
tow	Output Active from End-of-Write <sup>(1)</sup>	0	_	0	_	0	_	ns

2689 tbl 10a

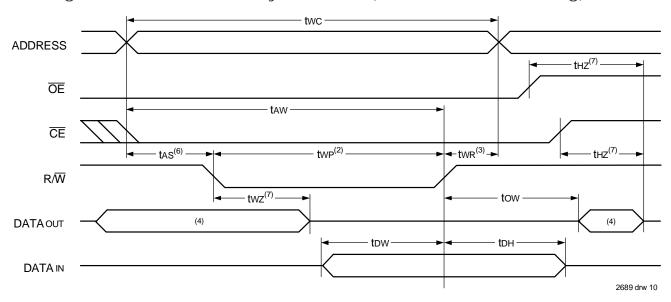
		714 Com	0X55 0X55 'I, Ind litary	7130X100 7140X100 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE						
twc	Write Cycle Time <sup>(3)</sup>	55	_	100	_	ns
tew	Chip Enable to End-of-Write	40	_	90	_	ns
taw	Address Valid to End-of-Write	40	_	90	_	ns
tas	Address Set-up Time	0	_	0	_	ns
twp	Write Pulse Width <sup>(4)</sup>	30	_	55	_	ns
twr	Write Recovery Time	0	_	0	_	ns
tow	Data Valid to End-of-Write	20	_	40	_	ns
tHZ	Output High-Z Time <sup>(1)</sup>	_	25	_	40	ns
tDH	Data Hold Time	0	_	0	_	ns
twz	Write Enable to Output in High-Z <sup>(1)</sup>		25	_	40	ns
tow	Output Active from End-of-Write <sup>(1)</sup>	0		0		ns

### NOTES:

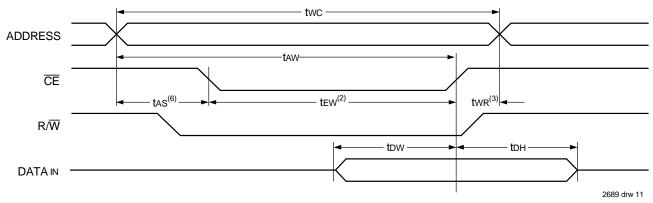
689 tbl 10b

- 1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
- 2. PLCC, TQFP and STQFP packages only.
- 3. For MASTER/SLAVE combination, two = tbaa + twp, since  $R/\overline{W} = VIL$  must occur after tbaa.
- 4. If  $\overline{OE}$  is LOW during a  $R\overline{W}$  controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If  $\overline{OE}$  is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
- 5. 'X' in part numbers indicates power rating (SA or LA).

## Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)(1,5,8)



# Timing Waveform of Write Cycle No. 2, (CE Controlled Timing)(1,5)



#### NOTES

- 1.  $R/\overline{W}$  or  $\overline{CE}$  must be HIGH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of  $\overline{CE} = VIL$  and  $R/\overline{W} = VIL$ .
- 3. two is measured from the earlier of  $\overline{\text{CE}}$  or  $R/\overline{W}$  going HIGH to the end of the write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the CE LOW transition occurs simultaneously with or after the RM LOW transition, the outputs remain in the HIGH impedance state.
- 6. Timing depends on which enable signal (CE or R/W) is asserted last.
- 7. This parameter is determined be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
- 8. If  $\widetilde{OE}$  is LOW during a  $R\overline{W}$  controlled write cycle, the write pulse width must be the larger of two or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If  $\widetilde{OE}$  is HIGH during a  $R\overline{W}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified two.

# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(7)</sup>

		7130X20 <sup>(1)</sup> 7140X20 <sup>(1)</sup> Com'l Only		7130X25 7140X25 Com'l, Ind & Military		7130X35 7140X35 Com'l & Military			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	
BUSY TIMING	G (For MASTER IDT 7130)								
tbaa	BUSY Access Time from Address		20	-	20	—	20	ns	
tbda	BUSY Disable Time from Address		20	_	20	_	20	ns	
<b>t</b> BAC	BUSY Access Time from Chip Enable	_	20	-	20	_	20	ns	
tBDC	BUSY Disable Time from Chip Enable	_	20	_	20	_	20	ns	
twн	Write Hold After BUSY <sup>(6)</sup>	12	_	15	_	20	_	ns	
twdd	Write Pulse to Data Delay <sup>(2)</sup>	_	40	_	50	_	60	ns	
todd	Write Data Valid to Read Data Delay (2)	_	30	_	35	_	35	ns	
taps	Arbitration Priority Set-up Time <sup>(3)</sup>	5	_	5	_	5	_	ns	
tBDD	BUSY Disable to Valid Data <sup>(4)</sup>	_	25	_	35	_	35	ns	
BUS Y INPUT	BUSY INPUT TIMING (For SLAVE IDT 7140)								
twB	Write to BUSY Input <sup>(5)</sup>	0	_	0	_	0	_	ns	
twн	Write Hold After BUSY <sup>(6)</sup>	12	_	15	_	20		ns	
twdd	Write Pulse to Data Delay <sup>(2)</sup>		40	_	50	_	60	ns	
todd	Write Data Valid to Read Data Delay <sup>(2)</sup>	— 30 —			35	_	35	ns	

2689 tbl 11 a

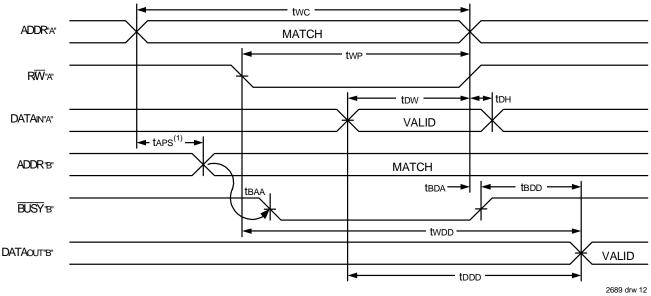
		Com	X55	7130X100 7140X100 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
<b>BUSY</b> TIMING	(For MASTER IDT 7130)					
tbaa	BUSY Access Time from Address]		30	ı	50	ns
tbda	BUSY Disable Time from Address		30	-	50	ns
tBAC	BUSY Access Time from Chip Enable		30	-	50	ns
tBDC	BUSY Disable Time from Chip Enable	_	30	_	50	ns
twн	Write Hold After BUSY <sup>(6)</sup>	20	l	20	_	ns
twdd	Write Pulse to Data Delay <sup>(2)</sup>	_	80	_	120	ns
tood	Write Data Valid to Read Data Delay <sup>(2)</sup>	_	55	-	100	ns
taps	Arbitration Priority Set-up Time <sup>(3)</sup>	5	1	5	_	ns
tBDD	BUSY Disable to Valid Data <sup>(4)</sup>	_	55	-	65	ns
<b>BUSY</b> INPUT 1	TIMING (For SLAVE IDT 7140)					
twB	Write to BUSY Input <sup>(5)</sup>	0	-	0	_	ns
twн	Write Hold After BUSY <sup>(6)</sup>	20	1	20	_	ns
twdd	Write Pulse to Data Delay <sup>(2)</sup>		80	_	120	ns
tooo	Write Data Valid to Read Data Delay <sup>(2)</sup>	_	55	_	100	ns

NOTES:

2689 tbl 11b

- 1. PLCC, TQFP and STQFP packages only.
- 2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port -to-Port Read and BUSY."
- 3. To ensure that the earlier of the two ports wins.
- 4. tbdd is a calculated parameter and is the greater of 0, twdd twp (actual) or tddd tdw (actual).
- 5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'.
- 6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
- 7. 'X' in part numbers indicates power rating (S or L).

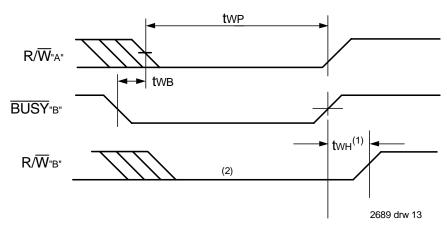
## Timing Waveform of Write with Port-to-Port Read and **BUSY**(2,3,4)



#### NOTES:

- 1. To ensure that the earlier of the two ports wins. tBDD is ignored for slave (IDT7140).
- 2.  $\overline{CE}L = \overline{CE}R = VIL$
- 3.  $\overline{OE} = V_{IL}$  for the reading port.
- 4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

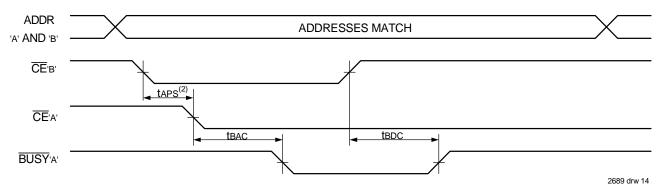
# Timing Waveform of Write with $\overline{\textbf{BUSY}}^{(3)}$



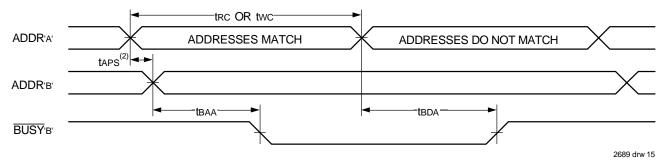
#### NOTES:

- 1. twn must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).
- 2. BUSY is asserted on port "B" blocking R/W"B", until BUSY"B" goes HIGH.
- 3. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is oppsite from port "A".

# Timing Waveform of **BUSY** Arbitration Controlled by **CE** Timing<sup>(1)</sup>



# Timing Waveform by **BUSY** Arbitration Controlled by Address Match Timing<sup>(1)</sup>



#### NOTES:

- 1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 2. If taps is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (7130 only).

# AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(2)</sup>

		7140	X20 <sup>(1)</sup> X20 <sup>(1)</sup> I Only	7140 Com'	0X25 0X25 I, Ind litary	7140 Co	0X35 0X35 m'l litary	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT T	INTERRUPT TIMING							
tas	Address Set-up Time	0	_	0	_	0	-	ns
twr	Write Recovery Time	0	_	0	_	0	1	ns
tins	Interrupt Set Time	_	20	_	25	_	25	ns
tinr	Interrupt Reset Time	_	20		25		25	ns

#### NOTES:

- 1. PLCC, TQFP and STQFP package only.
- 2. 'X' in part numbers indicates power rating (SA or LA).

2689 tbl 12a

# AC Electrical characteristics Over the

Operating Temperature and Supply Voltage Range<sup>(1)</sup>

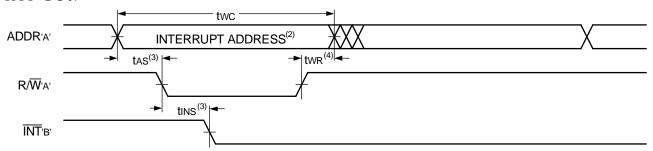
		7140 Com	0X55 0X55 'I, Ind litary	7130 7140 Com & Mi		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT 1	IMING					
tas	Address Set-up Time	0	_	0		ns
twr	Write Recovery Time	0	_	0		ns
tins	Interrupt Set Time	_	45	_	60	ns
tinr	Interrupt Reset Time	_	45	_	60	ns

re.

1. 'X' in part numbers indicates power rating (SA or LA).

# Timing Waveform of Interrupt Mode<sup>(1)</sup>

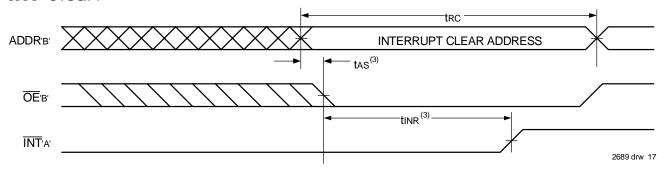
## **INT** Set:



2689 drw 16

2689 tbl 12b

### **INT** Clear:



#### NOTES:.

- 1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 2. See Interrupt Truth Table II.
- 3. Timing depends on which enable signal  $(\overline{CE} \text{ or } R/\overline{W})$  is asserted last.
- 4. Timing depends on which enable signal ( $\overline{CE}$  or  $R/\overline{W}$ ) is de-asserted first.

### **Truth Tables**

## Truth Table I — Non-Contention Read/Write Control<sup>(4)</sup>

Inputs <sup>(1)</sup>				
R/W	CE	ŌĒ	D <sub>0-7</sub>	Function
Х	Н	Х	Z	Port Disabled and in Power-Down Mode, ISB2 or ISB4
Х	Н	Χ	Z	CER = CEL = VH, Power-Down Mode, Isb1 or Isb3
L	L	Х	DATAIN	Data on Port Written into Memory <sup>(2)</sup>
Н	L	L	DATAout	Data in Memory Output on Port <sup>(3)</sup>
Н	L	Н	Z	High Impedance Outputs

NOTES:

2689 tbl 13

- 1. A0L A10L A0R A10R.
- 2. If  $\overline{BUSY} = L$ , data is not written.
- 3. If  $\overline{\text{BUSY}} = L$ , data may not be valid, see two and too timing.
- 4. 'H' = VIH, 'L' = VIL, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

## Truth Table II — Interrupt Flag<sup>(1,4)</sup>

		Left Port			Right Port					
R/WL	ΖĒL	<b>ŌĒ</b> L	A9L-A0L	ĪNTL	R/W̄R	CER	<b>ŌĒ</b> R	A9R-A0R	ĪNTR	Function
L	L	Х	3FF	Х	Х	Х	Х	Х	L <sup>(2)</sup>	Set Right INTR Flag
Х	Х	Х	Х	Х	Х	L	L	3FF	H <sup>(3)</sup>	Reset Right INTR Flag
Х	Х	Х	Х	L(3)	L	L	Х	3FE	Х	Set Left INTL Flag
Х	L	L	3FE	H <sup>(2)</sup>	Х	Х	Х	Х	Х	Reset Left INTL Flag

#### NOTES:

2689 tbl 14

- 1. Assumes  $\overline{BUSY}L = \overline{BUSY}R = VIH$
- 2. If  $\overline{BUSY}L = VIL$ , then No Change.
- 3. If  $\overline{\text{BUSY}}R = \text{VIL}$ , then No Change.
- 4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

# Truth Table III — Address **BUSY** Arbitration

	ln	puts	Out	puts	
ŒL	<b>ՇĒ</b> R	Aol-A9l Aor-A9r	BUS YL(1)	BUSY <sub>R</sub> (1)	Function
Х	Х	NO MATCH	Н	Н	Normal
Н	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit <sup>(3)</sup>

2689 tbl 15

NOTES:

- Pins BUSYL and BUSYR are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). BUSYx outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the BUSYx input internally inhibits writes.
- 'L' if the inputs to the opposite port were stable prior to the address and enable inputs
  of this port. 'H' if the inputs to the opposite port became stable after the address and
  enable inputs of this port. If tAPS is not met, either BUSYL or BUSYR = LOW will
  result. BUSYL and BUSYR outputs can not be LOW simultaneously.
- Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

### **Functional Description**

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by  $\overline{\text{CE}}$ . The  $\overline{\text{CE}}$  controls onchip power down circuitry that permits the respective port to go into a standby mode when not selected ( $\overline{\text{CE}}$  = ViH). When a port is enabled, access to the entire memory array is permitted.

### Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ( $\overline{\text{INTL}}$ ) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the  $\overline{\text{CER}}$  =  $R/\overline{\text{WR}}$  = VIL per Truth Table II. The left port clears the interrupt by access address location 3FE access when  $\overline{\text{CEL}}$  =  $\overline{\text{OEL}}$  = VIL, R/W is a "don't care". Likewise, the right port interrupt flag ( $\overline{\text{INTR}}$ ) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ( $\overline{\text{INTR}}$ ), the right port must access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

## **Busy Logic**

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of  $\overline{\text{BUSY}}$  logic is not required or desirable for all applications. In some cases it may be useful to logically OR the  $\overline{\text{BUSY}}$  outputs together and use any  $\overline{\text{BUSY}}$  indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the  $\overline{\text{BUSY}}$  pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the  $\overline{\text{BUSY}}$  pins HIGH. If desired, unintended write operations can be prevented to a port by tying the  $\overline{\text{BUSY}}$  pin for that port LOW.

The BUSY outputs on the IDT7130 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these

RAMs are being expanded in depth, then the BUSY indication for the resulting array does not require the use of an external AND gate.

# Width Expansion with Busy Logic Master/Slave Arrays

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAMs the  $\overline{\text{BUSY}}$  pin is an output if the part is Master (IDT7130), and the  $\overline{\text{BUSY}}$  pin is an input if the part is a Slave (IDT7140) as shown in Figure 3.

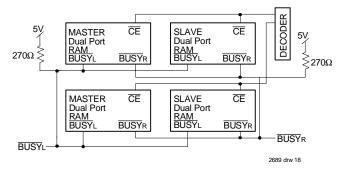
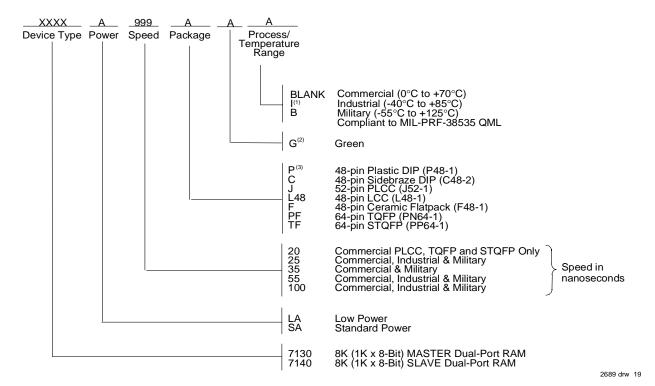


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7130 (Master) and IDT7140 (Slave)RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The  $\overline{BUSY}$  arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a  $\overline{BUSY}$  flag to be output from the master before the actual write pulse can be initiated with either the  $R/\overline{W}$  signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

## Ordering Information



#### NOTES

- 1. Contact your local sales office for industrial temp range for other speeds, packages and powers.
- 2. Green parts available. For specific speeds, pacakges and powers contact your local sales office.
- 3. For "P", plastic DIP, when ordering green package the suffix is "PDG".

# Datasheet Document History

03/15/99:		Initiated datasheet document history
		Converted to newformat
		Cosmetic and typographical corrections
	Pages 2 and 3	Added additional notes to pin configurations
06/08/99:	· ·	Changed drawing format
08/02/99:	Page 2	Corrected package number in note 3
09/29/99:	Page 2	Fixed pin 1 in DIP pin configuration
11/10/99:	Page 1 & 18	Replaced IDT logo
06/23/00:	Page 4	Increased storage temperature parameters
	· ·	Clarified TA parameter
	Page 5	DC Electrical parameters—changed wording from "open" to "disabled"
	Page 10	Changed ±500mV to 0mV in notes
01/08/02:	Page 1	Added Ceramic Flatpack to 48-pin package offerings
	Page 2 & 3	Added date revision to pin configurations
	Page 4, 5, 8, 10,	Removed industrial temp option footnote from all tables
	12,14 & 15	

Continued on page 19

# Datasheet Document History (cont'd)

01/08/02:	Page 5, 8, 10, 12, & 14 Page 5, 8, 10, 12, & 14 Page 18	Added industrial temp for 25ns to DC & AC Electrical Characteristics Removed industrial temp for 35ns to DC & AC Electrical Characteristics Added industrial temp for 25ns and removed industrial temp for 35ns in ordering information Updated industrial temp option footnote
	Page 1 & 19	Replaced IDT тм logo with IDT ® logo
01/11/06:	Page 1	Added green availability to features
	Page 18	Added green indicator to ordering information
	Page 1 & 19	Replaced old IDT тм with new IDT тм logo
04/14/06:	Page 18	Added "PDG" footnote to the ordering information
10/21/08:	Page 18	Removed "IDT" from orderable part number



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