

Memory Module Specification

Hynix T-Die

KVR1066D3Q8R7S/4GHT

4GB 512M x 72-Bit PC3-8500 CL7 Registered w/Parity 240-Pin DIMM

DESCRIPTION:

This document describes ValueRAM's 512M x 72-bit (4GB) DDR3-1066MHz CL7 SDRAM (Synchronous DRAM) registered w/parity, quad-rank memory module, based on thirty-six 128M x 8-bit SDRAMs. The SPD is programmed to JEDEC standard latency 1066MHz timing of 7-7-7 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

FEATURES: DRAM Supported:

JEDEC standard $1.5V \pm 0.075V$ Power Supply

 ∇ VDDQ = 1.5V ± 0.075V

533MHz fCK for 1066Mb/sec/pin

✓ 8 independent internal bank

Programmable CAS Latency: 6,7,8,9,10

Programmable Additive Latency: 0, CL - 2, or CL - 1 clock

Programmable CAS Write Latency(CWL) = 6(DDR3-1066)

8-bit pre-fetch

Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]

Bi-directional Differential Data Strobe

☑ Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)

On Die Termination using ODT pin

On-DIMM thermal sensor (Grade B)

Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE . 95°C

Asynchronous Reset

PCB: Height 1.180" (30.00mm), double sided component

PERFORMANCE:

$ \underline{\mathbf{A}} $	CL(IDD)	7 cycles
$ \sqrt{} $	Row Cycle Time (tRCmin)	50.63ns (min.)
$ \underline{\mathbf{A}} $	Refresh to Active/Refresh Command Time (tRFCmin)	110ns (min.)
$ \underline{\mathbf{A}} $	Row Active Time (tRASmin)	37.5ns (min.)
$ \overline{\mathbf{A}} $	Power	2.625 W (operating)
$ \underline{\mathbf{A}} $	UL Rating	94 V - 0
$ \underline{\checkmark} $	Operating Temperature	0° C to 85° C
	Storage Temperature	-55° C to +100° C

MODULE DIMENSIONS:

