64M X 72 Bits (512MB) 200-Pin DDR SDRAM SO-DIMM with ECC (PC2100)

FEATURES

- PC2100 Compliant
  (DDR266A 133MHz-7.5ns@CL = 2)
  (DDR266B 133MHz-7.5ns@CL = 2.5)
- 200-Pin SO-DIMM form factor
- Auto and self refresh capability
  (8192 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2V V_{DD}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC
- RoHS Compliant, lead-free version available

GENERAL DESCRIPTION

The SL72A8M64M8M-C75xW(U) is a 64M x 72 bit Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Small-Outline Dual In-line Memory Module (SO-DIMM).

The module consists of nine CMOS 16M x 8 bit x 4 bank DDR SDRAMs in 66-pin 400-mil TSOP II packages mounted on a 200-pin glass epoxy substrate.

A serial EEPROM using the two pin I^2C protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.22µF are mounted. Damping resistors are mounted for DQ, DQS, and DM signals. A PLL supplies clocks to the SDRAMs from one clock input.

The module has gold edge connections and is intended for mounting into 200-pin SO-DIMM edge connector sockets keyed for 2.5V.

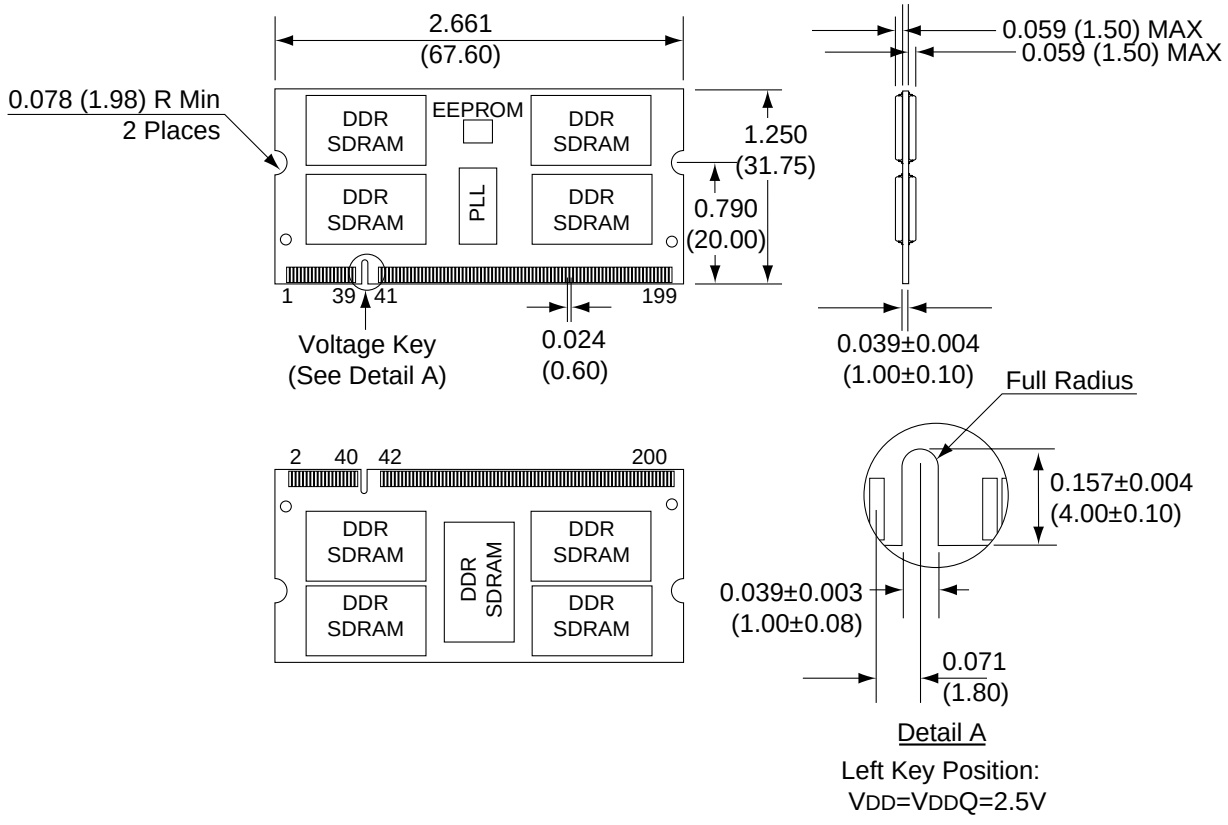
ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72A8M64M8M-C75DW(U)	2	133	2.1 GB/s
SL72A8M64M8M-C75EW(U)	2.5	133	2.1 GB/s

Note: The "U" suffix added to the part number selects the RoHS Compliant, lead-free module.

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ±0.005 (±0.127) unless otherwise specified.



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PIN CONFIGURATION *(* = Not Used; / = Active Low)*

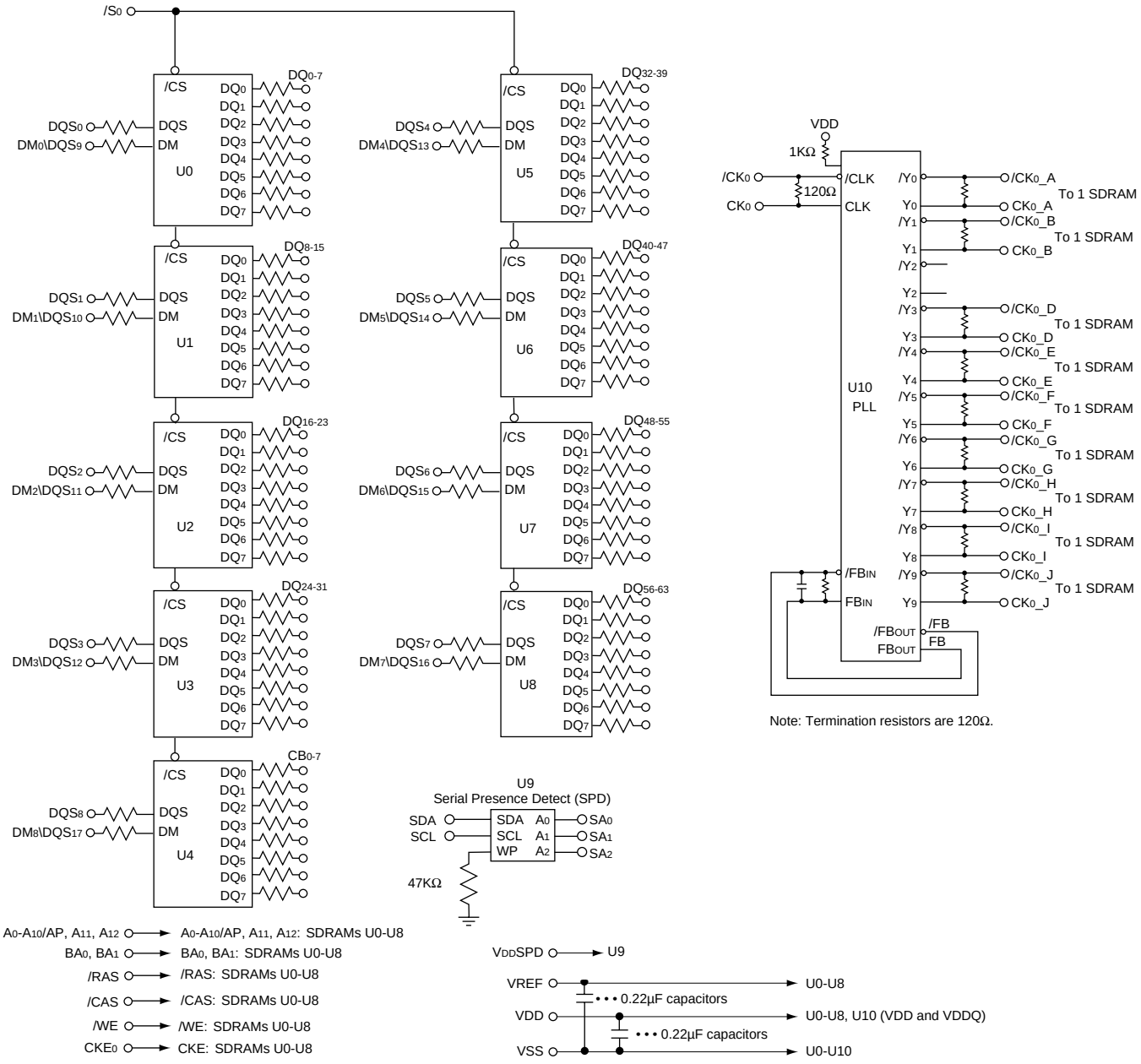
Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A_9	102	A_8	151	DQ_{42}	152	DQ_{46}
3	V_{SS}	4	V_{SS}	53	DQ_{19}	54	DQ_{23}	103	V_{SS}	104	V_{SS}	153	DQ_{43}	154	DQ_{47}
5	DQ_0	6	DQ_4	55	DQ_{24}	56	DQ_{28}	105	A_7	106	A_6	155	V_{DD}	156	V_{DD}
7	DQ_1	8	DQ_5	57	V_{DD}	58	V_{DD}	107	A_5	108	A_4	157	V_{DD}	158	/CK_1*
9	V_{DD}	10	V_{DD}	59	DQ_{25}	60	DQ_{29}	109	A_3	110	A_2	159	V_{SS}	160	CK_1*
11	DQS_0	12	DM_0\DQS_9	61	DQS_3	62	DM_3\DQS_{12}	111	A_1	112	A_0	161	V_{SS}	162	V_{SS}
13	DQ_2	14	DQ_6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ_{48}	164	DQ_{52}
15	V_{SS}	16	V_{SS}	65	DQ_{26}	66	DQ_{30}	115	A_{10}\AP	116	BA_1	165	DQ_{49}	166	DQ_{53}
17	DQ_3	18	DQ_7	67	DQ_{27}	68	DQ_{31}	117	BA_0	118	/RAS	167	V_{DD}	168	V_{DD}
19	DQ_8	20	DQ_{12}	69	V_{DD}	70	V_{DD}	119	/WE	120	/CAS	169	DQS_6	170	DM_6\DQS_{15}
21	V_{DD}	22	V_{DD}	71	CB_0	72	CB_4	121	/S_0	122	/S_1*	171	DQ_{50}	172	DQ_{54}
23	DQ_9	24	DQ_{13}	73	CB_1	74	CB_5	123	DU(A_{13})*	124	DU(BA_2)*	173	V_{SS}	174	V_{SS}
25	DQS_1	26	DM_1\DQS_{10}	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ_{51}	176	DQ_{55}
27	V_{SS}	28	V_{SS}	77	DQS_8	78	DM_8\DQS_{17}	127	DQ_{32}	128	DQ_{36}	177	DQ_{56}	178	DQ_{60}
29	DQ_{10}	30	DQ_{14}	79	CB_2	80	CB_6	129	DQ_{33}	130	DQ_{37}	179	V_{DD}	180	V_{DD}
31	DQ_{11}	32	DQ_{15}	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ_{57}	182	DQ_{61}
33	V_{DD}	34	V_{DD}	83	CB_3	84	CB_7	133	DQS_4	134	DM_4\DQS_{13}	183	DQS_7	184	DM_7\DQS_{16}
35	CK_0	36	V_{DD}	85	DU	86	DU(/RESET)*	135	DQ_{34}	136	DQ_{38}	185	V_{SS}	186	V_{SS}
37	/CK_0	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ_{58}	188	DQ_{62}
39	V_{SS}	40	V_{SS}	89	CK_2*	90	V_{SS}	139	DQ_{35}	140	DQ_{39}	189	DQ_{59}	190	DQ_{63}
41	DQ_{16}	42	DQ_{20}	91	/CK_2*	92	V_{DD}	141	DQ_{40}	142	DQ_{44}	191	V_{DD}	192	V_{DD}
43	DQ_{17}	44	DQ_{21}	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA_0
45	V_{DD}	46	V_{DD}	95	CKE_1*	96	CKE_0	145	DQ_{41}	146	DQ_{45}	195	SCL	196	SA_1
47	DQS_2	48	DM_2\DQS_{11}	97	DU	98	DU	147	DQS_5	148	DM_5\DQS_{14}	197	V_{DD}SPD	198	SA_2
49	DQ_{18}	50	DQ_{22}	99	A_{12}	100	A_{11}	149	V_{SS}	150	V_{SS}	199	V_{DD}ID*	200	DU

Pin Description

Pin Symbol	Pin Function	Pin Symbol	Pin Function
$CK_{(0:2)}$	Clock inputs, positive line	$DQ_{(0:63)}$	Data input/output
/$CK_{(0:2)}$	Clock inputs, negative line	$CB_{(0:7)}$	Data check bits input/output
$CKE_{(0:1)}$	Clock enables	$DM_{(0:8)}$\$DQS_{(9:17)}$	Low data masks/high data strobes
/RAS	Row address strobe	$DQS_{(0:8)}$	Low data strobes
/CAS	Column address strobe	/RESET	Register initialization
/WE	Write enable	V_{DD}	Core power
/$S_{(0:1)}$	Chip selects	V_{SS}	Ground
$A_{(0:9,11:13)}$	Address inputs	V_{REF}	Input/output reference
A_{10}/AP	Address input/Autoprecharge	V_{DD}SPD	SPD power (2.2V to 5.5V)
$BA_{(0:2)}$	SDRAM bank address	V_{DD}ID	V_{DD} identification flag
SCL	SPD clock input		
SDA	SPD data input/output	DU	Don't Use
$SA_{(0:2)}$	SPD address		

FUNCTIONAL BLOCK DIAGRAM



Note: Termination resistors are 120Ω.

Notes: 1. Unless otherwise noted, all series resistors are 22Ω .
2. DQ wiring may differ from that described in this drawing; however DQ, DQS, DM, CKE, and /S relationships are maintained as shown.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I^2C; Current sink capability of SDA driver <=3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)	08h
2	Fundamental memory type	DDR SDRAM	07h
3	# of row addresses on this assembly	13	0Dh
4	# of column addresses on this assembly	11	0Bh
5	# of physical banks on this assembly	1 bank	01h
6	Data width of this assembly	72 bits	48h
7	…Data width of this assembly (continued)	—	00h
8	Voltage interface level of this assembly	SSTL 2.5V	04h
9	SDRAM cycle time at CL=2.5 (t_{CYC})	7.5ns	75h
10	SDRAM access time from clock at CL=2.5 (t_{AC})	0.75ns	75h
11	DIMM configuration type	ECC	02h
12	Refresh rate/type	7.8µs, Self -refresh	82h
13	SDRAM width	8 bits	08h
14	Error Checking SDRAM data width	8 bits	08h
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK	01h
16	SDRAM device attributes: burst lengths supported	2,4,8	0Eh
17	SDRAM device attributes: # of banks on SDRAM device	4 banks	04h
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5	0Ch
19	SDRAM device attributes: CS latency	CS latency = 0	01h
20	SDRAM device attributes: Write latency	Write Latency = 1	02h
21	SDRAM module attributes	Differential clock, PLL	24h
22	SDRAM device attributes: general	V_{DD}±0.2V	00h
23	Minimum clock cycle time at CL=2 (t_{CYC})	7.5ns (DDR266A) 10ns (DDR266B)	75h A0h
24	Max. data access time form clock at CL=2 (t_{AC})	0.75ns	75h
25	Minimum clock cycle time at CL=1.5 (t_{CYC})	N/A	00h
26	Max. data access time from clock at CL=1.5 (t_{AC})	N/A	00h
27	Minimum row precharge time (t_{RP})	20.0ns	50h
28	Minimum row active to row active delay (t_{RRD})	15.0ns	3Ch
29	Minumum RAS to CAS (t_{RCD})	20.0ns	50h
30	Minumum RAS pulse width (t_{RAS})	45ns	2Dh
31	Module bank density	512MB	80h
32	Min. command and address signal setup time (t_{AS})	0.9ns	90h
33	Min. command and address signal hold time (t_{AH})	0.9ns	90h
34	Min. data/data mask signal input setup time (t_{DS})	0.5ns	50h
35	Min. data/data mask signal input hold time (t_{DH})	0.5ns	50h

continued on the next page

SERIAL PRESENCE DETECT INFORMATION *(continued)*

Byte #	Function Described	Function Supported	Hex Value
36-40	Superset information (may be used in future)	no superset	00h
41	Row cycle time (t_{RC})	65ns	41h
42	Auto refresh cycle time (t_{RFC})	75ns	4Bh
43	Maximum SDRAM device cycle time (t_{CK_MAX})	13ns	34h
44	DQS-DQ skew (t_{DQSQ})	0.50ns	32h
45	SDRAM device data hold skew factor (t_{QHS})	0.75ns	75h
46-61	Reserved		00h
62	SPD revision	JEDEC 1.0	10h
63	Checksum for bytes 0-62	JEDEC calculation	xxh
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code	7Fh
65	Man. JEDEC ID code (continued)	STEC's ID	A8h
66-71			00h
72	Manufacturing location	STEC USA or STEC Malaysia	01h (USA) or 02h
73-90	Manufacturer's part number		xxh
91	Revision code of PCB	RevA(01),RevB(02)	00h
92			00h
93	Manufacturing date	Year (BCD)	yy
94		Calender Week (BCD)	w w
95	Assembly serial number	Tester number	ss
96		Serial number (bits 7-0)	ss
97		Serial number (bits 15-8)	ss
98		Serial number (bits 23-16)	ss
99-127	Manufacture's specific data		xxh
128-255		Undefined	00h

ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional Operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time may affect device reliability.

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +3.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1.0 to +3.6	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1.0 to 3.6	V
Storage temperature	T_{STG}	–55 to +150	°C
Power Dissapation	P_D	13.5	W
Short circuit current	I_{OS}	50	mA

POWER and DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

Recommended operating conditions (Voltage referenced to V_{SS}=0V. T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7	V	
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	$V_{DD}Q$/2-50mV	$V_{DD}Q$/2+50mV	V	1
I/O Termination voltage (system)	V_{TT}	V_{REF}–0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	$V_{DD}Q$+0.3	V	4
Input logic low voltage	V_{IL}(DC)	–0.3	V_{REF}–0.15	V	4
Input voltage level, CK and /CK	V_{IN}(DC)	–0.3	$V_{DD}Q$+0.3	V	
Input differential voltage, CK and /CK	V_{ID}(DC)	0.3	$V_{DD}Q$+0.6	V	3
Input crossing point voltage, CK and /CK	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_L	–18	18	µA	
Output leakage current	I_{OZ}	–5	5	µA	
Output high current (V_{OUT}=V_{TT}+0.84V) (Normal strength driver)	I_{OH}	–16.8		mA	
Output low current (V_{OUT}=V_{TT}–0.84V) (Normal strength driver)	I_{OL}	16.8		mA	
Output high current (V_{OUT}=V_{TT}+0.45V) (Half strength driver)	I_{OH}	–9		mA	
Output low current (V_{OUT}=V_{TT}–0.45V) (Half strength driver)	I_{OL}	9		mA	

1. Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to VREF, both of which may result in V REF noise. VREF should be de-coupled with an inductance of <= 3nH.
2. V TT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
6. These charactericteristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted; Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.**)**

Parameter/Condition	Symbol	Max	Units
OPERATING CURRENT: One bank; Active-Precharge; t RC = t RC (MIN); t CK = t CK (MIN); DQ, DM and DQS inputs changing once per clock cyle; Address and control inputs changing once every two clock cycles;	IDD0	990	mA
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst =4; t RC = t RC (MIN); t CK = t CK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle	IDD1	1215	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t CK = t CK (MIN); CKE = (LOW)	IDD2P	45	mA
IDLE STANDBY CURRENT: /CS = HIGH; All banks idle; t CK = t CK MIN; CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM	IDD2F	270	mA
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t CK = t CK (MIN); CKE = LOW	IDD3P	270	mA
ACTIVE STANDBY CURRENT: /CS = HIGH; CKE = HIGH; One bank; Active-Precharge; t RC = t RAS (MAX); t CK = t CK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	450	mA
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); IOUT = 0mA	IDD4R	1350	mA
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t CK = t CK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	1395	mA
AUTO REFRESH CURRENT: t RC = t RC(MIN)	IDD5	2160	mA
SELF REFRESH CURRENT: CKE <= 0.2V	IDD6	45	mA
OPERATING CURRENT: Four bank interleaving READs (BL=4) with auto precharge, t RC = t RC (MIN); t CK = t CK (MIN); Address and control inputs change only during Active READ, or WRITE commands.	IDD7A	3060	mA

AC OPERATING CONDITIONS0

(V_{DD}=V_{DD}Q=2.5V, T_A=25°C, f=1MHz)

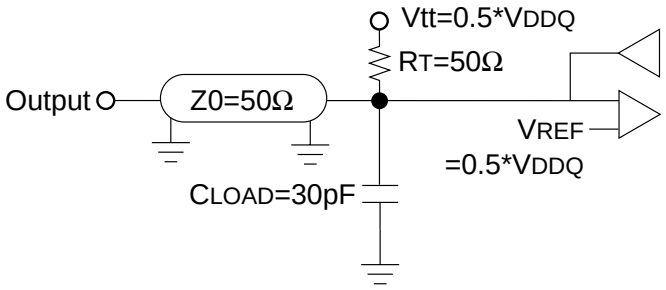
Parameter/Condition	Symbol	Min	Max	Units	Note
Input High (Logic 1) Voltage, DQ, DQS, and DM signals	VIH(AC)	VREF+0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS, and DM signals	VIL(AC)		VREF–0.31	V	3
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ–0.2	0.5*VDDQ+0.2	V	2

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V IX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

(V_{DD}=V_{DD}Q=2.5V, T_A=0°C to 70°C)

Parameter	Value	Unit
Input reference voltage for Clock	0.5*V_{DDQ}	V
Input signal maximum peak swing	1.5	V
Input signal minimum slew rate	0.5	V/ns
Input levels (V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}–0.31	V
Input timing measurement ref. level	V_{REF}	V
Output timing measurement ref. level	V_{TT}	V
Output load condition	See Load Circuit	



Output Load Circuit (SSTL_2)

INPUT/OUTPUT CAPACITANCE

(V_{DD}=V_{DD}Q=2.5V, T_A=25°C, f=1MHz)

Parameter	Symbol	Max	Units
Input Capacitance (A_0-A_{12}, BA_0, BA_1, /RAS, /CAS, /WE)	C_{IN1}	47	pF
Input Capacitance (CKE_0)	C_{IN2}	47	pF
Input Capacitance (/S_0)	C_{IN3}	47	pF
Input Capacitance (CK_0, /CK_0)	C_{IN4}	15	pF
Data and DQS I/O Capacitance (DQ_0-DQ_{63}, CB_0-CB_7, DQS_0-DQS_{17})	C_{OUT}	10	pF
Input Capacitance (DM_0-DM_8)	C_{IN5}	10	pF

AC TIMING PARAMETERS *(These AC characteristics were tested on the component.)*

Symbol	Parameter	Min	Max	Unit	Note
tRC	Row cycle time	65		ns	
t RFC	Refresh row cycle time	75		ns	
tRAS	Row active time	45	120K	ns	
tRCD	/RAS to /CAS delay	20		ns	
tRP	Row precharge time	20		ns	
tRRD	Row active to Row acitve delay	15		ns	
tWR	Write recovery time	2		tCK	
tCDLR	Last data in to Read command	1		tCK	
tCCD	Col. address to Col. address delay	1		tCK	
tCK	Clock cycle time CL=2.0 (DDR266A/DDR266B) Clock cycle time CL=2.5	7.5/10 7.5	13 13	ns ns	5 5
tCH	Clock high level width	0.45	0.55	tCK	
tCL	Clock low level width	0.45	0.55	tCK	
tDQSCK	DQS-out access time from CK, /CK	–0.75	+0.75	ns	
tAC	Output data access time from CK, /CK	–0.75	+0.75	ns	
tDQSQ	Data strobe edge to output data edge		+0.5	ns	5
tRPRE	Read Preamble	0.9	1.1	tCK	
tRPST	Read Postamble	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.75	1.25	tCK	
tWPRES	DQS-in setup time	0		ns	2
tWPREH	DQS-in hold time	0.25		tCK	
tDSS	DQS falling edge to CK rising-setup time	0.2		tCK	
tDSH	DQS falling edge from CK rising-hold time	0.2		tCK	
tDQSH	DQS-in high level width	0.35		tCK	
tDQSL	DQS-in low level width	0.35		tCK	
tDSC	DQS-in cycle time	0.9	1.1	tCK	
tIS	Address and Control Input setup time	0.9		ns	6
tIH	Address and Control Input hold time	0.9		ns	6
tHZ	Data-out high impedence time from CK,/CK	tACmin –400ps		ps	
tLZ	Data-out low impedence time from CK,/CK	tACmin -400ps		ps	
tSL(I)	Input Slew Rate (for input only pins)	0.5		V/ns	6
tSL(IO)	Input Slew Rate (for I/O pins)	0.5		V/ns	7
tSL(O)	Output Slew Rate	1.0	4.5	V/ns	10
tSLMR	Output Slew Rate Matching Ratio (rise to fall)	0.67	1.5	Ratio	
tMRD	Mode register set cycle time	15		ns	
tDS	DQ and DM setup time to DQS	0.5		ns	7,8,9
tDH	DQ and DM hold time to DQS	0.5		ns	7,8,9
tDIPW	DQ and DM input pulse width	1.75		ns	
tPDEX	Power down exit time	7.5		ns	
tXSNR	Exit self refresh to non-read command	75		ns	
tXSA	Exit self refresh to bank active command	75		ns	4
tXSR	Exit self refresh to read command	200		Cycle	
tREF	Refresh interval time	7.8		µs	1
tQH	Output DQS valid window	tHPmin –tQHS		ns	
tHP	Clock half period	tCLmin or tCHmin		ns	
tQHS	Data hold skew factor		0.75	ns	
tWPST	DQS write postamble time	0.4	0.6	tCK	3

Notes:

1. Maximum burst refresh of 8.
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter,but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are **>=** 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	**delta** tIS	**delta** tIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t IS /t IH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	**delta** tDS	**delta** tDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t DS /t DH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	**delta** tDS	**delta** tDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF **±** 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	**delta** tDS	**delta** tDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate = –0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is for system simulation purpose. It is guaranteed by design.

REVISION HISTORY

Rev.	Change Description from Previous Revision
-103	03/24/2004. Component-based specs added.
-104	03/25/2004. Board updated from PCB 955 (1.400") to PCB 1195 (1.250").
-105	04/12/2004. CK1 and CK2 termination removed from block. SPD bytes 62, 72, and 91 corrected.
-106	10/13/2006. U option added.
-107	07/30/2007. Logo updated. Byte 72 of SPD updated to include Malaysia.