SMALL-OUTLINE SDRAM MODULE

MT16LSDF3264HG, MT16LSDF6464HG

For the latest data sheet, please refer to the Micron Web site: www.micron.com/datasheets

FEATURES

- JEDEC-standard, PC100, PC133, 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 125 MHz and 133 MHz SDRAM components
- 256MB (32 Meg x 64) (x8 SDRAM)
- 512MB (64 Meg x 64) (x8 SDRAM)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 256MB module: 64ms, 4,096-cycle refresh; 512MB module: 64ms, 8,192-cycle refresh.
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS — MARKING

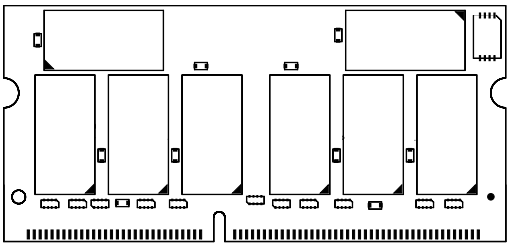
- Package
  144-pin SODIMM (gold) — G
- Frequency/CAS Latency
  133 MHz/CL = 2 — -13E
  133 MHz/CL = 3 — -133
  100 MHz/CL = 2 — -10E
- Self Refresh Current
  Standard — None
  Low power — L[1]

TIMING PARAMETERS

MODULE MARKING	PC133 (CL - ^{t}RCD - ^{t}RP)[2]	PC100 (CL - ^{t}RCD - ^{t}RP)[2]
-13E	2 - 2 - 2	2 - 2 - 2
-133	3 - 3 - 3	2 - 2 - 2
-10E	n/a	2 - 2 - 2

NOTE: 1. Consult Micron for availability
2. CL=CAS (READ) Latency

PIN ASSIGNMENT
144-Pin Small-Outline DIMM



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	73	DNU	74	CK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	S0#	70	NC/A12	141	SDA	142	SCL
71	S1#	72	RFU	143	VDD	144	VDD

NOTE: Pin 70 is not conncected (NC) for the 256MB module. For the 512MB module, pin 70 is address input A12.

PART NUMBERS

PART NUMBER	CONFIGURATION	VERSION
MT16LSDF3264HG-13E__	32 Meg x 64	133 MHz, CL = 2
MT16LSDF3264HG-133__	32 Meg x 64	133 MHz, CL = 3
MT16LSDF3264HG-10E__	32 Meg x 64	100 MHz, CL = 2
MT16LSDF6464HG-13E__	64 Meg x 64	133 MHz, CL = 2
MT16LSDF6464HG-133__	64 Meg x 64	133 MHz, CL = 3
MT16LSDF6464HG-10E__	64 Meg x 64	100 MHz, CL = 2

NOTE: All part numbers end with a five-place code, of which last two are not shown designating component and PCB revisions. Consult factory for current revision codes. Example: MT16LSDF3264HG-133B1.

ADDRESS TABLE

	256MB Module	512MB Module
Refresh Count	4K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Row Addressing	4K (A0–A11)	8K (A0–A12)
Column Addressing	1K (A0–A9)	1K (A0–A9)
Module Banks	2 (S0#, S1#)	2 (S0#, S1#)
Base Device Configuration	16 Meg x 8	32 Meg x 8

GENERAL DESCRIPTION

The Micron® MT16LSDF3264HG and MT16LSDF6464HG are high-speed CMOS, dynamic random-access, 256MB and 512MB memory modules, organized in a x64 configuration. These modules use SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signal CK0). Read and write accesses to the SDRAM modules is burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0-A11 select the device row for the 256MB module; A0-A12 for the 512MB module). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed device row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the device column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing the alternate device bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

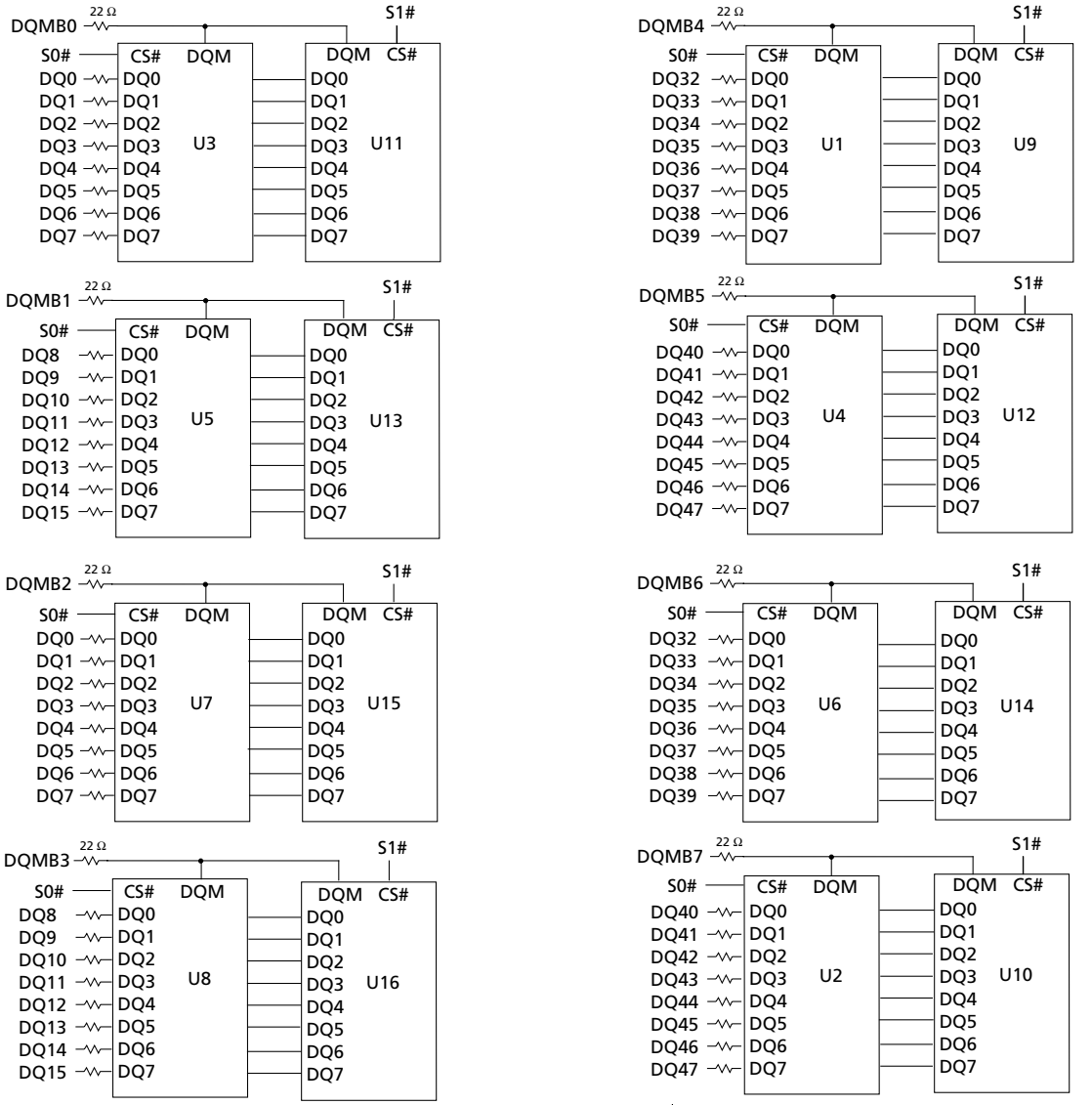
These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

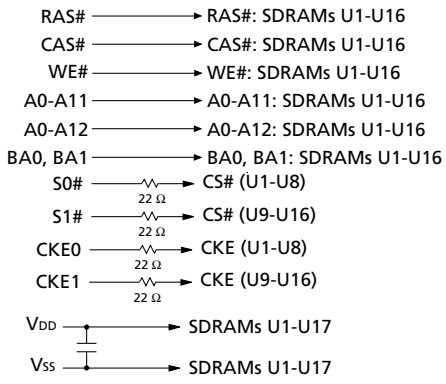
SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between device banks in order to hide precharge time, and the capability to randomly change device column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 128Mb and 256Mb data sheets.

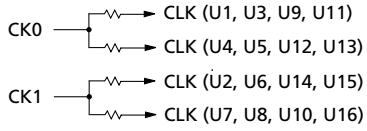
SERIAL PRESENCE-DETECT OPERATION

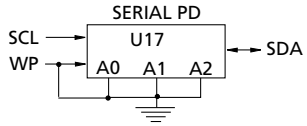
These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

FUNCTIONAL BLOCK DIAGRAM









NOTE: All resistor values are 10 ohms unless otherwise specified.

MT16LSDF3264HG (256MB): U1-U15 uses MT48LC16M8A2FB SDRAMs
MT16LSDF6464HG (512MB): U1-U15 uses MT48LC32M8A2FB SDRAMs

PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
RAS#, CAS#, WE#	Input	Command Inputs RAS#, CAS#, and WE# (along with S0#) define the command being entered.
CK0, CK1	Input	Clock: CK0 and CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
CKE0, CKE1	Input	Clock Enable: CKE0 and CKE1 activates (HIGH) and deactivates (LOW) the CK0-CK1 signals. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all device banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 and CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0 and CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK1, are disabled during power-down and self refresh modes, providing low standby power.
S0#, S1#	Input	Chip Select: S0# and S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# and S1# are registered HIGH. S0# and S1# are considered part of the command code.
DQMB0–DQMB7	Input	Input Mask: DQMB is an input mask signal for write accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
BA0, BA1	Input	Bank Address: BA0 and BA1 define to which internal device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the Mode Register.
A0-A12	Input	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column-address A0-A9, A11 [x4]; A0-A9 [x8]; A0-A8 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by (A10 LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground.

PIN DESCRIPTIONS (continued)

SYMBOL	TYPE	DESCRIPTION
DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
RFU	–	Reserved for Future Use
DNU	–	Do Not Use: This pin is not connected on these modules but is an assigned pin on the compatible DRAM version.
NC	–	No Connect: These pins should be left unconnected.

SDRAM COMPONENT DESCRIPTION

In general, the 128MB and 256Mb SDRAM memory devices used for these modules are quad-bank DRAMs, that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). The four banks of a x8, 128Mb device are each configured as 4,096 bit-rows, by 512 bit-columns, by 8 input/output bits. The four banks of a x8, 256Mb device are configured as 8,192 bit-rows by 512 bit columns, by 8 input/output bits.

MODULE FUNCTIONAL DESCRIPTION

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed BA0 and BA1 select the device bank, A0-A11 (for 256MB module), or A0-A12 (for 512MB module), select the device row. The address bits A0-A8, registered coincident with the READ or WRITE command are used to select the starting device column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all device banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

MODE REGISTER

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Mode Register Definition Diagram. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in the Burst Definition Table The block is uniquely selected by A1-A8 when the burst length is set to two; A2-A8 when the burst length is set to four; and by A3-A8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in the Burst Definition Table.

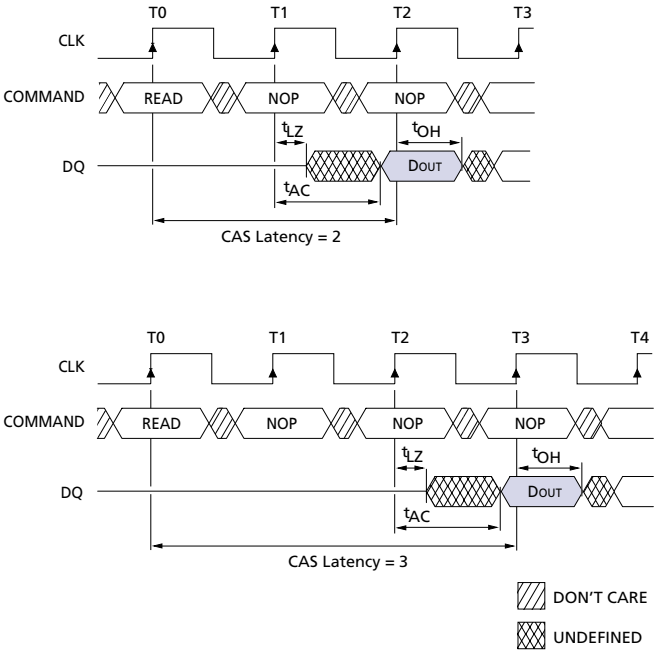
CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 1. Table 1 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 1
CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

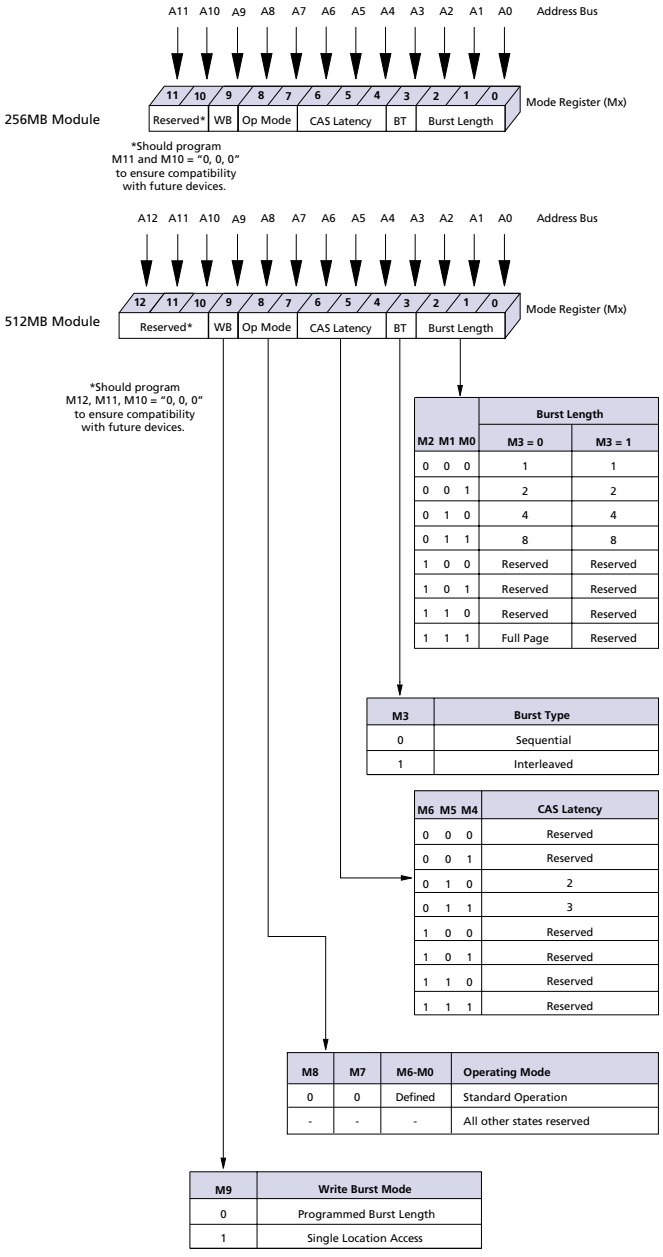
Table 1
CAS Latency

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133
-10E	≤ 100	≤ 125

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the Burst Definition Table.



Mode Register Definition Diagram

Burst Definition Table

Burst Length	Starting Column Address	Order of Accesses Within a Burst: Type = Sequential	Order of Accesses Within a Burst: Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A8 (location 0-y)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... …Cn - 1, Cn…	Not Supported

NOTE:
1. For full-page accesses: y = 512.
2. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A8 select the unique column to be accessed, and mode register bit M3 is ignored.

COMMANDS

The following Truth Table provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 128Mb and the 256Mb SDRAM component data sheet.

TRUTH TABLE – SDRAM COMMANDS AND DQMB OPERATION

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A11 (256MB), A0-A12 (512MB) define the op-code written to the Mode Register, and should be driven low.
3. A0-A11 (256MB), A0-A12 (512MB) provide device row address. BA0, BA1 determine which device bank is made active.
4. A0-A8 provide device column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: both device banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD}, $V_{DD}Q$ Supply
Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature,
T_A (commercial) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 16W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6; notes appear following the parameter tables) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}, $V_{DD}Q$	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	-80	80	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	-80	80	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

IDD SPECIFICATIONS AND CONDITIONS* - 256MB MODULE

(Notes: 1, 5, 6, 11, 13; notes appear following the parameter tables) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

			MAX				
PARAMETER/CONDITION - MT8LSDF3264HG		**SYMBOL**	**-13E**	**-133**	**-10E**	**UNITS**	**NOTES**
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}[a]	1,296	1,216	1,136	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW		I_{DD2}[b]	32	32	32	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}[a]	416	416	336	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active		I_{DD4}[a]	1,336	1,216	1,136	mA	3, 18, 19, 29
AUTO REFRESH CURRENT	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}[b]	5,280	4,960	4,320	mA	3, 12, 18, 19, 29, 30
CS# = HIGH; CKE = HIGH	^{t}RFC = 7.81 µs	I_{DD6}[b]	48	48	48	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD7}[b]	32	32	32	mA	4
	Low power (L)	I_{DD7}[b]	16	16	16	mA	

IDD SPECIFICATIONS AND CONDITIONS* - 512MB MODULE

(Notes: 1, 5, 6, 11, 13; notes appear following the parameter tables) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

			MAX				
PARAMETER/CONDITION - MT16LSDF6464HG		**SYMBOL**	**-13E**	**-133**	**-10E**	**UNITS**	**NOTES**
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		I_{DD1}[a]	1,056	1,016	1,016	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW		I_{DD2}[b]	32	32	32	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		I_{DD3}[a]	376	376	376	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active		I_{DD4}[a]	1,096	1,096	1,096	mA	3, 18, 19, 29
AUTO REFRESH CURRENT	^{t}RFC = ^{t}RFC (MIN)	I_{DD5}[b]	4,560	4,320	4,320	mA	3, 12, 18, 19, 29, 30
CS# = HIGH; CKE = HIGH	^{t}RFC = 7.81 µs	I_{DD6}[b]	64	64	64	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD7}[b]	40	40	40	mA	4
	Low power (L)	I_{DD7}[b]	24	24	24	mA	

*DRAM components only.
a - Value calculated as one module bank in this operating condition, and all other banks in Power-Down Mode.
b - Value calculated reflects all module banks in this operating condition.

CAPACITANCE

(Note 2; notes appear following parameter tables)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	40	60.8	pF
Input Capacitance: CK0-CK3	C_{I2}	13.3	17.3	pF
Input Capacitance: S0#-S3#	C_{I3}	10	15.2	pF
Input Capacitance: CKE0, CKE1	C_{I4}	20	30.4	pF
Input Capacitance: DQMB0-DQMB7	C_{I5}	5	7.6	pF
Input/Output Capacitance: SCL, SA0-SA2, SDA	C_{I6}	–	10	pF
Input/Output Capacitance: DQ0-DQ63	C_{IO}	8	12	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11, 31; notes appear following the parameter tables) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

AC CHARACTERISTICS			-13E		-133		-10E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	$^tAC(3)$		5.4		5.4		6	ns	27
	CL = 2	$^tAC(2)$		5.4		6		6	ns	
Address hold time		^tAH	0.8		0.8		1		ns	
Address setup time		^tAS	1.5		1.5		2		ns	
CLK high-level width		^tCH	2.5		2.5		3		ns	
CLK low-level width		^tCL	2.5		2.5		3		ns	
Clock cycle time	CL = 3	$^tCK(3)$	7		7.5		8		ns	23
	CL = 2	$^tCK(2)$	7.5		10		10		ns	23
CKE hold time		^tCKH	0.8		0.8		1		ns	
CKE setup time		^tCKS	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		2		ns	
Data-in hold time		^tDH	0.8		0.8		1		ns	
Data-in setup time		^tDS	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	$^tHZ(3)$		5.4		5.4		6	ns	10
	CL = 2	$^tHZ(2)$		5.4		6		6	ns	10
Data-out low-impedance time		^tLZ	1		1		1		ns	
Data-out hold time (load)		^tOH	3		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		^tRAS	37	120,000	44	120,000	50	120,000	ns	32
ACTIVE to ACTIVE command period		^tRC	60		66		70		ns	
ACTIVE to READ or WRITE delay		^tRCD	15		20		20		ns	
Refresh period (8,192 rows)		^tREF		64		64		64	ms	
AUTO REFRESH period		^tRFC	66		66		70		ns	
PRECHARGE command period		^tRP	15		20		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	14		15		20		ns	
Transition time		^tT	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		ns	24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		^tXSR	67		75		80		ns	20

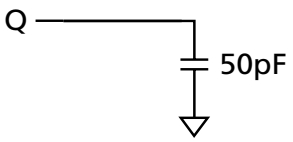
AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11, 31; notes appear following the parameter tables) (0°C ≤ T_A ≤ +70°C)

PARAMETER		SYMBOL	-13E	-133	-10E	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	0	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	0	0	^{t}CK	17
DQM to data high-impedance during READs		^{t}DQZ	2	2	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	0	0	^{t}CK	17
Data-in to ACTIVE command		^{t}DAL	4	5	4	^{t}CK	15, 21
Data-in to PRECHARGE command		^{t}DPL	2	2	2	^{t}CK	16, 21
Last data-in to burst STOP command		^{t}BDL	1	1	1	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	1	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	2	2	2	^{t}CK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	2	^{t}CK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	^{t}ROH(3)	3	3	3	^{t}CK	17
	CL = 2	^{t}ROH(2)	2	2	2	^{t}CK	17

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C ≤ T_A ≤ +70°C).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1 ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 10ns for -10E, and ^{t}CK = 7.5ns for -133 and -13E.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
25. Precharge mode only.
26. JEDEC and PC100 specify three clocks.
27. ^{t}AC for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. The value of ^{t}RAS. use in -13E speed grade module SPDs is calculated from ^{t}RC - ^{t}RP = 45ns.
30. For -10E, CL= 2 and ^{t}CK = 10ns; for -133, CL = 3 and ^{t}CK = 7.5ns; for -13E, CL = 2 and ^{t}CK = 7.5ns.
31. CKE is HIGH during refresh command period ^{t}RFC (MIN) else CKE is LOW. The I_{DD}6 limit is actually a nominal value and does not result in a fail value.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions as indicated in Figures 3 and 4.

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data as indicated in Figure 5.

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 3
Data Validity

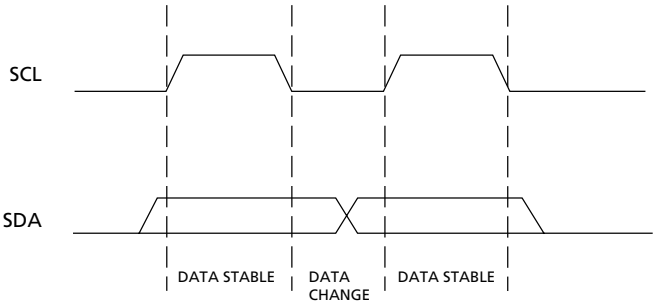


Figure 4
Definition of Start and Stop

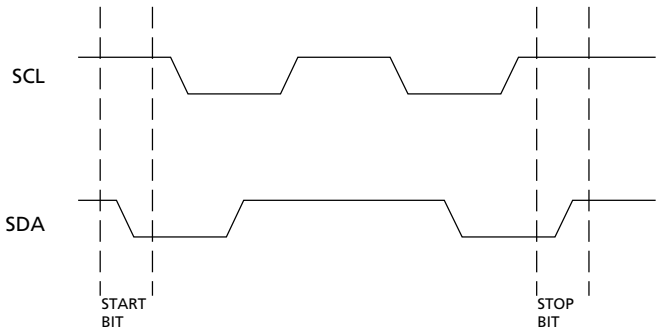
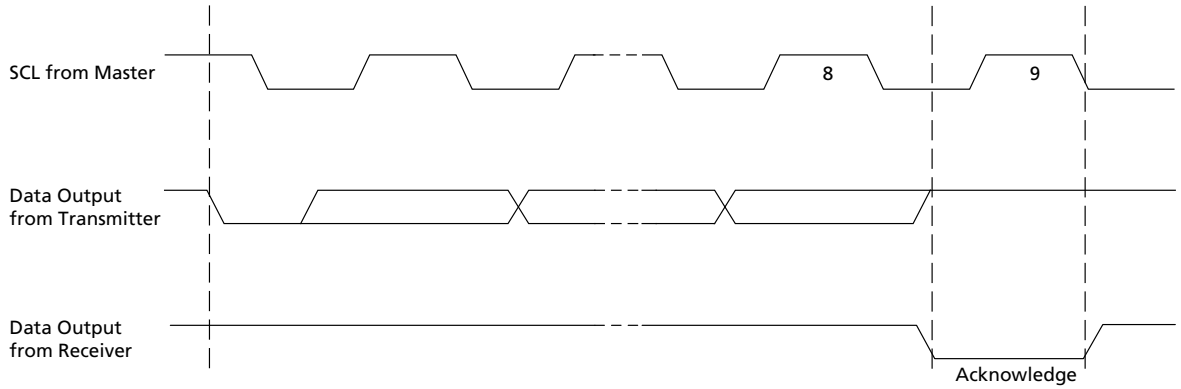


Figure 5
Acknowledge Response From Receiver



EEPROM DEVICE SELECT CODE

The most significant bit (b7) is sent first

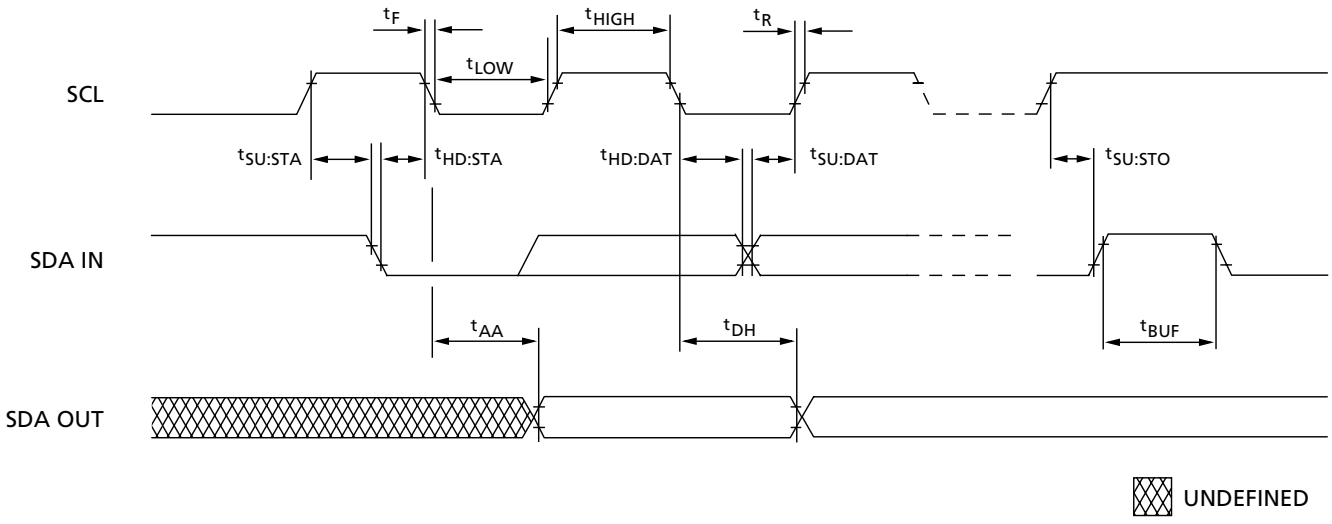
	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	RW
Protection Register Select Code	0	1	1	0	E2	E1	E0	RW

EEPROM OPERATING MODES

MODE	RW BIT	WC[1]	BYTES	INITIAL SEQUENCE
Current Address Read	1	X	1	START, Device Select, RW = '1'
Random Address Read	0	X	1	START, Device Select, RW = '0', Address
	1	X	1	reSTART, Device Select, RW = '1'
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, RW = '0'
Page Write	0	V_{IL}	≤ 16	START, Device Select, RW = '0'

NOTE: 1. X = V_{IH} or V_{IL}.

SPD EEPROM TIMING DIAGRAM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{AA}	0.3	3.5	µs
t_{BUF}	4.7		µs
t_{DH}	300		ns
t_{F}		300	ns
$t_{HD:DAT}$	0		µs
$t_{HD:STA}$	4		µs

SYMBOL	MIN	MAX	UNITS
t_{HIGH}	4		µs
t_{LOW}	4.7		µs
t_{R}		1	µs
$t_{SU:DAT}$	250		ns
$t_{SU:STA}$	4.7		µs
$t_{SU:STO}$	4.7		µs

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 2) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	3

NOTE: 1. All voltages referenced to V_{SS}.
2. All voltages referenced to V_{SS}.
3. Timing actually specified by ^{t}WR.

SERIAL PRESENCE-DETECT MATRIX

(Note: 1)

BYTE	DESCRIPTION	MT16LSDF3264G		MT16LSDF6464HG	
		ENTRY (VERSION)	HEX VALUE	ENTRY (VERSION)	HEX VALUE
0	NUMBER OF BYTES USED BY MICRON	128	80	128	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	256	08
2	MEMORY TYPE	SDRAM	04	SDRAM	04
3	NUMBER OF ROW ADDRESSES	12	0C	13	0D
4	NUMBER OF COLUMN ADDRESSES	10	0A	11	0B
5	NUMBER OF BANKS	2	02	2	02
6	MODULE DATA WIDTH (bit 0 is LSB)	64	40	64	40
7	MODULE DATA WIDTH (bit 7 is MSB)	0	00	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	01	LVTTL	01
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E)	70 75 80	70 7.5 (-133) 8 (-10E)	70 75 80
10	SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E)	54 60	5.4 (-13E/-133 6 (-10E)	54 60
11	MODULE CONFIGURATION TYPE	NON PARITY	00	NON PARITY	00
12	REFRESH RATE/TYPE	15.625/SELF	80	7.8/SELF	82
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08	8	08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE	00	NONE	00
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES, ^{t}CCD	1	01	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, FULL-PAGE	8F	1, 2, 4, 8, FULL-PAGE	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	4	04
18	CAS LATENCIES SUPPORTED	2, 3	06	2,3	06
19	CS LATENCY	1	01	1	01
20	WE LATENCY	1	01	1	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED	00	UNBUFFERED	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	14	0E	14	0E
23	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	7.5 (-13E) 10 (-133/-10E)	75 A0	7.5 (-13E) 10 (-133/-10E)	75 A0
24	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 2)	5.4 (-13E) 6 (-133/-10E)	54 60	5.4 (-13E) 6 (-133/-10E)	54 60
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	–	00	00	00
26	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 1)	–	00	00	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	15 (-13E) 20 (-133/-10E)	0F 14	0F 14	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	14 (-13E) 15 (-133) 20 (-10E)	0E 0F 14	0E 0F 14	0E 0F 14
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	15 (-13E) 20 (-133/-10E)	0F 14	15 (-13E) 20 (-133/-10E)	0F 14
30	MINIMUM RAS# PULSE WIDTH, (^{t}RAS MODULE = ^{t}RC - ^{t}RP)	45 (-13E)* 44 (-133) 50 (-10E)	2D 2C 32	45 (-13E)* 44 (-133) 50 (-10E)	2D 2C 32

*The value of ^{t}RAS used for the -13E module is calculated from ^{t}RC - ^{t}RP. Actual device spec value is 37ns.

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

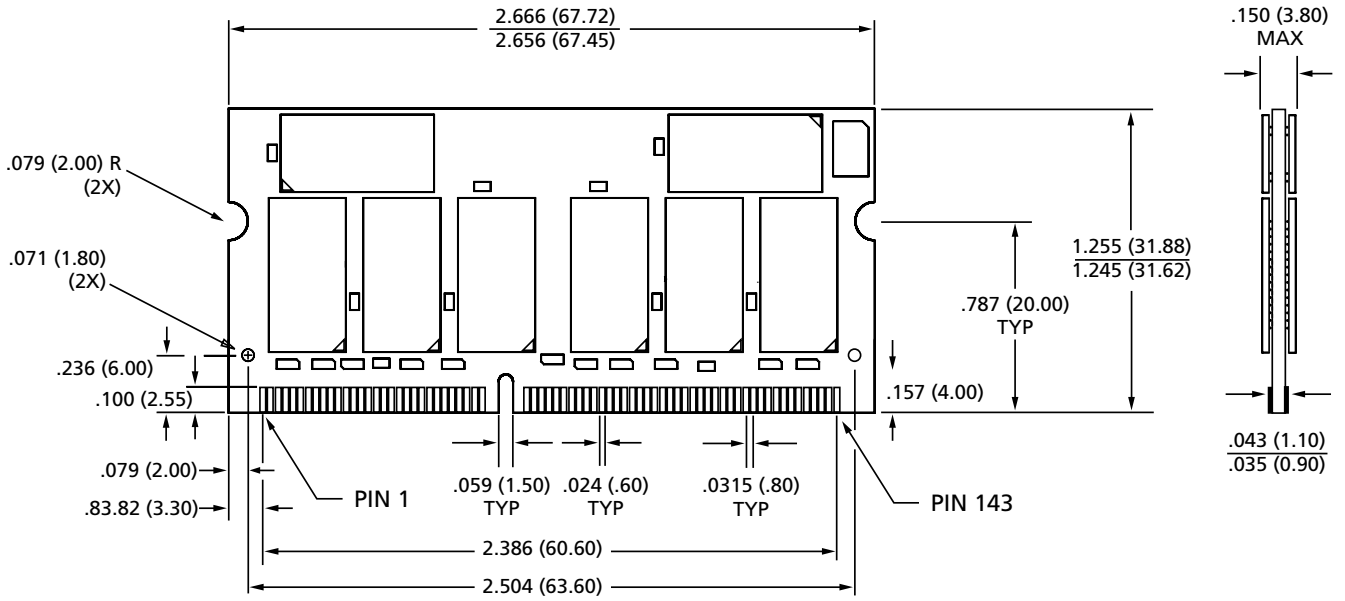
SERIAL PRESENCE-DETECT MATRIX (continued)

(Note2: 1, 2)

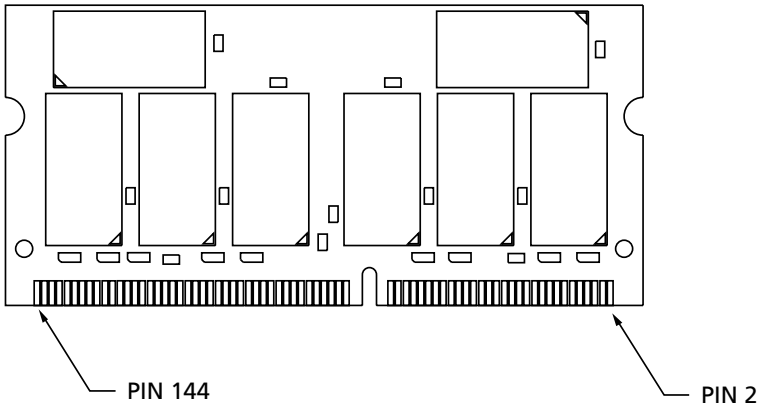
BYTE	DESCRIPTION	MT16LSDF3264G		MT16LSDF6464HG	
		ENTRY (VERSION)	HEX VALUE	ENTRY (VERSION)	HEX VALUE
31	MODULE BANK DENSITY	128MB	20	256MB	40
32	COMMAND AND ADDRESS SETUP TIME, ^{t}AS, ^{t}CMS	1.5 (-13E/-133)	15	1.5 (-13E/-133)	15
		2 (-10E)	20	2 (-10E)	20
33	COMMAND AND ADDRESS HOLD TIME, ^{t}AH, ^{t}CMH	0.8 (--13E/133)	08	0.8 (--13E/133)	08
		1 (-10E)	10	1 (-10E)	10
34	DATA SIGNAL INPUT SETUP TIME, ^{t}DS	1.5 (-13E/-133)	15	1.5 (-13E/-133)	15
		2 (-10E)	20	2 (-10E)	20
35	DATA SIGNAL INPUT HOLD TIME, ^{t}DH	0.8 (-13E/-133)	08	0.8 (-13E/-133)	08
		1 (-10E)	10	1 (-10E)	10
36-61	RESERVED	00	00	00	00
62	SPD REVISION	REV. 1.2B	12	REV. 1.2B	12
63	CHECKSUM FOR BYTES 0-62	-13E	69	-13E	8C
		-133	AF	-133	D2
		-10E	F7	-10E	1A
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	MICRON	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)	FF	FF	FF	FF
72	MANUFACTURING LOCATION		01		01
			02		02
			03		03
			04		04
			05		05
			06		06
			07		07
			08		08
			09		09
73-90	MODULE PART NUMBER (ASCII)		xx		xx
91	PCB IDENTIFICATION CODE	1	01	1	01
		2	02	2	02
		3	03	3	03
		4	04	4	04
		5	05	5	05
		6	06	6	06
		7	07	7	07
		8	08	8	08
		9	09	9	09
92	IDENTIFICATION CODE (CONT.)	0	00	0	00
93	YEAR OF MANUFACTURE IN BCD		xx	xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx	xx
95-98	MODULE SERIAL NUMBER		xx	xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–	–
126	SYSTEM FREQUENCY	100/133 MHz	64	100/133 MHz	64
127	SDRAM COMPONENT AND CLOCK DETAIL		8F	8F	8F

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

FRONT VIEW



BACK VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

DATA SHEET DESIGNATION

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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