Features

- **ConcurrentFlash™ Memory**
  - **Unique Architecture Allows the Flash Array To Be Read During the E²PROM Write Cycle**
- **4 Megabit 5-volt Flash**
  - **Configured as a 512K x 8 Memory Array**
  - **120 ns Read Access Time**
  - **Sector Program Operation**
    - **Single Cycle Reprogram (No Erase Necessary)**
    - **2048 Sectors, 256-Bytes Wide**
    - **10 ms Sector Rewrite**
  - **JEDEC Standard Software Data Protection**
- **256K bit Full Feature E²PROM**
  - **Configured as a 32K x 8 Memory Array**
  - **Byte or Page (16 bytes) Write Capability**
  - **Write Cycle Time: 10 ms**
  - **JEDEC Standard Software Data Protection**
- **Pinout Similar to 32-Pin 4 Mb Flash**
- **Data Memory Endurance: 10,000 cycles**

4 Megabit 5-volt Flash with 256K E²PROM Memory

AT29C432 ConcurrentFlash™

Preliminary

Description

The AT29C432 is a CMOS memory specifically designed for applications requiring both a high density nonvolatile program memory and a smaller nonvolatile data memory. The AT29C432 provides this in the form of a 4 megabit Flash array integrated with a 256K bit full featured E²PROM array on the same device. A unique feature of this device is its concurrent read while writing capability. This provides the host system read access to the Flash program memory during the write cycle time of the E²PROM.

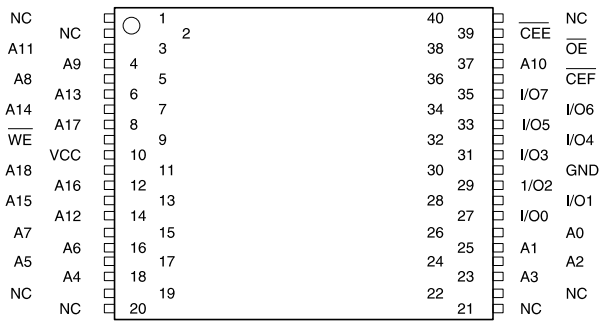
The two memory arrays share all I/O lines, Address lines and $\overline{OE}$ and $\overline{WE}$ inputs. Each memory array has its own Chip Enable input: $\overline{CEF}$ for the Flash array and $\overline{CEE}$ for the E²PROM array.

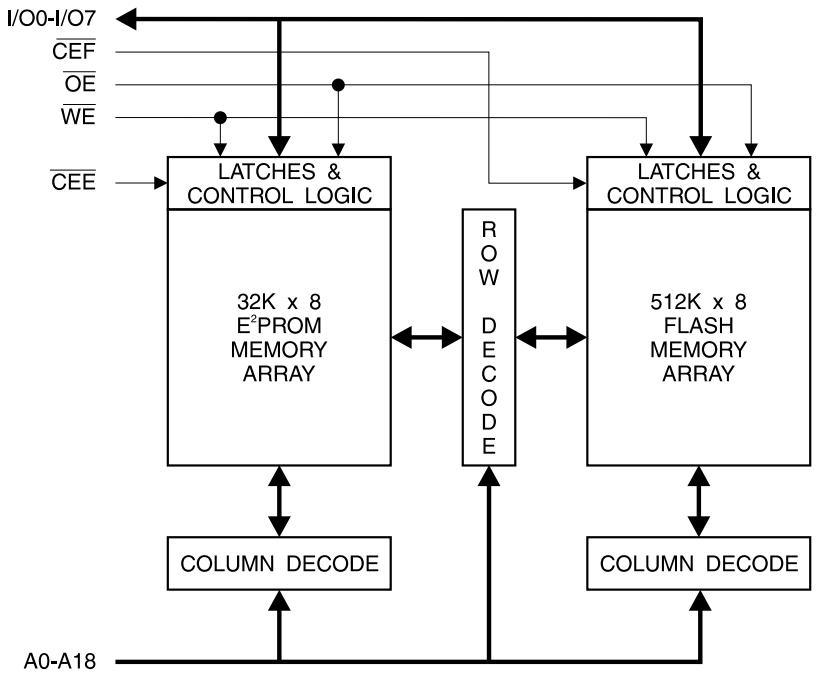
Additionally, Software Data Protection has been independently implemented for both arrays and is always enabled. The AT29C432 has a pinout similar to the AT29C040A Flash memory. A system designer using a Flash memory for program storage and another smaller, non volatile memory for data storage can easily replace both memories with the AT29C432.

Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
$\overline{CEE}$	Chip Enable E²PROM
$\overline{CEF}$	Chip Enable Flash
NC	No Connect

TSOP
Type 1





Device Operation

Flash Memory Array

READ: The Flash memory array is read like a Static RAM. When CEF and OE are low, and WE and CEE are high, the data stored at the memory location determined by the address inputs is asserted on the I/O's.

PROGRAM: The Flash memory array is divided into 2048 sectors, each comprised of 256 bytes. For read operations these sectors appear seamless; however, for reprogramming the sector boundaries must be taken into account. The state of adresses A0 - A3 and A15 - A18 specify the individual byte address within a sector and the state of addresses A4 - A14 define the sector to be written.

The AT29C432 employs the JEDEC standard software data protection feature; therefore, each programming sequence must be preceded by the three byte program command sequence. Using the software data protection feature, byte loads are used to enter the 256 bytes of a sector to be programmed. The Flash memory array can only be programmed using the software data protection feature. The Flash memory array is programmed on a sector basis. If a byte of data within the sector is to be changed, data for the entire 256-byte sector must be loaded into the device. The Flash memory array automatically does a sector erase prior to loading the data into the sector. An erase command is not required.

Software data protection protects the device from inadvertent programming. A series of three program commands to specific addresses with specific data must be presented to the device before programming may occur. The same three program commands must begin each program operation. All software program commands must obey the sector program timing specifications. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WCF}, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the WE or CEF input with CEF or WE low (respectively) and OE and CEE high. The address is latched on the falling edge of CEF or WE, whichever occurs last. The data is latched by the first rising edge of CEF or WE.

The 256 bytes of data must be loaded into each sector. Any byte that is not loaded during the programming of its sector will be indeterminate. Once the bytes of a sector are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on WE (or CEF) within 150 µs of the low to high transition of WE (or CEF) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to

(continued)

Device Operation (Continued)

high transition, the load period will end and the internal programming period will start. The sector address must be valid during each high to low transition of WE (or CEF). The bytes may be loaded in any order; sequential loading is not required. Once a programming operation has been initiated, and for the duration of t_{WCF}, a read operation will effectively be a data polling operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the Flash memory array in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay—once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit—holding any one of OE low, CEF high or WE high inhibits program cycles. (d) Noise filter—pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a program cycle.

DATA POLLING: A maximum amount of time for program and write operations is specified; the actual time is frequently faster than the specification. In order to take advantage of the faster typical times, the Flash memory array features DATA polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA polling may begin at any time during the program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product. In addition, users may wish to use the software product identification mode to identify the part (i.e. using the device code), and have the system software use the appropriate sector size for program operations.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

E^2PROM Memory Array

READ: The E^2PROM memory array is read like a Static RAM. When CEE and OE are low and WE and CEF are high, the data stored at the memory location determined by the address inputs is asserted on the I/O's.

WRITE: The E^2PROM memory array may be written in either a single byte write or page write operation. Because software data protection is always enabled both write operations must be preceded by the three byte write command sequence. This sequence should then immediately be followed by one to sixteen bytes of data. After the last byte has been written, the AT29C432 will automatically time itself to completion of the internal write cycle.

The write cycle is initiated by both WE and CEE going low; the address is latched by the falling edge of WE or CEE (whichever occurs last) and the data is latched by the rising edge of WE or CEE (whichever occurs first). All write operations (byte or page) must conform to the page write limits as shown in the timing diagram for E^2PROM write operations. All bytes during a page write operation must reside on the same page as defined by the state of the A4 - A14 inputs. For each WE high to low transition during the page write operation, A4 - A14 must be the same.

The A0 - A3 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

During the internal write operation (t_{WCE}) attempts to read the E^2PROM will be equivalent to DATA polling operations; however, attempts to read the Flash array will return valid data.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the E^2PROM memory array in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay—once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit—holding any one of OE low, CEE high or WE high inhibits program cycles. (d) Noise filter—pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a program cycle.

DATA POLLING: A maximum amount of time for program and write operations is specified; the actual time is frequently faster than the specification. In order to take advantage of the faster typical times, the E^2PROM memory array features DATA polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. DATA polling may begin at any time during the program cycle.

(continued)

Device Operation (Continued)

Memory Arrays

Concurrent Read While Write

The architecture of the AT29C432 provides concurrent read while write capability. With other programmable non-volatile memories internal high voltage operations prevent the reading of data while a write operation is in process. However, the AT29C432 is partitioned in a manner to allow read operations from the Flash memory array during a write operation within the E^2PROM memory array.

Conceptually the device was designed assuming the Flash memory array would be utilized for infrequently updated program storage and the E^2PROM memory array would be used for frequently updated data storage. This simple concept eliminates complicated software and hardware schemes using multiple blocks of memory just to hold duplicate down-load routines.

Valid Concurrent Read

Reads from the Flash are allowed throughout the E^2PROM write cycle time (t_{WCE}). The E^2PROM memory array must be deselected ($\overline{CEE}$ HIGH).

Reads from the Flash are allowed during t_{WPH} of a E^2PROM write so long as t_{BLC} for the E^2PROM write is not violated. The E^2PROM memory array must be deselected ($\overline{CEE}$ HIGH).

Invalid Concurrent Reads

Attempts to read the Flash memory array during t_{WCF} will effectively be polling operations.

Attempts to access the Flash memory array while $\overline{CEE}$ is low will be ignored. That is, $\overline{CEE}$ low and $\overline{CEF}$ low at the same time is not allowed. Attempts to read the E^2PROM memory array while a write to the Flash memory array is in progress is not allowed.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	4	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC and AC Operating Range

		AT29C432-12	AT29C432-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		4.5V - 5.5V	4.5V - 5.5V

Operating Modes

Mode	$\overline{CEE}$	$\overline{CEF}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Flash Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
E^2PROM Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{OUT}
Flash Program	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
E^2PROM Program	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	V_{IH}	X	X	X	High Z
Program Inhibit	X (2)	X	X	V_{IH}		
Program Inhibit	X	X	V_{IL}	X		
Output Disable	X	X	V_{IH}	X		High Z
Illegal	V_{IL}	V_{IL}	V_{IL}	X		D_{OUT} Undefined
Illegal	V_{IL}	V_{IL}	V_{IH}	X		High Z
Product Identification						
Hardware	V_{IH}	V_{IL}	V_{IL}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IL}	Manufacturer Code (4)
					A1 - A18 = V_{IL}, A9 = V_H, (3) A0 = V_{IH}	Device Code (4)
Software (5)					A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code (4)
					A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code (4)

Notes: 1. For detailed operational timing refer to the appropriate timing diagrams and AC characteristics tables.
2. X indicates input state can be either V_{IH} or V_{IL}.
3. V_H = 12.0V ± 0.5V
4. Manufacturer Code: 1F, Device Code: B4
5. See details under Software Product Identification Entry/Exit.

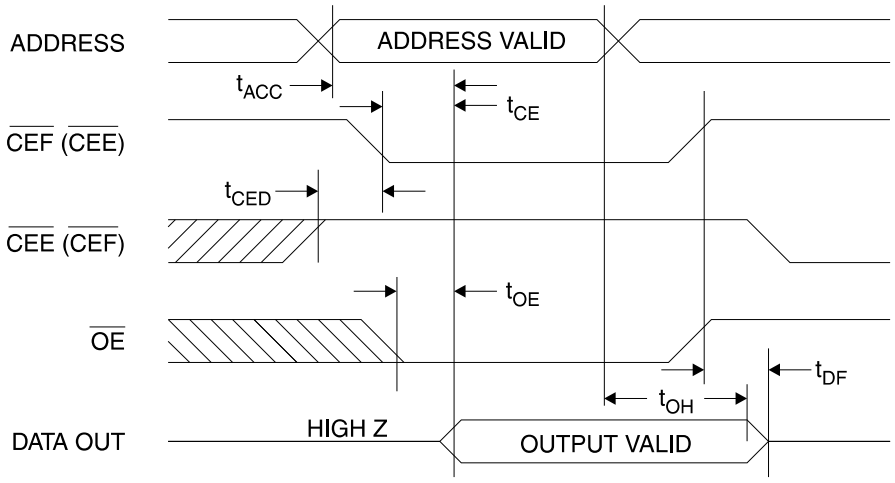
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB}	V_{CC} Standby Current	$\overline{CEE}$ = $\overline{CEF}$ = V_{CC} - 0.3V to V_{CC} + 1.0V		300	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA; V_{CC} = 4.5V	2.4		V
		I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

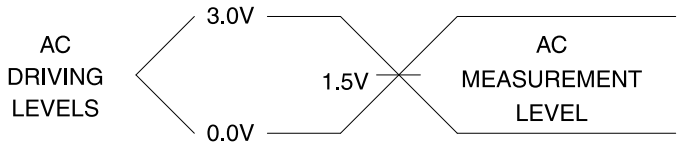
Symbol	Parameter	AT29C432-12		AT29C432-15		Units
		Min	Max	Min	Max	
t_{CED}	$\overline{CEE}$ to $\overline{CEF}$ Active Delay (or $\overline{CEF}$ to $\overline{CEE}$ Active Delay)	100		100		ns
t_{ACC}	Address to Output Delay		120		150	ns
t_{CE} (1)	$\overline{CEE}$ (or $\overline{CEF}$) to Output Delay		120	0	150	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	50	0	70	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	30	0	40	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CEE}$ or $\overline{CEF}$ or Address change	0		0		ns

AC Read Waveforms (1, 2, 3, 4)



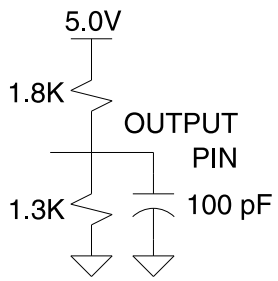
Notes:
1. $\overline{CEF}$ ($\overline{CEE}$) may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CEF}$ ($\overline{CEE}$) without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CEF}$ ($\overline{CEE}$) whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

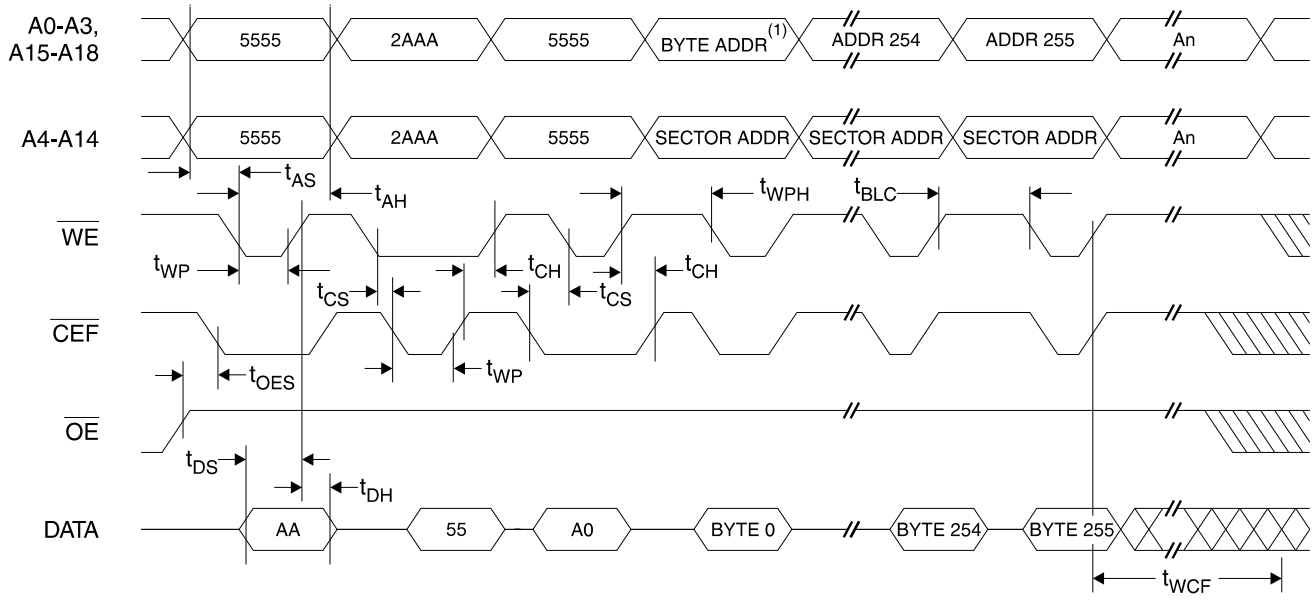
Output Test Load



Flash Array
AC Write Timing Characteristics

Symbol	Parameter	Min	Max	Units
t_{WCF}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CEF}$)	100		ns
t_{OES}	$\overline{OE}$ Disable to $\overline{WE}$ or $\overline{CEF}$ Active	0		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{CS}	$\overline{CEF}$ to $\overline{WE}$ or $\overline{WE}$ to $\overline{CEF}$ Setup Time	0		ns
t_{CH}	$\overline{CEF}$ to $\overline{WE}$ or $\overline{WE}$ to $\overline{CEF}$ Hold Time	0		ns
t_{OEH}	$\overline{WE}$ or $\overline{CEF}$ Disable to $\overline{OE}$ Active	10		ns
t_{WPH}	$\overline{WE}$ or $\overline{CEF}$ Pulse Width High	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs

AC Flash Array Write Waveforms

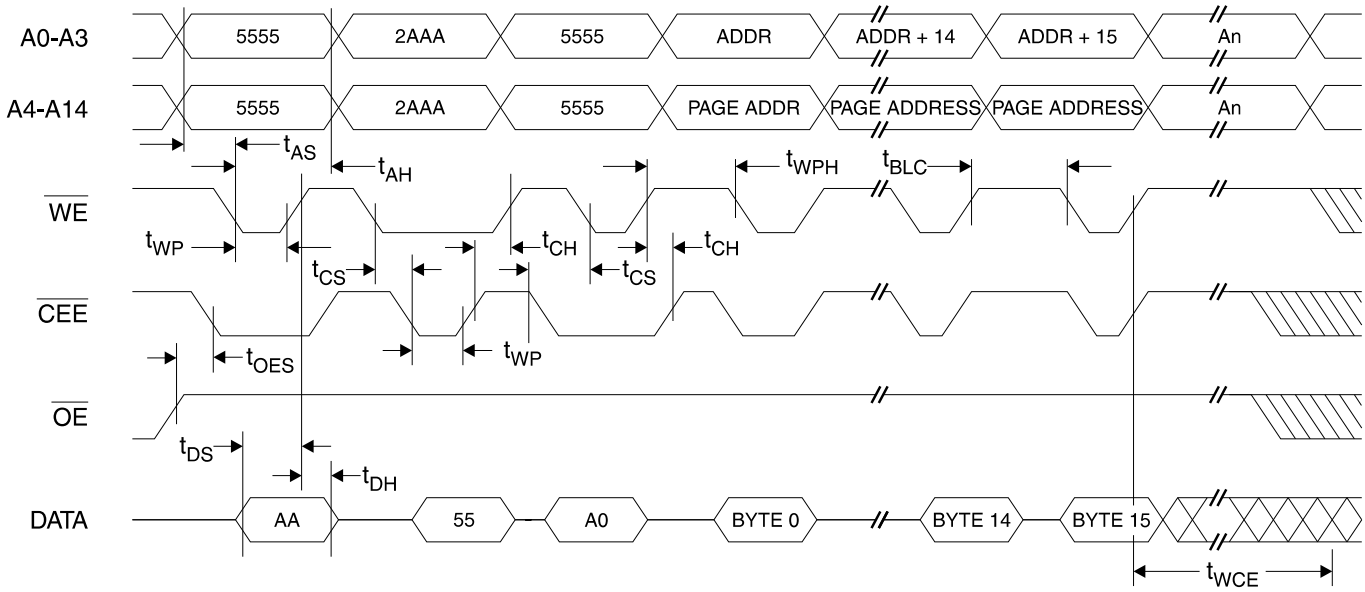


Note: 1. BYTE ADDRESS is the first destination address for the sector write operation. All write operations must begin with the three byte write enable sequence.

E²PROM Array
AC Write Timing Characteristics

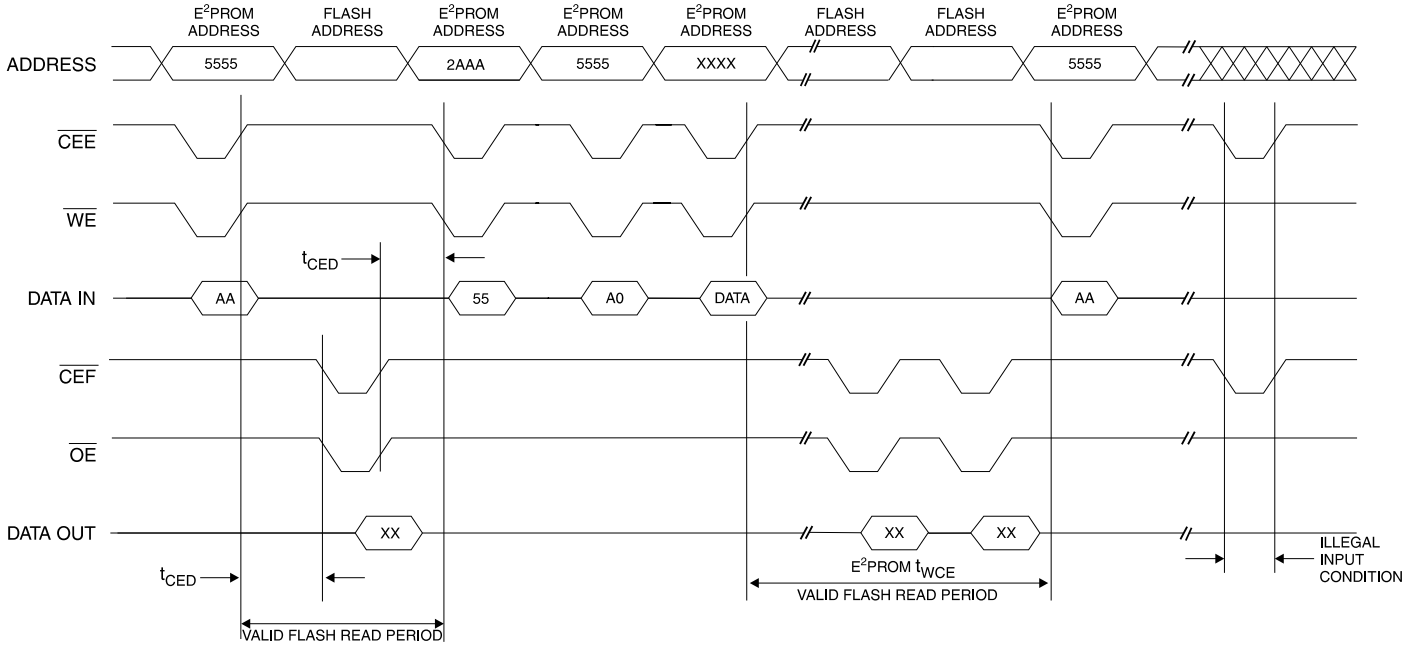
Symbol	Parameter	Min	Max	Units
t_{WCE}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CEE}$)	100		ns
t_{OES}	$\overline{OE}$ Disable to $\overline{WE}$ or $\overline{CEE}$ Active	0		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{CS}	$\overline{CEE}$ to $\overline{WE}$ or $\overline{WE}$ to $\overline{CEE}$ Setup Time	0		ns
t_{CH}	$\overline{CEE}$ to $\overline{WE}$ or $\overline{WE}$ to $\overline{CEE}$ Hold Time	0		ns
t_{OEH}	$\overline{WE}$ or $\overline{CEE}$ Disable to $\overline{OE}$ Active	10		ns
t_{WPH}	$\overline{WE}$ or $\overline{CEE}$ Pulse Width High	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs

AC E²PROM Array Write Waveforms



Note: 1. Only A0 - A14 are valid address inputs for the E²PROM write operations, A15 - A18 are don't care. BYTE ADDRESS is the first destination address for either a byte write or page write operation. All write operations, byte only or page write, must begin with the three byte write enable sequence.

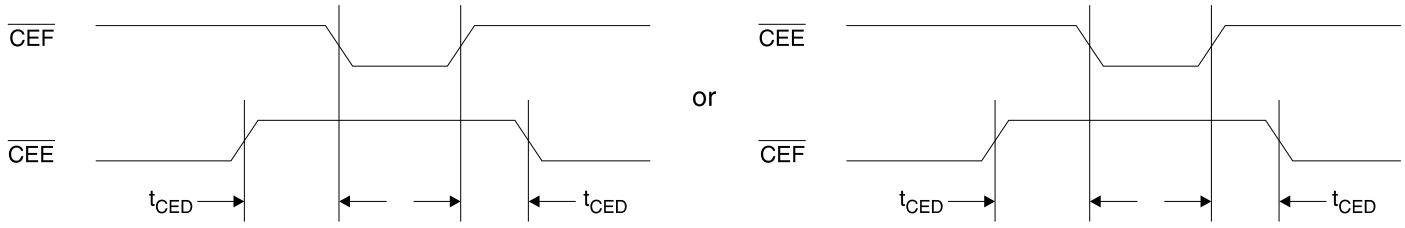
Concurrent Read While Write



Notes: 1. The Flash array may be read in between individual byte loads to the E^{2}PROM array as shown above. This diagram only illustrates one read access between byte loads, but the host processor may continue reading the Flash array so long as t_{BLC} is not violated. This effectively allows the host the opportunity to respond to system interrupts while operating out of the Flash program memory, even in the middle of performing an E^{2}PROM data update.

2. Flash read operations are also valid throughout the E^{2}PROM's internal write cycle defined by t_{WCE}.
3. Having both $\overline{CEF}$ and $\overline{CEE}$ active simultaneously is an illegal state.

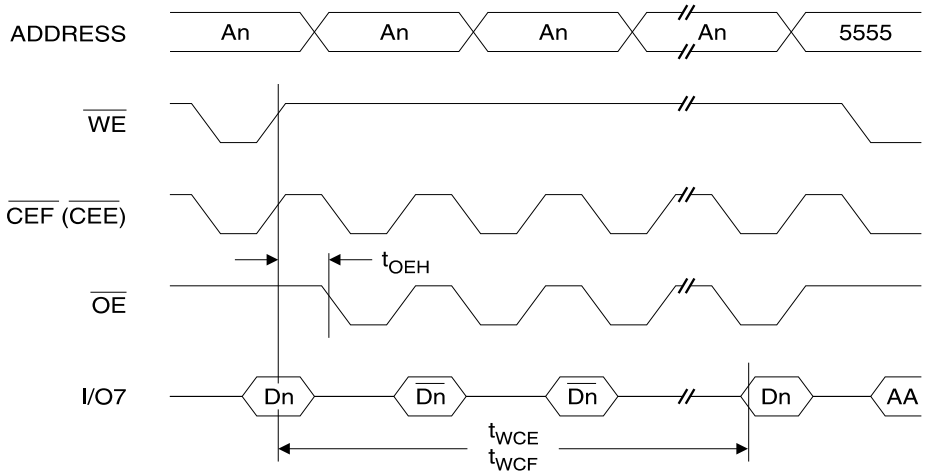
Chip Enable Delays



AC Data Polling Characteristics (1)

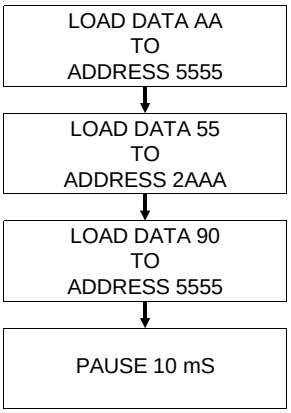
Symbol	Parameter	Min	Max	Units
t_{WCE}	Write Cycle Time, E^2PROM		10	ms
t_{WCF}	Write cycle Time, Flash		10	ms
t_{OEH}	$\overline{WE}$ or $\overline{CEE}$ ($\overline{CEF}$) Disable to $\overline{OE}$ Active	10		ns

AC Data Polling Waveform



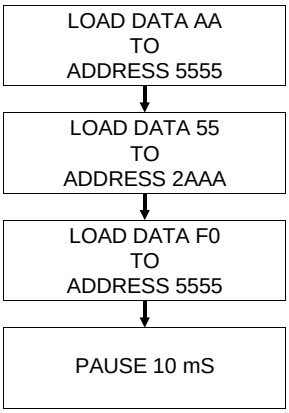
Note: 1. The above timing diagram illustrates $\overline{DATA}$ Polling where Dn is equal to the state of I/07 for the last byte written and $\overline{Dn}$ is its complement.

Software Product Identification Entry (1)



ENTER PRODUCT IDENTIFICATION MODE (2, 3, 5)

Software Product Identification Exit (1)



EXIT PRODUCT IDENTIFICATION MODE (4)

Notes for software product identification:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}. Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}. $\overline{CEF}$ = Low, $\overline{CEE}$ = High
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1F
   Device Code: B4

Ordering Information

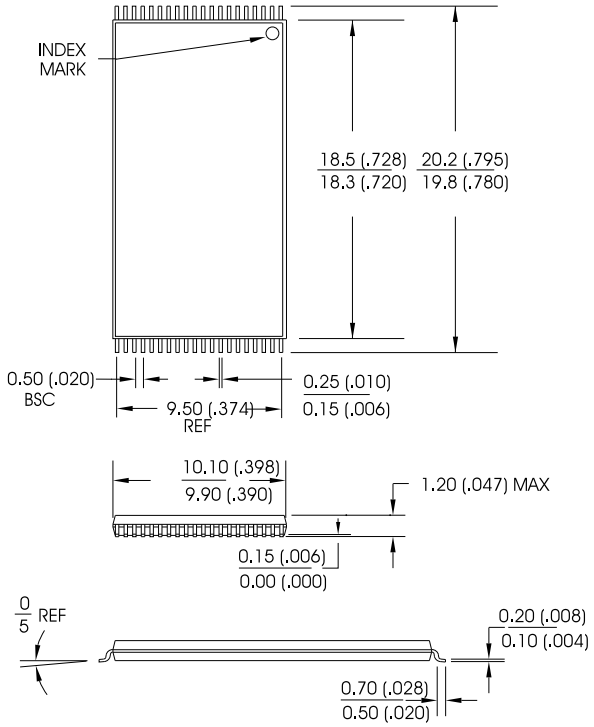
t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
120	40	0.3	AT29C432-12TC	40T	Commercial (0° to 70°C)
	40	0.3	AT29C432-12TI	40T	Industrial (-40° to 85°C)
150	40	0.3	AT29C432-15TC	40T	Commercial (0° to 70°C)
	40	0.3	AT29C432-15TI	40T	Industrial (-40° to 85°C)

Package Type	
40T	40 Lead, Thin Small Outline Package (TSOP)

Packaging Information

40T, 40 Lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches) *



*Controlling dimension: millimeters