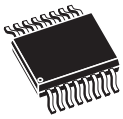
Numonyx® Omneo™ P5Q PCM

128-Mbit, Quad/Dual/Single Serial Interface, 128-Kbyte Sectors Phase Change Memory (PCM) with 66MHz SPI Bus Interface

Features

- SPI bus compatible serial interface
- Maximum Clock Frequency
  - 66MHz (0 to +70 °C)
  - 33MHz (-30 to +85 °C)
- 2.7 V to 3.6 V single supply voltage
- Supports legacy SPI protocol and new Quad I/O or Dual I/O SPI protocol
- Quad I/O frequency of 50MHz, resulting in an equivalent clock frequency up to 200 MHz:
- Dual I/O frequency of 66MHz, resulting in an equivalent clock frequency up to 132 MHz:
- Continuous read of entire memory via single instruction:
  - Quad & Dual Output Fast Read
  - Quad & Dual Input Fast Program
- Uniform 128-Kbyte sectors (flash emulation)
- Write Operations
  - 128-Kbyte sectors erase (emulated)
  - Legacy Flash Page Program
  - Bit-alterable Page Writes
  - Page Program on all 1s (PreSet Writes)
- Write protections
  - Protected area size defined by four non-volatile bits (BP0, BP1, BP2, and BP3)
- Electronic signature
  - JEDEC standard two-byte signature (DA18h)
- Density and Packaging
  - 128 Mbit density with SOIC16 package



SO16 (MF)
300 mils width

- More than 1,000,000 write cycles
- Phase Change Memory (PCM)
  - Chalcogenide phase change storage element
  - Bit alterable write operation

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1 Description

1.1 Introduction

Numonyx® Omneo™ Phase Change Memory for embedded applications offers all of the best attributes from other memory types in a new, highly scalable and flexible technology.

Omneo™ P5Q PCM is a new type of nonvolatile semiconductor memory that stores information through a reversible structural phase change in a chalcogenide material. The material exhibits a change in material properties, both electrical and optical, when changed from the amorphous (disordered) to the polycrystalline (regularly ordered) state. In the case of Phase Change Memory, information is stored via the change in resistance the chalcogenide material experiences upon undergoing a phase change. The material also changes optical properties after experiencing a phase change, a characteristic that has been successfully mastered for use in current rewritable optical storage devices such as rewritable CDs and DVDs.

The Omneo™ P5Q PCM storage element consists of a thin film of chalcogenide contacted by a resistive heating element. In PCM, the phase change is induced in the memory cell by highly localized Joule heating caused by an induced current at the material junction. During a write operation, a small volume of the chalcogenide material is made to change phase. The phase change is a reversible process, and is modulated by the magnitude of injected current, the applied voltage, and the duration of the heating pulse.

Omneo™ P5Q PCM combines the benefits of traditional floating gate flash, both NOR-type and NAND-type, with some of the key attributes of RAM and EEpROM. Like NOR flash and RAM technology, PCM offers fast random access times. Like NAND flash, PCM has the ability to write moderately fast. And like RAM and EEpROM, PCM supports bit alterable writes (overwrite). Unlike flash, no separate erase step is required to change information from 0 to 1 and 1 to 0. Unlike RAM, however, the technology is nonvolatile with data retention comparable to NOR flash. However, at the current time, PCM technology appears to have a write cycling endurance better than that of NAND or NOR flash, but less than that of RAM.

Unlike other proposed alternative memories, Omneo™ P5Q PCM technology uses a conventional CMOS process with the addition of a few additional layers to form the memory storage element. Overall, the basic memory manufacturing process used to make PCM is less complex than that of NAND, NOR or DRAM.

Historically, systems have adopted many different types of memory to meet different needs within a design. Some systems might include boot memory, configuration memory, data storage memory, high speed execution memory, and dynamic working memory. The demands of many of today's designs require better performance from the memory subsystem and a reduction in the overall component count. PCM provides many of the attributes of different kinds of memory found in a typical design, enabling the opportunity to consolidate or eliminate of different types of memory.

1.2 Product Description

The Omneo™ P5Q PCM s a 128-Mbit (16 Mb x 8) SPI phase change memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

Omneo™ P5Q PCM product supports four new, high-performance dual and quad input/output instructions:

- Dual output fast read (DOFR) instruction used to read data at up to 66 MHz by using both DQ0 and DQ1 pins as outputs
- Quad output fast read (QOFR) instruction used to read data at up to 50 MHz by using DQ0, DQ1, DQ2(W) and DQ3(HOLD) pins as outputs
- Dual input fast program (DIFP) instruction used to program data at up to 66 MHz by using both DQ0 and DQ1 pins as inputs
- Quad input fast program (QIFP) instruction used to program data at up to 50 MHz by using DQ0, DQ1, DQ2(W) and DQ3(HOLD) pins as inputs

These new instructions double or quadruple the transfer bandwidth for read and program operations.

The memory can be programmed 1 to 64 bytes at a time, using the page program, dual input fast program and quad input fast program instructions.

The memory is organized as 128 sectors that are further divided into 1,024 pages each (131,072 pages in total).

For compatibility with flash memory devices, Omneo™ P5Q PCM supports sector erase (128-Kbyte sector) and bulk erase instructions.

It can be write protected by software using a mix of volatile and non-volatile protection features, depending on the application needs. The protection granularity is of 128 Kbytes (sector granularity).

Figure 1. Logic diagram

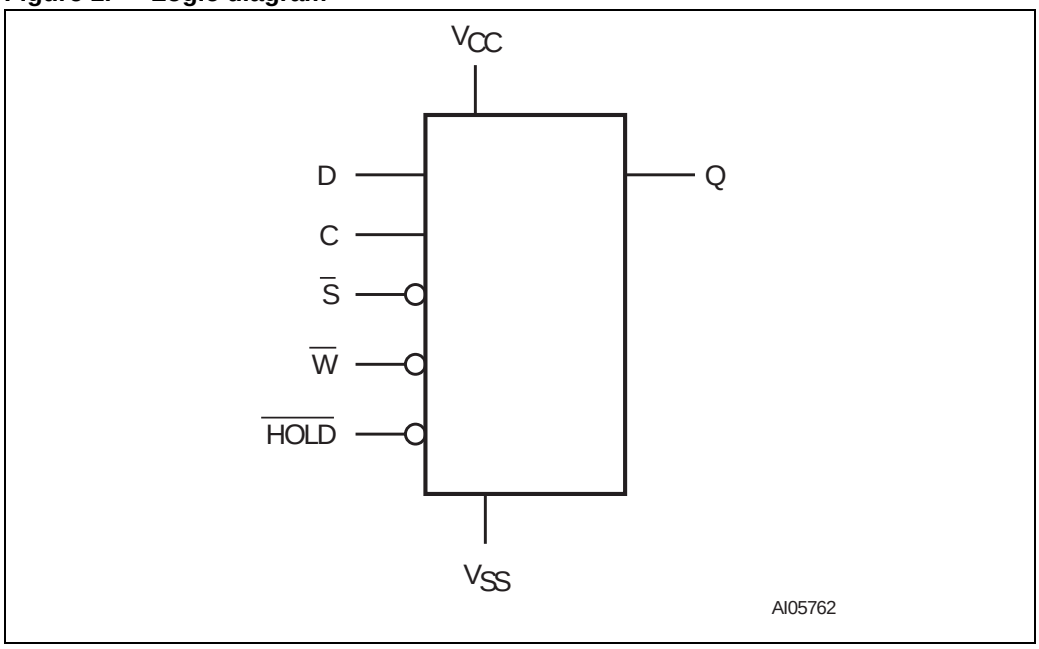
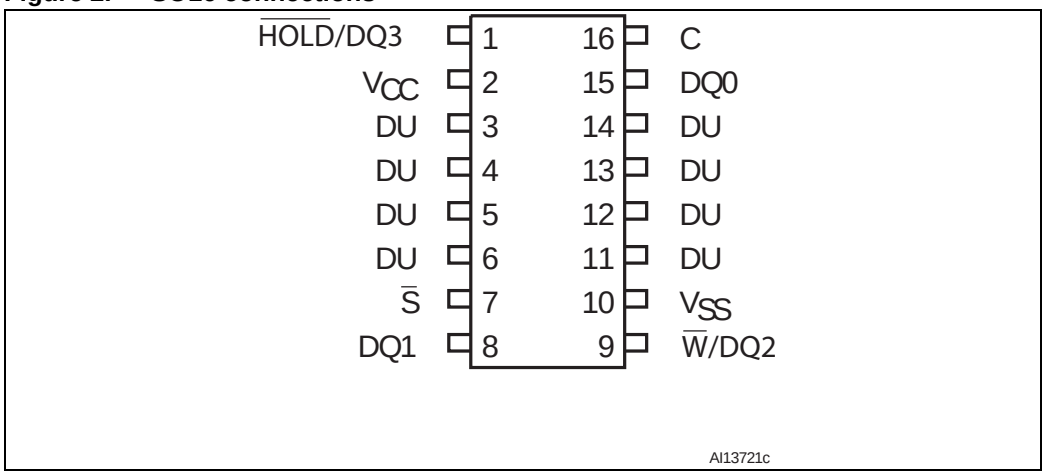


Table 1. Signal names

Signal Name	Standard x1 Mode		Dual Mode		Quad Mode	
	Function	Direction	Function	Direction	Function	Direction
C	Serial Clock	Input	Serial Clock	Input	Serial Clock	Input
D (DQ0)	Serial Data Input	Input	Serial Data Input/Output	I/O(1)	Serial Data Input/Output	I/O(1)
Q (DQ1)	Serial Data Output	Output	Serial Data Input/Output	I/O(1)	Serial Data Input/Output	I/O(1)
$\overline{S}$	Chip Select	Input	Chip Select	Input	Chip Select	Input
$\overline{W}$ (DQ2)	Write Protect	Input	Write Protect	Input	Serial Data Input/Output	I/O(1)
$\overline{HOLD}$ (DQ3)	Hold	Input	Hold	Input	Serial Data Input/Output	I/O(1)
V_{CC}	Supply voltage					
V_{SS}	Ground					

1. Serves as an input during Dual Input Fast Program (DIFP) and Quad Input Fast Program (QIFP) instructions. Serves as an output during Dual Output Fast Read (DOFR) and Quad Output Fast Read (QOFR) instructions.

Figure 2. SO16 connections



1. DU = don't use. User must float these pins.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.
3. For SO8 package solutions please contact your local Numonyx field representative.

2 Signal descriptions

2.1 Serial data input (D/DQ0)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

During the dual output fast read (DOFR) and quad output fast read (QOFR) instructions, this pin is used as an output (DQ0). Data is shifted out on the falling edge of the Serial Clock (C).

2.2 Serial data output (Q/DQ1)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

During the dual input fast program (DIFP) and quad input fast program (QIFP) instructions, this pin is used for data input (DQ1). It is latched on the rising edge of the Serial Clock (C).

During the dual output fast read (DOFR) and quad output fast read (QOFR) instructions, this pin is used as data output (DQ1). Data is shifted out on the falling edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at serial data input (DQ0) are latched on the rising edge of Serial Clock (C). Data on serial data output (DQ1) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and serial data output (DQ1) is at high impedance. Unless an internal program, erase, or write status register cycle is in progress, the device will be in the standby power mode. Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{\text{HOLD}}$/DQ3)

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without deselecting the device.

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

To start the hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) driven Low.

During the quad input fast program (QIFP) instruction, this pin is used for data input (DQ3). It is latched on the rising edge of the Serial Clock (C).

During the quad output fast read (QOFR) instructions, this pin is used for data output (DQ3). Data is shifted out on the falling edge of Serial Clock (C).

2.6 Write protect ($\overline{\text{W}}$/DQ2)

This input signal is used to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP3, BP2, BP1 and BP0 bits of the status register).

During the quad input fast program (QIFP) instruction, this pin is used for data input (DQ2). It is latched on the rising edge of the Serial Clock (C).

During the quad output fast read (QOFR) instructions, this pin is used for data output (DQ2). Data is shifted out on the falling edge of Serial Clock (C).

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

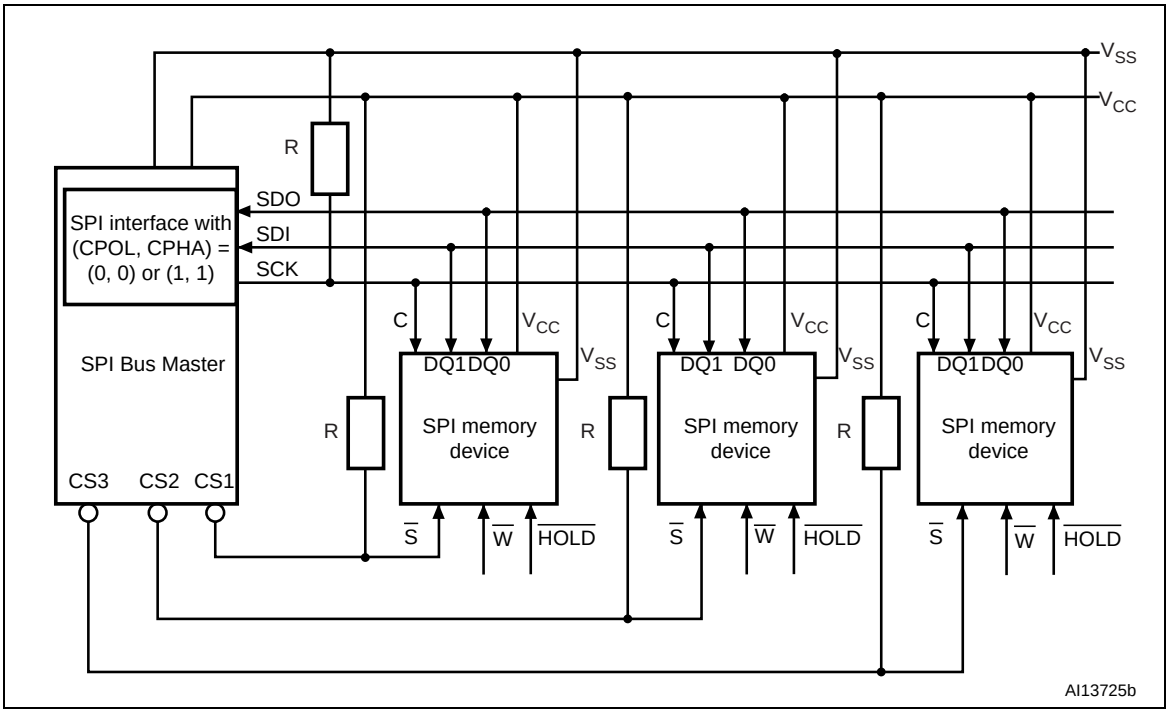
– CPOL=0, CPHA=0
– CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in standby mode and not transferring data:

– C remains at 0 for (CPOL=0, CPHA=0)
– C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. Bus master and memory devices on the SPI bus



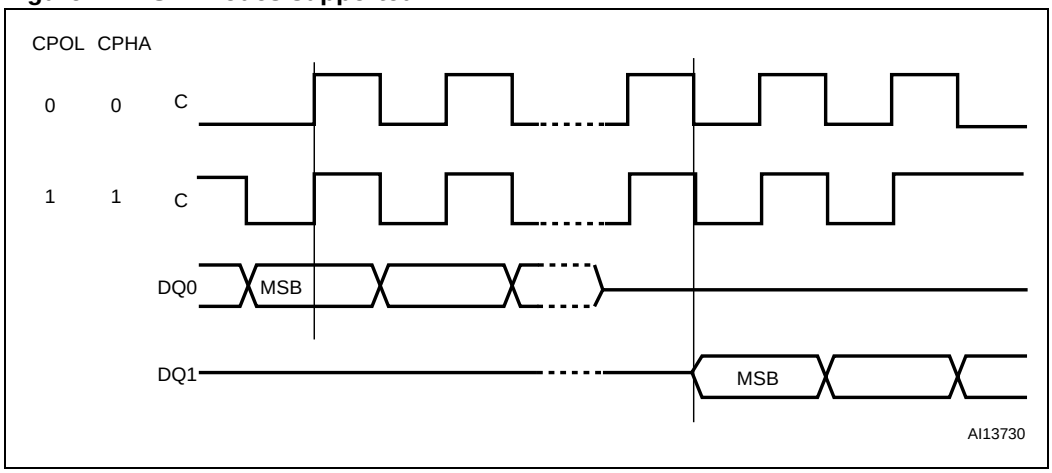
1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 3 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the serial data output (DQ1) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 3*) ensure that the Omneo™ P5Q PCM is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant $R*C_p$

(C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 4. SPI modes supported



4 Operating features

Note: *Definition of 'Program', 'Bit-alterable Write' and 'Program on All 1s':*

- ***Program*** *on Omneo™ P5Q PCM devices writes only 0s of the user data to the array and treats 1s as data masks. This is similar to programming on a floating gate flash device.*
- ***Bit-alterable Write*** *on Omneo™ P5Q PCM devices involves writing both 0s and 1s of the user data to the array.*
- ***Program on all 1s*** *is similar to 'program' where only 0s are written to the array and 1s are treated as data masks. Program on all 1s also requires that the entire page being written is previously set to all 1s. Program on all 1s is also referred to as PreSET Write.*

4.1 Page programming

To program/write one data byte, two instructions are required: write enable (WREN), which is one byte, and a page program (PP) sequence, which consists of four bytes plus data byte. This is followed by the internal program cycle (of duration t_{PP}).

To spread this overhead, the page program (PP) instruction allows up to 64 bytes to be programmed/written at a time, provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Page program (PP)* and *Table 16: AC characteristics*).

4.2 Dual input fast program

The dual input fast program (DIFP) instruction makes it possible to program/write up to 64 bytes using two input pins at the same time.

For optimized timings, it is recommended to use the dual input fast program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather than using several dual input fast program (DIFP) sequences each containing only a few bytes (see *Section 6.11: Dual input fast program (DIFP)*).

4.3 Quad input fast program

The quad input fast program (QIFP) instruction makes it possible to program/write up to 64 bytes using four input pins at the same time.

For optimized timings, it is recommended to use the quad input fast program (QIFP) instruction to program all consecutive targeted bytes in a single sequence rather than using several quad input fast program (QIFP) sequences each containing only a few bytes (see *Section 6.12: Quad input fast program (QIFP)*).

4.4 Sector erase and bulk erase

A sector can be erased to all 1s (FFh) at a time using the sector erase (SE) instruction. The entire memory can be erased using the bulk erase (BE) instruction. This starts an internal erase cycle (of duration t_{SE} or t_{BE}).

The erase instruction must be preceded by a write enable (WREN) instruction.

4.5 Polling during a write, program or erase cycle

A further improvement in the time to write status register (WRSR), page program (PP), dual input fast program (DIFP), quad input fast program (QIFP), or erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SMEN}, t_{SMEX}, t_{SE}, or t_{BE}). The write in progress (WIP) bit is provided in the status register so that the application program can monitor its value, polling it to establish when the previous write cycle, program cycle, or erase cycle is complete.

4.6 Active power and standby power

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write status register). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

4.7 Status register

The status register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.4: Read status register (RDSR)* for a detailed description of the status register bits.

4.8 Protection modes

There are protocol-related and specific hardware and software protection modes. They are described below.

4.8.1 Protocol-related protections

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the Omneo™ P5Q PCM features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification
- Program, erase, and write status register are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write disable (WRDI) instruction completion
  - Write status register (WRSR) instruction completion
  - Page program (PP) instruction completion
  - Dual input fast program (DIFP) instruction completion
  - Quad input fast program (QIFP) instruction completion
  - Sector erase (SE) instruction completion
  - Bulk erase (BE) instruction completion
- The Block Protect bits (see *Section 6.4.3: BP3, BP2, BP1, BP0 bits*) and top/bottom bit (see *Section 6.4.4: Top/bottom bit*) allow part of the memory to be configured as read-only. This is the Software Protect Mode (SPM).
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP3, BP2, BP1, BP0) bits, Top/Bottom (TB) bit and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM). For more details, see *Section 6.5: Write status register (WRSR)*.

Table 2. Protected area sizes

Status register contents					Memory content	
TB bit	BP bit 3	BP bit 2	BP bit 1	BP bit 0	Protected area	Unprotected area
0	0	0	0	0	none	All sectors(1) (Sectors 0 to 127)
0	0	0	0	1	Upper 128th (Sector 127)	Sectors 0 to 126
0	0	0	1	0	Upper 64th (Sectors 126 to 127)	Sectors 0 to 125
0	0	0	1	1	Upper 32nd (Sectors 124 to 127)	Sectors 0 to 123
0	0	1	0	0	Upper 16th (Sectors 120 to 127)	Sectors 0 to 119
0	0	1	0	1	Upper 8th (Sectors 112 to 127)	Sectors 0 to 111
0	0	1	1	0	Upper quarter (Sectors 96 to 127)	Sectors 0 to 95
0	0	1	1	1	Upper half (Sectors 64 to 127)	Sectors 0 to 63
0	1	X(2)	X(2)	X(2)	All sectors (Sectors 0 to 127)	None
1	0	0	0	0	none	All sectors(1) (Sectors 0 to 127)
1	0	0	0	1	Lower 128th (Sector 0)	Sectors 1 to 127
1	0	0	1	0	Lower 64th (Sectors 0 to 1)	Sectors 2 to 127
1	0	0	1	1	Lower 32nd (Sectors 0 to 3)	Sectors 4 to 127
1	0	1	0	0	Lower 16th (Sectors 0 to 7)	Sectors 8 to 127
1	0	1	0	1	Lower 8th (Sectors 0 to15)	Sectors 16 to 127
1	0	1	1	0	Lower 4th (Sectors 0 to 31)	Sectors 32 to 127
1	0	1	1	1	Lower half (Sectors 0 to 63)	Sectors 64 to 127
1	1	X(2)	X(2)	X(2)	All sectors (Sectors 0 to 127)	None

1. The device is ready to accept a bulk erase instruction if, and only if, all block protect (BP3, BP2, BP1, BP0) are 0
2. X can be 0 or 1

4.9 Hold condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any write status register, program or erase cycle that is currently in progress.

To enter the hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) Low.

The hold condition starts on the falling edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in *Figure 5*).

The hold condition ends on the rising edge of the Hold ($\overline{\text{HOLD}}$) signal, provided that this coincides with Serial Clock (C) being Low.

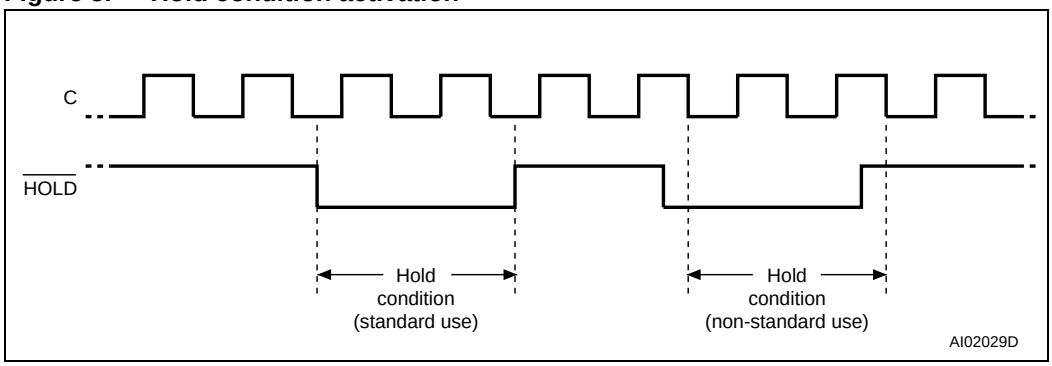
If the falling edge does not coincide with Serial Clock (C) being Low, the hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the hold condition ends after Serial Clock (C) next goes Low (this is shown in *Figure 5*).

During the hold condition, the serial data output (DQ1) is high impedance, and serial data input (DQ0) and Serial Clock (C) are don't care.

Normally, the device is kept selected, with Chip Select ($\overline{\text{S}}$) driven Low, for the whole duration of the hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the hold condition.

If Chip Select ($\overline{\text{S}}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{\text{HOLD}}$) High, and then to drive Chip Select ($\overline{\text{S}}$) Low. This prevents the device from going back to the hold condition.

Figure 5. Hold condition activation



5 Memory organization

The memory is organized as:

- 16,772,216 bytes (8 bits each)
- 8 Super Page programming regions (16 sectors each)
- 128 sectors (128 Kbytes each)
- 262,144 pages (64 bytes each)

Each page can be individually programmed (bits are programmed from ‘1’ to ‘0’) or written (bit alterable: ‘1’ can be altered to ‘0’ and ‘0’ can be altered to ‘1’). The device is sector or bulk erasable (bits are erased from ‘0’ to ‘1’).

Table 3. Memory organization

Sector	Address range		Sector	Address range	
127	FE0000	FFFFFF	102	CC0000	CDFFFF
126	FC0000	FDFFFF	101	CA0000	CBFFFF
125	FA0000	FBFFFF	100	C80000	C9FFFF
124	F80000	F9FFFF	99	C60000	C7FFFF
123	F60000	F7FFFF	98	C40000	C5FFFF
122	F40000	F5FFFF	97	C20000	C3FFFF
121	F20000	F3FFFF	96	C00000	C1FFFF
120	F00000	F1FFFF	95	BE0000	BFFFFF
119	EE0000	EFFFFF	94	BC0000	BDFFFF
118	EC0000	EDFFFF	93	BA0000	BBFFFF
117	EA0000	EBFFFF	92	B80000	B9FFFF
116	E80000	E9FFFF	91	B60000	B7FFFF
115	E60000	E7FFFF	90	B40000	B5FFFF
114	E40000	E5FFFF	89	B20000	B3FFFF
113	E20000	E3FFFF	88	B00000	B1FFFF
112	E00000	E1FFFF	87	AE0000	AFFFFF
111	DE0000	DFFFFF	86	AC0000	ADFFFF
110	DC0000	DDFFFF	85	AA0000	ABFFFF
109	DA0000	DBFFFF	84	A80000	A9FFFF
108	D80000	D9FFFF	83	A60000	A7FFFF
107	D60000	D7FFFF	82	A40000	A5FFFF
106	D40000	D5FFFF	81	A20000	A3FFFF
105	D20000	D3FFFF	80	A00000	A1FFFF
104	D00000	D1FFFF	79	9E0000	9FFFFF
103	CE0000	CFFFFF	78	9C0000	9DFFFF

Table 3. Memory organization (continued)

Sector	Address range		Sector	Address range	
77	9A0000	9BFFFF	42	540000	55FFFF
76	980000	99FFFF	41	520000	53FFFF
75	960000	97FFFF	40	500000	51FFFF
74	940000	95FFFF	39	4E0000	4FFFFF
73	920000	93FFFF	38	4C0000	4DFFFF
72	900000	91FFFF	37	4A0000	4BFFFF
71	8E0000	8FFFFF	36	480000	49FFFF
70	8C0000	8DFFFF	35	460000	47FFFF
69	8A0000	8BFFFF	34	440000	45FFFF
68	880000	89FFFF	33	420000	43FFFF
67	860000	87FFFF	32	400000	41FFFF
66	840000	85FFFF	31	3E0000	3FFFFF
65	820000	83FFFF	30	3C0000	3DFFFF
64	800000	81FFFF	29	3A0000	3BFFFF
63	7E0000	7FFFFF	28	380000	39FFFF
62	7C0000	7DFFFF	27	360000	37FFFF
61	7A0000	7BFFFF	26	340000	35FFFF
60	780000	79FFFF	25	320000	33FFFF
59	760000	77FFFF	24	300000	31FFFF
58	740000	75FFFF	23	2E0000	2FFFFF
57	720000	73FFFF	22	2C0000	2DFFFF
56	700000	71FFFF	21	2A0000	2BFFFF
55	6E0000	6FFFFF	20	280000	29FFFF
54	6C0000	6DFFFF	19	260000	27FFFF
53	6A0000	6BFFFF	18	240000	25FFFF
52	680000	69FFFF	17	220000	23FFFF
51	660000	67FFFF	16	200000	21FFFF
50	640000	65FFFF	15	1E0000	1FFFFF
49	620000	63FFFF	14	1C0000	1DFFFF
48	600000	61FFFF	13	1A0000	1BFFFF
47	5E0000	5FFFFF	12	180000	19FFFF
46	5C0000	5DFFFF	11	160000	17FFFF
45	5A0000	5BFFFF	10	140000	15FFFF
44	580000	59FFFF	9	120000	13FFFF
43	560000	57FFFF	8	100000	11FFFF

Table 3. Memory organization (continued)

Sector	Address range			Sector	Address range	
7	0E0000	0FFFFF		3	060000	07FFFF
6	0C0000	0DFFFF		2	040000	05FFFF
5	0A0000	0BFFFF		1	020000	03FFFF
4	080000	09FFFF		0	000000	01FFFF

Table 4. Organization of Super Page regions

Programming Region	Sectors	Address Range
7	112 to 127	E00000 to FFFFFF
6	96 to 111	C00000 to DFFFFF
5	80 to 95	A00000 to BFFFFF
4	64 to 79	800000 to 9FFFFF
3	48 to 63	600000 to 7FFFFF
2	32 to 47	400000 to 5FFFFF
1	16 to 31	200000 to 3FFFFF
0	0 to 15	000000 to 1FFFFF

6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial data input DQ0 is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on serial data input DQ0, each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 5*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a read data bytes (READ), read data bytes at higher speed (FAST_READ), dual output fast read (DOFR), quad output fast read (QOFR), read status register (RDSR) or read identification (RDID) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (S) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a page program (PP), dual input fast program (DIFP), quad input fast program (QIFP), sector erase (SE), bulk erase (BE), write status register (WRSR), write enable (WREN), write disable (WRDI), Chip Select (S) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (S) must driven High when the number of clock pulses after Chip Select (S) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a write status register cycle, program cycle erase cycle are ignored, and the internal write status register cycle, program cycle, erase cycle continues unaffected.

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Table 5. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID	Read identification	1001 1111	9Fh	0	0	1 to 3
		1001 1110	9Eh	0	0	1 to 3
RDSR	Read status register	0000 0101	05h	0	0	1 to ∞
WRSR	Write status register	0000 0001	01h	0	0	1
READ	Read data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
DOFR	Dual output fast read	0011 1011	3Bh	3	1	1 to ∞
QOFR	Quad output fast read	0110 1011	6Bh	3	1	1 to ∞
PP	Page program (Legacy Program)	0000 0010	02h	3	0	1 to 64
	Page program (Bit-alterable write)	0010 0010	22h	3	0	1 to 64
	Page program (On all 1s)	1101 0001	D1h	3	0	1 to 64
DIFP	Dual input fast program (Legacy Program)	1010 0010	A2h	3	0	1 to 64
	Dual input fast program (Bit-alterable write)	1101 0011	D3h	3	0	1 to 64
	Dual input fast program (On all 1s)	1101 0101	D5h	3	0	1 to 64
QIFP	Quad input fast program (Legacy Program)	0011 0010	32h	3	0	1 to 64
	Quad input fast program (Bit-alterable write)	1101 0111	D7h	3	0	1 to 64
	Quad input fast program (On all 1s)	1101 1001	D9h	3	0	1 to 64
SE	Sector erase	1101 1000	D8h	3	0	0
BE	Bulk erase (2)	1100 0111	C7h	0	0	0

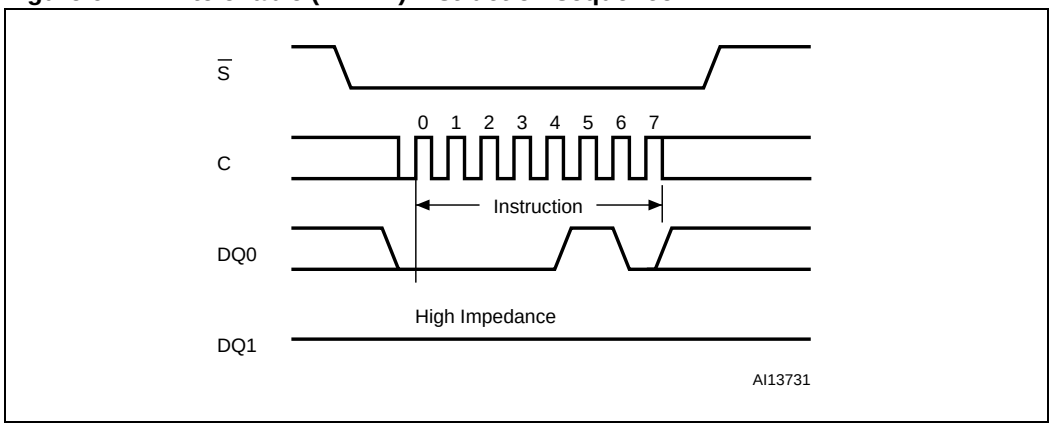
6.1 Write enable (WREN)

The write enable (WREN) instruction (*Figure 6*) sets the write enable latch (WEL) bit.

The write enable latch (WEL) bit must be set prior to every page program (PP), dual input fast program (DIFP), sector erase (SE), bulk erase (BE), write status register (WRSR) instruction.

The write enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 6. Write enable (WREN) instruction sequence



6.2 Write disable (WRDI)

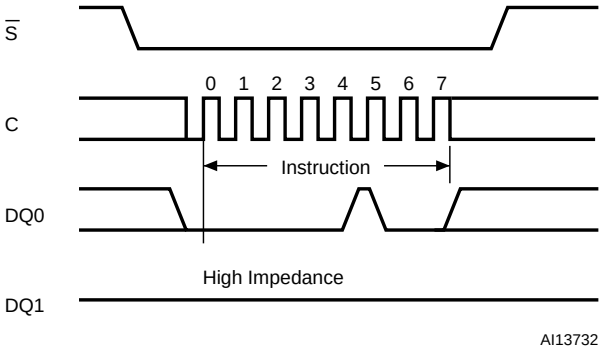
The write disable (WRDI) instruction (*Figure 7*) resets the write enable latch (WEL) bit.

The write disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The write enable latch (WEL) bit is reset under the following conditions:

- Power-up
- Write disable (WRDI) instruction completion
- Write status register (WRSR) instruction completion
- Page program (PP) instruction completion
- Dual input fast program (DIFP) instruction completion
- Quad input fast program (QIFP) instruction completion
- Sector erase (SE) instruction completion
- Bulk erase (BE) instruction completion

Figure 7. Write disable (WRDI) instruction sequence



6.3 Read identification (RDID)

The read identification (RDID) instruction allows to read the device identification data:

- Manufacturer identification (1 byte)
- Device identification (2 bytes)

The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx.

Any read identification (RDID) instruction while an erase or program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. After this, the 24-bit device identification stored in the memory will be shifted out on serial data output (DQ1). Each bit is shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 8*.

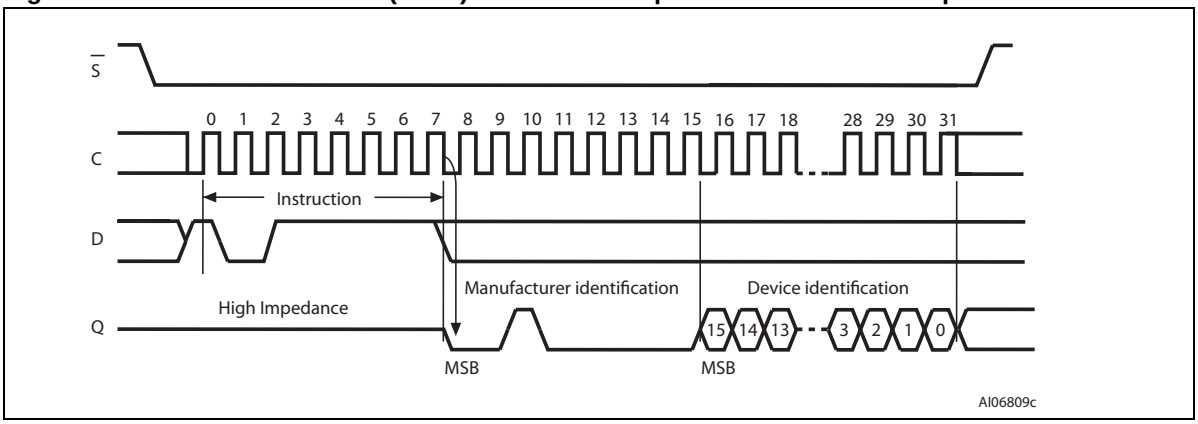
The read identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 6. Read identification (RDID) data-out sequence

Manufacturer identification	Device identification	
	Memory Type (Upper Byte)	Memory Capacity (Lower Byte)
20h	DAh	18h

Figure 8. Read identification (RDID) instruction sequence and data-out sequence

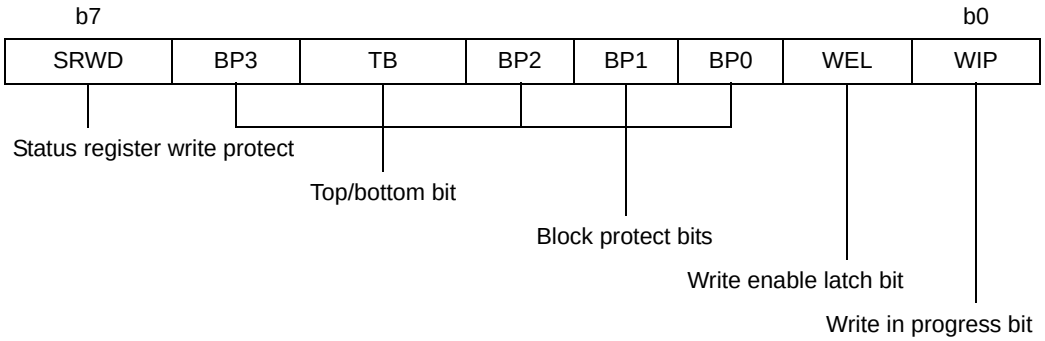


6.4 Read status register (RDSR)

The read status register (RDSR) instruction allows the status register to be read. The status register may be read at any time, even while a program, erase, write status register cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new instruction to the device. It is also possible to read the status register continuously, as shown in *Figure 9*.

RDSR is the only instruction accepted by the device while a program, erase, write status register operation is in progress.

Table 7. Status register format



The status and control bits of the status register are as follows:

6.4.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write status register, program, erase cycle. When set to ‘1’, such a cycle is in progress, when reset to ‘0’ no such cycle is in progress.

While WIP is ‘1’, RDSR is the only instruction the device will accept; all other instructions are ignored.

6.4.2 WEL bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When set to ‘1’ the internal write enable latch is set, when set to ‘0’ the internal write enable latch is reset and no write status register, program, erase instruction is accepted.

6.4.3 BP3, BP2, BP1, BP0 bits

The block protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against program (or write) and erase instructions. These bits are written with the write status register (WRSR) instruction. When one or more of the block protect (BP3, BP2, BP1, BP0) bits is set to ‘1’, the relevant memory area (as defined in *Table 2*) becomes protected against page program (PP), dual input fast program (DIFP),quad input fast program (QIFP), and sector erase (SE) instructions. The block protect (BP3, BP2, BP1, BP0) bits can be written provided that the hardware protected mode has not been set.The bulk erase (BE) instruction is executed if, and only if, all block protect (BP3, BP2, BP1, BP0) bits are 0.

6.4.4 Top/bottom bit

The top/bottom (TB) bit is non-volatile. It can be set and reset with the write status register (WRSR) instruction provided that the write enable (WREN) instruction has been issued. The top/bottom (TB) bit is used in conjunction with the block protect (BP0, BP1, BP2, BP3) bits to determine if the protected area defined by the block protect bits starts from the top or the bottom of the memory array:

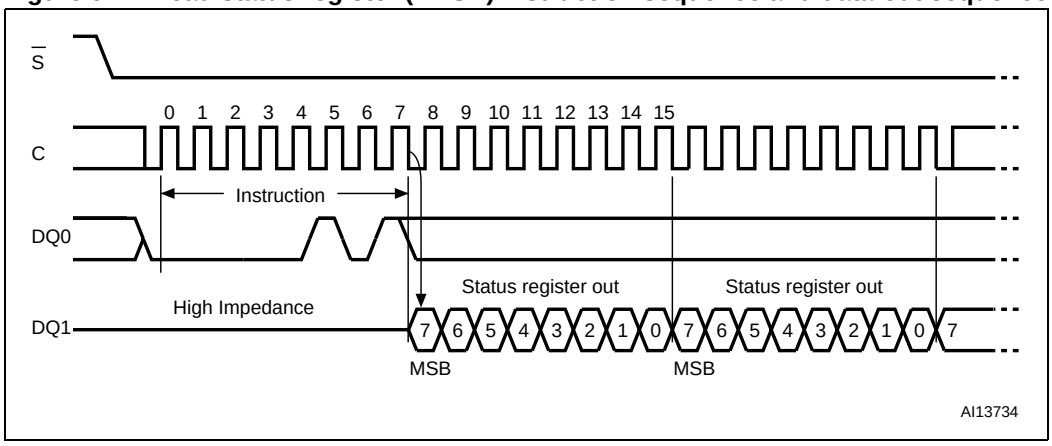
– When top/bottom bit is reset to ‘0’ (default value), the area protected by the block protect bits starts from the top of the memory array (see *Table 2: Protected area sizes*)
– When top/bottom bit is set to ‘1’, the area protected by the block protect bits starts from the bottom of the memory array (see *Table 2: Protected area sizes*).

The top/bottom bit cannot be written when the SRWD bit is set to ‘1’ and the $\overline{W}$ pin is driven Low.

6.4.5 SRWD bit

The status register write disable (SRWD) bit is operated in conjunction with the write protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and the write protect ($\overline{W}$) signal allow the device to be put in the hardware protected mode (when the status register write disable (SRWD) bit is set to ‘1’, and write protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the status register (SRWD, TB, BP3, BP2, BP1, BP0) become read-only bits and the write status register (WRSR) instruction is no longer accepted for execution.

Figure 9. Read status register (RDSR) instruction sequence and data-out sequence



6.5 Write status register (WRSR)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded and executed, the device sets the write enable latch (WEL).

The write status register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on serial data input (DQ0).

The instruction sequence is shown in *Figure 10*.

The write status register (WRSR) instruction has no effect on b1 and b0 of the status register.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the write status register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed write status register cycle (whose duration is t_W) is initiated. While the write status register cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed write status register cycle, and is 0 when it is completed. When the cycle is completed, the write enable latch (WEL) is reset.

The write status register (WRSR) instruction allows the user to change the values of the block protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 2*. The write status register (WRSR) instruction also allows the user to set and reset the status register write disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the hardware protected mode (HPM). The write status register (WRSR) instruction is not executed once the hardware protected mode (HPM) is entered.

Read Status Register (RDSR) is the only instruction accepted while WRSR operation is in progress; all other instructions are ignored.

Figure 10. Write status register (WRSR) instruction sequence

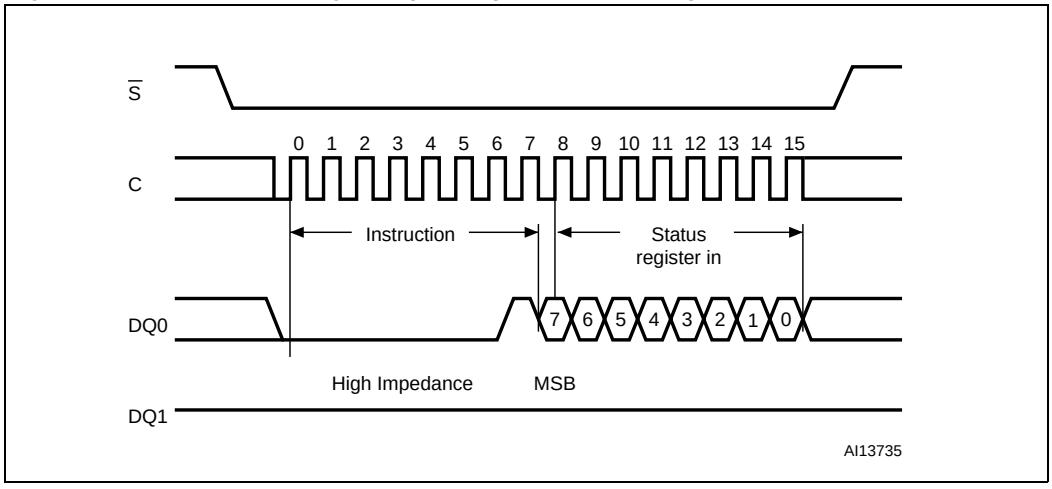


Table 8. Protection modes

$\overline{W}$	SRWD bit	Mode	Write protection of the status register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software protected (SPM)	Status register is writable (if the WREN instruction has set the WEL bit) The values in the SRWD, TB, BP3, BP2, BP1 and BP0 bits can be changed	Protected against page program, sector erase, and bulk erase	Ready to accept page program, and sector erase instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status register is hardware write protected The values in the SRWD, TB, BP3, BP2, BP1 and BP0 bits cannot be changed	Protected against page program, sector erase, and bulk erase	Ready to accept page program, and sector erase instructions

1. As defined by the values in the block protect (BP3, BP2, BP1, BP0) bits of the status register, as shown in *Table 2*.

The protection features of the device are summarized in *Table 8*.

When the status register write disable (SRWD) bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the status register write disable (SRWD) bit of the status register is set to ‘1’, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

– If Write Protect ($\overline{W}$) is driven High, it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction.

– If write protect ($\overline{W}$) is driven Low, it is not possible to write to the status register even if the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction (attempts to write to the status register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the block protect (BP3, BP2, BP1, BP0) bits of the status register, are also hardware protected against data modification.

Regardless of the order of the two events, the hardware protected mode (HPM) can be entered:

– by setting the status register write disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low

– or by driving Write Protect ($\overline{W}$) Low after setting the status register write disable (SRWD) bit.

The only way to exit the hardware protected mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the hardware protected mode (HPM) can never be activated, and only the software protected mode (SPM), using the block protect (BP3, BP2, BP1, BP0) bits of the status register, can be used.

6.6 Read data bytes (READ)

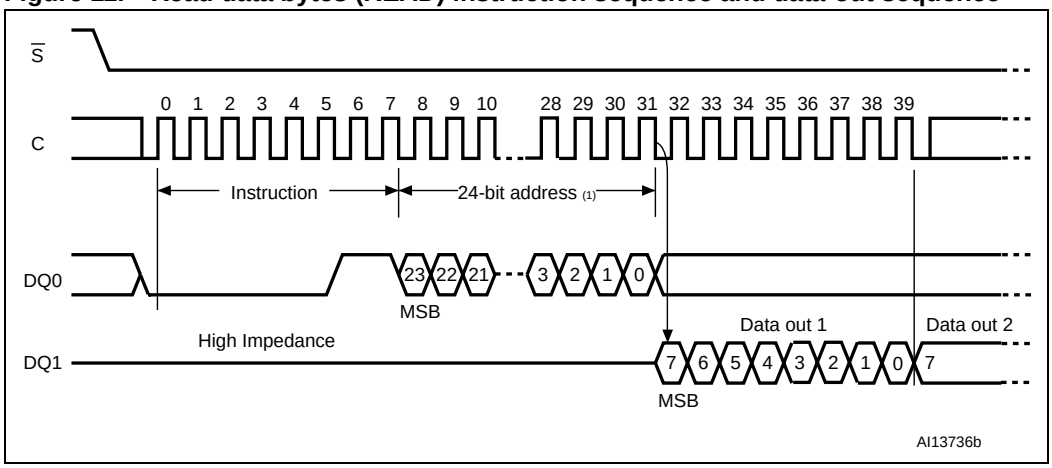
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes (READ) instruction is followed by a 3-byte address A[23:0], each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on serial data output (DQ1), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 11*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes (READ) instruction, while an erase, program, write is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 11. Read data bytes (READ) instruction sequence and data-out sequence



6.7 Read data bytes at higher speed (FAST_READ)

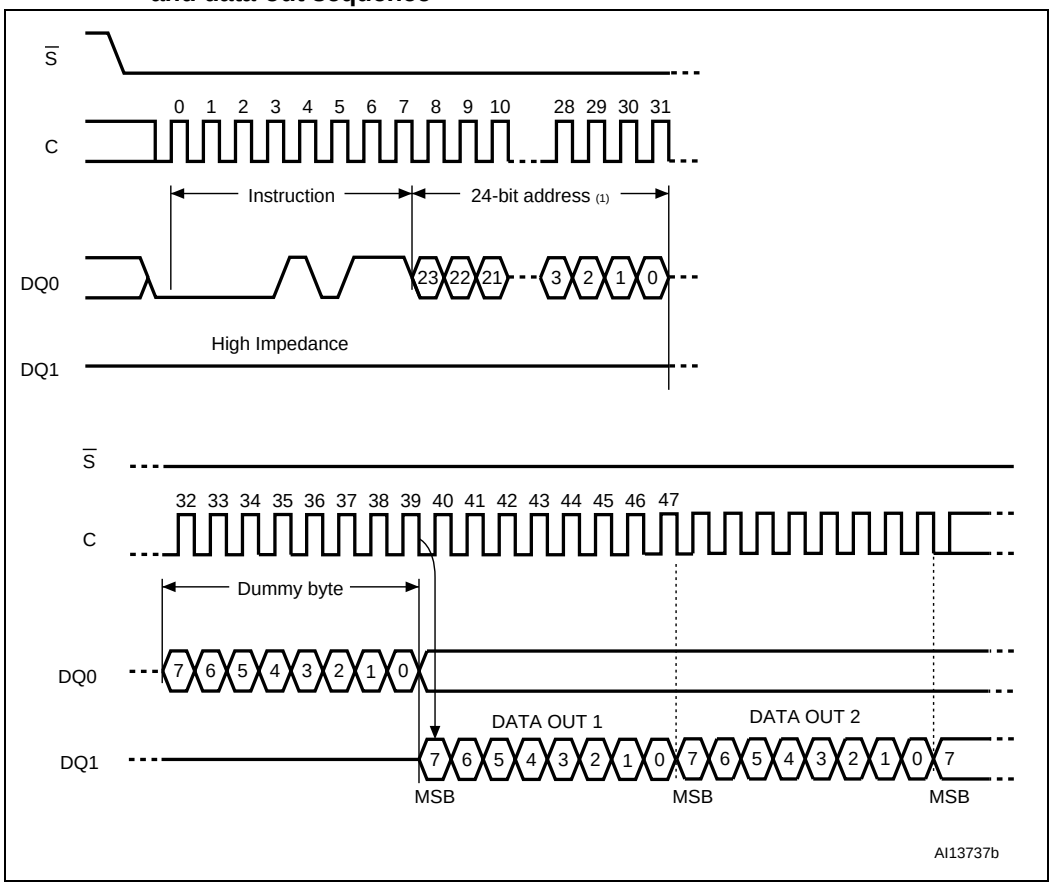
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes at higher speed (FAST_READ) instruction is followed by a 3-byte address A[23:0] and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on serial data output (DQ1) at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 12*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes at higher speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The read data bytes at higher speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes at higher speed (FAST_READ) instruction, while an erase, program, write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read data bytes at higher speed (FAST_READ) instruction sequence and data-out sequence



6.8 Dual output fast read (DOFR)

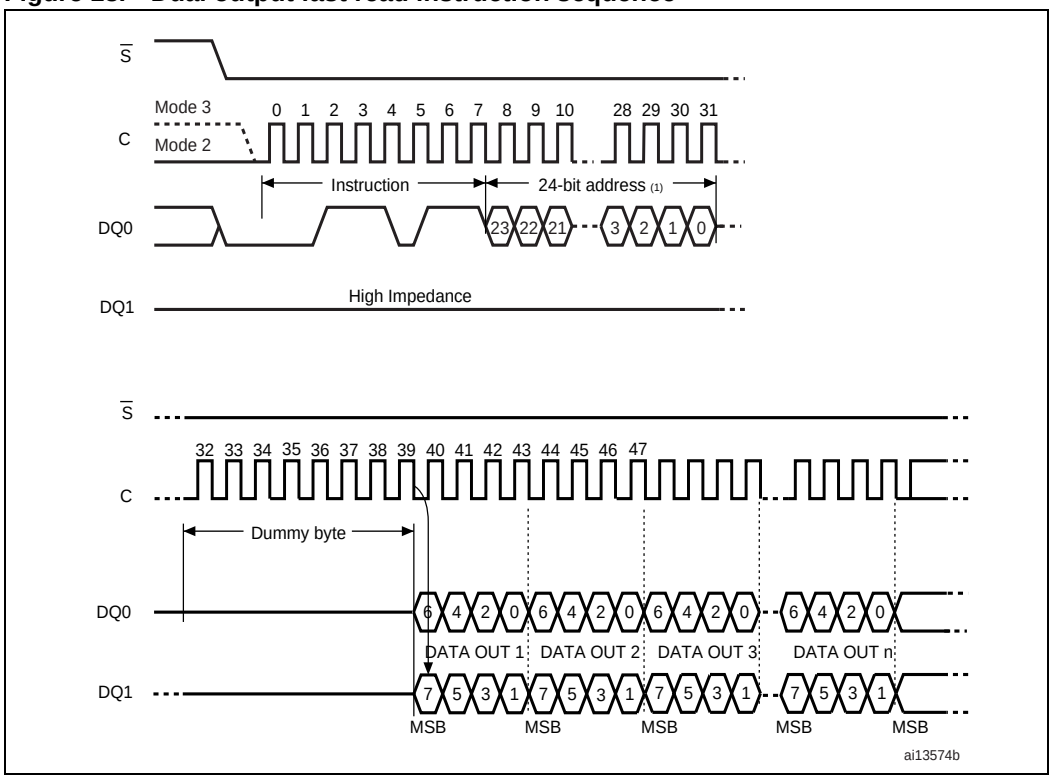
The dual output fast read (DOFR) instruction is very similar to the read data bytes at higher speed (FAST_READ) instruction, except that the data are shifted out on two pins (pin DQ0 and pin DQ1) instead of only one. Outputting the data on two pins instead of one doubles the data transfer bandwidth compared to the read data bytes at higher speed (FAST_READ) instruction.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the dual output fast read instruction is followed by a 3-byte address A[23:0] and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on DQ0 and DQ1 at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 13*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out on DQ0 and DQ1. The whole memory can, therefore, be read with a single dual output fast read (DOFR) instruction. When the highest address is reached, the address counter rolls over to 00 0000h, so that the read sequence can be continued indefinitely.

Figure 13. Dual output fast read instruction sequence



6.9 Quad output fast read (QOFR)

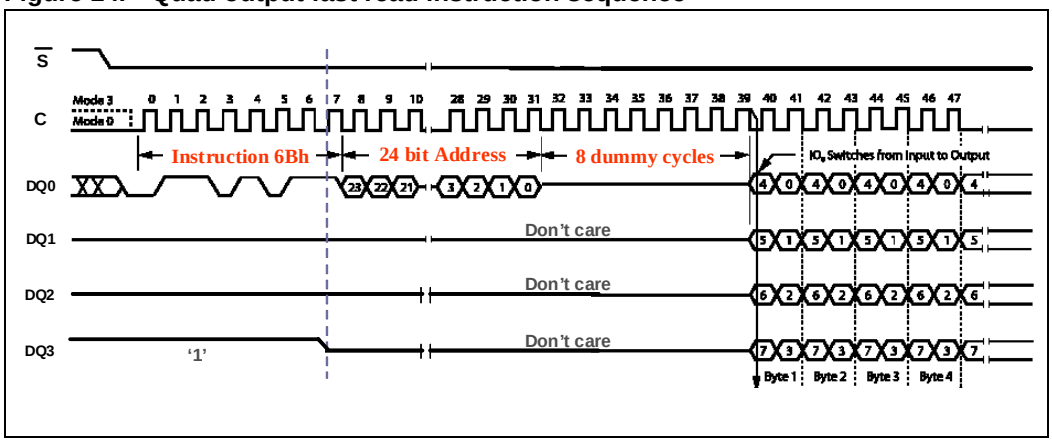
The quad output fast read (QOFR) instruction is very similar to the read data bytes at higher speed (FAST_READ) instruction, except that the data are shifted out on four pins (pins DQ0, DQ1, DQ2 and DQ3) instead of only one. Outputting the data on four pins instead of one quadruples the data transfer bandwidth compared to the read data bytes at higher speed (FAST_READ) instruction.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the quad output fast read instruction is followed by a 3-byte address A[23:0] and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, are shifted out on DQ0, DQ1, DQ2 and DQ3 at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 14*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out on DQ0, DQ1, DQ2 and DQ3. The whole memory can, therefore, be read with a single quad output fast read (QOFR) instruction. When the highest address is reached, the address counter rolls over to 00 0000h, so that the read sequence can be continued indefinitely.

Figure 14. Quad output fast read instruction sequence



1. After 40 clock cycles (cycle labeled 39 in the figured), data inputs (DQi) must be released because they become outputs.
2. Once 6Bh command is recognized, $\overline{W}$ and $\overline{HOLD}$ functionality is automatically disabled.

6.10 Page program (PP)

Note: This definition applies to all flavors of Page Program: Legacy Program, Bit-alterable Write and Program on all 1s.

The page program (PP) instruction allows bytes to be programmed/written in the memory. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (DQ0). If the 6 least significant address bits (A5-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 6 least significant bits (A5-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 15*.

If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are guaranteed to be programmed/written correctly within the same page. If less than 64 data bytes are sent to device, they are correctly programmed/written at the requested addresses without having any effects on the other bytes of the same page. (With Program on all 1s, the entire page should already have been set to all 1s (FFh).)

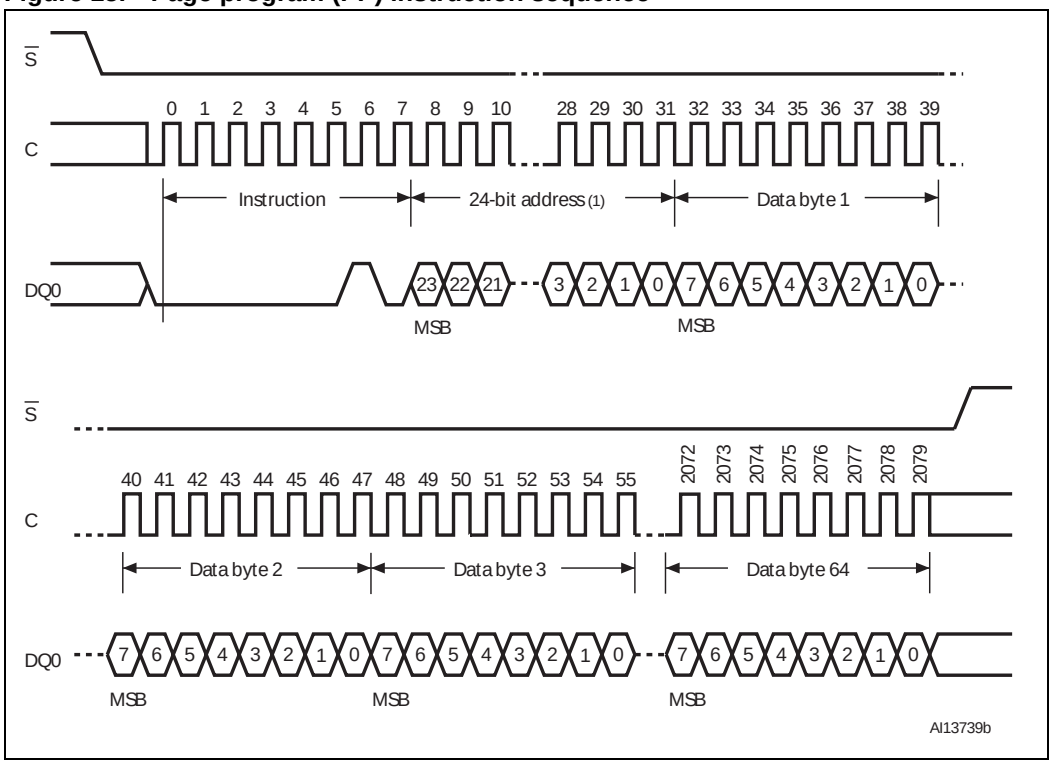
For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Table 16: AC characteristics*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the page program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the page program cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset. RDSR is the only instruction accepted while a Page Program operation is in progress; all other instructions are ignored.

A page program (PP) instruction applied to a page which is protected by the block protect (BP3, BP2, BP1, BP0) bits (see *Table 2* and *Table 3*) is not executed.

Figure 15. Page program (PP) instruction sequence



6.11 Dual input fast program (DIFP)

Note: This definition applies to all flavors of Dual input fast program: Legacy Program, Bit-alterable Write and Program on all 1s.

The dual input fast program (DIFP) instruction is very similar to the page program (PP) instruction, except that the data are entered on two pins (pin DQ0 and pin DQ1) instead of only one. Inputting the data on two pins instead of one doubles the data transfer bandwidth compared to the page program (PP) instruction.

The dual input fast program (DIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (DQ0).

If the 6 least significant address bits (A5-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 6 least significant bits (A5-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 16*.

If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are guaranteed to be programmed/written correctly within the same page. If less than 64 data bytes are sent to device, they are correctly programmed/written at the requested addresses without having any effects on the other bytes in the same page. (With Program on all 1s, the entire page should already have been set to all 1s (FFh).)

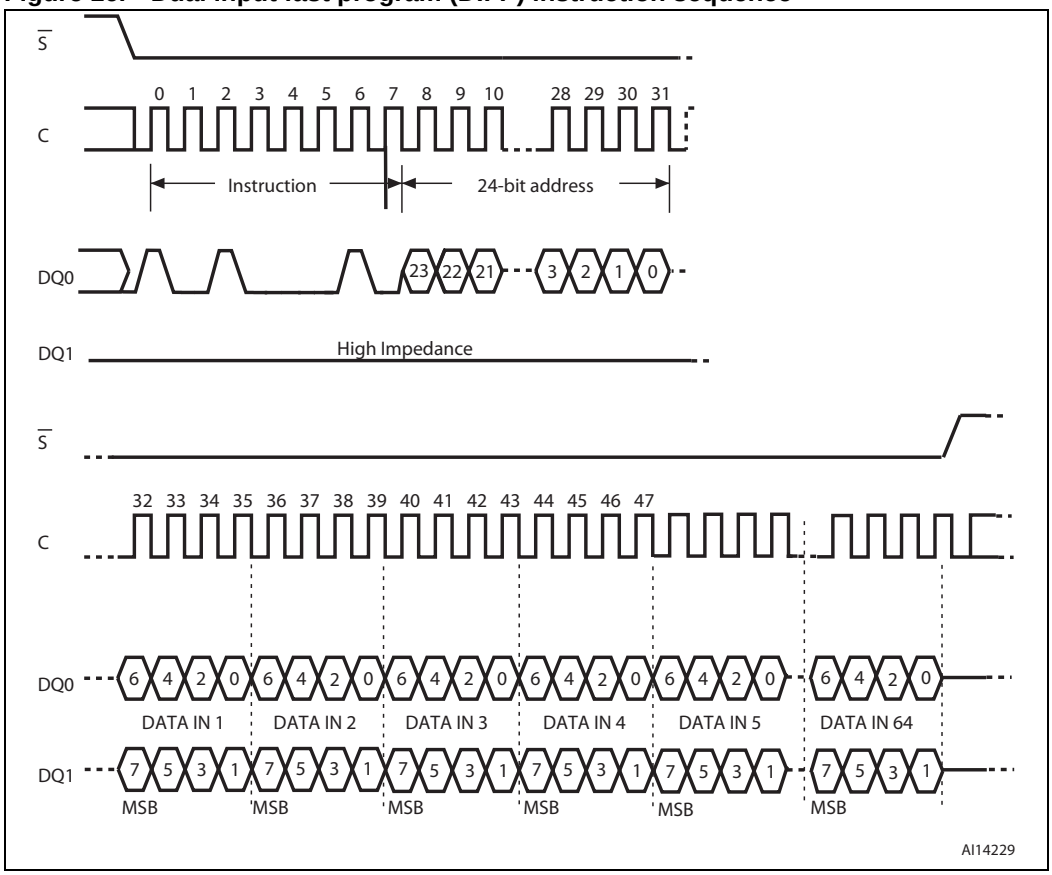
For optimized timings, it is recommended to use the dual input fast program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several dual input fast program (DIFP) sequences each containing only a few bytes (see *Table 16: AC characteristics*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the dual input fast program (DIFP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the dual input fast program (DIFP) cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset. RDSR is the only instruction accepted while a dual input fast program operation is in progress; all other instructions are ignored.

A dual input fast program (DIFP) instruction applied to a page that is protected by the block protect (BP3, BP2, BP1, BP0) bits (see *Table 2*) is not executed.

Figure 16. Dual input fast program (DIFP) instruction sequence



6.12 Quad input fast program (QIFP)

Note: The following description applies to all flavors of Quad input fast program: Legacy Program, Bit-alterable Write and Program on all 1s.

The quad input fast program (QIFP) instruction is very similar to the page program (PP) instruction, except that the data are entered on four pins (pin DQ0, DQ1, DQ2 and DQ3) instead of only one. Inputting the data on four pins instead of one quadruples the data transfer bandwidth compared to the page program (PP) instruction.

The quad input fast program (QIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on serial data input (DQ0).

If the 6 least significant address bits (A5-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 6 least significant bits (A5-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 17*.

If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are guaranteed to be programmed correctly within the same page. If less than 64 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes in the same page. (With Program on all 1s, the entire page should already have been set to all 1s (FFh).)

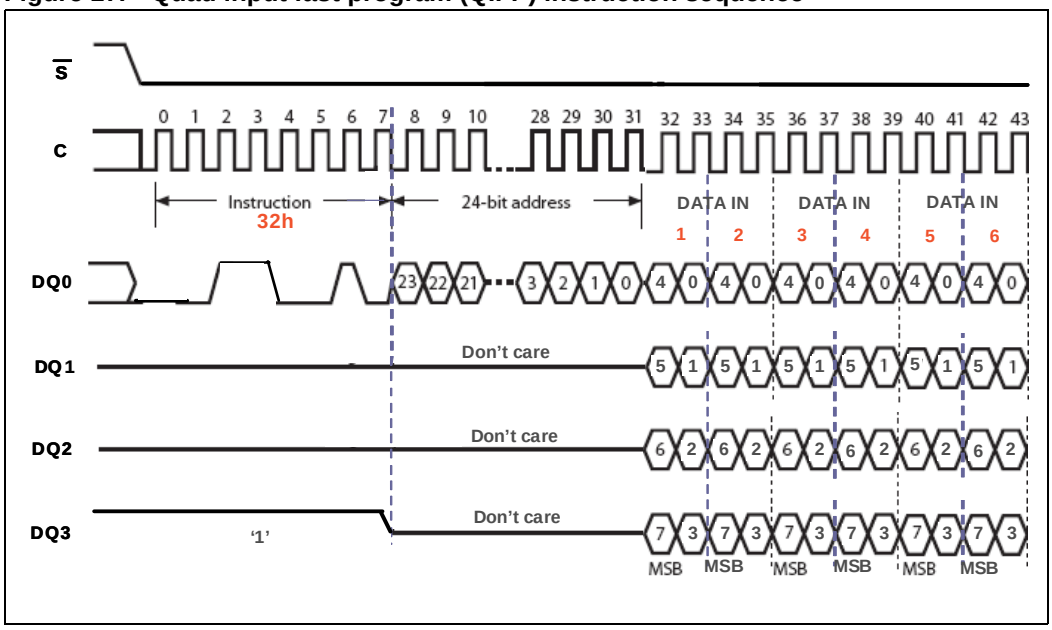
For optimized timings, it is recommended to use the quad input fast program (QIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several quad input fast program (QIFP) sequences each containing only a few bytes (see *Table 16: AC characteristics*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the quad input fast program (QIFP) instruction is not executed

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the quad input fast program (DIFP) cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset. RDSR is the only instruction accepted while a quad input fast program operation is in progress; all other instructions are ignored.

A quad input fast program (QIFP) instruction applied to a page that is protected by the block protect (BP3, BP2, BP1, BP0) bits (see *Table 2*) is not executed

Figure 17. Quad input fast program (QIFP) instruction sequence



1. Once 32h is recognized, $\overline{W}$ and $\overline{HOLD}$ functionality is automatically disabled.

6.13 Sector erase (SE)

The sector erase (SE) instruction sets to '1' (FFh) all bits inside the chosen sector. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

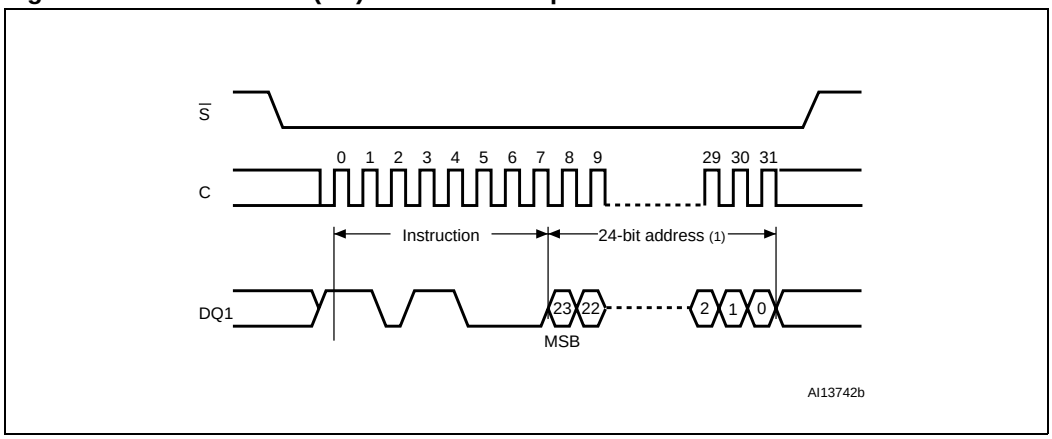
The sector erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on serial data input (DQ0). Any address inside the sector (see *Table 3*) is a valid address for the sector erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 18*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the sector erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed sector erase cycle (whose duration is t_{SE}) is initiated. While the sector erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed sector erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset. RDSR is the only instruction accepted while device is busy with erase operation; all other instructions are ignored.

A sector erase (SE) instruction applied to a page which is protected by the block protect (BP3, BP2, BP1, BP0) bits (see *Table 2* and *Table 3*) is not executed.

Figure 18. Sector erase (SE) instruction sequence



6.14 Bulk erase (BE)

The bulk erase (BE) instruction sets all bits to ‘1’ (FFh). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

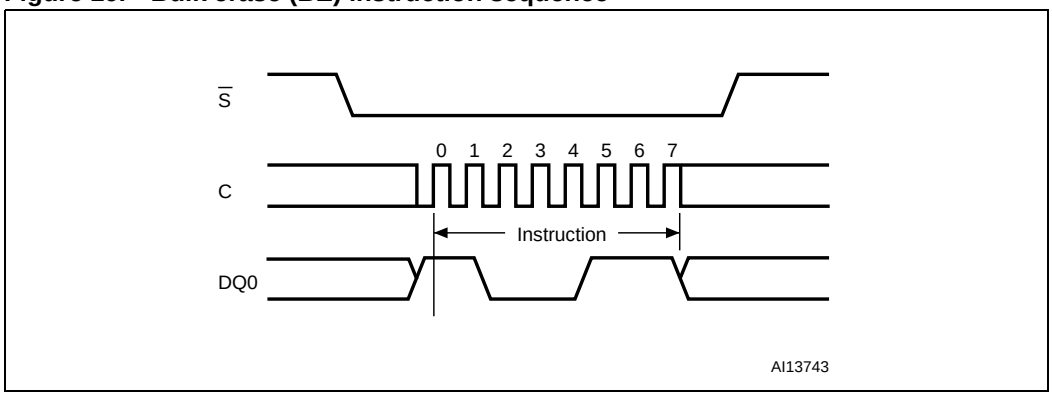
The bulk erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on serial data input (DQ0). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 19*.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the bulk erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed bulk erase cycle (whose duration is t_{BE}) is initiated. While the bulk erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed bulk erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset. RDSR is the only instruction accepted while device is busy with erase operation; all other instructions are ignored.

The bulk erase (BE) instruction is executed only if all block protect (BP3, BP2, BP1, BP0) bits are 0. The bulk erase (BE) instruction is ignored if one, or more, sectors are protected.

Figure 19. Bulk erase (BE) instruction sequence



7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC} until V_{CC} reaches the correct value:

- V_{CC}(min) at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down.

A safe configuration is provided in *Section 3: SPI modes*.

To avoid data corruption and inadvertent write operations during power-up, a power on reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the power on reset (POR) threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all write enable (WREN), page program (PP), dual input fast program (DIFP), sector erase (SE), bulk erase (BE), write status register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No write status register, program, erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} has passed the V_{WI} threshold
- t_{VSL} after V_{CC} has passed the V_{CC}(min) level.

These values are specified in *Table 9*.

If the time, t_{VSL}, has elapsed, after V_{CC} rises above V_{CC}(min), the device can be selected for read instructions even if the t_{PUW} delay has not yet fully elapsed.

After power-up, the device is in the following state:

- The device is in the standby power mode
- The write enable latch (WEL) bit is reset
- The write in progress (WIP) bit is reset

Normal precautions must be taken for supply line decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} line decoupled by a suitable capacitor close to the package pins (generally, this capacitor is of the order of 100 nF).

At power-down, when V_{CC} drops from the operating voltage, to below the power on reset (POR) threshold voltage, V_{WI}, all operations are disabled and the device does not respond to any instruction (the designer needs to be aware that if power-down occurs while a write, program or erase cycle is in progress, some data corruption may result).

Figure 20. Power-up timing

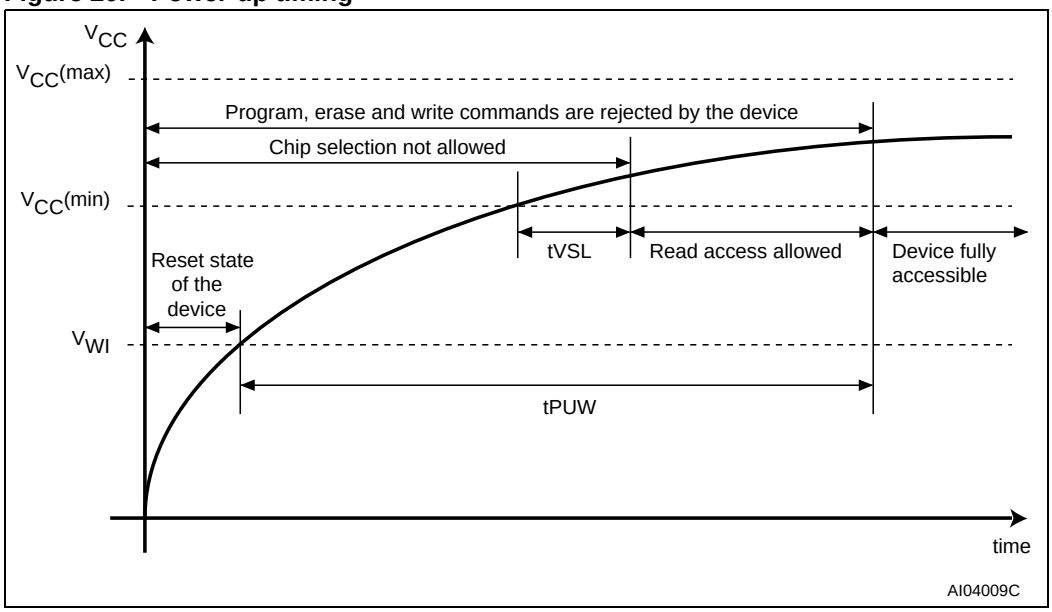


Table 9. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL} (1)	V_{CC}(min) to $\overline{S}$ Low	100		µs
t_{PUW} (1)	Time delay to write instruction	1	10	ms
V_{WI} (1)	Write inhibit voltage	1.5	2.5	V

1. These parameters are characterized only.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to ‘1’ (each byte contains FFh). The status register contains 00h (all status register bits are 0).

9 Maximum ratings

Stressing the device outside the ratings listed in *Table 10: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE program and other relevant quality documents.

Table 10. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{ESD}	Electrostatic discharge voltage (human body model)(1)	–2000	2000	V

1. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 11. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	2.7		3.6	V
T_A	Ambient operating temperature (66MHz)	0		70	°C
T_A	Ambient operating temperature (33MHz)	-30		+85	°C

Omneo™ P5Q PCM endurance is different than traditional non-volatile memory. For PCM a “write cycle” is defined as any time a bit changes within a 32-byte page.

Table 12. Endurance Specification

Parameter	Condition	Min	Units	Notes	Parameter
Write Cycle	Main Block	1,000,000	Cycles per 32-Byte Page	1	Write Cycle
	Parameter Block	1,000,000			

Table 13. AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	V_{CC} / 2		V

Figure 21. AC measurement I/O waveform

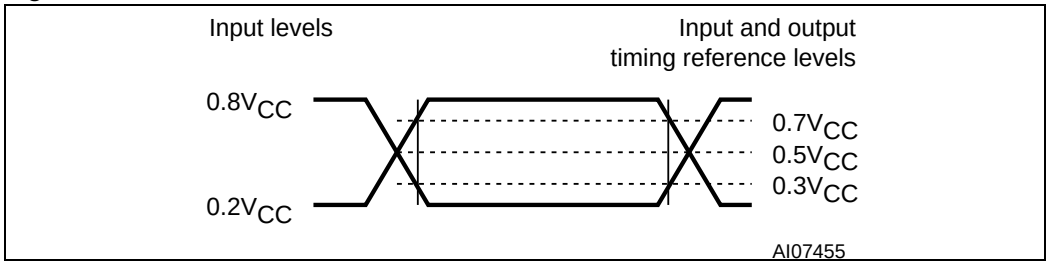


Table 14. Capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
$C_{IN/OUT}$	Input/output capacitance (DQ0/DQ1)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A=25 °C and a frequency of 33 MHz.

Table 15. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 11*)	Min	Max	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		200	µA
I_{CC3}	Operating current (READ)	C = 0.1V_{CC} / 0.9V_{CC} at 66 MHz, DQ1 = open		16	mA
		C = 0.1V_{CC} / 0.9V_{CC} at 33 MHz, DQ1 = open		7	mA
	Operating current (DOFR)	C = 0.1V_{CC} / 0.9V_{CC} at 66 MHz, DQ0=DQ1 = open		20	mA
	Operating current (QOFR)	C = 0.1V_{CC} / 0.9V_{CC} at 50 MHz, DQ0=DQ1=DQ2=DQ3 = open		24	mA
I_{CC4}	Operating current (PP)	$\overline{S} = V_{CC}$		50	mA
	Operating current (DIFP)	$\overline{S} = V_{CC}$		50	mA
	Operating current (QIFP)	$\overline{S} = V_{CC}$		50	mA
I_{CC5}	Operating current (WRSR)	$\overline{S} = V_{CC}$		50	mA
I_{CC6}	Operating current (SE, BE)	$\overline{S} = V_{CC}$		50	mA
V_{IL}	Input low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 16. AC characteristics(1)

Test conditions specified in *Table 11* and *Table 13*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ(2)**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: DOFR, DIFP, FAST_READ, SE, BE, WREN, WRDI, RDID, RDSR, WRSR (**0 to +70 °C**)	D.C.		66	MHz
		Clock frequency for the following instructions: QOFR, QIFP (**0 to +70 °C**)	D.C.		50	MHz
f_R		Clock frequency for READ instructions (**0 to +70 °C**)	D.C.		33	MHz
f_C / f_R		Clock frequency for ALL instructions: QOFR, QIFR, DOFR, DIFP, FAST_READ, READ SE, BE, WREN, WRDI, RDID, RDSR, WRSR (**-30 to +85 °C**)	D.C.		33	MHz
t_{CH}(3)	t_{CLH}	Clock High time	6.5			ns
t_{CL}(2)	t_{CLL}	Clock Low time	6.5			ns
t_{CLCH}(4)		Clock rise time(5) (peak to peak)	0.1			V/ns
t_{CHCL}(4)		Clock fall time(5) (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	80			ns
t_{SHQZ}(4)	t_{DIS}	Output disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output valid under 30 pF			9	ns
		Clock Low to Output valid under 10 pF			8	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHL}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHQX}(4)	t_{LZ}	$\overline{HOLD}$ to Output Low-Z			10	ns
t_{HLQZ}(4)	t_{HZ}	$\overline{HOLD}$ to Output High-Z			10	ns
t_{WHSL}(6)		Write protect setup time	20			ns
t_{SHWL}(6)		Write protect hold time	100			ns
t_{RDP}(4)		$\overline{S}$ High to standby mode			30	µs

Table 16. AC characteristics(1) (continued)

Test conditions specified in *Table 11* and *Table 13*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ(2)**	**Max**	**Unit**
t_W		Write status register cycle time		200	350	µs
t_{PP}(7)		Page program cycle time (64 bytes) (Legacy Program & Bit-alterable Write)		120	360	µs
		Page program cycle time (64 bytes) (Program on all 1s)		71	280	
t_{SE}		Sector erase cycle time		400	800	ms
t_{BE}		Bulk erase cycle time		50	100	s

1. Preliminary data.
2. Typical values given for T_A = 25° C @ nominal V_{CC}.
3. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C.
4. Value guaranteed by characterization, not 100% tested in production.
5. Expressed as a slew-rate.
6. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.
7. When using the page program (PP) instruction to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes (1 ≤ n ≤ 64).

Figure 22. Serial input timing

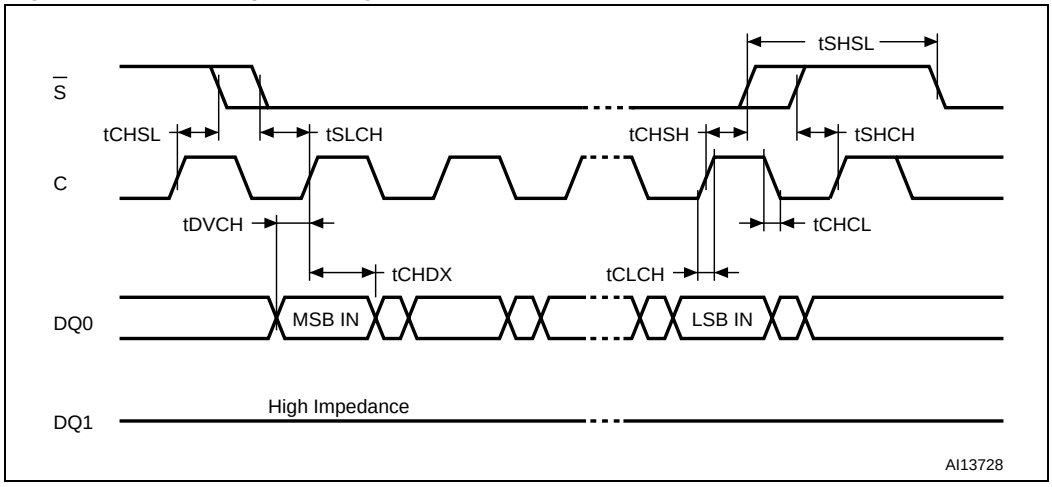


Figure 23. Write protect setup and hold timing during WRSR when SRWD=1

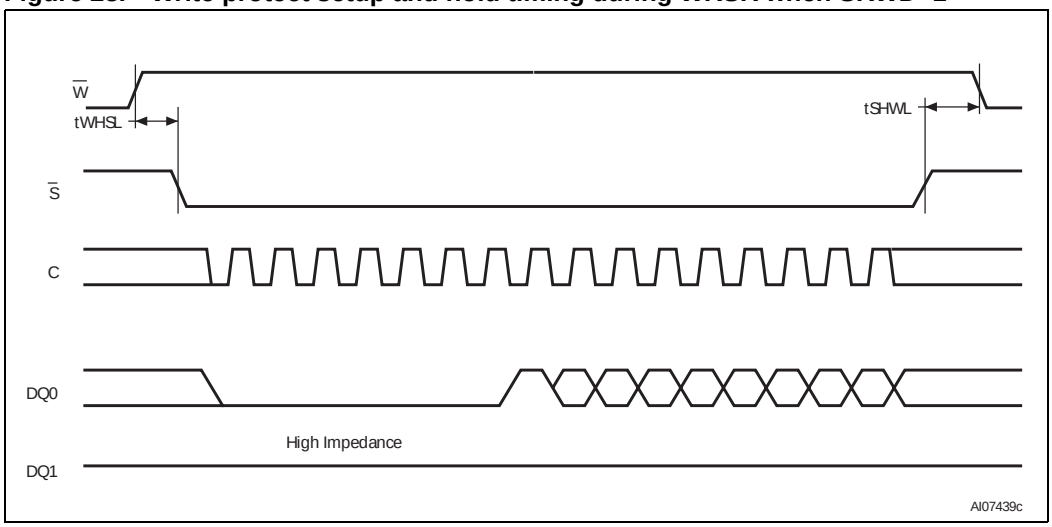


Figure 24. Hold timing

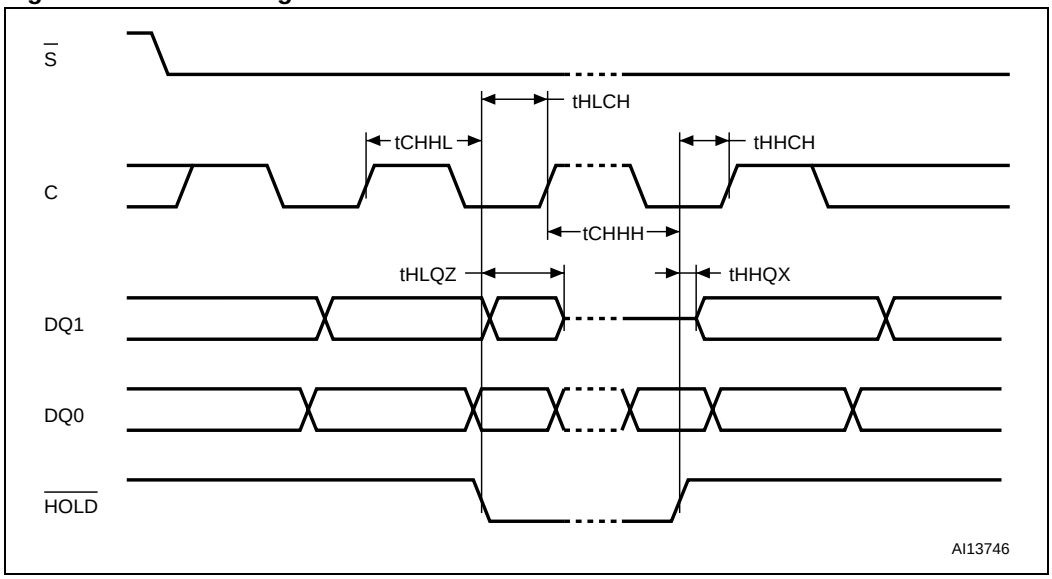
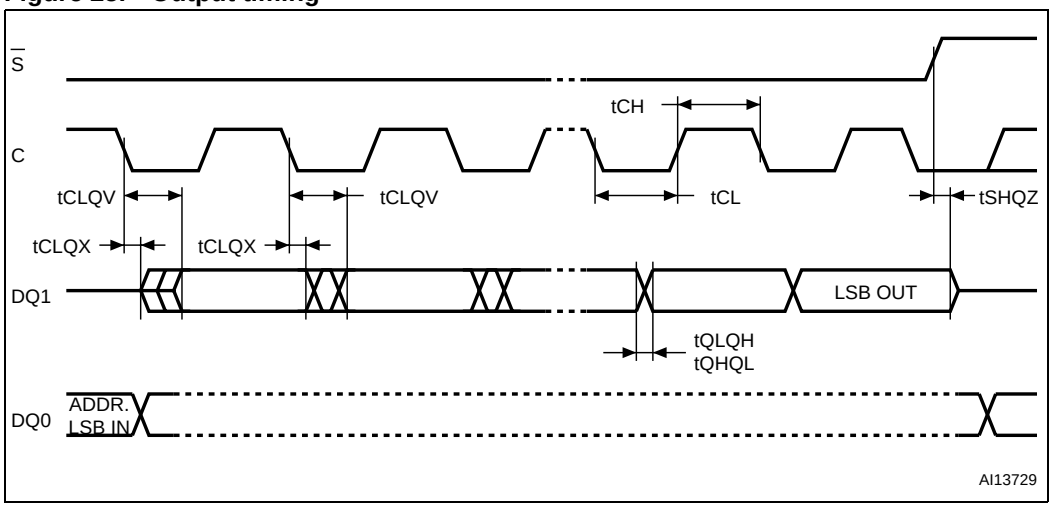


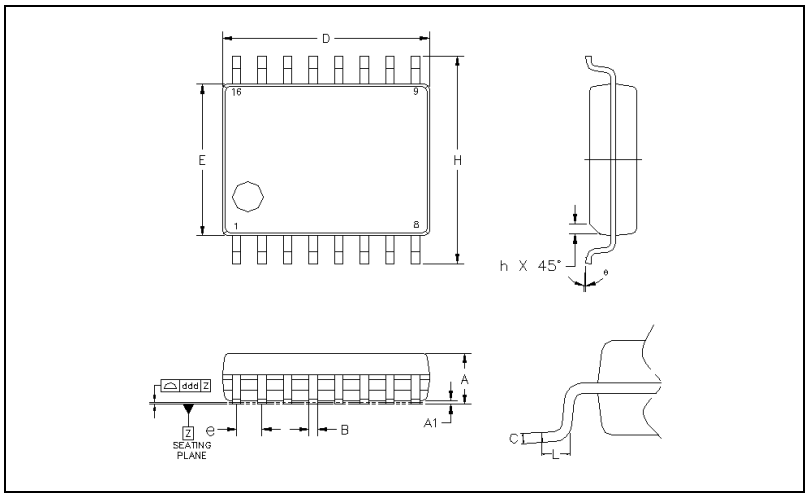
Figure 25. Output timing



11 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 26. SO16 wide - 16-lead plastic small outline, 300 mils body width, package outline



1. Drawing is not to scale.

Table 17. SO16 wide - 16-lead plastic small outline, 300 mils body width, mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A		2.35	2.65		0.093	0.104
A1		0.10	0.30		0.004	0.012
B		0.33	0.51		0.013	0.020
C		0.23	0.32		0.009	0.013
D		10.10	10.50		0.398	0.413
E		7.40	7.60		0.291	0.299
e	1.27	–	–	0.050	–	–
H		10.00	10.65		0.394	0.419
h		0.25	0.75		0.010	0.030
L		0.40	1.27		0.016	0.050
θ		0°	8°		0°	8°
ddd			0.10			0.004

12 Ordering information

This section defines all active line items that can be ordered.

Table 18. Active Line Item Ordering Table

Part Number	Description
NP5Q128A13ESFC0E	3V, SOIC, PbFree,10.34x10.34x2.54, 16 lead (0 to +70 ^{o}C)
NP5Q128AE3ESFC0E	3V, SOIC, PbFree,10.34x10.34x2.54, 16 lead (-30 to +85 ^{o}C)

Note: For SO8 packaging solutions please contact your local Numonyx representative for details.

13 Revision history

Table 19. Document revision history

Date	Revision	Changes
June 2009	1	Initial release
August 2009	2	Removed Numonyx Confidential Added Figures 23&24 Revised Hold Condition Verbiage 4.9 Removed Streaming Mode from Datasheet Added P5Q Product Designator
April 2010	3	Added Numonyx® Omneo™ Branding Added endurance verbiage (table-11) Revised DC and AC Section: tVSL (min), tCLQV (max), tHLQZ (max), Page Program (typ/max), Sector Erase (typ/max), Bulk Erase (max)
July 2010	4	Revised cover page with -30 to +85C Revised read current at 33MHz (Table 14) Revised AC characteristics for -30 to +85C (Table 15) Revised Ordering information

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