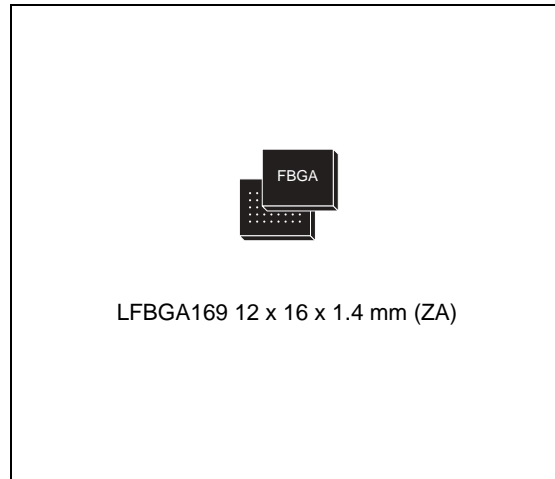


Features

- Packaged NAND flash memory with MultiMediaCard interface
- Up to 8 Gbytes of formatted data storage
- High capacity memory access
- eMMC/MultiMediaCard system specification, compliant with V4.3
- Full backward compatibility with previous MultiMediaCard system specification
- Bus mode
 - High-speed MultiMediaCard protocol
 - Three different data bus widths: 1 bit, 4 bits, 8 bits
 - Data transfer rate: up to 52 Mbyte/s
- Operating voltage range:
 - $V_{CCQ} = 1.8\text{ V}/3.3\text{ V}$
 - $V_{CC} = 3.3\text{ V}$
- Multiple block read (x8 at 52 MHz): up to 29 Mbyte/s
- Multiple block write (x8 at 52 MHz): up to 11 Mbyte/s
- Power dissipation
 - Standby current: down to 200 μA (typ)
 - Read current: down to 40 mA (typ)
 - Write current: down to 100 mA (typ)



- Error free memory access
 - Internal error correction code
 - Internal enhanced data management algorithm (wear levelling, bad block management, garbage collection)
 - Possibility for the host to make sudden power failure safe-update operations for data content
- Security
 - Password protection of data
 - Built-in write protection
- Boot
 - Simple boot sequence method
- Power saving
 - Enhanced power saving method by introducing sleep functionality

Table 1. Device summary

| Root part number | Package | Operating voltage |
|------------------|----------|--|
| NAND32GAH0H | LFBGA169 | $V_{CC} = 3.3\text{ V}, V_{CCQ} = 1.8\text{ V}/3.3\text{ V}$ |
| NAND64GAH0H | | |

Contents

| | | |
|----------|--|-----------|
| 1 | Description | 6 |
| 1.1 | eMMC Standard Specification | 6 |
| 2 | Product specification | 7 |
| 2.1 | System performance | 7 |
| 3 | Device physical description | 8 |
| 3.1 | Package connections | 9 |
| 3.2 | Form factor | 9 |
| 4 | Memory array partitioning | 10 |
| 5 | MultiMediaCard interface | 11 |
| 5.1 | Signals description | 11 |
| 5.1.1 | Clock (CLK) | 11 |
| 5.1.2 | Command (CMD) | 11 |
| 5.1.3 | Input/outputs (DAT0-DAT7) | 11 |
| 5.1.4 | V _{CC} core supply voltage | 11 |
| 5.1.5 | V _{SS} ground | 11 |
| 5.1.6 | V _{CCQ} input/output supply voltage | 12 |
| 5.1.7 | V _{SSQ} supply voltage | 12 |
| 5.2 | Bus topology | 13 |
| 5.3 | Power-up | 13 |
| 5.4 | Power cycling | 13 |
| 5.5 | Bus operating conditions | 15 |
| 5.6 | Bus signal levels | 15 |
| 5.7 | Bus timing | 15 |
| 6 | High speed MultiMediaCard operation | 16 |
| 6.1 | Boot mode | 16 |
| 6.2 | Identification mode | 16 |
| 6.3 | Data transfer mode | 16 |
| 6.4 | Clock control | 16 |

| | | |
|-----------|--------------------------------------|-----------|
| 6.5 | Error conditions | 16 |
| 6.6 | Commands | 17 |
| 6.7 | State transition | 17 |
| 6.8 | Response | 17 |
| 6.9 | Timing diagrams and values | 17 |
| 6.10 | Minimum performance | 17 |
| 7 | Device registers | 18 |
| 7.1 | Operation conditions register (OCR) | 18 |
| 7.2 | Card identification (CID) register | 19 |
| 7.3 | Card specific data register (CSD) | 19 |
| 7.4 | Extended CSD register | 21 |
| 7.5 | RCA (relative card address) register | 24 |
| 7.6 | DSR (driver stage register) register | 24 |
| 7.7 | Status register | 24 |
| 8 | Package mechanical | 25 |
| 9 | Ordering information | 27 |
| 10 | Revision history | 28 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | Device summary | 1 |
| Table 2. | System performance | 7 |
| Table 3. | Current consumption | 7 |
| Table 4. | Communication channel performance | 7 |
| Table 5. | Signal names | 12 |
| Table 6. | OCR register definition | 18 |
| Table 7. | Card identification (CID) register | 19 |
| Table 8. | Card specific data register | 20 |
| Table 9. | Extended CSD | 21 |
| Table 10. | LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package mechanical data | 26 |
| Table 11. | Ordering information scheme | 27 |
| Table 12. | Document revision history | 28 |

List of figures

| | | |
|-----------|---|----|
| Figure 1. | Device block diagram | 8 |
| Figure 2. | LFPGA169 package connections (top view through package). | 9 |
| Figure 3. | Form factor | 9 |
| Figure 4. | Memory array structure. | 10 |
| Figure 5. | Power-up | 14 |
| Figure 6. | Power cycling | 14 |
| Figure 7. | LFPGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package outline | 25 |

1 Description

The NANDxxxAH0H is an embedded flash memory storage solution with MultiMediaCard™ interface (eMMC™). The eMMC™ was developed for universal low cost data storage and communication media. The NANDxxxAH0H is fully compatible with MMC bus and hosts.

The NANDxxxAH0H communications are made through an advanced 13-pin bus. The bus can be either 1-bit, 4-bit, or 8-bit in width. The device operates in high-speed mode at clock frequencies equal to or higher than 20 MHz, which is the MMC standard. The communication protocol is defined as a part of this MMC standard and referred to as MultiMediaCard mode.

The device is designed to cover a wide area of applications such as smart phones, cameras, organizers, PDA, digital recorders, MP3 players, pagers, electronic toys, etc. They feature high performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, the NANDxxxAH0H supports both 3.3 V supply voltage (V_{CC}), and 1.8 V/3.3 V input/output voltage (V_{CCQ}).

The address argument for the NANDxxxAH0H is the sector address (512-byte sectors) instead of the byte address. This means that NANDxxxAH0H is not backward compatible with devices of density lower than 2 Gbytes. If there is no indication by the host to the memory that the host is capable of handling sector type of addressing, the NANDxxxAH0H will change its state to inactive.

The device has a built-in intelligent controller which manages interface protocols, data storage and retrieval, wear leveling, bad block management, garbage collection, and internal ECC.

The NANDxxxAH0H makes available to the host sudden power failure safe-update operations for the data content, by supporting reliable write features.

The device supports boot operation and sleep/awake commands. In particular, during the sleep state the host power regulator for V_{CC} can be switched off, thus minimizing the power consumption of the NANDxxxAH0H.

The system performance and characteristics are given in [Table 2](#), [Table 3](#), and [Table 4](#).

1.1 eMMC Standard Specification

The NANDxxxAH0H device is fully compatible with the JEDEC Standard Specification No. JESD84-A43.

This datasheet describes the key and specific features of the NANDxxxAH0H device. Any additional information required to interface the device to a host system and all the practical methods for card detection and access can be found in the proper sections of the JEDEC Standard Specification.

2 Product specification

2.1 System performance

Table 2. System performance

| System performance | Typical value ⁽¹⁾ | | Unit |
|--|------------------------------|--|---------|
| | NAND32GAH0H, NAND64GAH0H | | |
| Multiple block read sequential ⁽²⁾ | 29 | | Mbyte/s |
| Multiple block read 64-Kbyte chunk ⁽³⁾ | 19 | | Mbyte/s |
| Multiple block write sequential ⁽²⁾ | 11 | | Mbyte/s |
| Multiple block write 64-Kbyte chunk ⁽³⁾ | 5 | | Mbyte/s |

1. Values given for an 8-bit bus width, a clock frequency of 52 MHz, $V_{CC} = 3.3\text{ V}$ and $V_{CCQ} = 1.8\text{ V}$.

2. Based on a 4-Mbyte file transfer.

3. Test performed by writing/reading a 64-Kbyte chunk of data to/from random logical addresses (aligned to physical block boundaries) of the card. The performance is calculated as an average out of several 64-Kbyte accesses.

Table 3. Current consumption

| Operation | Test conditions | Current consumption ⁽¹⁾ | | | | Unit |
|-----------|---|------------------------------------|-----|-------------|-----|---------------|
| | | NAND32GAH0H | | NAND64GAH0H | | |
| | | Typ | Max | Typ | Max | |
| Read | $V_{CC} = 3.3\text{ V} \pm 5\%$ $V_{CCQ} = 1.8\text{ V} \pm 5\%$ | 40 | 80 | 40 | 80 | mA |
| Write | | 100 | 150 | 100 | 150 | |
| Standby | $V_{CC} = 3.3\text{ V} \pm 5\%$ | 20 | | 40 | | μA |
| | $V_{CCQ} = 1.8\text{ V} \pm 5\%$ | 80 | | 80 | | |

1. Values given for an 8-bit bus width and a clock frequency of 26 MHz.

Table 4. Communication channel performance

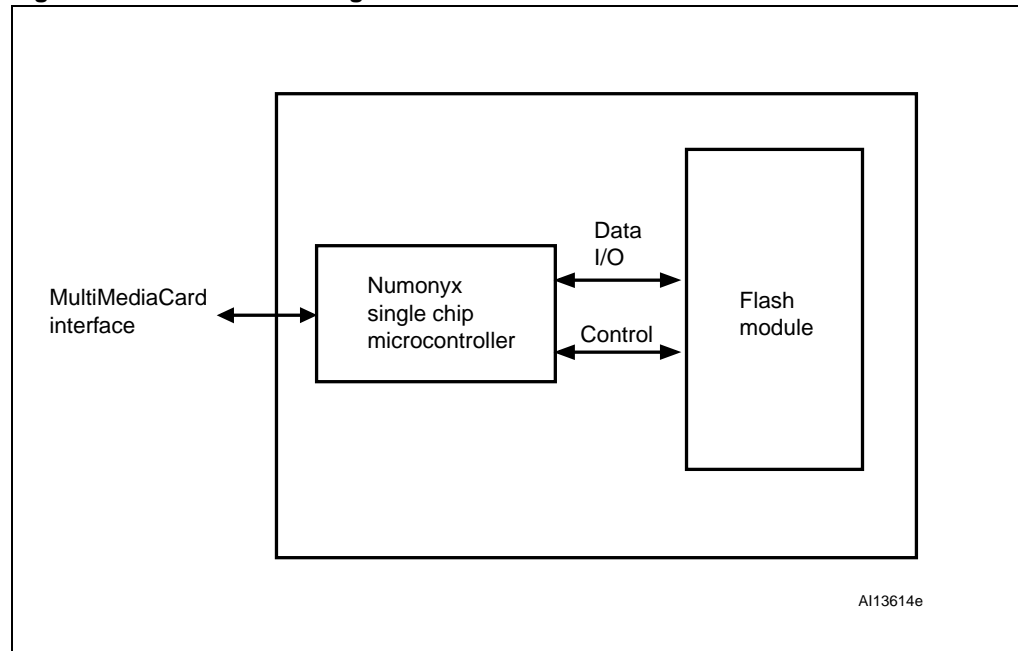
| MultiMediaCard communication channel performance |
|---|
| Three-wire serial data bus (clock, command, data) |
| Variable clock rate 0, 26, 52 MHz |
| Easy card identification |
| Error protected data transfer |
| Sequential and single/multiple block oriented data transfer |

3 Device physical description

The NANDxxxAH0H contains a single chip controller and flash memory module, see [Figure 1: Device block diagram](#). The microcontroller interfaces with a host system allowing data to be written to and read from the flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

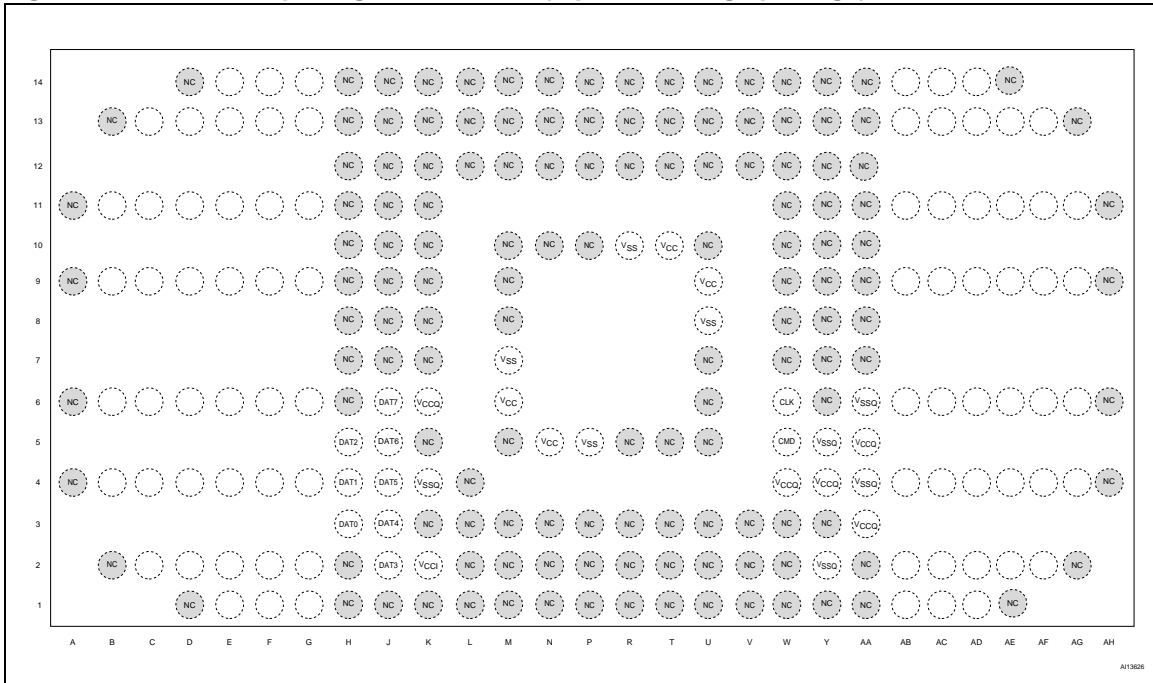
[Figure 2](#) shows the package connections. See [Table 5: Signal names](#) for the description of the signals corresponding to the balls.

Figure 1. Device block diagram



3.1 Package connections

Figure 2. LFBGA169 package connections (top view through package)



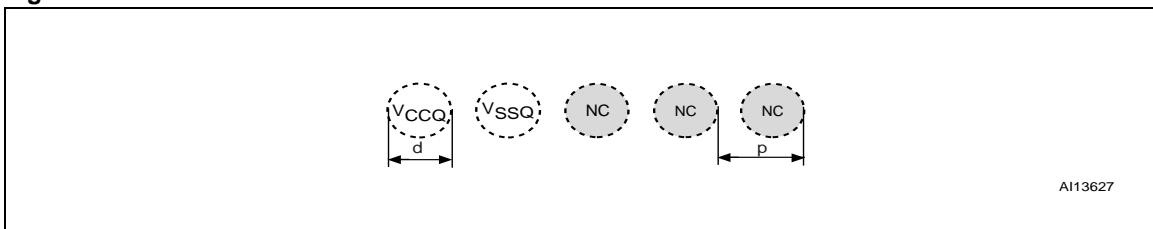
1. The ball corresponding to V_{CCQ} must be decoupled with an external capacitance.

3.2 Form factor

The ball diameter, d , and the ball pitch, p , for the LFBGA169 package are:

- $d = 0.30 \text{ mm}$ (solder ball diameter)
- $p = 0.5 \text{ mm}$ (ball pitch)

Figure 3. Form factor



4 Memory array partitioning

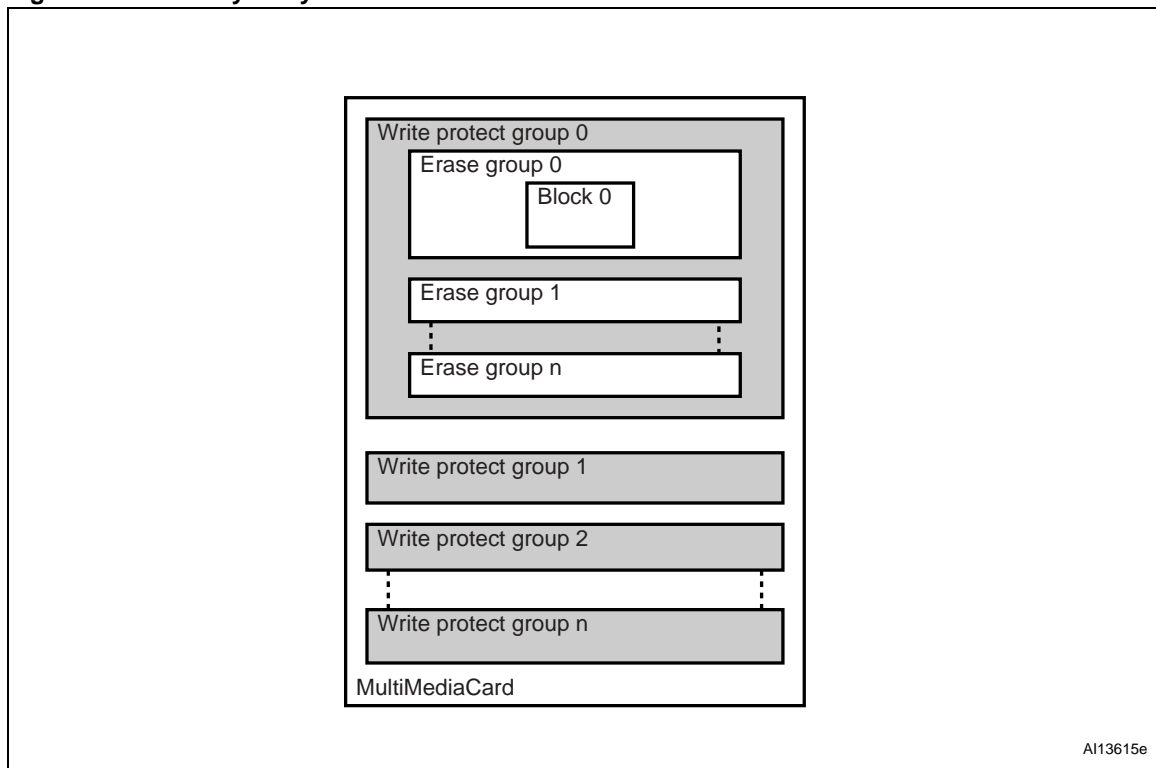
The basic unit of data transfer to/from the device is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

For block oriented commands, the following definitions are used:

- **Block:** the unit which is related to the block oriented read and write commands. Its size is the number of bytes which are transferred when one block command is issued by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD register.
- **Erase group:** the unit which is related to special erase and write commands defined for R/W cards. Its size is the smallest number of consecutive write blocks which can be addressed for erase. The size of the erase group depends on each device and is stored in the CSD.
- **Write protect group:** the smallest unit that may be individually write protected. Its size is defined in units of erase groups. The size of a WP-group depends on each device and is stored in the CSD.

Figure 4 shows the NANDxxxAH0H memory array organization.

Figure 4. Memory array structure



1. n = number of last erase group or last write protect group.

5 MultiMediaCard interface

The signal/pin assignments are listed in [Table 5](#). Refer to this table in conjunction with [Figure 2](#) and [Figure 3: Form factor](#).

5.1 Signals description

5.1.1 Clock (CLK)

The Clock input, CLK, is used to synchronize the memory to the host during command and data transfers. Each clock cycle gates one bit on the command and on all the data lines. The Clock frequency, f_{PP} , may vary between zero and the maximum clock frequency.

5.1.2 Command (CMD)

The CMD signal is a bidirectional command channel used for device initialization and command transfer. The CMD signal has two operating modes: open-drain and push-pull. The open-drain mode is used for initialization, while the push-pull mode is used for fast command transfer. Commands are sent by the MultiMediaCard bus master (or host) to the device who responds by sending back responses.

5.1.3 Input/outputs (DAT0-DAT7)

DAT0 to DAT7 are bidirectional data channels. The signals operate in push-pull mode. The NANDxxxAH0H includes internal pull ups for all data lines. These signals cannot be driven simultaneously by the host and the NANDxxxAH0H device. Right after entering the 4-bit mode, the card disconnects the internal pull ups of lines DAT1 and DAT2 (DAT3 internal pull up is left connected due to the SPI mode CS backward compatible usage). Correspondingly right after entering the 8-bit mode, the card disconnects the internal pull ups of lines DAT1, DAT2 and DAT4-DAT7.

By default, after power-up or hardware reset, only DAT0 is used for data transfers. The host can configure the device to use a wider data bus, DAT0, DAT0-DAT3 or DAT0-DAT7, for data transfer.

5.1.4 V_{CC} core supply voltage

V_{CC} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase). The core voltage (V_{CC}) can be within 2.7 V and 3.6 V.

5.1.5 V_{SS} ground

Ground, V_{SS} , is the reference for the power supply. It must be connected to the system ground.

5.1.6 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

The input/output voltage (V_{CCQ}) can be either within 1.65/1.7 V and 1.95 V (low voltage range) or 2.7 V and 3.6 V (high voltage range).

5.1.7 V_{SSQ} supply voltage

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}.

Table 5. Signal names

| Name | Type ⁽¹⁾ | Description |
|------------------|---------------------|--|
| DAT0 | I/O (PP) | Data |
| DAT1 | I/O (PP) | Data |
| DAT2 | I/O (PP) | Data |
| DAT3 | I/O (PP) | Data |
| DAT4 | I/O (PP) | Data |
| DAT5 | I/O (PP) | Data |
| DAT6 | I/O (PP) | Data |
| DAT7 | I/O (PP) | Data |
| CMD | I/O (OD or PP) | Command |
| CLK | I (PP) | Clock |
| V _{CCQ} | | Input/output power supply |
| V _{CC} | | Core power supply |
| V _{SSQ} | | Input/output ground |
| V _{CCI} | I | Must be decoupled with an external capacitance |
| V _{SS} | | Ground |
| NC | NC | Not connected ⁽²⁾ |

1. I: input; O: output, OD: open drain, PP: push-pull.

2. NC pins can be connected to ground or left floating.

5.2 Bus topology

The NANDxxxAH0H device supports the MMC protocol. For more details, refer to section 6.4 of the JEDEC Standard Specification No. JESD84-A43. The section 12 of the JEDEC Standard Specification contains a bus circuitry diagram for reference.

5.3 Power-up

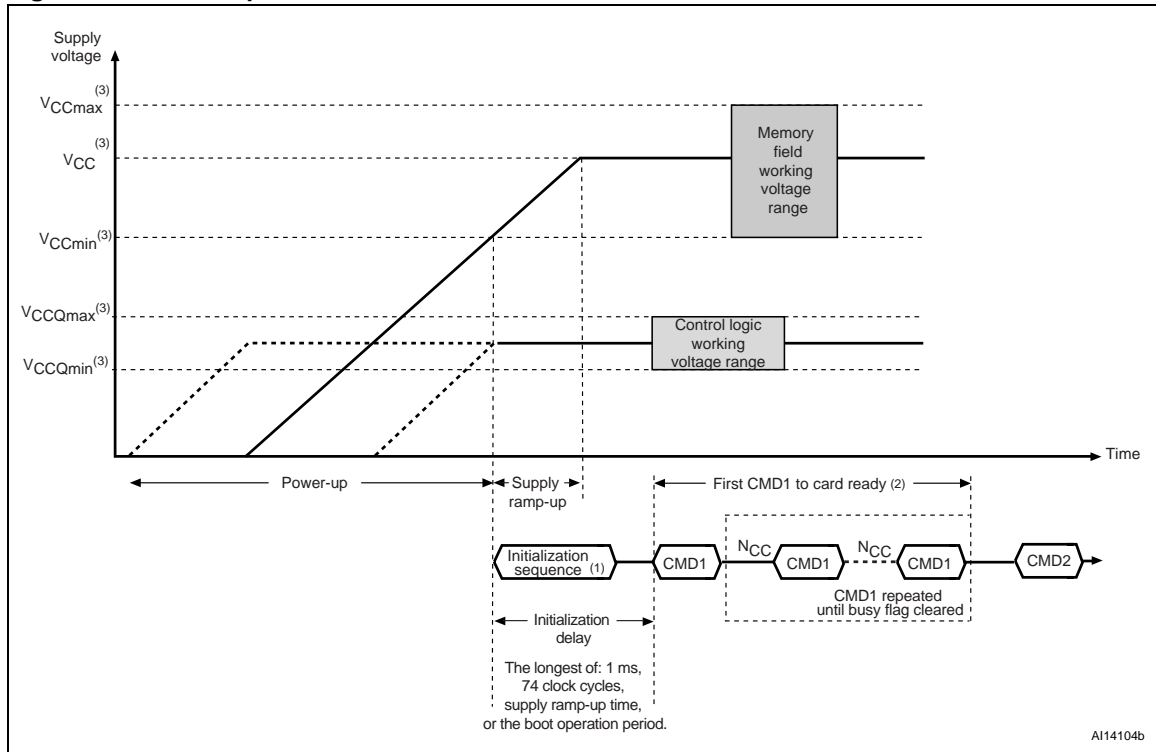
The power-up is handled locally in each device and in the bus master. [Figure 5: Power-up](#) shows the power-up sequence. Refer to section 12.3 of the JEDEC Standard Specification No. JESD84-A43 for specific instructions regarding the power-up sequence.

After power-up, the maximum initial load the NANDxxxAH0H can present on the V_{CC} line is C4, in parallel with a minimum of R4. During operation, device capacitance on the V_{CC} line must not exceed 10 μ F.

5.4 Power cycling

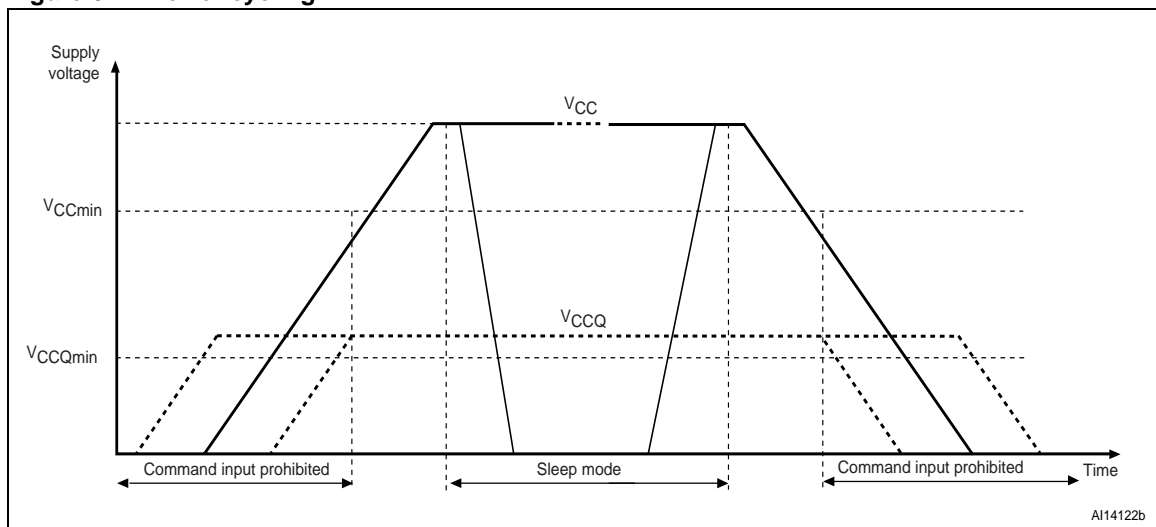
The bus master can execute any sequences of V_{CC} and V_{CCQ} power-up/power down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. For more information about power cycling see Section 12.3.3 of the JEDEC Standard Specification No. JESD84-A43 and [Figure 6: Power cycling](#).

Figure 5. Power-up



1. The initialization sequence is a contiguous stream of logic 1's. Its length is either 1 ms, 74 clocks or the supply ramp up time, whichever is the longest. The device shall complete its initialization within 1 second from the first CMD1 with a valid V range.
2. N_{CC} is the number of clock cycles.
3. Refer to [Section 7.1: Operation conditions register \(OCR\)](#) for details on voltage ranges.

Figure 6. Power cycling



5.5 Bus operating conditions

Refer to section 12.6 of the JEDEC Standard Specification No. JESD84-A43.

5.6 Bus signal levels

Refer to section 12.6 of the JEDEC Standard Specification No. JESD84-A43.

5.7 Bus timing

Refer to section 12.7 of the JEDEC Standard Specification No. JESD84-A43.

6 High speed MultiMediaCard operation

All communication between the host and the device is controlled by the host (master).

The following section provides an overview of the identification and data transfer modes, commands, dependencies, various operation modes and restrictions for controlling the clock signal. For detailed information, refer to section 7 of the JEDEC Standard Specification No. JESD84-A43.

6.1 Boot mode

The host can read boot data from NANDxxxAH0H by keeping CMD line Low after power-on or sending CMD0 with argument + 0xFFFFFFFF (optional for slave), before issuing CMD1. The data can be read from either boot area or user area depending on the register setting. Refer to section 7.2 of the JEDEC Standard Specification No. JESD84-A43.

6.2 Identification mode

When in card identification mode, the host resets the NANDxxxAH0H, validates the operating voltage range and the access mode, identifies the device and assigns a relative address (RCA) to it. For more information see section 7.3 of the JEDEC Standard Specification No. JESD84-A43.

6.3 Data transfer mode

The device enters data transfer mode once an RCA is assigned to it. When the device is in standby mode, issuing the CMD7 command along with the RCA, selects the device and puts it into the transfer state. The host enters data transfer mode after identifying the NANDxxxAH0H on the bus. When the device is in standby state, communication over the CMD and DAT lines is in push-pull mode.

The section 7.5 of the JEDEC Standard Specification No. JESD84-A43 contains more detailed information about data read and write, erase, write protect management, lock/unlock operations, the switch function command, high speed mode selection, and bus testing procedure. Moreover section 7.5.7 contains a detailed description of the reliable write features supported by the NANDxxxAH0H.

6.4 Clock control

Refer to section 7.6 of the JEDEC Standard Specification No. JESD84-A43.

6.5 Error conditions

Refer to section 7.7 of the JEDEC Standard Specification No. JESD84-A43.

6.6 Commands

Refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A43.

6.7 State transition

Refer to section 7.10 and 7.12 of the JEDEC Standard Specification No. JESD84-A43.

6.8 Response

Refer to section 7.11 of the JEDEC Standard Specification No. JESD84-A43.

6.9 Timing diagrams and values

Refer to section 7.14 of the JEDEC Standard Specification No. JESD84-A43.

6.10 Minimum performance

Refer to section 7.8 of the JEDEC Standard Specification No. JESD84-A43.

7 Device registers

There are five different registers within the device interface:

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (driver stage register)
- Extended card specific data register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands (refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A43. The device does not implement the DSR register.

The MultiMediaCard has a status register to provide information about the device current state and completion codes for the last host command.

7.1 Operation conditions register (OCR)

The 32-bit operation conditions register stores the V_{CCQ} , the input/output voltage of the flash memory component. The device is capable of communicating (identification procedure and data transfer) with any MultiMediaCard host using any operating voltage within 1.7 V and 1.95 V (low-voltage range) or 2.7 V and 3.6 V (high-voltage range) depending on the voltage range supported by the host. For further details, refer to section 8.1 of the JEDEC Standard Specification No. JESD84-A43.

If the host tries to change the OCR values during an initialization procedure the changes in the OCR content will be ignored.

The level coding of the OCR register is as follows:

- Restricted voltage windows = Low
- Device busy = Low

Table 6. OCR register definition

| OCR bit | Description | MultiMediaCard |
|----------|---|-------------------|
| 6 to 0 | Reserved | 000 0000b |
| 7 | Low V_{CCQ} | 1b |
| 14 to 8 | 2.0 - 2.6 | 000 0000b |
| 23 to 15 | 2.7 - 3.6 (High V_{CCQ} range) | 1 1111 1111b |
| 28 to 24 | Reserved | 000 0000b |
| 30 to 29 | Access mode | 10b (sector mode) |
| 31 | Power-up status bit (busy) ⁽¹⁾ | |

1. This bit is set to Low if the device has not finished the power-up routine.

7.2 Card identification (CID) register

The CID register is 16-byte long and contains a unique card identification number used during the card identification procedure. It is a 128-bit wide register with the content as defined in [Table 7](#). It is programmed during device manufacturing and can not be changed by MultiMediaCard hosts. For details, refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A43.

Table 7. Card identification (CID) register

| Name | Field | Width | CID - slice | CID - value | Note |
|-----------------------|-------|-------|-------------|----------------|------|
| Manufacturer ID | MID | 8 | [127:120] | 0xFE | |
| Reserved | | 6 | [119:114] | | |
| Card/BGA | CBX | 2 | [113:112] | 0x01 | BGA |
| OEM/application ID | OID | 8 | [111:104] | TBD | |
| Product name | PNM | 48 | [103:56] | MMC04G, MMC08G | |
| Product revision | PRV | 8 | [55:48] | | |
| Product serial number | PSN | 32 | [47:16] | TBD | |
| Manufacturing date | MDT | 8 | [15:8] | TBD | |
| CRC7 checksum | CRC | 7 | [7:1] | TBD | |
| Not used, always '1' | – | 1 | [0:0] | 1 | |

7.3 Card specific data register (CSD)

All the configuration information required to access the device data is stored in the CSD register. The MSB bytes of the register contain the manufacturer data and the two least significant bytes contains the host controlled data (the device copy, write protection and the user ECC register).

The host can read the CSD register and alter the host controlled data bytes using the SEND_CSD and PROGRAM_CSD commands.

In [Table 8](#), the cell type column defines the CSD field as read only (R), one time programmable (R/W) or erasable (R/W/E). The programmable part of the register (entries marked by W or E) can be changed by command CMD27.

The copy bit in the CSD can be used to mark the device as an original or a copy. Once set it cannot be cleared. The device can be purchased with the copy bit set (copy) or cleared, indicating the device is a master.

The one time programmable (OTP) characteristic of the copy bit is implemented in the MultiMediaCard controller firmware and not with a physical OTP cell.

For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A43.

Table 8. Card specific data register

| Name | Field | Width [bits] | Cell type | CSD-slice | CSD-value |
|--|--------------------|--------------|-----------|-----------|-----------------------------|
| CSD structure | CSD_STRUCTURE | 2 | R | [127:126] | 2 |
| MultiMediaCard protocol version | SPEC_VERS | 4 | R | [125:122] | 4 |
| Reserved | | 2 | R | [121:120] | TBD |
| Data read access-time-1 | TAAC | 8 | R | [119:112] | 79 |
| Data read access-time-2 in CLK cycles (NSAC*100) | NSAC | 8 | R | [111:104] | |
| Max. data transfer rate | TRAN_SPEED | 8 | R | [103:96] | 50 |
| Command classes | CCC | 12 | R | [95:84] | 245 |
| Max. read data block length | READ_BL_LEN | 4 | R | [83:80] | 512 |
| Partial blocks for read allowed | READ_BL_PARTIAL | 1 | R | [79:79] | 1 |
| Write block misalignment | WRITE_BLK_MISALIGN | 1 | R | [78:78] | 0x00 |
| Read block misalignment | READ_BLK_MISALIGN | 1 | R | [77:77] | 0 |
| DSR implemented | DSR_IMP | 1 | R | [76:76] | 0x00 |
| Reserved | | 2 | R | [75:74] | TBD |
| Device size | C_SIZE | 12 | R | [73:62] | According to device density |
| Max. read current at $V_{CC}(\min)$ | VDD_R_CURR_MIN | 3 | R | [61:59] | 100 mA |
| Max. read current at $V_{CC}(\max)$ | VDD_R_CURR_MAX | 3 | R | [58:56] | 200 mA |
| Max. write current at $V_{CC}(\min)$ | VDD_W_CURR_MIN | 3 | R | [55:53] | 100 mA |
| Max. write current at $V_{CC}(\max)$ | VDD_W_CURR_MAX | 3 | R | [52:50] | 200 mA |
| Device size multiplier | C_SIZE_MULT | 3 | R | [49:47] | According to device density |
| Erase group size | ERASE_GRP_SIZE | 5 | R | [46:42] | 32 |
| Erase group size multiplier | ERASE_GRP_MULT | 5 | R | [41:37] | 32 |
| Write protect group size | WP_GRP_SIZE | 5 | R | [36:32] | According to device density |
| Write protect group enable | WP_GRP_ENABLE | 1 | R | [31:31] | 1 |
| Manufacturer default ECC | DEFAULT_ECC | 2 | R | [30:29] | TBD |
| Write speed factor | R2W_FACTOR | 3 | R | [28:26] | 4 |
| Max. write data block length | WRITE_BL_LEN | 4 | R | [25:22] | 512 |
| Partial blocks for write allowed | WRITE_BL_PARTIAL | 1 | R | [21:21] | 0 |
| Reserved | | | | [20:20] | TBD |
| Content protection application | CONTENT_PROT_APP | 1 | R | [16:16] | 0 |
| File format group | FILE_FORMAT_GROUP | 1 | R/W | [15:15] | 0 |
| Copy flag (OTP) | COPY | 1 | R/W | [14:14] | 0 |

Table 8. Card specific data register (continued)

| Name | Field | Width [bits] | Cell type | CSD-slice | CSD-value |
|----------------------------|--------------------|--------------|-----------|-----------|---|
| Permanent write protection | PERM_WRITE_PROTECT | 1 | R/W | [13:13] | 0 |
| Temporary write protection | TMP_WRITE_PROTECT | 1 | R/W/E | [12:12] | 0 |
| File format | FILE_FORMAT | 2 | R/W | [11:10] | Hard disk like file system with partition table |
| ECC code 2 R/W/E none 0 | ECC | 2 | R/W/E | [9:8] | 0 |
| CRC | CRC | 7 | R/W/E | [7:1] | TBD |
| Not used, always '1' | | 1 | – | [0:0] | TBD |

7.4 Extended CSD register

The extended CSD register defines the device properties and selected modes. It is 512-byte long. The 320 most significant bytes are the properties segment that defines the device capabilities and cannot be modified by the host. The 192 lower bytes are the modes segment that defines the configuration the device is working in. For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A43.

These modes can be changed by the host by means of the Switch command.

Table 9. Extended CSD⁽¹⁾

| Name | Field | Size (bytes) | Cell type | CSD-slice | CSD-slice value |
|--|--------------------|--------------|-----------|-----------|-----------------|
| Properties segment | | | | | |
| Reserved ⁽²⁾ | | 7 | | [511:505] | TBD |
| Supported command sets | S_CMD_SET | 1 | R | [504] | 0 |
| Reserved ⁽²⁾ | | 275 | TBD | [503:229] | TBD |
| Boot information | BOOT_INFO | 1 | R | [228] | 1 |
| Reserved ⁽²⁾ | | 1 | TBD | [227] | TBD |
| Boot partition size | BOOT_SIZE_MULT | 1 | R | [226] | 256 Kbytes |
| Access size | ACC_SIZE | 1 | R | [225] | 0 |
| High-capacity erase unit size | HC_ERASE_GRP_SIZE | 1 | R | [224] | 0 |
| High-capacity erase timeout | ERASE_TIMEOUT_MULT | 1 | R | [223] | 0 |
| Reliable write sector count | REL_WR_SEC_C | 1 | R | [222] | 1 sector |
| High-capacity write protect group size | HC_WP_GRP_SIZE | 1 | R | [221] | 0 |
| Sleep current (V _{CC}) | S_C_VCC | 1 | R | [220] | TBD |
| Sleep current (V _{CCQ}) | S_C_VCCQ | 1 | R | [219] | TBD |
| Reserved ⁽²⁾ | | 1 | TBD | [218] | TBD |

Table 9. Extended CSD⁽¹⁾ (continued)

| Name | Field | Size (bytes) | Cell type | CSD-slice | CSD-slice value |
|--|----------------------|--------------|-----------|-----------|-----------------------------|
| Sleep/awake timeout | S_A_TIMEOUT | 1 | R | [217] | TBD |
| Reserved ⁽²⁾ | | 1 | TBD | [216] | TBD |
| Sector count | SEC_COUNT | 4 | R | [215:212] | According to device density |
| Reserved ⁽²⁾ | | 1 | | [211] | TBD |
| Minimum write performance for 8 bit at 52 MHz | MIN_PERF_W_8_52 | 1 | R | [210] | 8 |
| Minimum read performance for 8 bit at 52 MHz | MIN_PERF_R_8_52 | 1 | R | [209] | 8 |
| Minimum write performance for 8 bit at 26 MHz, for 4 bit at 52 MHz | MIN_PERF_W_8_26_4_52 | 1 | R | [208] | 8 |
| Minimum read performance for 8 bit at 26 MHz, for 4 bit at 52 MHz | MIN_PERF_R_8_26_4_52 | 1 | R | [207] | 8 |
| Minimum write performance for 4 bit at 26 MHz | MIN_PERF_W_4_26 | 1 | R | [206] | 8 |
| Minimum read performance for 4 bit at 26 MHz | MIN_PERF_R_4_26 | 1 | R | [205] | 8 |
| Reserved ⁽²⁾ | | 1 | | [204] | TBD |
| Power class for 26 MHz at 3.6 V | PWR_CL_26_360 | 1 | R | [203] | 0 |
| Power class for 52 MHz at 3.6 V | PWR_CL_52_360 | 1 | R | [202] | 0 |
| Power class for 26 MHz at 1.95 V | PWR_CL_26_195 | 1 | R | [201] | 0 |
| Power class for 52 MHz at 1.95 V | PWR_CL_52_195 | 1 | R | [200] | 0 |
| Reserved ⁽²⁾ | | 3 | | [199:197] | TBD |
| Card type | CARD_TYPE | 1 | R | [196] | 3 |
| Reserved ⁽²⁾ | | 1 | | [195] | TBD |
| CSD structure version | CSD_STRUCTURE | 1 | R | [194] | 2 |
| Reserved ⁽²⁾ | | 1 | | [193] | TBD |
| Extended CSD revision | EXT_CSD_REV | 1 | R | [192] | 2 |
| Modes segment | | | | | |
| Command set | CMD_SET | 1 | R/W | [191] | 0 |

Table 9. Extended CSD⁽¹⁾ (continued)

| Name | Field | Size (bytes) | Cell type | CSD-slice | CSD-slice value |
|-------------------------------------|-----------------|--------------|-----------|-----------|-----------------|
| Reserved ⁽²⁾ | | 1 | | [190] | TBD |
| Command set revision | CMD_SET_REV | 1 | RO | [189] | 0 |
| Reserved ⁽²⁾ | | 1 | | [188] | TBD |
| Power class | POWER_CLASS | 1 | R/W | [187] | 0 |
| Reserved ⁽²⁾ | | 1 | | [186] | TBD |
| High speed interface timing | HS_TIMING | 1 | R/W | [185] | 0 |
| Reserved ⁽²⁾ | | 1 | | [184] | TBD |
| Bus width mode | BUS_WIDTH | 1 | WO | [183] | 2 |
| Reserved ⁽²⁾ | | 1 | | [182] | TBD |
| Erased memory content | ERASED_MEM_CONT | 1 | RO | [181] | TBD |
| Reserved ⁽²⁾ | | 1 | | [180] | TBD |
| Boot configuration | BOOT_CONFIG | 1 | R/W | [179] | 0 |
| Reserved ⁽²⁾ | | 1 | | [178] | TBD |
| Boot bus width 1 | BOOT_BUS_WIDTH | 1 | R/W | [177] | 0 |
| Reserved ⁽²⁾ | | 1 | | [176] | TBD |
| High-density erase group definition | ERASE_GROUP_DEF | 1 | R/W | [175] | 0 |
| Reserved ⁽²⁾ | | 175 | | [174:0] | TBD |

1. TBD stands for 'to be defined'.

2. Reserved bits should read as '0'.

7.5 RCA (relative card address) register

The writable 16-bit relative card address (RCA) register carries the device address assigned by the host during the device identification. This address is used for the addressed host-card communication after the device identification procedure. The default value of the RCA register is '0x0001'. The value '0x0000' is reserved to set all cards into the standby state with CMD7. For details refer to section 8.5 of the JEDEC Standard Specification No. JESD84-A43.

7.6 DSR (driver stage register) register

The 16-bit driver stage register (DSR) can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices on the bus).

The CSD register contains the information concerning the DSR register usage.

The default value of the DSR register is '0x404'. For details refer to section 8.6 of the JEDEC Standard Specification No. JESD84-A43.

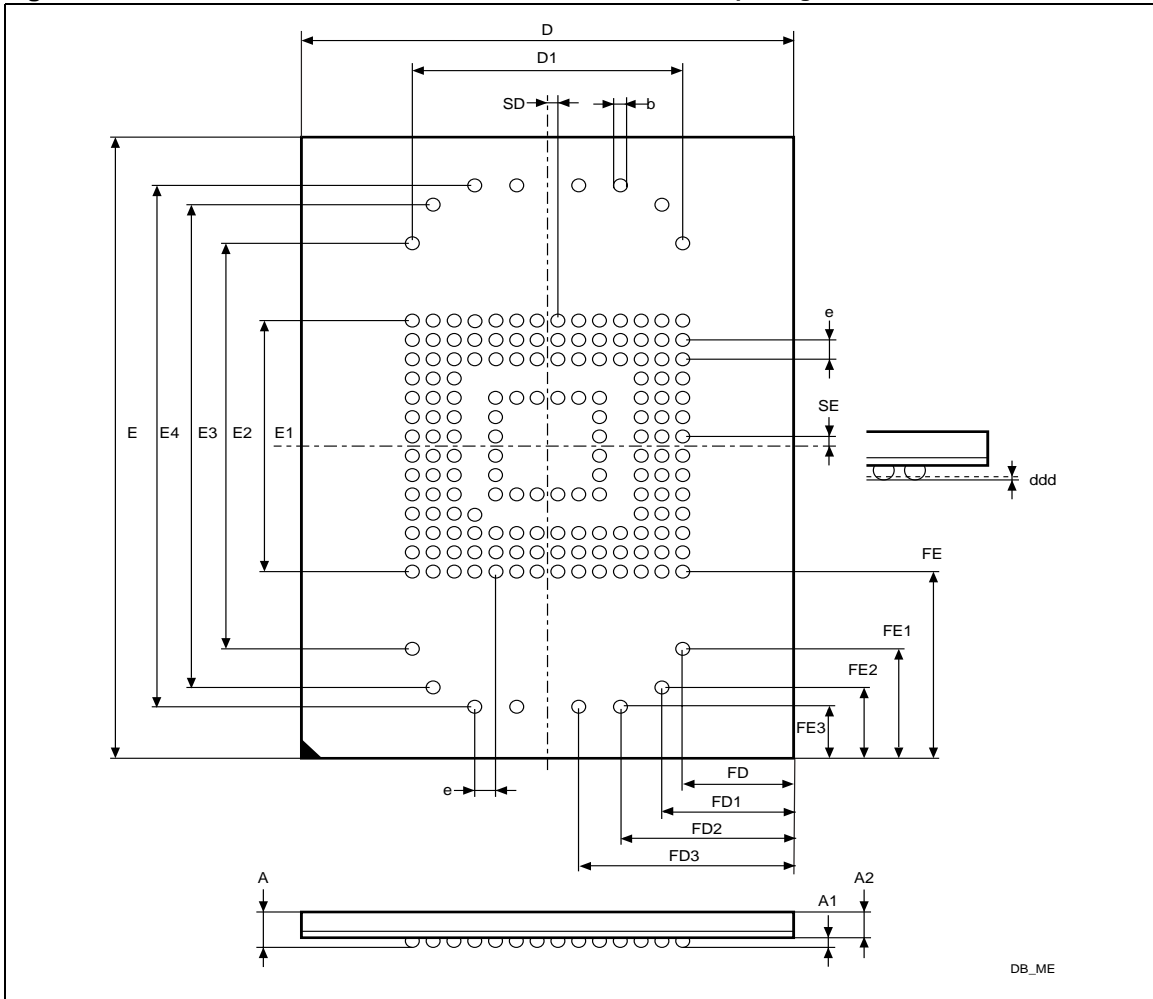
7.7 Status register

The status register provides information about the device current state and completion codes for the last host command. The device status can be explicitly read (polled) with the SEND_STATUS command. The MultiMediaCard status register structure is defined in section 7.12 of the JEDEC Standard Specification No. JESD84-A43.

8 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK[®] packages. ECOPACK[®] packages are lead-free. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 7. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package outline



1. Drawing is not to scale.

Table 10. LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.40 | | | 0.055 |
| A1 | | 0.15 | | | 0.006 | |
| A2 | 1.00 | | | 0.039 | | |
| b | 0.30 | 0.25 | 0.35 | 0.012 | 0.010 | 0.014 |
| D | 12.00 | 11.90 | 12.10 | 0.472 | 0.469 | 0.476 |
| D1 | 6.50 | | | 0.256 | | |
| ddd | | | 0.08 | | | 0.003 |
| E | 16.00 | 15.90 | 16.10 | 0.630 | 0.626 | 0.634 |
| E1 | 6.50 | | | 0.256 | | |
| E2 | 10.50 | | | 0.413 | | |
| E3 | 12.50 | | | 0.492 | | |
| E4 | 13.50 | | | 0.531 | | |
| e | 0.50 | – | – | 0.020 | – | – |
| FD | 2.75 | | | 0.108 | | |
| FD1 | 3.25 | | | 0.128 | | |
| FD2 | 4.25 | | | 0.167 | | |
| FD3 | 5.25 | | | 0.207 | | |
| FE | 4.75 | | | 0.187 | | |
| FE1 | 2.75 | | | 0.108 | | |
| FE2 | 1.75 | | | 0.069 | | |
| FE3 | 1.25 | | | 0.049 | | |
| SD | 0.25 | – | – | 0.010 | – | – |
| SE | 0.25 | – | – | 0.010 | – | – |

9 Ordering information

Table 11. Ordering information scheme

| Example: | NAND32GAH | 0 | H | ZA | 5 | F |
|--|-----------|---|---|----|---|---|
| Device type NAND flash memory | | | | | | |
| Density 32G = 4 Gbytes 64G = 8 Gbytes | | | | | | |
| Operating voltage A = $V_{CC} = 3.3\text{ V}$, $V_{CCQ} = 1.8\text{ V}$ or 3.3 V | | | | | | |
| Memory type H = eMMC | | | | | | |
| Device options 0 = no option | | | | | | |
| Product version H = version H | | | | | | |
| Package ZA = LFBGA169 12 x 16 x 1.4 mm | | | | | | |
| Temperature range 5 = -25 to 85 °C | | | | | | |
| Packing E = ECOPACK package, standard packing F = ECOPACK package, tape & reel packing | | | | | | |

Note: Other digits may be added to the ordering code for preprogrammed parts or other options. Devices are shipped from the factory with the memory content bits erased to '1'. For further information on any aspect of the device, please contact your nearest Numonyx sales office.

10 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 22-Sep-2008 | 1 | Initial release. |
| 18-Nov-2008 | 2 | Document's status promoted from target specification to preliminary data. Removed: density of 16 Gbytes and package LFBGA169 14 x 18 x 1.4 mm (ZD) throughout the document. Modified: Table 3: Current consumption and Figure 2: LFBGA169 package connections (top view through package) . |
| 04-Dec-2008 | 3 | Modified Figure 7: LFBGA169 12 x 16 x 1.4 mm 132+21+16 3R14 0.50 mm, package outline . Minor text changes. |

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