Async/Page PSRAM Memory

MT45W512KW16PGA

For the latest data sheet, refer to Micron's Web site: www.micron.com/products/psram/

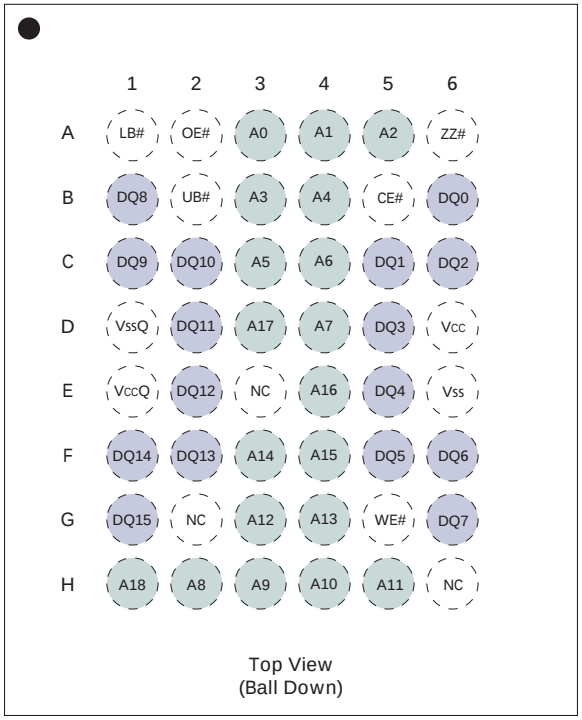
Features

- Asynchronous and page mode interface
- Random access time: 70ns
- VCC, VCCQ voltages:
  - 1.7V–1.95V VCC
  - 1.7V–3.6V VCCQ
- Page mode read access:
  - 16-word page size
  - Interpage read access: 70ns
  - Intrapage read access: 20ns
- Low power consumption:
  - Asynchronous READ: <20mA
  - Intrapage READ: <15mA
  - Standby: 80µA
  - Deep power-down: <10µA (TYP @ 25°C)
- Low power features:
  - Temperature compensated refresh (TCR)
  - On-chip temperature sensor
  - Partial array refresh (PAR)
  - Deep power-down (DPD) mode

Options	Designator
• Configuration	
– 512K x 16	MT45W512KW16P
• Package	
– 48-ball VFBGA (green)	GA
• Access time	
– 70ns	–70
• Operating temperature range	
– Wireless (–30°C to +85°C)	WT
– Industrial (–40°C to +85°C)[1]	IT

Notes: 1. Contact factory for availability.

Figure 1: Ball Assignment – 48-Ball VFBGA



Part Number Example:

MT45W512KW16PGA-70WT

General Description

Micron® PSRAM products are high-speed, CMOS PSRAM memory devices developed for low-power, portable applications. The MT45W512KW16P is an 8Mb DRAM core device organized as 512K x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or PSRAM offerings.

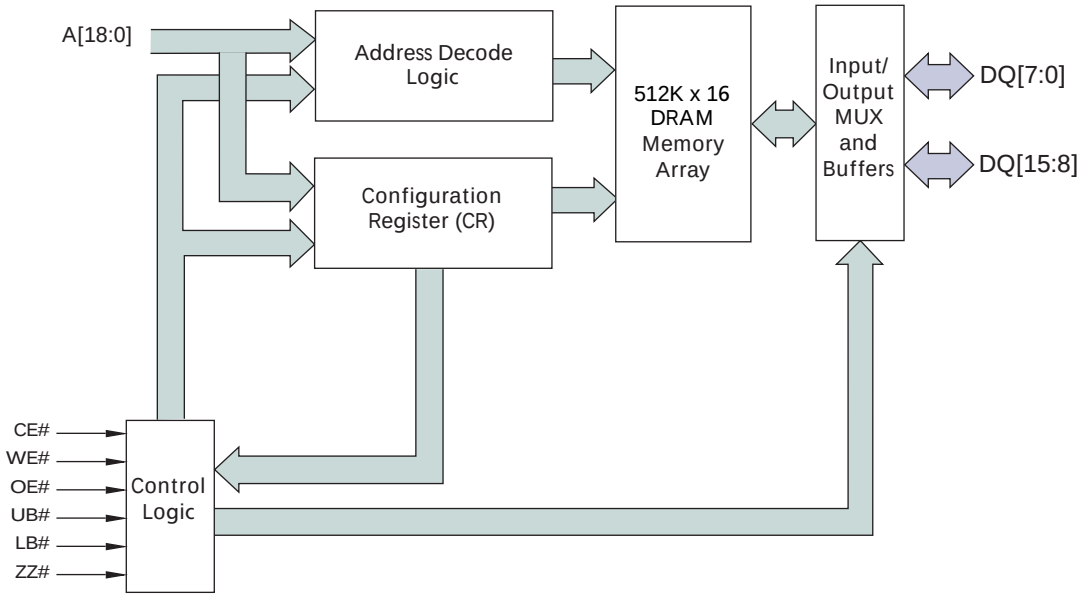
A user-accessible configuration register (CR) defines how the PSRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power up and can be updated at any time during normal operation.

To ensure seamless operation on an asynchronous memory bus, PSRAM products incorporate a transparent self refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Special attention has been focused on current consumption during self refresh. These PSRAM products include three system-accessible mechanisms to minimize refresh current. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature. The refresh rate decreases at lower temperatures to minimize current consumption during standby. TCR can also be set by the system for maximum device temperatures of +85°C, +45°C, and +15°C. Setting sleep enable (ZZ#) to LOW enables one of two low-power modes: partial-array refresh (PAR) or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are accessed through the CR.

Functional Block Diagram

Figure 2: Functional Block Diagram 512K x 16



Notes: 1. Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

Ball Descriptions

Table 1: VFBGA Ball Descriptions

VFBGA Ball Assignment	Symbol	Type	Description
H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3	A[18:0]	Input	**Address inputs:** Inputs for the address accessed during READ or WRITE operations. The address lines are also used to define the value to be loaded into the CR.
A6	ZZ#	Input	**Sleep enable:** When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR).
B5	CE#	Input	**Chip enable:** Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
A2	OE#	Input	**Output enable:** Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	**Write enable:** Enables WRITE operations when LOW.
A1	LB#	Input	**Lower byte enable:** DQ[7:0]
B2	UB#	Input	**Upper byte enable:** DQ[15:8]
G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6	DQ[15:0]	Input/ Output	**Data inputs/outputs.**
H6, E3, G2	NC		Not internally connected.
D6	V_{CC}	Supply	**Device power supply:** (1.7V–1.95V) Power supply for device core operation.
E1	V_{CCQ}	Supply	**I/O power supply:** (1.7V–3.6V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

Bus Operations

Table 2: Bus Operations

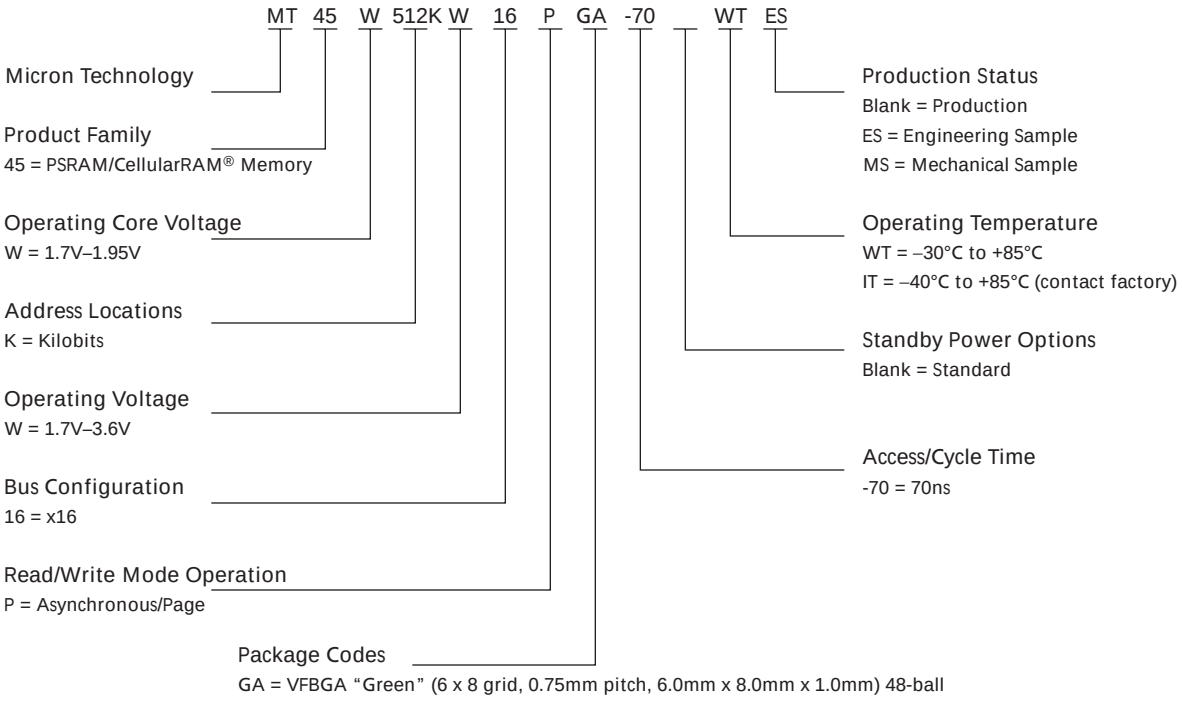
Mode	Power	CE#	WE#	OE#	LB#/UB#	ZZ#	DQ[15:0][1]	Notes
Standby	Standby	H	X	X	X	H	High-Z	1, 2
Read	Active	L	H	L	L	H	Data-out	3, 4
Write	Active	L	L	X	L	H	Data-in	3, 5, 4
No operation	Idle	L	X	X	X	H	X	4, 2
PAR	Partial-array refresh	H	X	X	X	L	High-Z	6
DPD	Deep power-down	H	X	X	X	L	High-Z	6
Load configuration register	Active	L	L	X	X	L	High-Z	

Notes:
1. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
2. V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) in order to achieve minimum standby current.
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When LB# alone is in select mode, only DQ[7:0] are affected. When UB# alone is in the select mode, only DQ[15:8] are affected.
4. The device will consume active power in this mode whenever addresses are changed.
5. When WE# is active, the OE# input is internally disabled and has no effect on the I/Os.
6. DPD is enabled when configuration register bit CR[4] is "0"; otherwise, PAR is enabled.

Part Numbering Information

Micron PSRAM devices are available in several different configurations and densities (see Figure 3).

Figure 3: Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart, go to the Micron Part Marking Decoder Web site at www.micron.com/products/parametric to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/products/parametric. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," available on Micron's Web site.

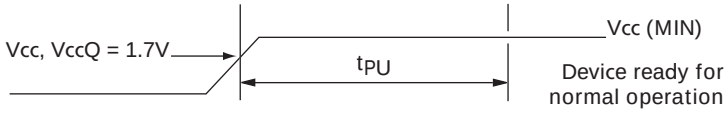
Functional Description

In general, the MT45W512KW16P device is a high-density alternative to SRAM and PSRAM products, popular in low-power, portable applications. The MT45W512KW16P contains an 8,388,608-bit DRAM core organized as 524,288 addresses by 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or PSRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

Micron PSRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default setting. V_{CC} and $V_{CC}Q$ must be applied simultaneously, and when they reach a stable level above 1.7V, the device will require 150µs to complete its self-initialization process (see Figure 4). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 4: Power-Up Initialization Timing



Bus Operating Modes

The MT45W512KW16P PSRAM product incorporates the industry-standard, asynchronous interface found on other low-power SRAM or PSRAM offerings. This bus interface supports asynchronous READ and WRITE operations as well as the bandwidth-enhancing page mode READ operation. The specific interface that is supported is defined by the value loaded into the CR.

Asynchronous Mode

Micron PSRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5 on page 7) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6 on page 7) occur when CE#, WE#, and LB#/UB# are driven LOW. During WRITE operations, the level of OE# is a “Don't Care”; WE# will override OE#. The data to be written will be latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). WE# LOW time must be limited to ^{t}CEM.

Figure 5: READ Operation

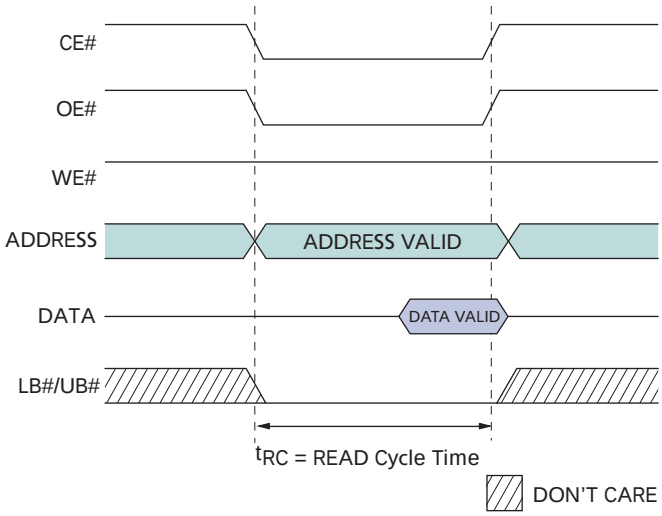
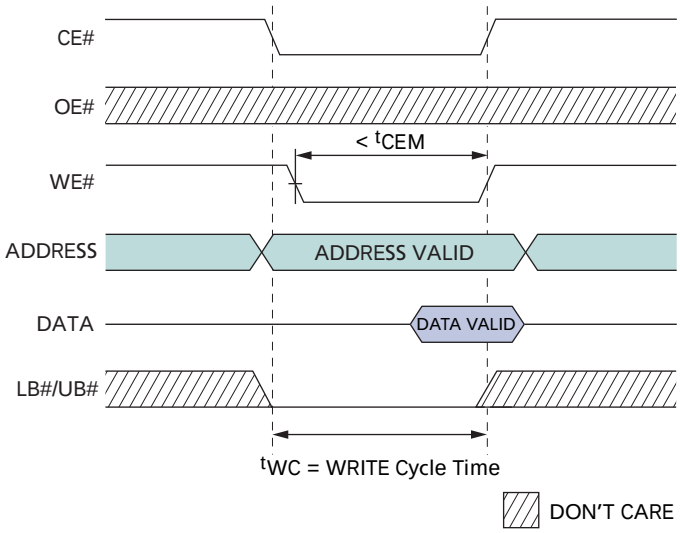


Figure 6: WRITE Operation



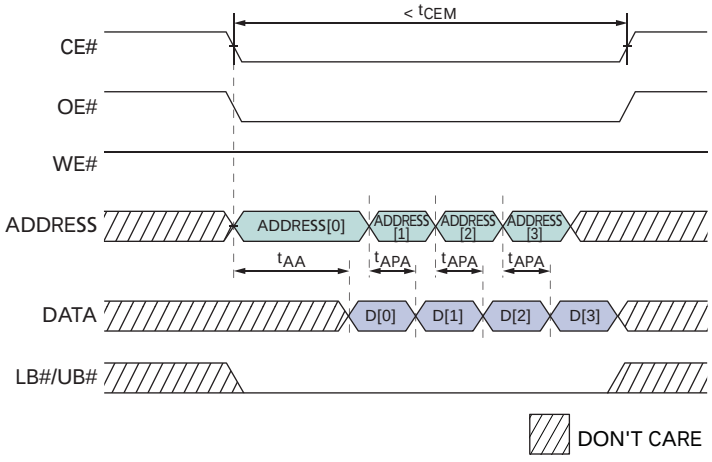
Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed. Adjacent addresses can then be quickly read by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address PSRAM page. Any change in addresses A[4] or higher will initiate a new ^{t}AA access. Figure 7 shows the timing diagram for a page mode access.

Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than ^{t}CEM.

Figure 7: Page READ Operation



LB#/UB# Operation

The lower byte (LB#) enable and upper byte (UB#) enable signals allow for byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the memory array and the internal value will remain unchanged. During a WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will appear to be deselected, it remains in an active mode as long as CE# is LOW.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation on the full array. Standby operation occurs when CE# and ZZ# are HIGH.

The device will enter a reduced power state during READ and WRITE operations where the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

Temperature-Compensated Refresh (TCR)

TCR allows for adequate refresh at different temperatures. This PSRAM device includes an on-chip temperature sensor. When the sensor is enabled, it continually adjusts the refresh rate according to the operating temperature. The on-chip sensor is enabled by default.

Three fixed refresh rates are also available, corresponding to temperature thresholds of +15°C, +45°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the PSRAM device. If the case temperature is +35°C, the system can minimize self refresh current consumption by selecting the +45°C setting. Using the +15°C setting in the same environment would result in an inadequate refresh rate and cause data corruption.

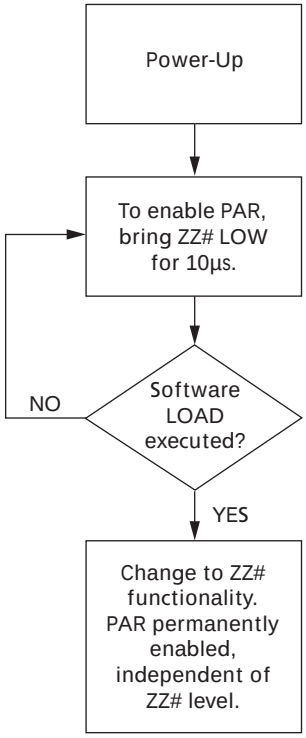
Partial-Array Refresh (PAR)

PAR restricts refresh operation to a portion of the total memory array. This feature enables the system to reduce refresh current by only refreshing that part of the memory array that is absolutely necessary. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (Table 3 on page 13). READ and WRITE operations are ignored during PAR operation.

The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bringing the ZZ# ball to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see “Software Access to the Configuration Register” on page 11). PAR is enabled immediately upon setting CR[4] to “1” using this method. However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up (see Figure 8 on page 10).

Figure 8: Software Access PAR Functionality



Deep Power-Down (DPD) Operation

DPD operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the PSRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the PSRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing ZZ# to the LOW state for longer than 10µs. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

Driving ZZ# LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

The device should not be put into DPD using CR software access.

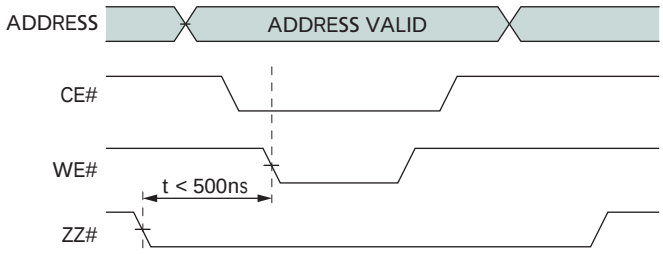
Configuration Register (CR) Operation

The CR defines how the PSRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the CR. This register can be updated any time the device is operating in a standby state. Figure 12 on page 13 describes the control bits used in the CR. At power-up, the CR is set to 0010h.

Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (see Figure 9). The values placed on addresses A[18:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

Figure 9: Load Configuration Register Operation



Software Access to the Configuration Register

The contents of the CR can either be read or modified using a software sequence. The nature of this access mechanism may eliminate the need for the ZZ# ball.

If the software mechanism is used, ZZ# can simply be tied to $V_{CC}Q$. The port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to $V_{CC}Q$ if the system will use DPD; DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 10 on page 12). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 11 on page 12). Note that a third READ cycle of the highest address will cancel the access sequence until a different address is read.

The address used during all READ and WRITE operations is the highest address of the PSRAM device being accessed (7FFFFh for 8Mb); the content of this address is not changed by using this sequence. The data bus is used to transfer data into or out of bits 15–0 of the CR.

Writing to the CR using the software sequence modifies the function of the ZZ# ball. Once the software sequence loads the CR, the level of the ZZ# ball no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This ZZ# functionality will continue until the next time the device is powered up. The operation of the ZZ# ball is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ#-controlled) method of loading the CR.

Figure 10: Software Access Load Configuration Register

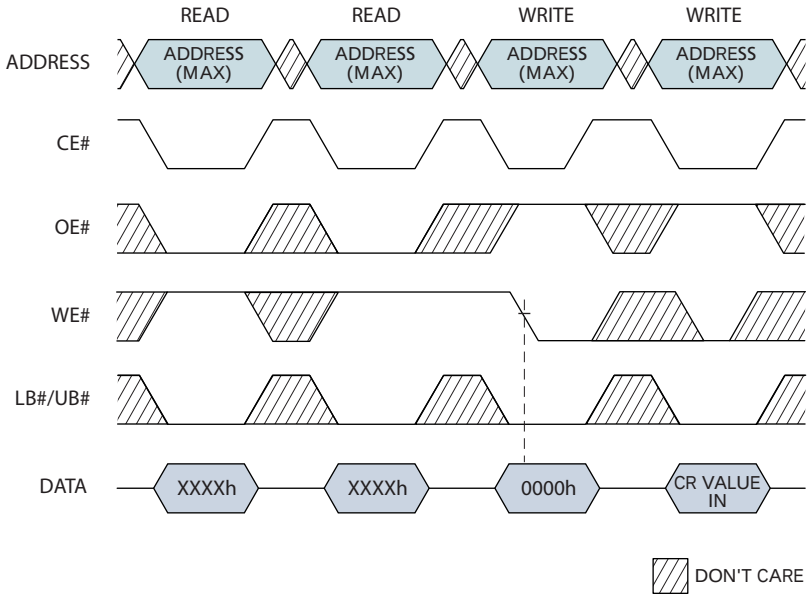


Figure 11: Software Access Read Configuration Register

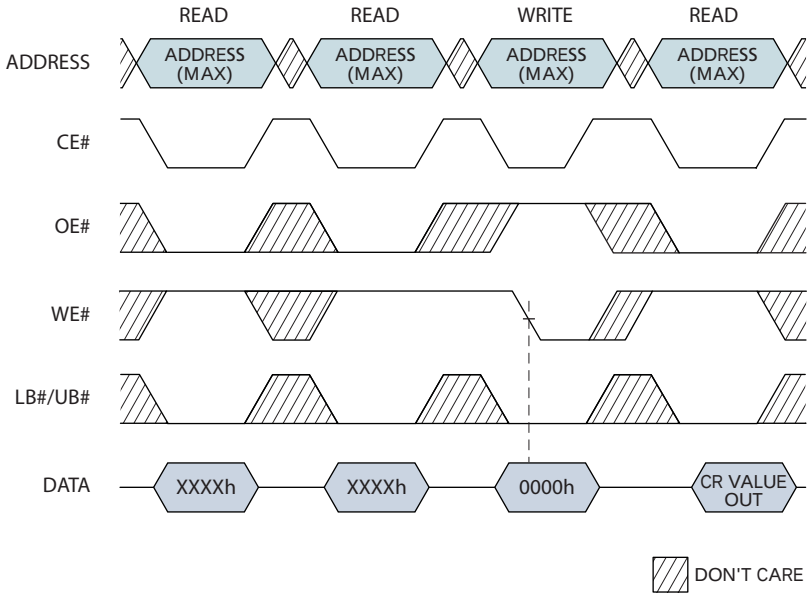
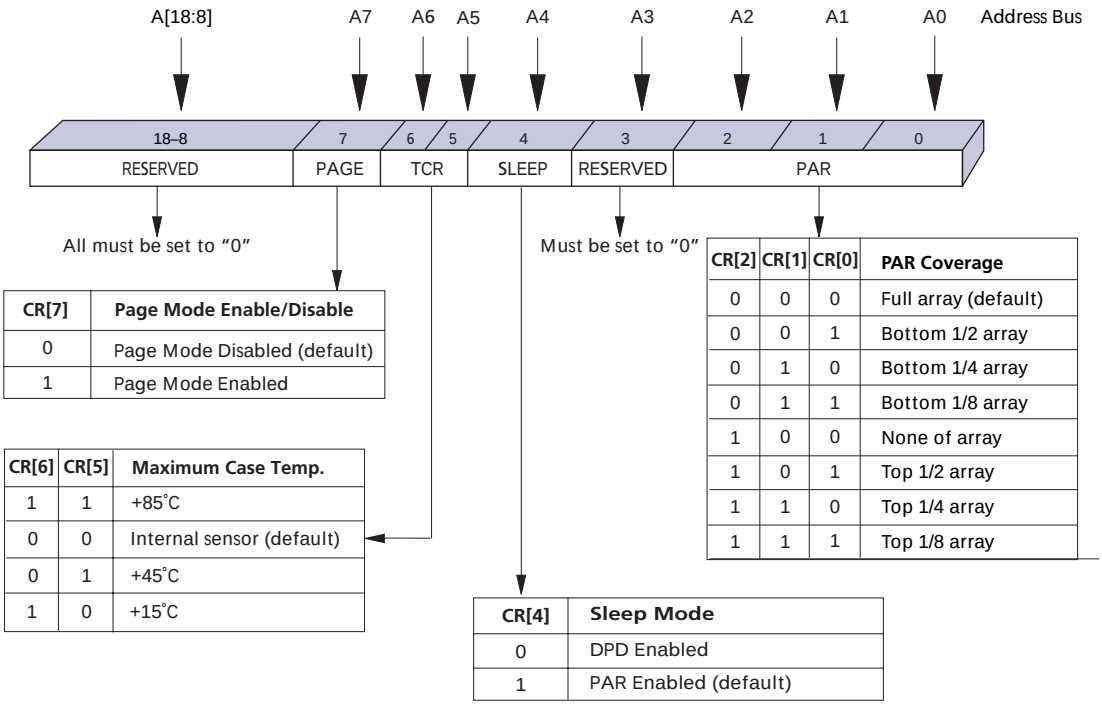


Figure 12: Configuration Register Bit Mapping



CR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enabled

CR[6]	CR[5]	Maximum Case Temp.
1	1	+85°C
0	0	Internal sensor (default)
0	1	+45°C
1	0	+15°C

CR[2]	CR[1]	CR[0]	PAR Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 1/8 array

CR[4]	Sleep Mode
0	DPD Enabled
1	PAR Enabled (default)

Partial Array Refresh (CR[2:0]) Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the system to reduce current by only refreshing that part of the memory array required by the host system. The refresh options are: full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 3).

Table 3: 8Mb Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–07FFFFh	512K x 16	8Mb
0	0	1	One-half of die	000000h–03FFFFh	256K x 16	4Mb
0	1	0	One-quarter of die	000000h–01FFFFh	128K x 16	2Mb
0	1	1	One-eighth of die	000000h–00FFFFh	64K x 16	1Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	40000h–07FFFFh	256K x 16	4Mb
1	1	0	One-quarter of die	60000h–07FFFFh	128K x 16	2Mb
1	1	1	One-eighth of die	70000h–07FFFFh	64K x 16	1Mb

Sleep Mode (CR[4]) Default = PAR Enabled, DPD Disabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; this should only be done using ZZ# to access the CR.

DPD operation disables all refresh-related activity. This mode will be used when the system does not require the storage provided by the PSRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the PSRAM device will require 150µs to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

TCR (CR[6:5]) Default = On-Chip Temperature Sensor

This PSRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The on-chip TCR is enabled by clearing both of the TCR bits in the refresh configuration register (CR[6:5] = 00b). Any other TCR setting enables a fixed refresh rate. When the on-chip temperature sensor is enabled, the device continually adjusts the refresh rate according to the operating temperature.

The TCR bits also allow for adequate fixed rate refresh at three different temperature thresholds (+15°C, +45°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the PSRAM device. If the case temperature is +35°C, the system can minimize self-refresh current consumption by selecting the +45°C setting. Using the +15°C setting in the same environment would result in an inadequate refresh rate and cause data corruption.

Page Mode READ Operation (CR[7]) Default = Disabled

The page mode operation bit determines whether page mode READ operations are enabled. In the power-up default state, page mode is disabled.

Electrical Characteristics

Stresses greater than those listed in Table 4 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Parameter	Rating
Voltage to any ball except V_{CC}, V_{CCQ} relative to V_{SS}	–0.50V to (4.0V or VCCQ + 0.3V, whichever is less)
Voltage on V_{CC} supply relative to V_{SS}	–0.2V to 2.45V
Voltage on V_{CCQ} supply relative to V_{SS}	–0.2V to 4.0V
Storage temperature	–55°C to 150°C
Operating temperature (case) Wireless Industrial	 –30°C to 85°C –40°C to 85°C
Soldering temperature and time 10 seconds (solder ball only)	 260°C

Table 5: Electrical Characteristics and Operating Conditions
Wireless Temperature ($–30^{o}C \le T_C \le +85\ ^{o}C$), Industrial Temperature ($–40^{o}C < T_C < +85^{o}C$)

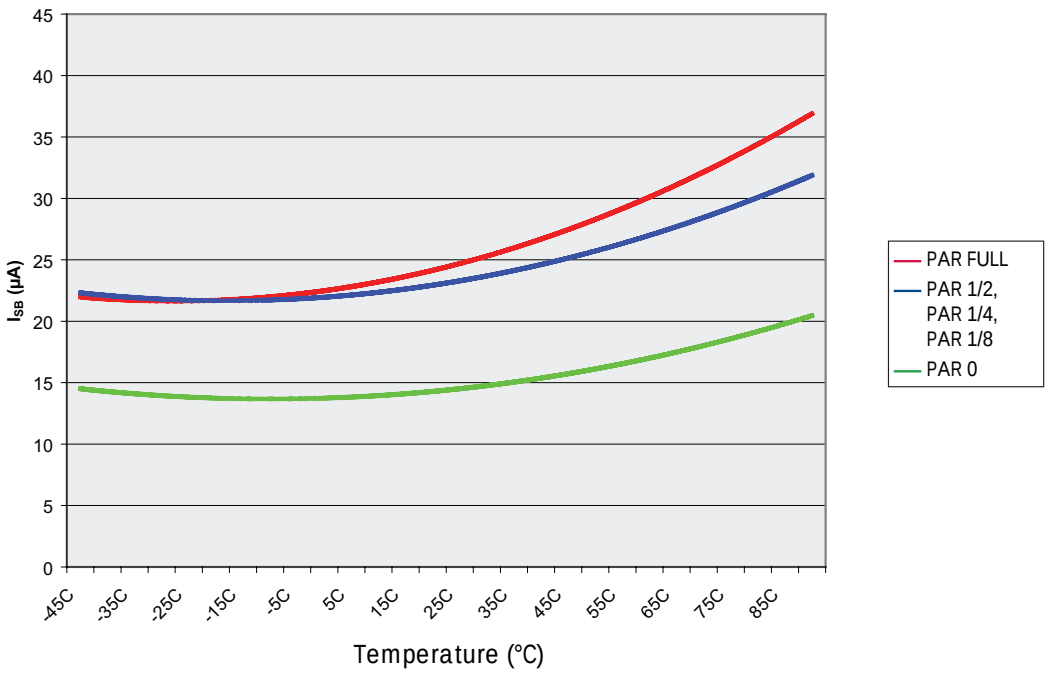
Description	Conditions	Symbol		Min	Max	Units	Notes
Supply voltage		V_{CC}		1.7	1.95	V	
I/O supply voltage		V_{CCQ}		1.7	3.6	V	
Input high voltage		V_{IH}		1.4	V_{CCQ} + 0.2	V	1
Input low voltage		V_{IL}		–0.2	0.4	V	2
Output high voltage	I_{OH} = –0.2mA	V_{OH}		0.8 V_{CCQ}		V	
Output low voltage	I_{OL} = 0.2mA	V_{OL}			0.2 V_{CCQ}	V	
Input leakage current	V_{IN} = 0 to V_{CCQ}	I_{LI}			1	µA	
Output leakage current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous random READ/WRITE	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0	I_{CC1}	–70		20	mA	3
Asynchronous page READ		I_{CC1P}	–70		15	mA	3
Standby current	V_{IN} = V_{CCQ} or 0V CE# = V_{CCQ}	I_{SB}			80	µA	4

Notes:
1. Input signals may overshoot to V_{CCQ} + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions
3. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
4. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. In order to achieve low standby current, all inputs must be driven to V_{CCQ} or V_{SS}. I_{SB} may be slightly higher for up to 500ms after power-up or when entering standby mode.

Typical Standby Currents

Figure 13 refers to the typical standby currents for the MT45W512KW16P device. The values shown in Figure 13 are measured with the on-chip temperature sensor control enabled (default setting).

Figure 13: Typical Refresh Current vs. Temperature (I_{TCR})



Notes: 1. Typical I_{SB} currents for each PAR setting with the appropriate TCR selected, or temperature sensor enabled.

Table 6: DPD Specifications and Conditions

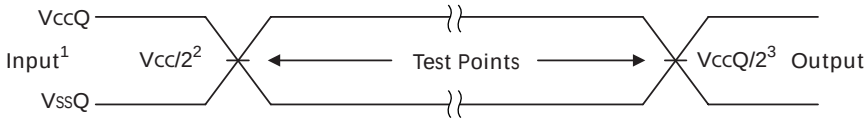
Description	Conditions	Symbol	TYP	Units
Deep power-down	V_{IN} = VccQ or 0V; +25°C ZZ# = 0V CR[4] = 0	I_{ZZ}	10	µA

Table 7: Capacitance Specifications and Conditions

Description	Conditions	Symbol	Min	Max	Units	Notes
Input capacitance	T_C = +25ºC; f = 1 MHz; V_{IN} = 0V	C_{IN}	2.0	6.5	pF	1
Input/output capacitance (DQ)		C_{IO}	3.0	6.5	pF	1

Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.

Figure 14: AC Input/Output Reference Waveform



Notes:
1. AC test inputs are driven at VccQ for a logic 1 and VssQ for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at Vcc/2. Due to the possibility of a difference between Vcc and VccQ, the input test point may not be shown to scale.
3. Output timing ends at VccQ/2.

Figure 15: Output Load Circuit

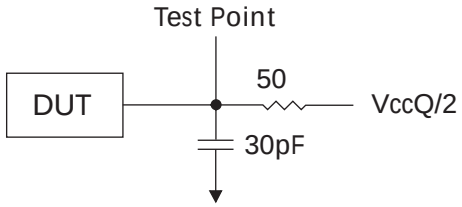


Table 8: READ Cycle Timing Requirements

Parameter	Symbol	70ns		Units	Notes
		Min	Max		
Address access time	^{t}AA		70	ns	
Page access time	^{t}APA		20	ns	
LB#/UB# access time	^{t}BA		70	ns	
LB#/UB# disable to High-Z output	^{t}BHZ		8	ns	1
LB#/UB# enable to Low-Z output	^{t}BLZ	10		ns	2
Maximum CE# pulse width	^{t}CEM		8	µs	3
Chip select access time	^{t}CO		70	ns	
Chip disable to High-Z output	^{t}HZ		8	ns	1
Chip enable to Low-Z output	^{t}LZ	10		ns	1
Output enable to valid output	^{t}OE		20	ns	
Output hold from address change	^{t}OH	5		ns	
Output disable to High-Z output	^{t}OHZ		8	ns	1
Output enable to Low-Z output	^{t}OLZ	5		ns	1
Page cycle time	^{t}PC	20		ns	
READ cycle time	^{t}RC	70		ns	

Notes:
1. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 17. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 17. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
3. Page mode enabled only.

Table 9: WRITE Cycle Timing Requirements

Parameter	Symbol	70ns		Units	Notes
		Min	Max		
Address setup time	^{t}AS	0		ns	
Address valid to end of write	^{t}AW	70		ns	
Byte select to end of write	^{t}BW	70		ns	
CE# HIGH time during write	^{t}CPH	5		ns	
Chip enable to end of write	^{t}CW	70		ns	
Data hold from write time	^{t}DH	0		ns	
Data write setup time	^{t}DW	23		ns	
Chip enable to Low-Z output	^{t}LZ	10		ns	1
End write to Low-Z output	^{t}OW	5		ns	1
WRITE cycle time	^{t}WC	70		ns	
WRITE to High-Z output	^{t}WHZ		8	ns	2
WRITE pulse width	^{t}WP	46		ns	3
WRITE pulse width HIGH	^{t}WPH	10		ns	
WRITE recovery time	^{t}WR	0		ns	

Notes:
1. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 17. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 17. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. WE# LOW time must be limited to ^{t}CEM (8µs).

Table 10: Load Configuration Register Timing Requirements

Description	Symbol	70ns		Units
		Min	Max	
Address setup time	^{t}AS	0		ns
Address valid to end of write	^{t}AW	70		ns
Chip deselect to ZZ# LOW	^{t}CDZZ	5		ns
Chip enable to end of write	^{t}CW	70		ns
WRITE cycle time	^{t}WC	70		ns
WRITE pulse width	^{t}WP	40		ns
WRITE recovery time	^{t}WR	0		ns
ZZ# LOW to WE# LOW	^{t}ZZWE	10	500	ns

Table 11: DPD Timing Requirements

Description	Symbol	70ns		Units
		Min	Max	
Chip deselect to ZZ# LOW	^{t}CDZZ	5		ns
DPD recovery	^{t}R	150		µs
Minimum ZZ# pulse width	^{t}ZZ (MIN)	10		µs

Timing Diagrams

Figure 16: Power-Up Initialization Period

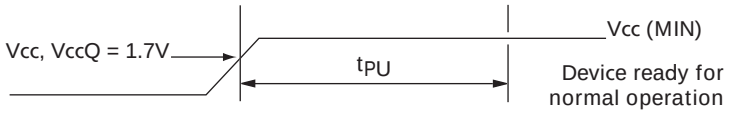


Table 12: Initialization Timing Parameters

Parameter	Symbol	70ns		Units
		Min	Max	
Initialization period (required before normal operations)	tPU	150		µs

Figure 17: Load Configuration Register

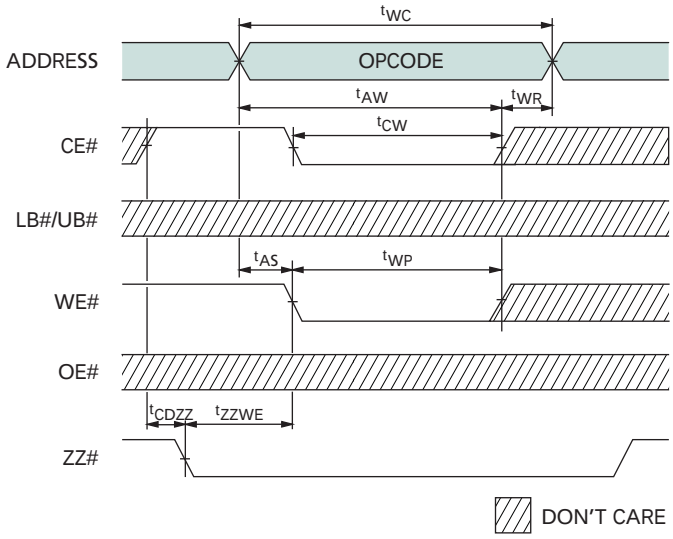


Figure 18: Deep Power-Down – Entry/Exit

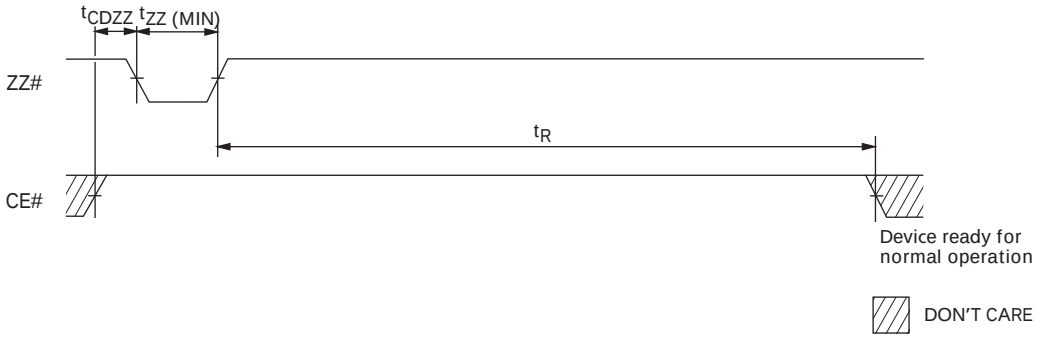


Figure 19: Single READ Operation (WE# = VIH)

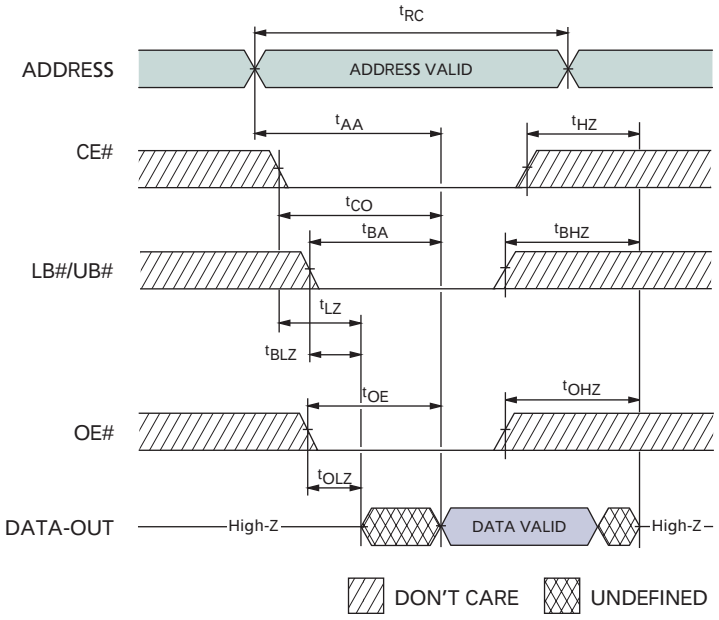


Figure 20: Page Mode READ Operation (WE# = VIH)

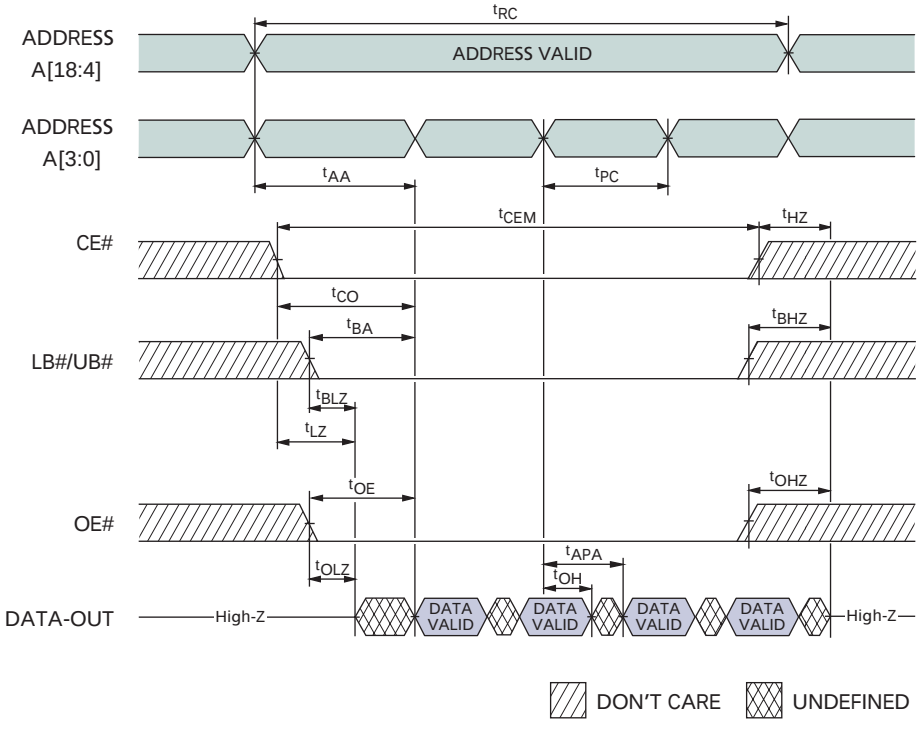


Figure 21: WRITE Cycle (WE# Control)

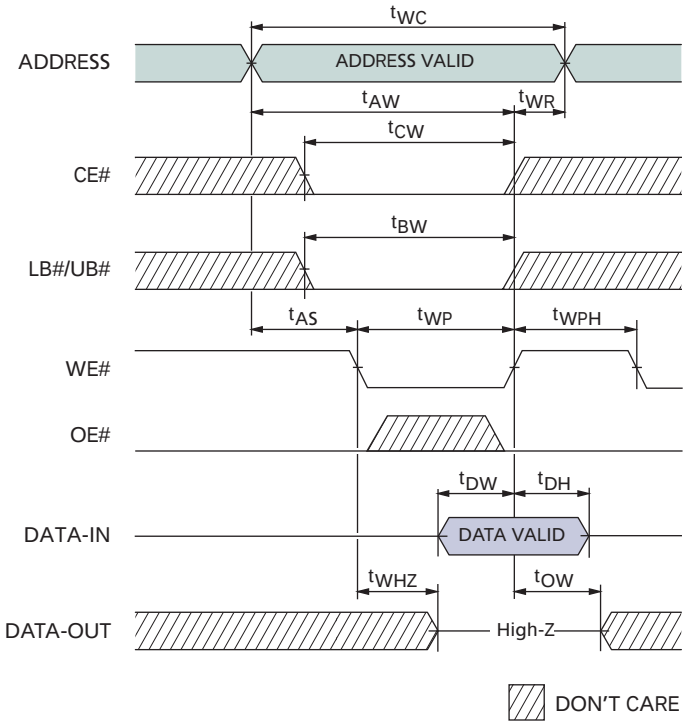


Figure 22: WRITE Cycle (CE# Control)

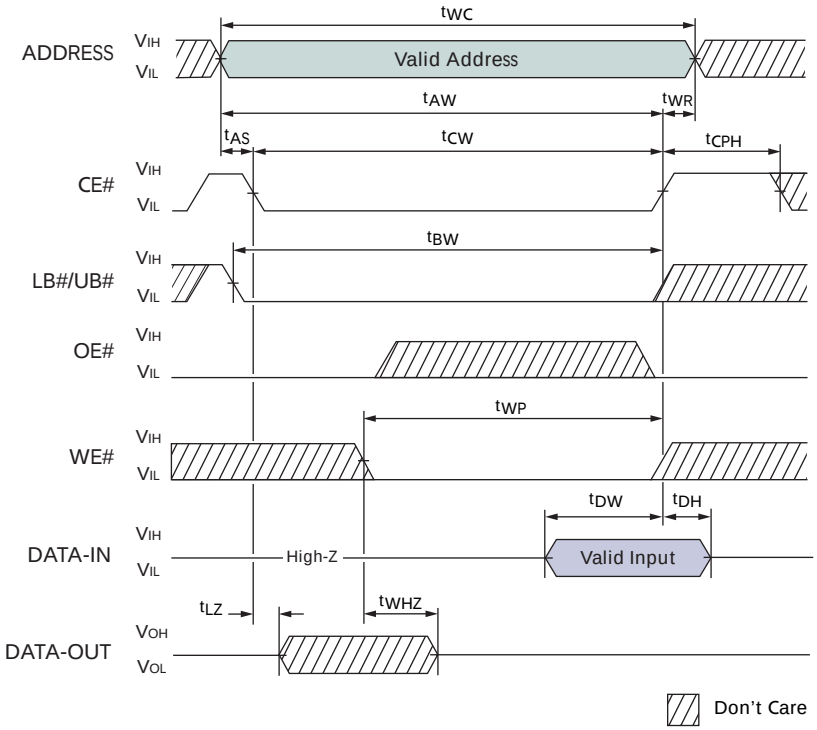
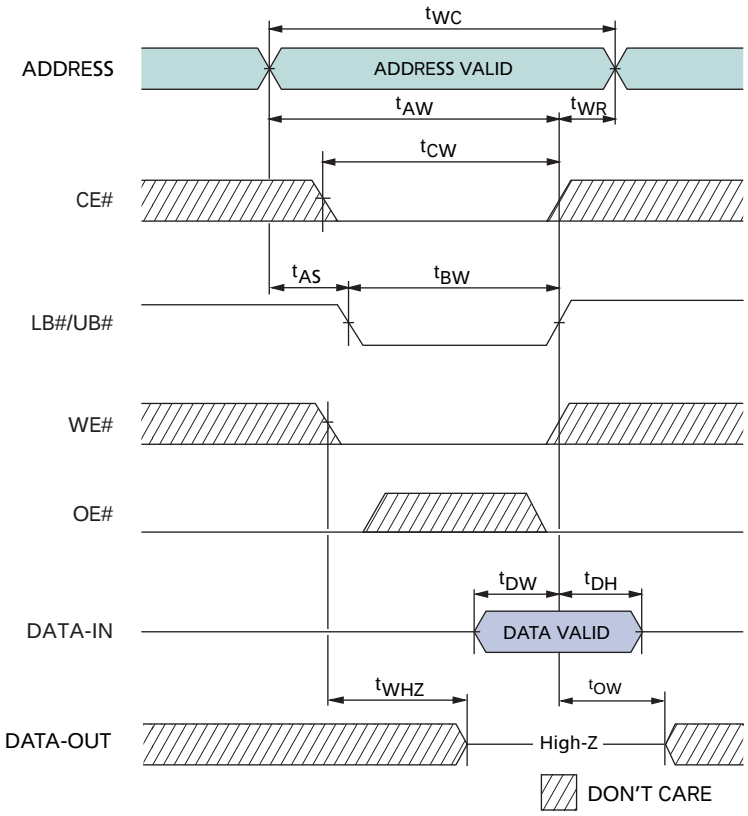
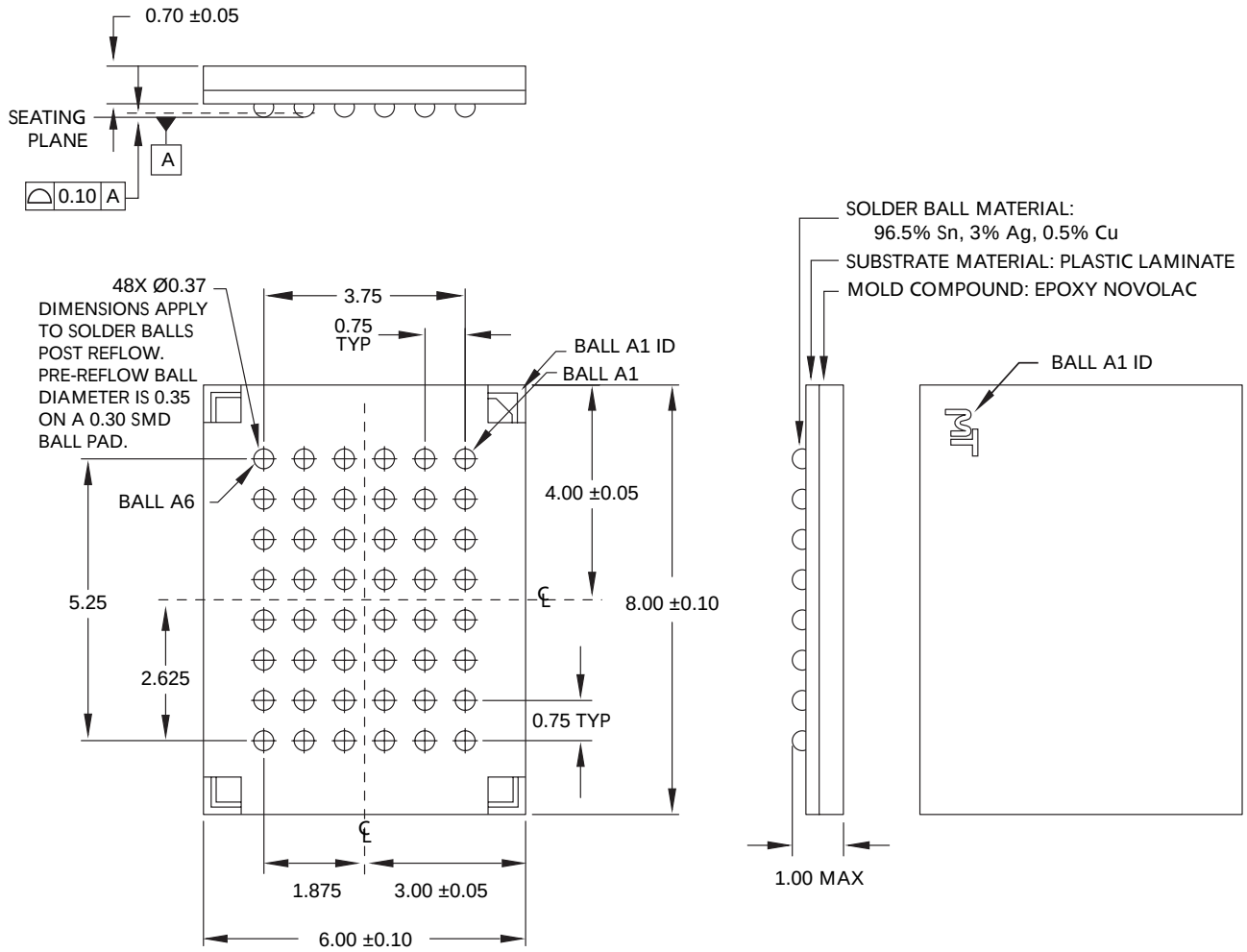


Figure 23: WRITE Cycle (LB#/UB# Control)



Package Dimensions

Figure 24: 48-Ball VFBGA



Notes:
1. All dimensions in millimeters, MAX/MIN or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. The MT45W512KW16P uses “green” packaging.

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