M69AW048B

32 Mbit (2M x16) 3V Asynchronous PSRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.3V
- ACCESS TIMES: 70ns
- LOW STANDBY CURRENT: 100µA
- DEEP POWER-DOWN CURRENT: 10µA
- BYTE CONTROL: $\overline{UB}$/$\overline{LB}$
- PROGRAMMABLE PARTIAL ARRAY
- COMPATIBLE WITH STANDARD LPSRAM
- TRI-STATE COMMON I/O
- 8 WORD PAGE ACCESS CAPABILITY: 18ns
- WIDE OPERATING TEMPERATURE
  - T_A = –30 to +85°C
- POWER-DOWN MODES
  - Deep Power-Down
  - 4 Mbit Partial Array Refresh
  - 8 Mbit Partial Array Refresh
  - 16 Mbit Partial Array Refresh

Figure 1. Package

TFBGA48 (ZB)
6x8 mm

TABLE OF CONTENTS

SUMMARY DESCRIPTION

The M69AW048B is a 32 Mbit (33,554,432 bit) CMOS memory, organized as 2,097,152 words by 16 bits, and is supplied by a single 2.7V to 3.3V supply voltage range.

M69AW048B is a member of STMicroelectronics PSRAM memory family. These devices are manufactured using dynamic random access memory cells, to minimize the cell size, and maximize the amount of memory that can be implemented in a given area.

However, through the use of internal control logic, the device is fully static in its operation, requiring no external clocks or timing strobes, and has a standard Asynchronous SRAM Interface.

The internal control logic of the M69AW048B handles the periodic refresh cycle, automatically, and without user involvement.

Write cycles can be performed on a single byte by using Upper Byte Enable ($\overline{UB}$) and Lower Byte Enable ($\overline{LB}$).

The device can be put into standby mode using Chip Enable ($\overline{E1}$) or in Power-Down mode by using Chip Enable (E2).

The device features various kinds of Power-Down modes for power saving as a user configurable option:

- The Partial Array Refresh (PAR) performs a limited refresh of the part of the PSRAM array (4 Mbits, 8 Mbits, 16Mbits) that contains essential data.
- Deep Power-Down mode: this mode achieves a very low current consumption by halting all the internal activities. Since the refresh circuitry is halted, the duration of the power-down should be less than the maximum period for refresh.

Figure 2. Logic Diagram

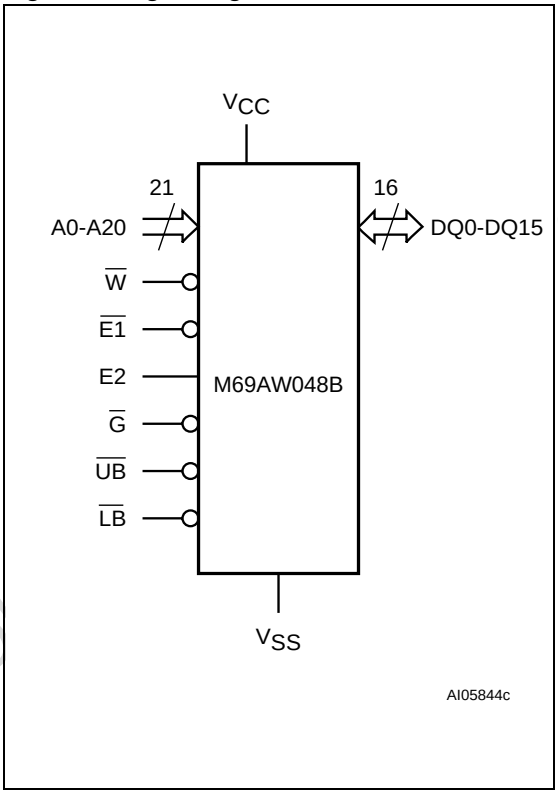
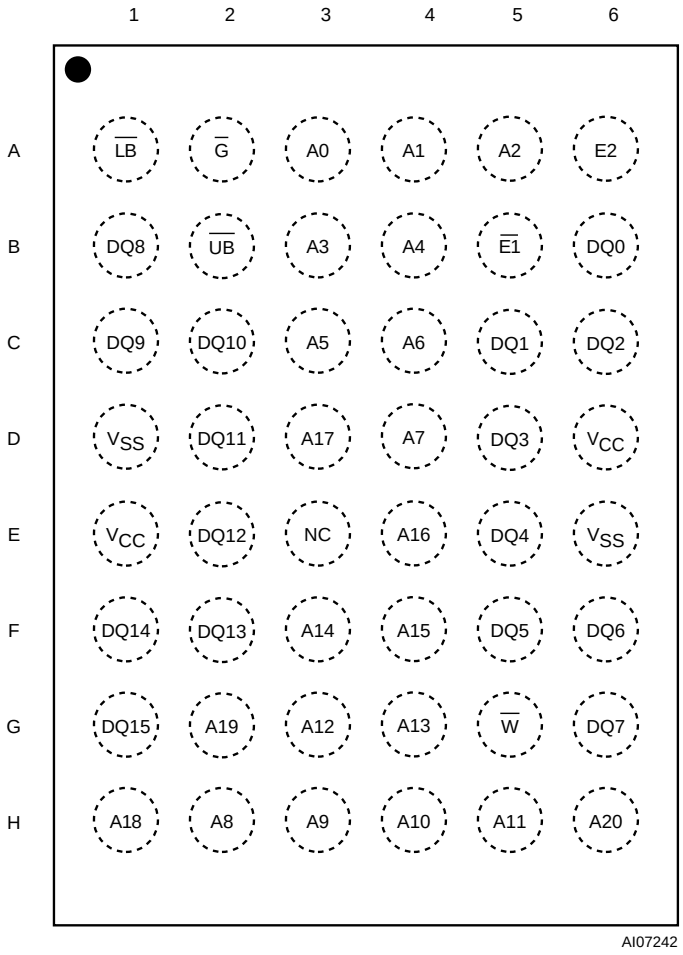


Table 1. Signal Names

A0-A20	Address Input
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enable, Power Down
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable
$\overline{LB}$	Lower Byte Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected (no internal connection)

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram, and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). The Address Inputs select the cells in the memory array to access during Read and Write operations.

Data Inputs/Outputs (DQ8-DQ15). The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable (UB) is driven Low.

Data Inputs/Outputs (DQ0-DQ7). The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable (LB) is driven Low.

Chip Enable ($\overline{E1}$). When asserted (Low), the Chip Enable, $\overline{E1}$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is put, automatically, in low-power Standby mode.

Chip Enable (E2). The Chip Enable, E2, puts the device in Power-down mode (Deep Power-Down, PAR and Standby) when it is driven Low. One of these, Deep Power-Down mode, is the lowest power mode.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

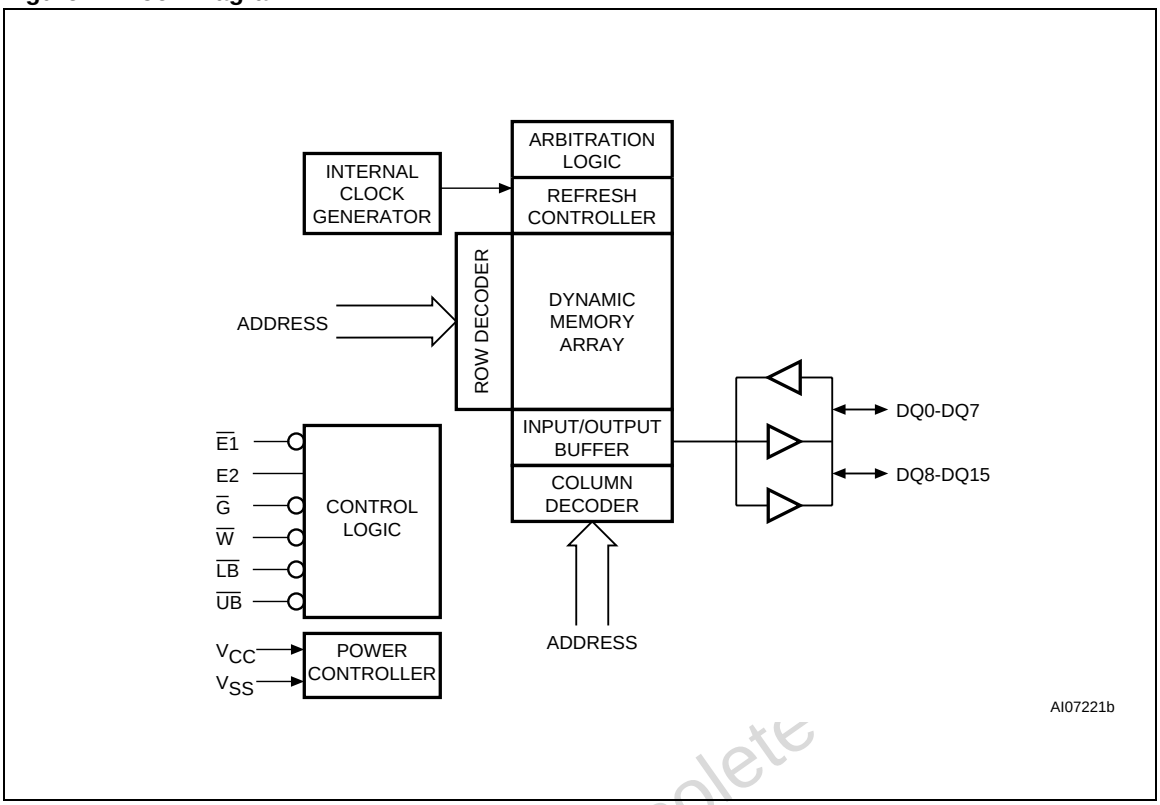
Upper Byte Enable ($\overline{UB}$). The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

Lower Byte Enable ($\overline{LB}$). The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read, Write, etc.) and for driving the refresh logic, even when the device is not being accessed.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

Figure 4. Block Diagram



OPERATION

Operational modes are determined by device control inputs W, E1, E2, LB and UB as summarized in the Operating Modes table (see Table 2., Operating Modes).

Power-Up Sequence

Because the internal control logic of the M69AW048B needs to be initialized, the following Power-Up procedure must be followed before the memory is used:

- Apply power and wait for V_{CC} to stabilize,
- Wait 300µs while driving both Chip Enable signals ($\overline{E1}$ and E2) High.

See also Figure 24. for details on the Power-Up AC waveforms.

Read Mode

The device is in Read mode when:

- Write Enable ($\overline{W}$) is High and
- Output Enable ($\overline{G}$) Low and
- the two Chip Enable signals are asserted ($\overline{E1}$ is Low, and E2 is High).

The time taken to enter Read mode (t_{ELQV}, t_{GLQV} or t_{BLQV}) depends on which of the above signals was the last to reach the appropriate level.

Data out (DQ15-DQ0) may be indeterminate during t_{ELQX}, t_{GLQX} and t_{BLQX} but data will always be valid during t_{AVQV}. See Figures 7, 8, 9, 10 and 11 and Table 11., Read Mode AC Characteristics, for details of when the outputs become valid.

Write Mode

The device is in Write mode when

- Write Enable ($\overline{W}$) is Low and
- Chip Enable ($\overline{E1}$) is Low and E2 is High
- at least one of Upper Byte Enable (UB) and Lower Byte Enable (LB) is Low.

The Write cycle begins just after the event (the falling edge) that causes the last of these conditions to become true (t_{AVWL} or t_{AVEL} or t_{AVBL}).

The Write cycle is terminated by the rising edge of Write Enable (W) or Chip Enable ($\overline{E1}$), whichever occurs first.

If the device is in Write mode (Chip Enable ($\overline{E1}$) is Low, Output Enable ($\overline{G}$) is Low, Upper Byte Enable (UB) and/or Lower Byte Enable (LB) is Low, then Write Enable (W) will return the outputs to high impedance within t_{WHDZ} of its rising edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable (W), or for t_{DVEH} before the rising edge of Chip Enable ($\overline{E1}$), whichever occurs first, and remain valid for t_{BHDZ}, t_{WHDZ}, t_{EHDZ}.

See Figures 12, 13, 14, 15, 16 and 17 and Table 12., Write Mode AC Characteristics, for details of when the outputs become valid.

Standby Mode

The device is in Standby mode when:

- Chip Enable ($\overline{E1}$) is High and
- Chip Enable (E2) is High

The input/output buffers and the decoding/control logic are switched off, but the dynamic array continues to be refreshed. In this mode, the memory current consumption, I_{SB}, is reduced, and the data remains valid.

See Figures 17 and Table 13., Standby/Power-Down Mode AC Characteristics, for details of when the outputs become valid.

Power-down Modes

Description of Power-Down Modes. The M69AW048B has four Power-down modes, Deep Power-Down, 4 Mbit Partial Array Refresh, 8 Mbit Partial Array Refresh, and 16 Mbit Partial Array Refresh (see Table 4. and Figure 22.).

These can be entered using a series of read and write operations. Each mode has following features. The default state is Deep Power-Down and it is the lowest power consumption but all data will be lost once E2 is brought Low for Power-down. No sequence is required to put the device in Deep Power-Down mode after Power-up.

The device is in one of the Power-down modes when:

- Chip Enable (E2) is Low

All the device logic is switched off and all internal operations are suspended. This gives the lowest power consumption. In this operating mode, no refresh is performed, and data is lost if the duration is longer than 10ns. This mode is useful for those applications where the data contents are no longer needed, and can be lost, but where reduced current consumption is of major importance.

Power-Down Program Sequence. The Power-Down Program sequence is used to program the Power-Down Configuration. It requires a total of six read and write operations, with specific addresses and data. Between each read or write operation the device must be in Standby mode.

Table 4. shows the sequence. In the first cycle, the Byte at the highest memory address (MSB) is read. In the second and third cycles, the data (RDa) read by first cycle are written back. If the third cycle is written into a different address, the sequence is aborted, and the data written by the third cycle is valid as in a normal write operation. In the fourth and fifth cycles, the Power-Down Configuration data is written. The data of the fourth cycle must be

set to '0000h', and the data of the fifth cycle is the Power-Down Configuration data (see Table 5., Power-Down Configuration Data). If the fourth cycle is written into a different address, the sequence is aborted. In the last cycle, a read is made from the specific Power-Down Configuration address (see Table 6., Power-Down Configuration Addresses). The Power-Down Configuration data and address must correspond, otherwise the sequence is aborted.

When this sequence is performed to take the device from one PAR mode to another, the write data may be lost. So, if a PAR mode is used, this sequence should be performed prior to any normal read or write operations.

Table 2. Operating Modes

Operation	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Standby (Deselected)	V_{IH}	V_{IH}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Power-Down (2)	X	V_{IL}	X	X	X	X	Hi-Z	Hi-Z	Power-Down (I_{CCPD}, I_{CCP4}, I_{CCP8}, I_{CCP16})
No Read (1)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Output Disable
Lower Byte Read (1)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write (1)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
No Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Output Disable
Upper Byte Read (1)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write (1)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read (1)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write (1)	V_{IL}	V_{IH}	V_{IL}	V_{IH}(3)	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})

Note: X = V_{IH} or V_{IL}.

1. Should not be kept in this logic condition for a period longer than 1µs.
2. Power-Down mode can be entered from Standby state and all DQ pins are in High-Z state. The Power-Down current and data retention depend on the selection of Power-Down programming.
3. $\overline{G}$ can be V_{IL} during the Write operation if the following conditions are satisfied:
   a. Write pulse is initiated by $\overline{E1}$ ($\overline{E1}$ Controlled Write timing), or cycle time of the previous operation cycle is satisfied;
   b. $\overline{G}$ stays V_{IL} during the entire Write cycle.

Table 3. Power-Down Modes

Mode	Data Retention	Retention Address
Deep Power-Down (Default)	No	N/A
4Mb PAR	4 Mbit	00000h – 3FFFFh
8Mb PAR	8 Mbit	00000h – 7FFFFh
16Mb PAR	16 Mbit	00000h – FFFFFh

Table 4. Power-Down Program Sequence

Cycle #	Operation	Address	Data
1st	Read	1FFFFFh (MSB)	Read Data (RDa)
2nd	Write	1FFFFFh	RDa
3rd	Write	1FFFFFh	RDa
4th	Write	1FFFFFh	0000h
5th	Write	1FFFFFh	PDC Data(1)
6th	Read	PDC Address(1)	Read Data (RDb)

Note: 1. PDC Power-Down Configuration.

Table 5. Power-Down Configuration Data

Power-Down Modes	Power-Down Configuration Data			
	DQ15–DQ9	DQ8-DQ2	DQ1	DQ0
Deep Power-Down (default)	0	0	1	1
4Mb PAR	0	0	1	0
8Mb PAR	0	0	0	1
16Mb PAR	0	0	0	0

Table 6. Power-Down Configuration Addresses

Power-Down Modes	Power-Down Configuration Addresses			
	A20	A19	A18–A0	Binary
Deep Power-Down (default)	1	1	1	1FFFFFh
4Mb PAR	0	1	1	0FFFFFh
8Mb PAR	1	0	1	17FFFFh
16Mb PAR	0	0	1	07FFFFh

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
I_O	Output Current	–50	50	mA
T_A	Ambient Operating Temperature	–30	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{CC}	Core Supply Voltage	–0.5	3.6	V
V_{IO}	Input or Output Voltage	–0.5	3.6	V

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 8., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 8. Operating and AC Measurement Conditions

Parameter	M69AW048B		Unit
	70		
	Min	Max	
V_{CC} Supply Voltage[1]	2.7	3.3	V
Ambient Operating Temperature	–30	85	°C
Load Capacitance (C_L)	50		pF
Output Circuit Protection Resistance (R_1)	50		Ω
Input Pulse Voltages	0	V_{CC}	V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		V
Output Transition Timing Ref. Voltages	$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$		V
Input Transition Time[2] (t_τ) between V_{IL} and V_{IH}	5		ns

Note: 1. All voltages are referenced to V_{SS}.
2. The Input Transition Time used in AC measurements is 5ns. For other input transition times, see Table 8.

Figure 5. AC Measurement I/O Waveform

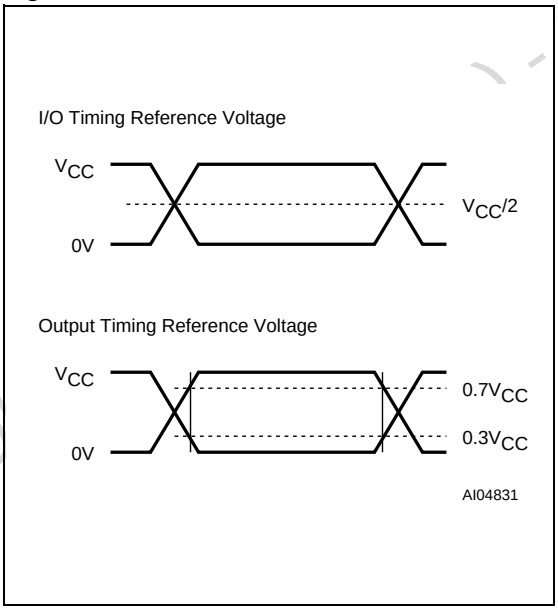


Figure 6. AC Measurement Load Circuit

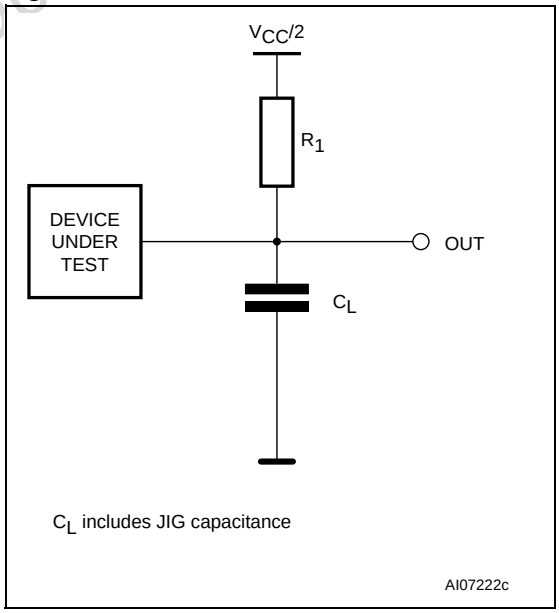


Table 9. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		8	pF

Table 10. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{CC1}	V_{CC} Active Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$ and E2 = V_{IH}, I_{OUT} = 0mA	t_{RC} / t_{WC} = minimum		30	mA
I_{CC2}			t_{RC} / t_{WC} = 1 µs		3	mA
I_{CC3}	V_{CC} Page Read Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{E1} = V_{IL}$ and E2 = V_{IH}, I_{OUT} = 0mA, t_{PRC} = min.			10	mA
I_{CCPD}	V_{CC} Power Down Current	V_{CC} = 3.3V, $V_{IN} = V_{IH}$ or V_{IL}, E2 ≤ 0.2V	Deep Power-Down		10	µA
I_{CCP4}			4 Mb PAR		40	µA
I_{CCP8}			8 Mb PAR		50	µA
I_{CCP16}			16 Mb PAR		65	µA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		–1	1	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		–1	1	µA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 3.3V, $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$, $\overline{E1} = E2 \ge V_{CC} - 0.2V$			100	µA
V_{IH} (1)	Input High Voltage			0.8V_{CC}	V_{CC} + 0.2	V
V_{IL} (2)	Input Low Voltage			–0.3	0.2V_{CC}	V
V_{OH}	Output High Voltage	V_{CC} = 2.7V, I_{OH} = –0.5mA		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	V

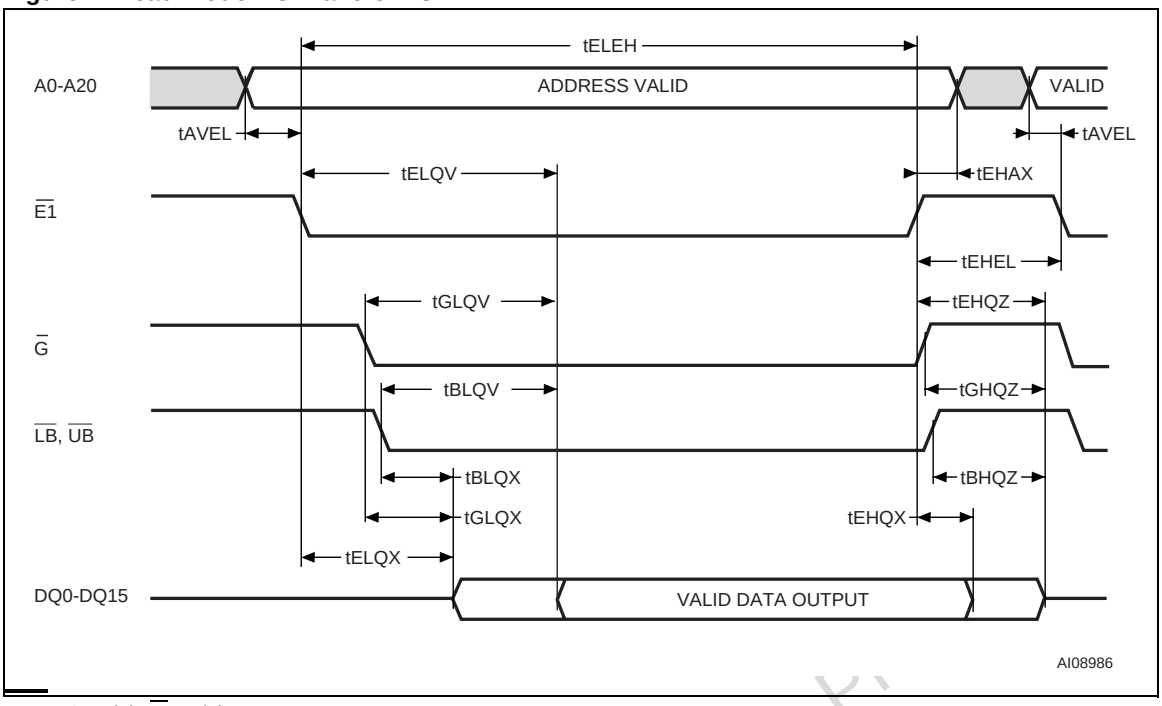
Note: 1. Maximum DC voltage on input and I/O pins is V_{CC} + 0.2V.
During voltage transitions, input may positive overshoot to V_{CC} + 1.0V for a period of up to 5ns.
2. Minimum DC voltage on input or I/O pins is –0.3V.
During voltage transitions, input may positive overshoot to V_{SS} + 1.0V for a period of up to 5ns.

Table 11. Read Mode AC Characteristics

Symbol	Alt.	Parameter	M69AW048B		Unit
			Min	Max	
t_{AVAX} (1,2)	t_{RC}	Address Valid Time	70	1000	ns
t_{AVAX2} (1,6,7)	t_{PRC}	Page Read Cycle Time	25	1000	ns
t_{AVEH2} (1,6,7)	t_{PRC}	Page Read Cycle Time	25	1000	ns
t_{AVEL}	t_{ASC}	Address Valid to Chip Enable Low	–5		ns
t_{AVGL}	t_{ASO}	Address Valid to Output Enable Low	10		ns
t_{AVQV} (3,5)	t_{AA}	Address Valid to Output Valid		70	ns
t_{AVQV2} (3,6)	t_{PAA}	Page Address Access Time		18	ns
t_{AXAV} (5,8)	t_{AX}	Address Invalid Time		10	ns
t_{AXAV2} (6,8)	t_{AXP}	Page Address Invalid Time		10	ns
t_{AXQX} (3)	t_{OH}	Data hold from address change	3		ns
t_{BHQX} (3)	t_{OH}	Upper/Lower Byte Enable High to Output Transition	3		ns
t_{BHQZ} (4)	t_{BHZ}	Upper/Lower Byte Enable High to Output Hi-Z		20	ns
t_{BLQV} (3)	t_{BA}	Upper/Lower Byte Enable Low to Output Valid		30	ns
t_{BLQX} (4)	t_{BLZ}	Upper/Lower Byte Enable Low to Output Transition	0		ns
t_{EHAX} (9)	t_{CHAH}	Chip Enable High to Address Invalid	–5		ns
t_{EHEL}	t_{CP}	Chip Enable High to Chip Enable Low	15		ns
t_{EHQX} (3)	t_{OH}	Chip Enable High to Output Transition	3		ns
t_{EHQZ} (4)	t_{CHZ}	Chip Enable High to Output Hi-Z		20	ns
t_{ELAX} (1,2)	t_{RC}	Read Cycle Time	70	1000	ns
t_{ELEH} (1,2)	t_{RC}	Read Cycle Time	70	1000	ns
t_{ELQV} (3)	t_{CE}	Chip Enable Low to Output Valid		70	ns
t_{ELQX} (4)	t_{CLZ}	Chip Enable Low to Output Transition	3		ns
t_{GHAX}	t_{OHAH}	Output Enable High to Address Invalid	–5		ns
t_{GHQX} (3)	t_{OH}	Output Data Hold Time	3		ns
t_{GHQZ} (4)	t_{OHZ}	Output Enable High to Output Hi-Z		20	ns
t_{GLQV} (3)	t_{OE}	Output Enable Low to Output Valid		40	ns
t_{GLQX} (4)	t_{OLZ}	Output Enable Low to Output Transition	0		ns

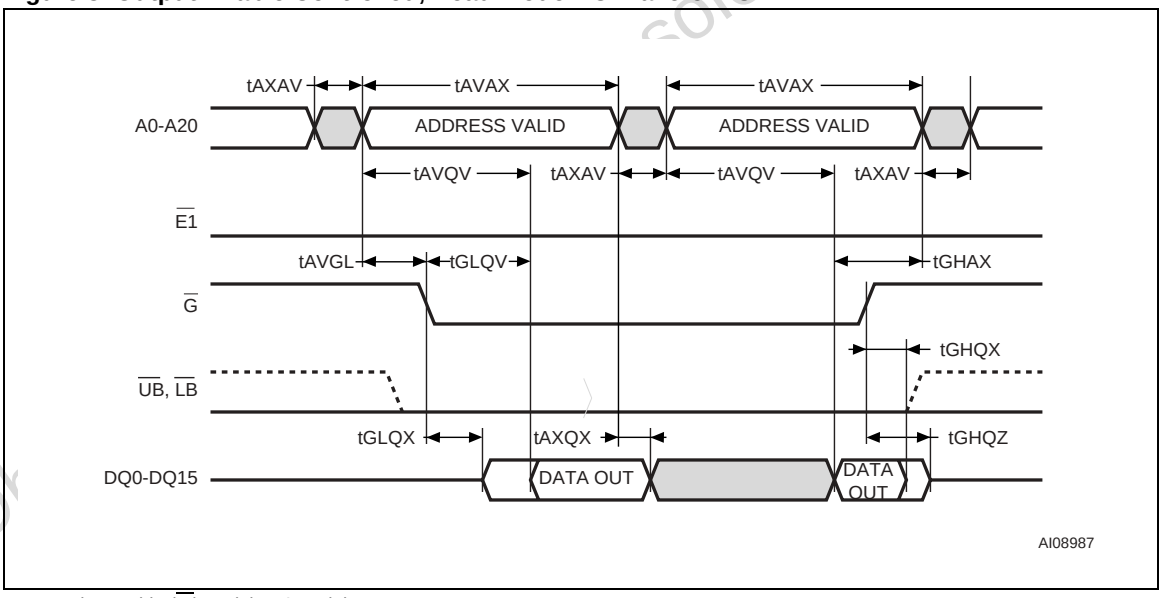
Note: 1. Maximum value is applicable if $\overline{E1}$ is kept Low without change of address input of A3 to A20. If needed by system operation, please contact your local ST representative for relaxation of the 1000ns limitation.
2. Address should not be changed within minimum Read Cycle Time.
3. The output load 50pF with 50Ω termination to V_{CC}*0.5 V.
4. The output load 5pF without any other load.
5. Applicable to A3 to A20 when $\overline{E1}$ is kept Low.
6. Applicable only to A0, A1 and A2 when $\overline{E1}$ is kept Low for the page address access.
7. In case Page Read Cycle is continued with keeping $\overline{E1}$ stays Low, $\overline{E1}$ must be brought to High within 4µs. In other words, Page Read Cycle must be closed within 4µs.
8. Applicable when at least two of address inputs among applicable are switched from previous state.
9. Minimum Read Cycle TIme and minimum Page Read Cycle Time must be satisfied.

Figure 7. Read Mode AC Waveforms



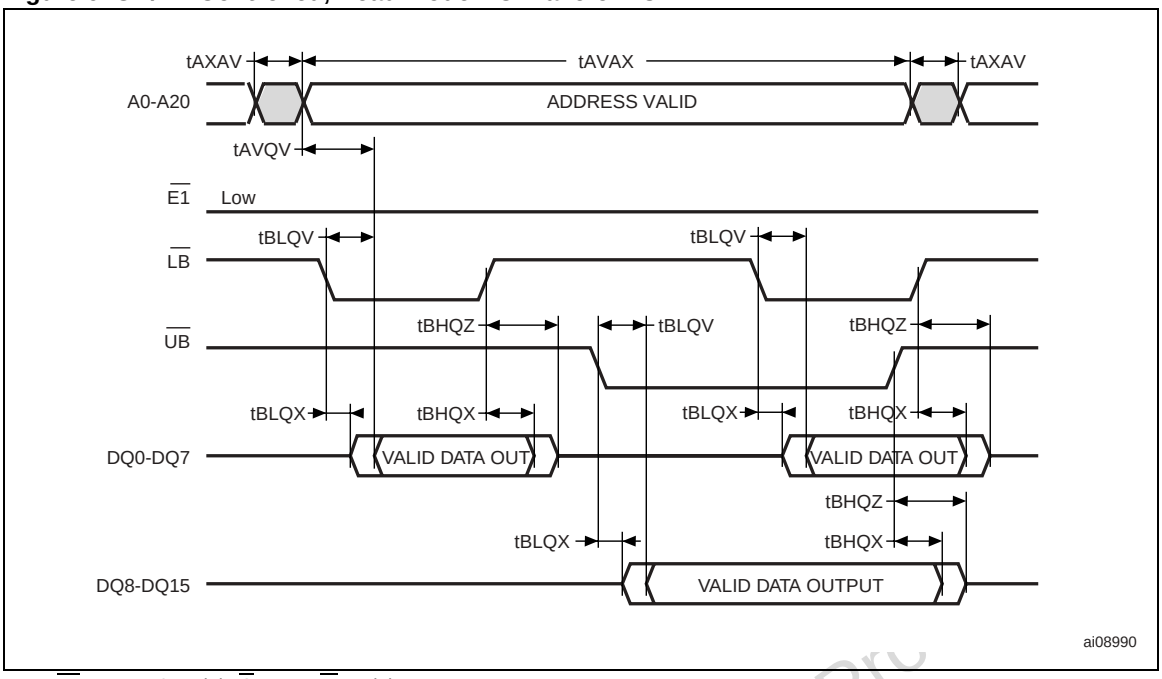
Note: E2 = High, $\overline{W}$ = High.

Figure 8. Output Enable Controlled, Read Mode AC Waveforms



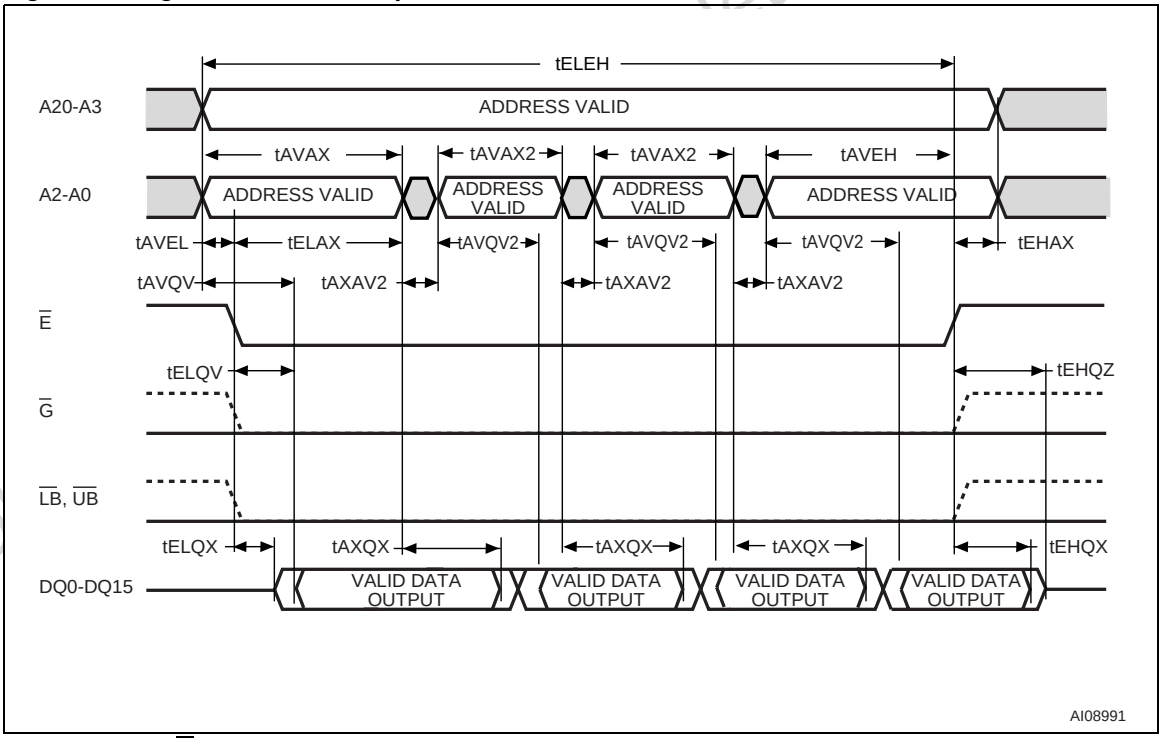
Note: Write Enable ($\overline{W}$) = High, E2 = High.

Figure 9. $\overline{UB}$/$\overline{LB}$ Controlled, Read Mode AC Waveforms



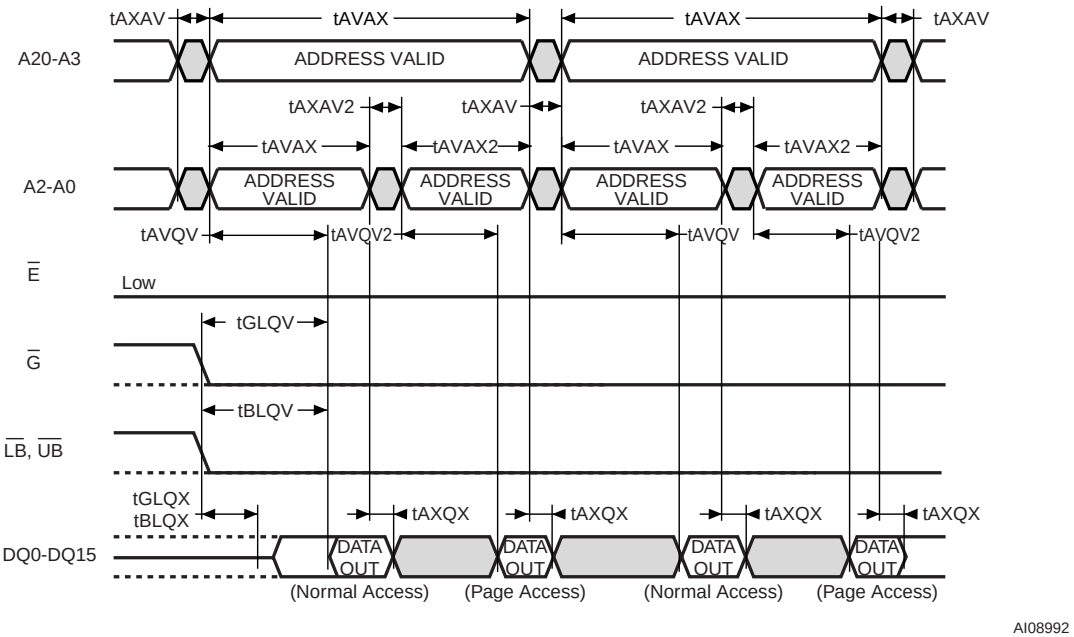
Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High.

Figure 10. Page Address and Chip Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High, E2 = High.

Figure 11. Random and Page Address Controlled, Read Mode AC Waveforms



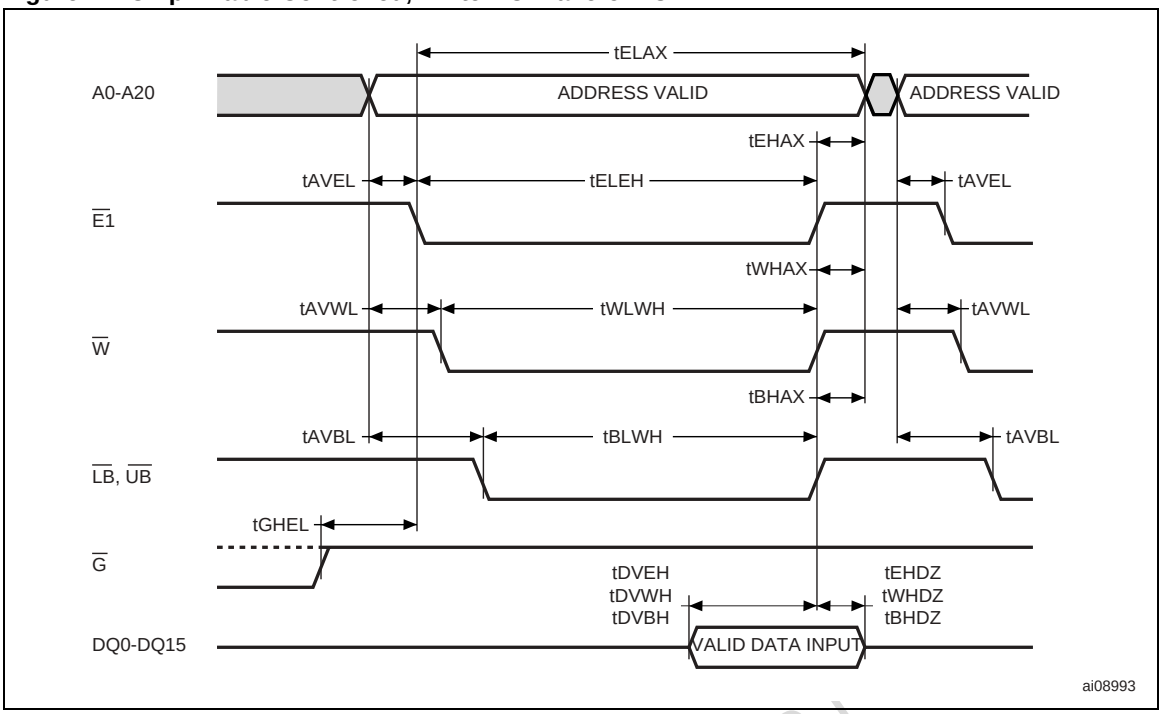
Note: E2 = High.

Table 12. Write Mode AC Characteristics

Symbol	Alt.	Parameter	M69AW048B		Unit
			Min	Max	
t_{AVAX} (1,2)	t_{WC}	Write Cycle Time	70	1000	ns
t_{AVBL} (2)	t_{AS}	Address Valid to $\overline{LB}$, $\overline{UB}$ Low	0		ns
t_{AVEL} (2)	t_{AS}	Address Valid to Chip Enable Low	0		ns
t_{AVWL} (2)	t_{AS}	Address Valid to Write Enable Low	0		ns
t_{AXAV} (5)	t_{AXW}	Address Invalid Time for Write		10	ns
t_{BHAX} (4)	t_{BR}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	15	1000	ns
t_{BHDZ}	t_{DH}	$\overline{LB}$, $\overline{UB}$ High to Input High-Z	0		ns
t_{BLBH} (3)	t_{BW}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	45		ns
t_{BLBH2}	t_{BWO}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High for Page Access	20		ns
t_{BLWH} (3)	t_{BW}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	45		ns
t_{DVBH}	t_{DS}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	20		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	20		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	20		ns
t_{EHAX} (4)	t_{WRC}	Chip Enable High to Address Transition	15		ns
t_{EHDZ}	t_{DH}	Chip Enable High to Input High-Z	0		ns
t_{EHEL}	t_{CP}	Chip Enable High to Chip Enable Low	15		ns
t_{ELAX} (1,2)	t_{WC}	Write Cycle Time	70	1000	ns
t_{ELEH} (3)	t_{CW}	Chip Enable Low to Chip Enable High	45		ns
t_{GHAV} (7)	t_{OES}	Output Enable High to Address Valid	0		ns
t_{GHEL} (6)	t_{OHCL}	Output Enable High to Chip Enable Low	–5		ns
t_{GHDZ} (4)	t_{OHZ}	Output Enable High to Output Hi-Z		20	ns
t_{WHAX} (4)	t_{WR}	Write Enable High to Address Transition	15	1000	ns
t_{WHDZ}	t_{DH}	Write Enable High to Input High-Z	0		ns
t_{WLBH} (3)	t_{WP}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	45		ns
t_{WLWH} (3)	t_{WP}	Write Enable Low to Write Enable High	45		ns

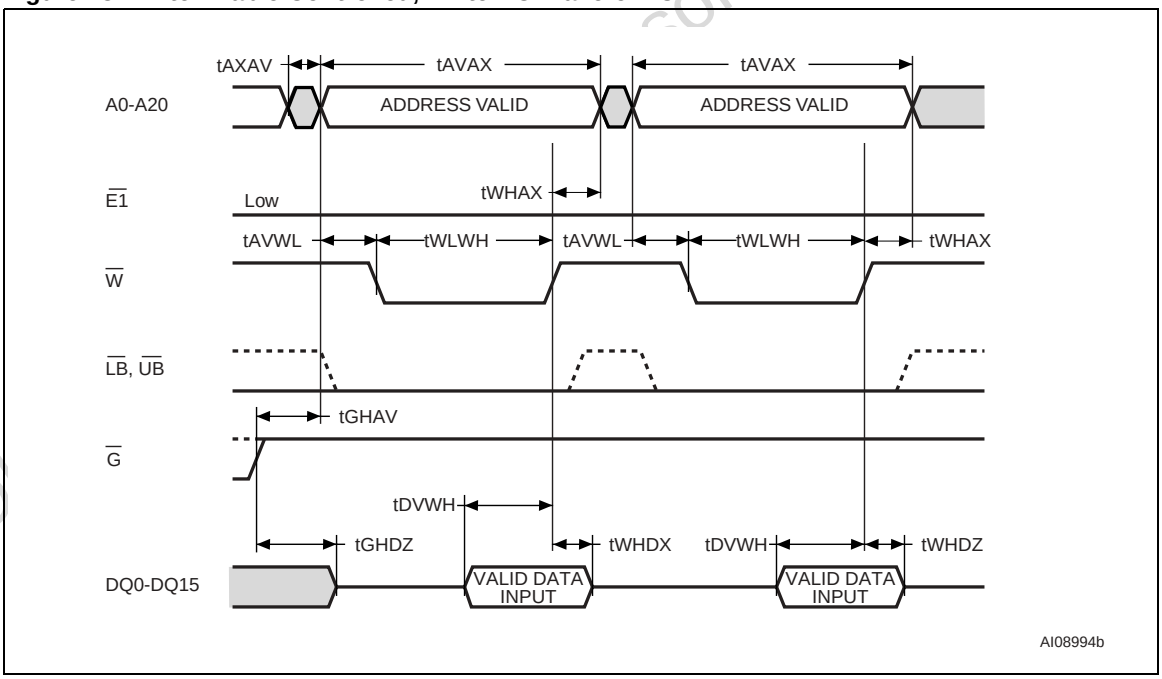
Note: 1. Maximum value is applicable if $\overline{E1}$ is kept Low without any address change. If needed by system operation, please contact your local ST representative for relaxation of the 1000ns limitation.
2. Minimum value must be equal to or greater than the sum of write pulse (t_{ELEH}, t_{WLBH} or t_{BLBH}) and write recovery time (t_{EHAX}, t_{WHAX} or t_{BHAX}).
3. Write pulse is defined from the falling edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs last.
4. Write recovery is defined from Write pulse is defined from the rising edge of $\overline{E1}$, $\overline{W}$, or $\overline{LB}$/$\overline{UB}$, whichever occurs first.
5. Applicable to any address change when $\overline{E1}$ stays Low.
6. If $\overline{G}$ is Low after minimum t_{GHEL}, the read cycle is initiated. In other words, $\overline{G}$ must be brought High within 5ns after $\overline{E1}$ is brought Low. Once the read cycle is initiated, new write pulse should be input after minimum Read Cycle Time is met.
7. If $\overline{G}$ is Low after new address input, the read cycle is initiated. In other words, $\overline{G}$ must be brought High at the same time or before new address valid. Once the read cycle is initiated, new write pulse should be input after minimum Read Cycle Time is met.

Figure 12. Chip Enable Controlled, Write AC Waveforms



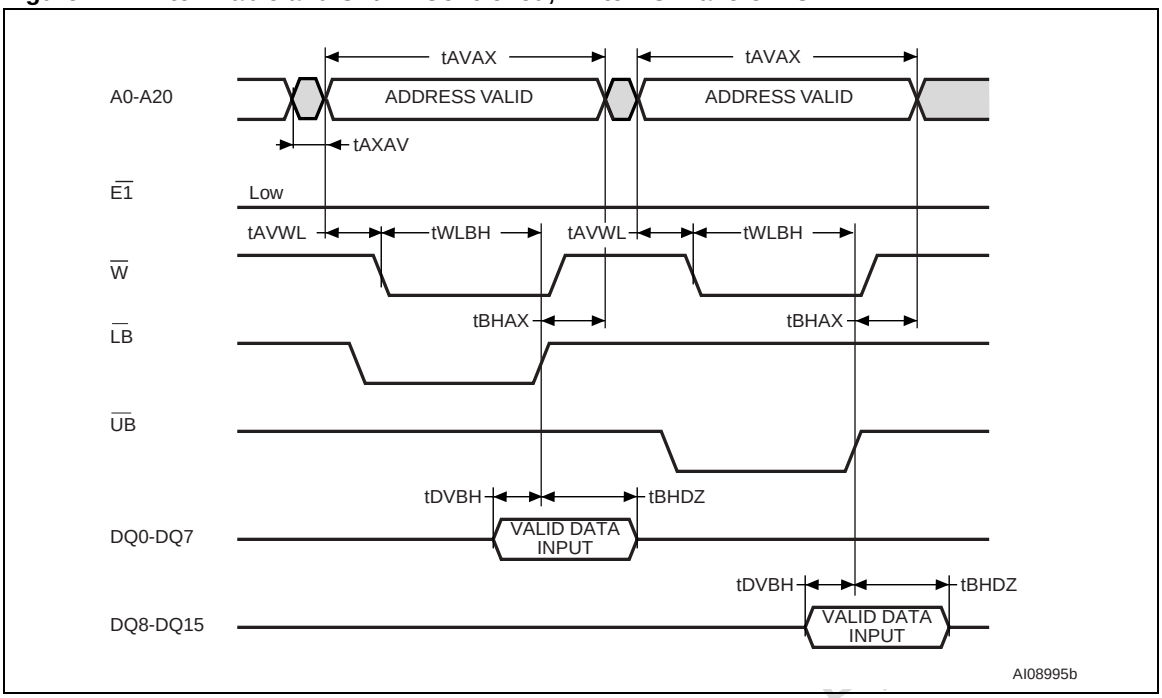
Note: E2 = High.

Figure 13. Write Enable Controlled, Write AC Waveforms



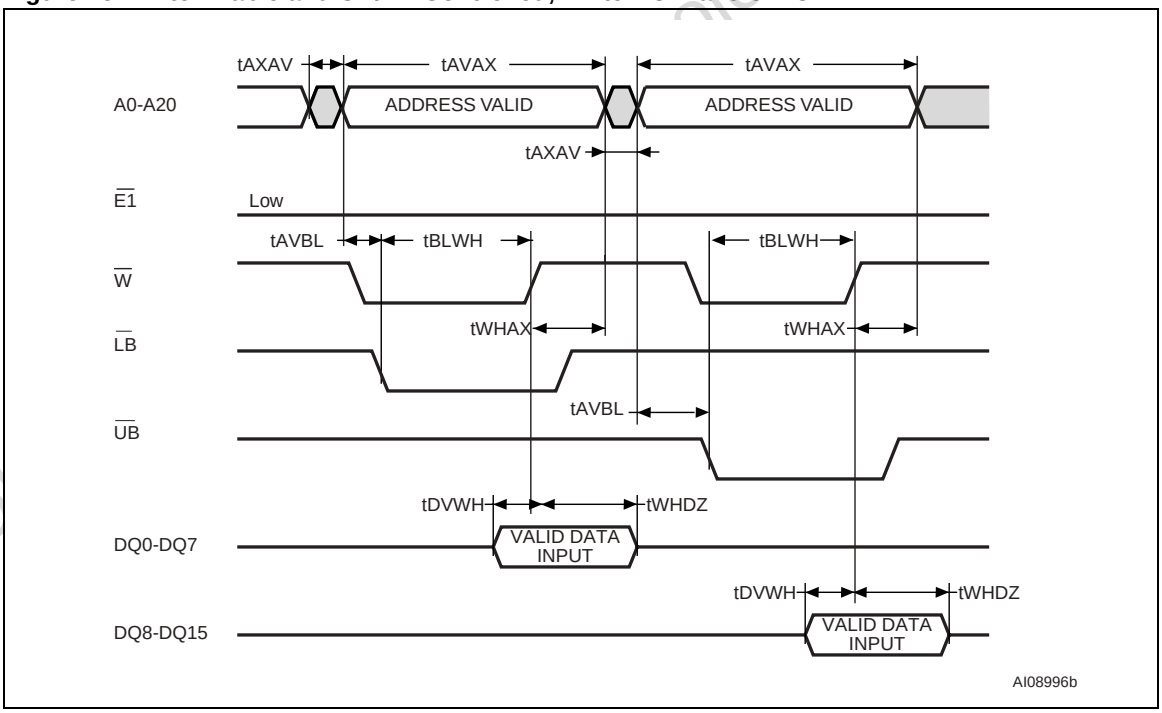
Note: E2 = High.

Figure 14. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 1



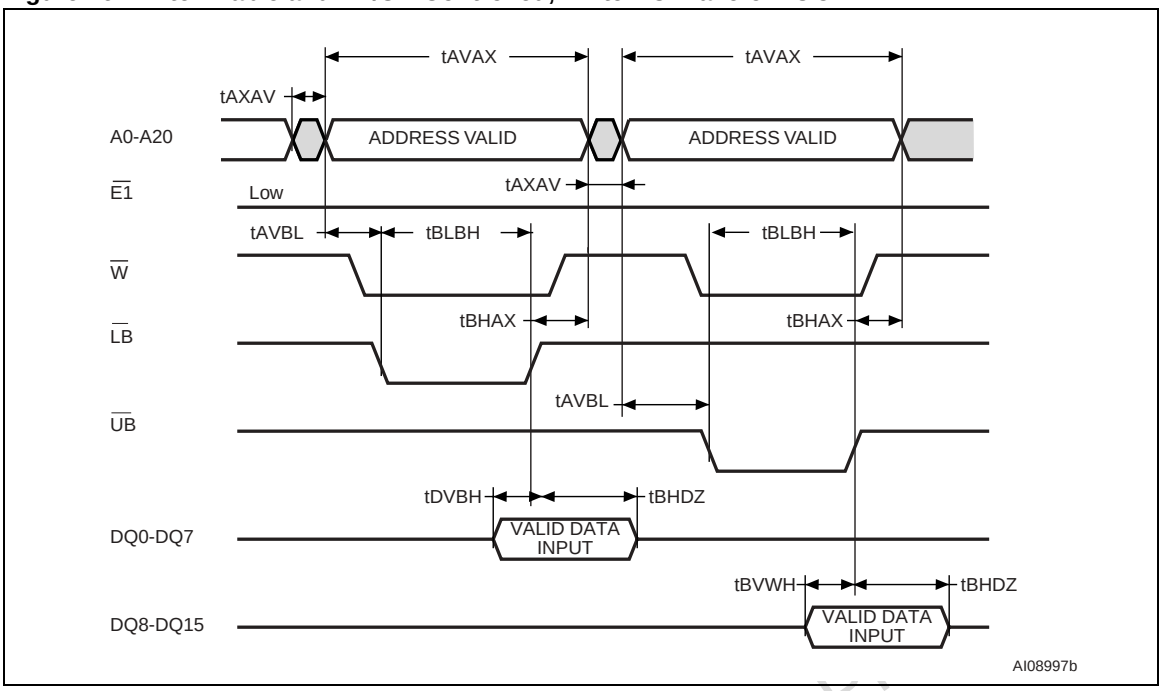
Note: E2 = High.

Figure 15. Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms 2



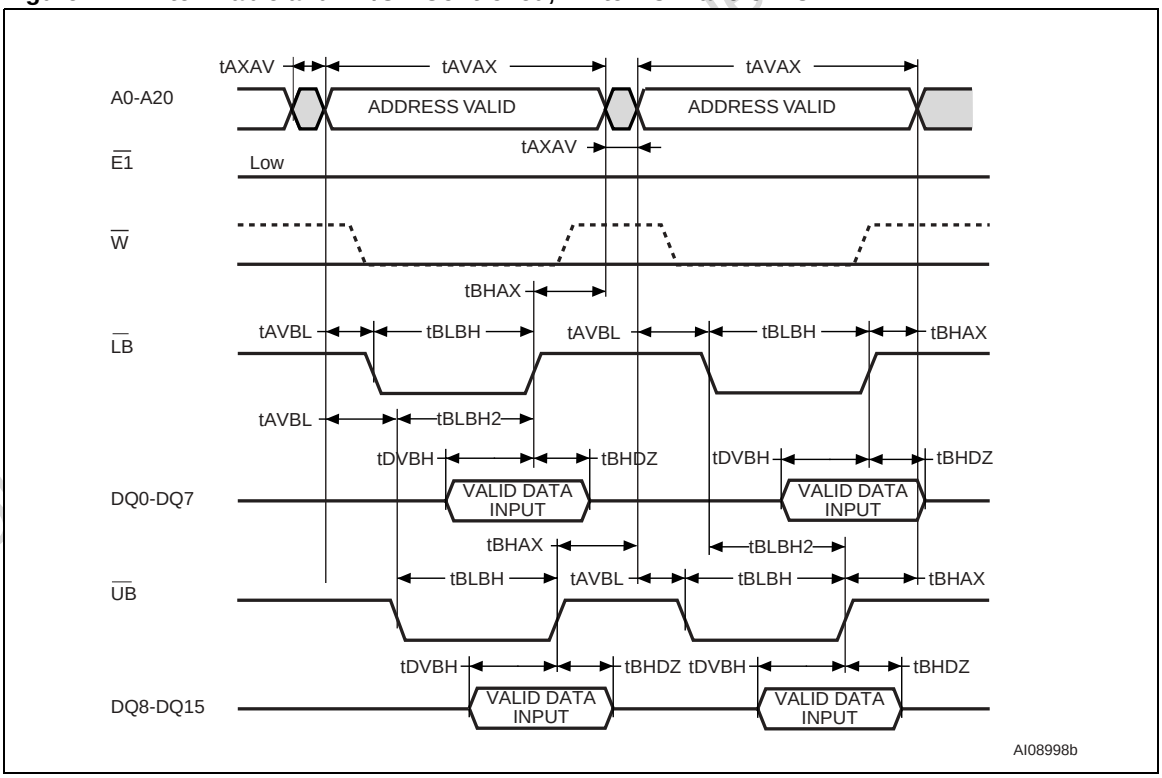
Note: E2 = High.

Figure 16. Write Enable and $\overline{LB}$/$\overline{UB}$ Controlled, Write AC Waveforms 3



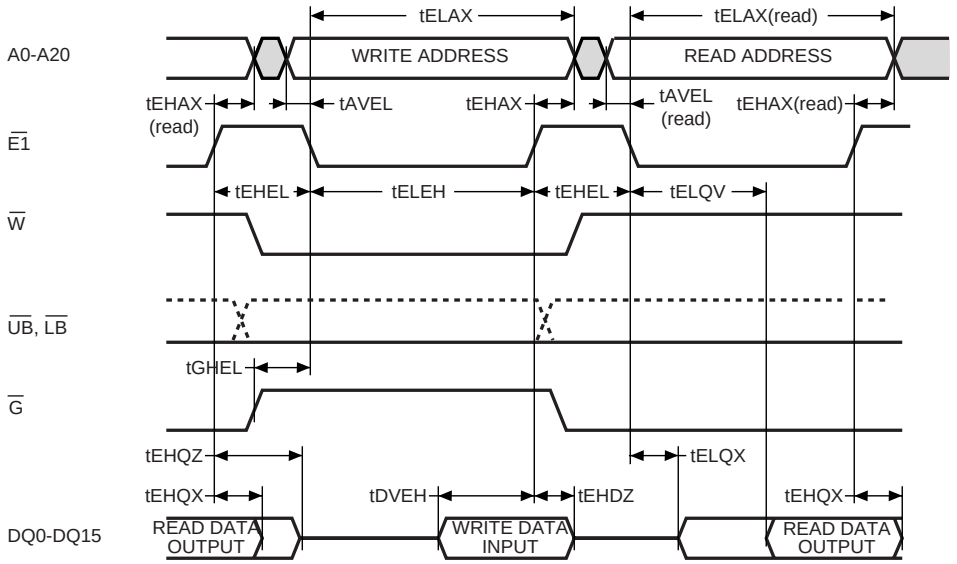
Note: E2 = High.

Figure 17. Write Enable and $\overline{LB}$/$\overline{UB}$ Controlled, Write AC Waveforms 4



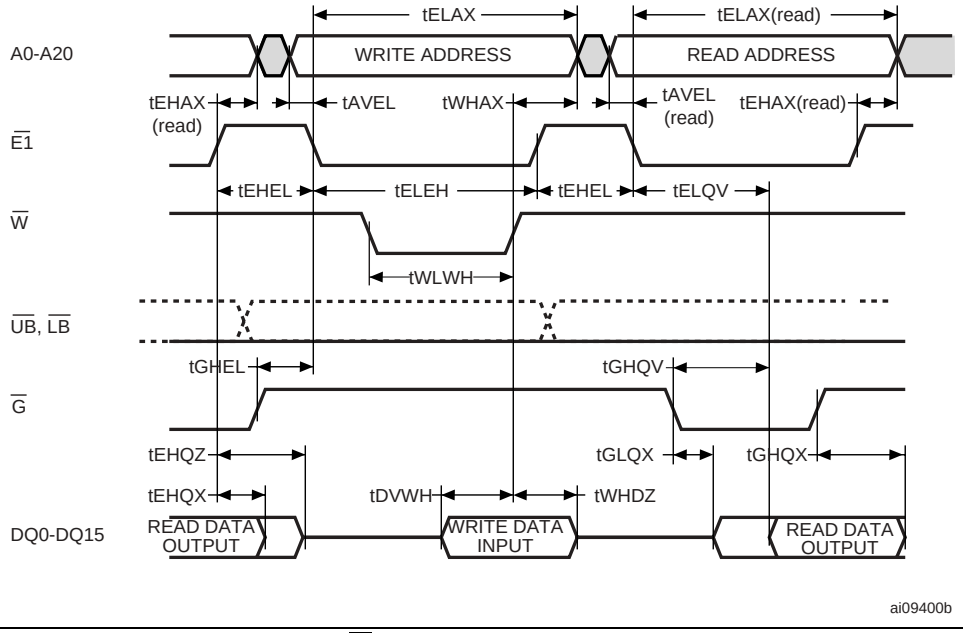
Note: E2 = High.

Figure 18. Chip Enable Controlled, Read Followed by Write Mode AC Waveforms



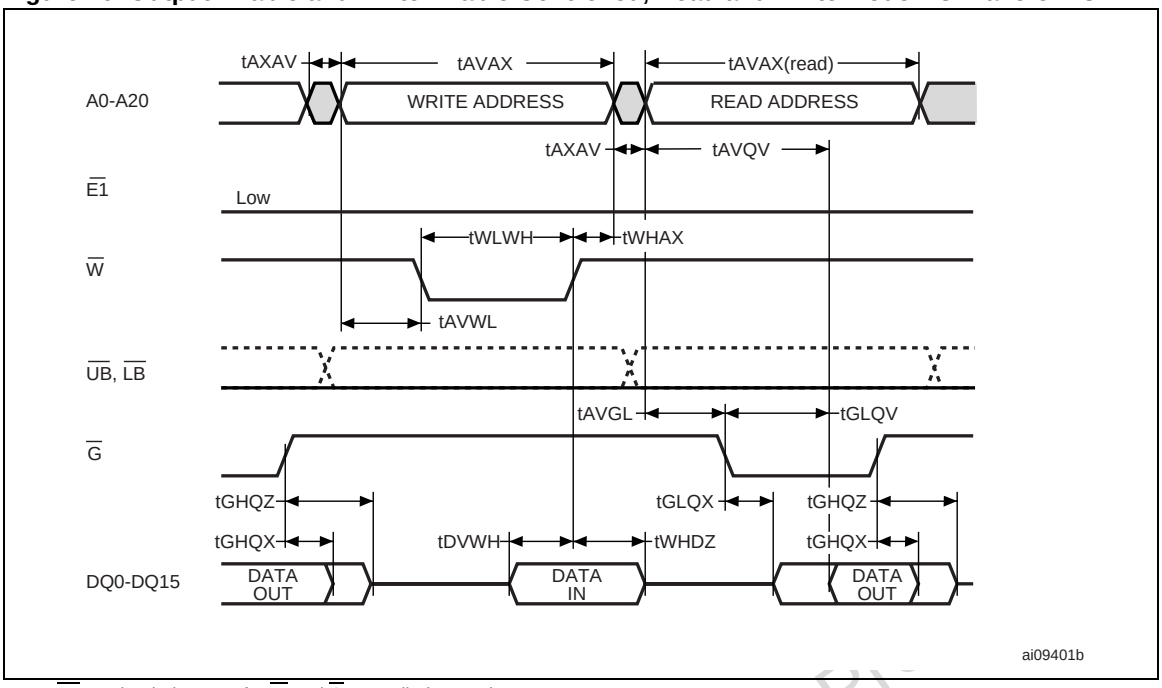
Note: Write address is valid from either $\overline{E1}$ or $\overline{W}$ of last falling edge.

Figure 19. $\overline{E1}$, $\overline{W}$, $\overline{G}$ Controlled, Read and Write Mode AC Waveforms



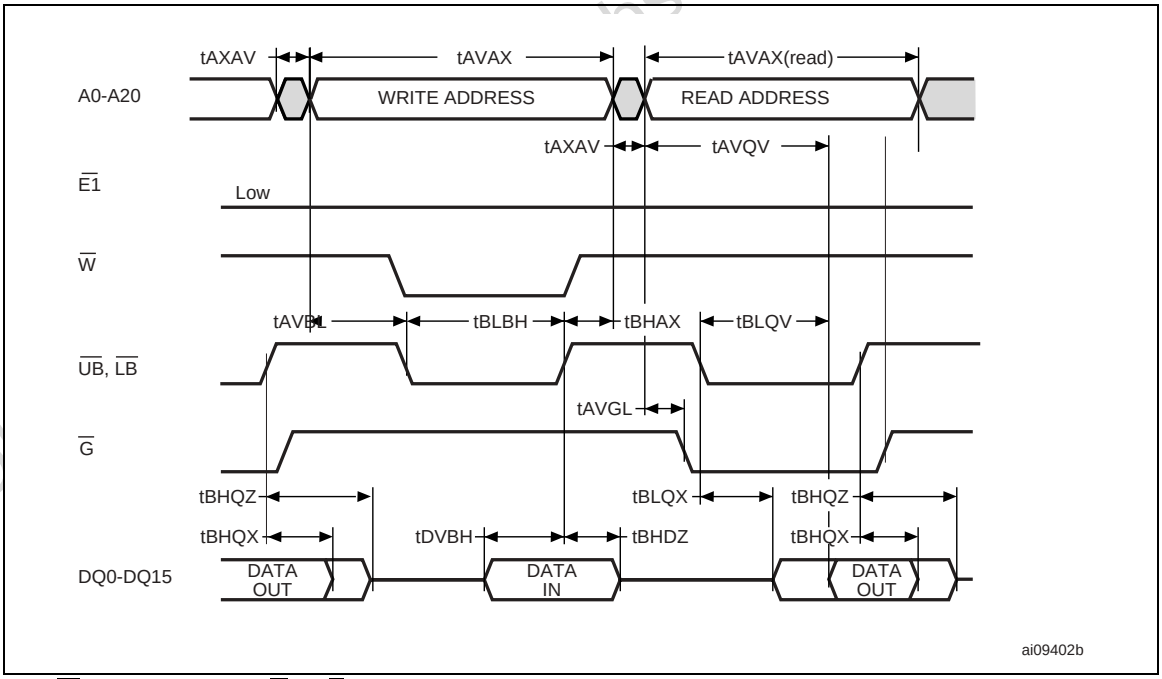
Note: $\overline{G}$ can be Low fixed in write operation under $\overline{E1}$ control read-write-read operation.

Figure 20. Output Enable and Write Enable Controlled, Read and Write Mode AC Waveforms



Note: $\overline{E1}$ can be tied to Low for $\overline{W}$ and $\overline{G}$ controlled operation.
When $\overline{E1}$ is tied to Low, output is exclusively controlled by $\overline{G}$.

Figure 21. Output Enable, Write Enable and $\overline{UB}$/$\overline{LB}$ Controlled, Read and Write Mode AC Waveforms



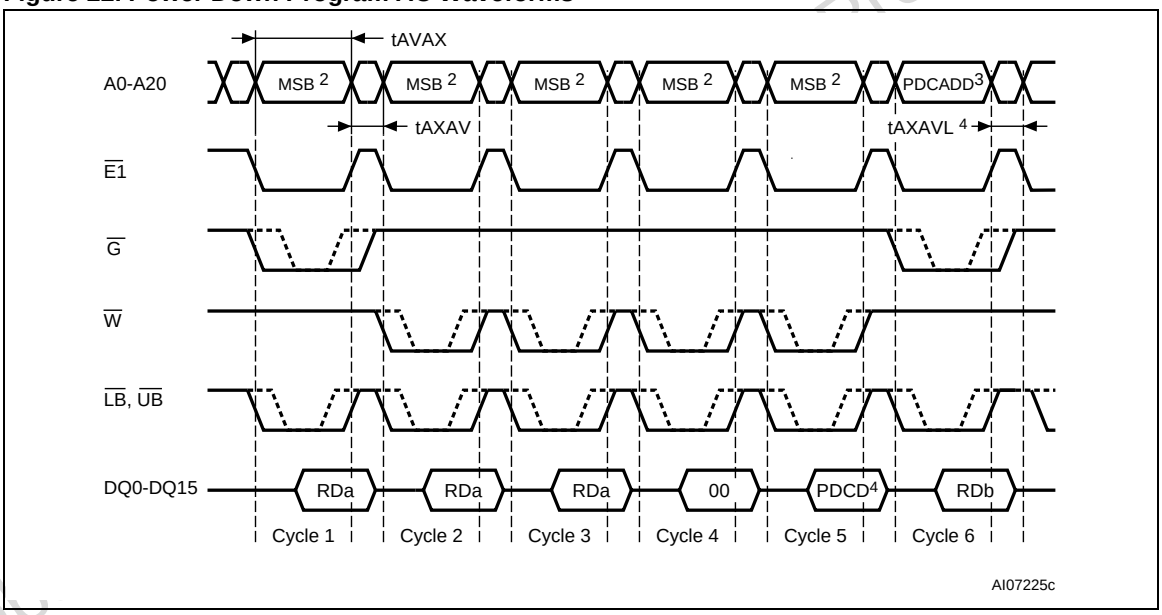
Note: $\overline{E1}$ can be tied to Low for $\overline{W}$ and $\overline{G}$ controlled operation.
When $\overline{E1}$ is tied to Low, output is exclusively controlled by $\overline{G}$.

Table 13. Standby/Power-Down Mode AC Characteristics

Symbol	Alt.	Parameter	M69AW048B		Unit
			Min	Max	
t_{CLEX}	t_{CSP}	E2 Low Setup Time for Power Down Entry	10		ns
t_{EXCH}	t_{C2LP}	E2 Low Hold Time after Power Down Entry	70		ns
t_{EHEV} (1)	t_{CHH}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (Deep Power-Down Mode only)	300		µs
t_{CHEL} (2)	t_{CHHP}	$\overline{E1}$ High Hold Time following E2 High after Power-Down Exit (not in Deep Power-Down Mode)	1		µs
t_{EHCH}	t_{CHS}	$\overline{E1}$ High Setup Time following E2 High after Power-Down Exit	0		µs
t_{EHGL}	t_{CHOX}	$\overline{E1}$ High to $\overline{G}$ Invalid Time for Standby Entry	10		ns
t_{EHWL} (3)	t_{CHWX}	$\overline{E1}$ High to $\overline{W}$ Invalid Time for Standby Entry	10		ns
t_τ (4)	t_τ	Input Transition Time	1	25	ns

Note: 1. Applicable also to Power-up.
2. Applicable when 4Mb, 8Mb and 16Mb PAR mode is programmed
3. Some data might be written into any address location if t_{EHWL} (min) is not satisfied.
4. The Input Transition Time (t_τ) at AC testing is 5ns as shown below. If actual t_τ is longer than 5ns, it may violate AC specification of some timing parameters.

Figure 22. Power Down Program AC Waveforms



Note: 1. E2 = High.
2. All address inputs must be High from Cycle 1 to Cycle 5.
3. PDCADD stands for Power-Down Configuration Address. It must be compliant with the format specified in Table 6 otherwise the data programmed during the Power-Down Program sequence may be incorrect.
4. PDCDAT stands for Power-Down Configuration Data. It must be compliant with the format specified in Table 5 otherwise the data programmed during the Power-Down Program sequence may be incorrect.
5. t_{EHEL} after the end of Cycle 6, the Power Down Program is completed and the device returns to normal operation.

Figure 23. Power-Down Mode AC Waveforms

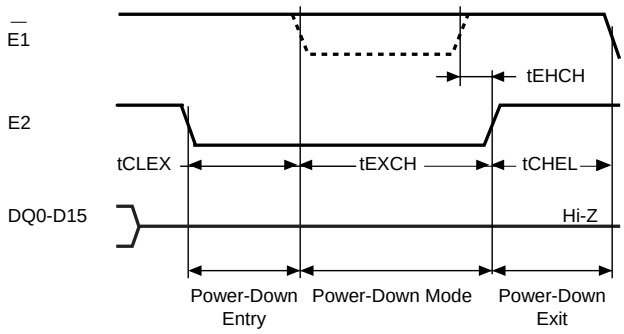


Figure 24. Power-Up Mode AC Waveforms

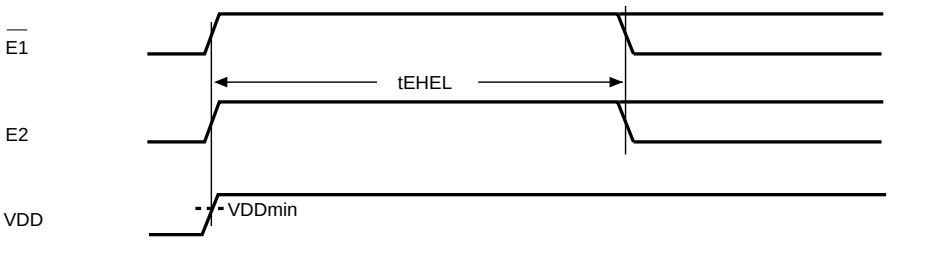
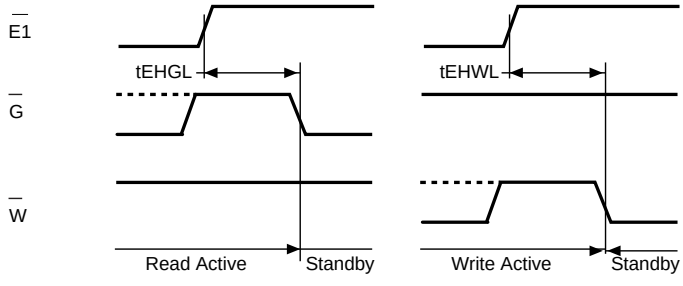


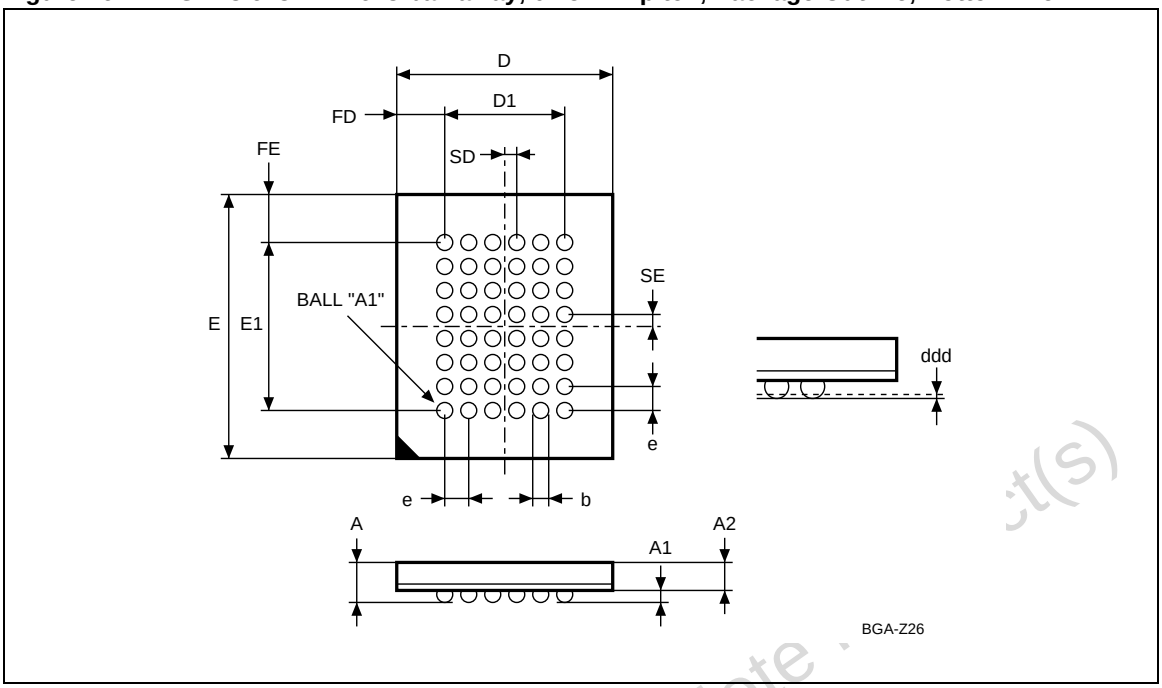
Figure 25. Standby Mode Entry AC Waveforms, After Read



Note: E2 = High.

PACKAGE MECHANICAL

Figure 26. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Package Outline, Bottom View



Note: Drawing is not to scale.

Table 14. TFBGA48 6x8mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 15. Ordering Information Scheme

Example: M69AW048 B L 70 ZB 8

Device Type
M69 = PSRAM

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.3V

Array Organization
048 = 32 Mbit (2M x16)

Option 1
B = 2 Chip Enable

Option 2
L = Low Leakage

Speed Class
70= 70 ns

Package
ZB = TFBGA48, 0.75mm pitch

Operative Temperature
8 = –30 to 85 °C

The notation used for the device number is as shown in Table 15.. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

REVISION HISTORY

Table 16. Document Revision History

Date	Version	Revision Details
07-Oct-2002	-01	First Issue
10-Mar-2003	2.0	Document completely revised
9-Mar-2004	3.0	Data Key and Address Key renamed Power-Down Configuration data and Power-Down Configuration Address respectively. Sleep mode renamed Deep Power-Down mode. I_{CCS} removed and I_{PD} renamed I_{CCPD} in Table 10., DC Characteristics. Partial mode renamed Partial Array Refresh. Table 12. Write Mode AC Characteristics: t_{GHDZ} added and Note 2 updated. t_{GHQZ} changed to t_{GHDZ} in Figure 13.Write Enable Controlled, Write AC Waveforms. AC Waveforms converted to ST standard.
21-Sep-2004	4.0	t_{ELQZ}, t_{GLQZ}, t_{BLQZ} changed into t_{ELQX}, t_{GLQX}, t_{BLQX} in Table 11., Read Mode AC Characteristics.
15-Nov-2004	5.0	V_{OH} value updated in Table 10., DC Characteristics.