



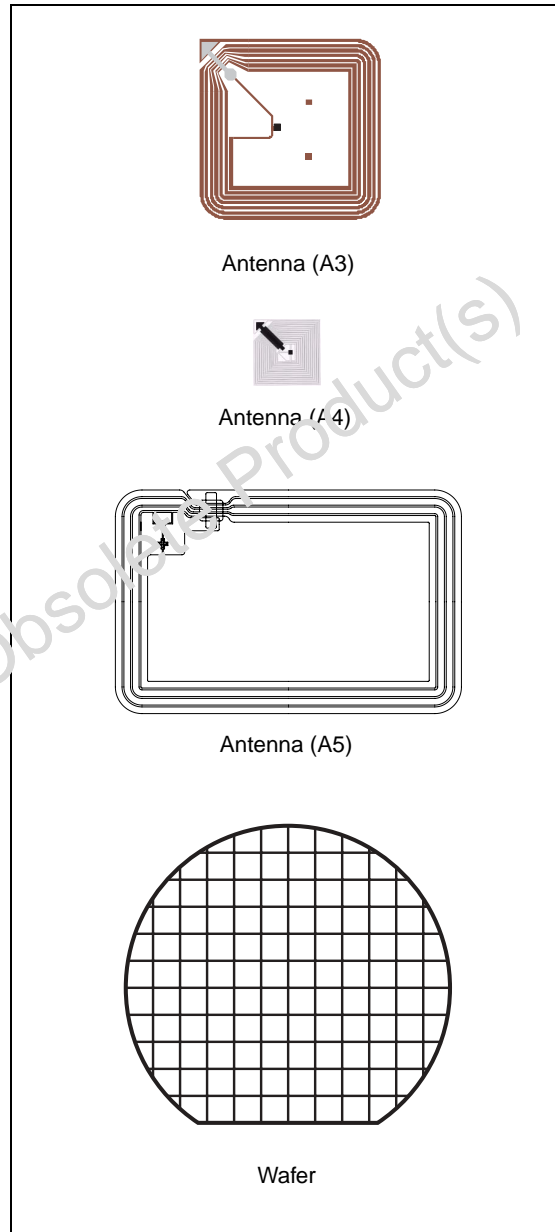
SR176

13.56 MHz, 176-bit short range contactless user EEPROM  
with 64-bit Unique ID

Not For New Design

Features

- ISO 14443-2 Type B air interface compliant
- ISO 14443-3 Type B frame format compliant
- 13.56 MHz carrier frequency
- 847.5 kHz subcarrier frequency
- 106 Kbit/s data transfer
- Data transfer
  - ASK modulation from Reader to Tag
  - BPSK coding from Tag to Reader
- 176-bit EEPROM with Write Protect feature
- 64-bit Unique Identifier
- READ BLOCK and WRITE BLOCK (16 bits)
- Internal tuning capacitor
- Self-timed programming cycle
- 5 ms programming time (typical)
- More than 100 000 Erase/Write cycles
- More than 40 year data retention
- Packages
  - ECOPACK® (RoHS compliant)



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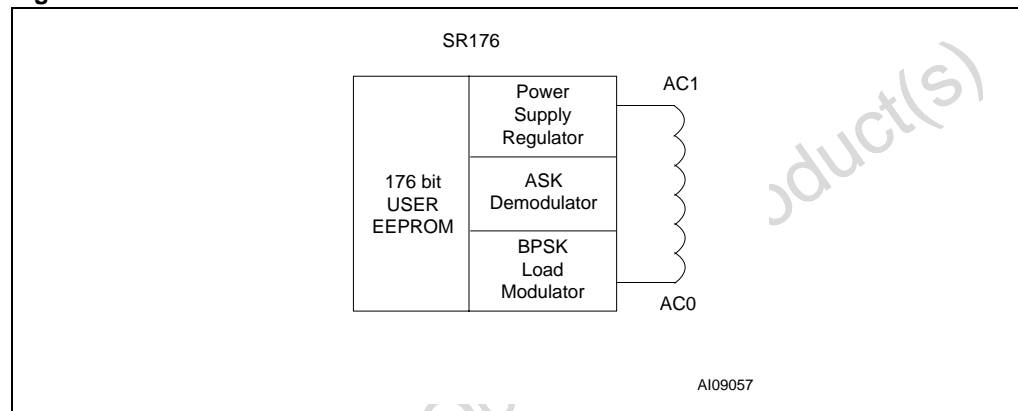
# 1 Description

The SR176 is a contactless memory, powered by an externally transmitted radio wave. It contains 176 bits of user EEPROM, fabricated with STMicroelectronics CMOS technology. The memory is organized as 16 blocks of 16 bits, of which 11 blocks are user accessible.

The SR176 is accessed via the 13.56 MHz carrier. Incoming data are demodulated and decoded from the received Amplitude Shift Keying modulation signal (ASK). The modulation index of this signal is 10%. Outgoing data are generated by load variation using Bit Phase Shift Keying (BPSK) of a 847.5 kHz subcarrier. The Data transfer rate between the SR176 and the reader is 106 Kbit/s in both reception and emission modes.

The SR176 follows the ISO 14443-2 Type B recommendation for radio frequency power and signal interfacing.

**Figure 1. Pad connections**



The SR176 is principally designed for short range applications, such as object identification, that need a low cost and non-reusable tag. The SR176 does not include any anticollision mechanism. It provides an “addressed” selection mechanism to cope with cases where more than one tag is present within the range of the reader.

**Table 1. Signal names**

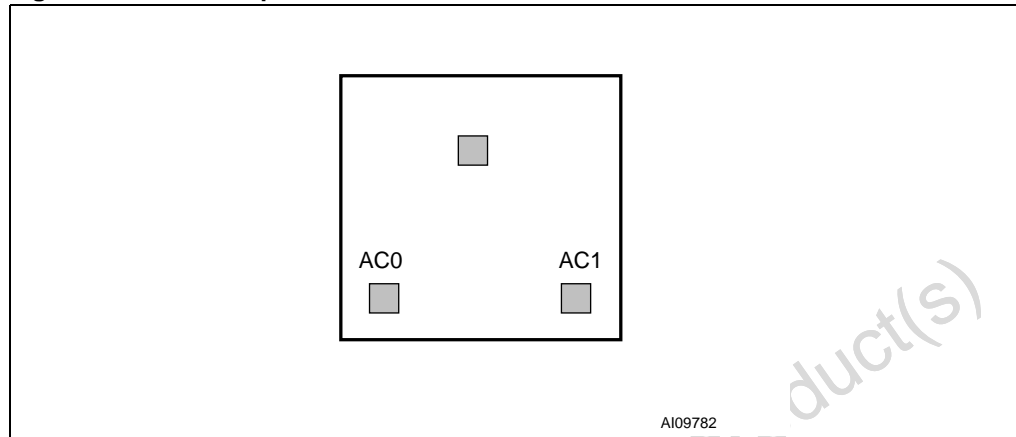
AC1	Antenna coil
AC0	Antenna coil

The SR176 contactless EEPROM offers read and write random access in block mode. One block is composed by 16 bits. The device has an instruction set containing seven commands:

- READ\_BLOCK
- WRITE\_BLOCK
- INITIATE
- SELECT
- COMPLETION
- PROTECT\_BLOCK
- GET\_PROTECTION.

The memory array of the SR176 is divided into two main areas: the unique identifier (UID) and the User EEPROM. The UID is a 64-bit unique identifier, written by ST during product manufacture. The User EEPROM is divided into areas which can be write-protected so that they behave as ROM. The write protection is activated using an OTP lock bits register. It is possible to program the SR176 4-bit chip\_ID used by the SELECT command. Its default value is fixed at the value 0 (0000<sub>b</sub>) by ST. When correctly set, up to sixteen SR176 devices can be selected individually.

**Figure 2. Die floor plan**



## 2 Signal description

### 2.0.1 AC1, AC0

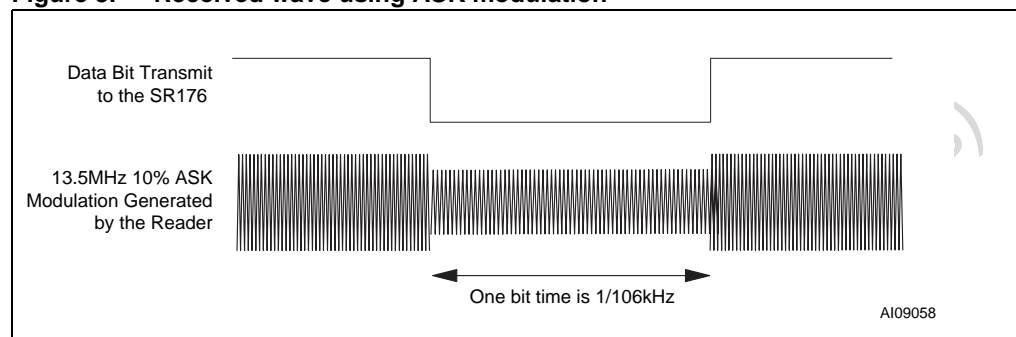
AC1 and AC0 pads must be directly bonded to the antenna.

### 3 Data transfer

#### 3.1 Input data transfer from the Reader to the SR176 (request frame)

The reader that accesses the SR176 must generate a 13.56 MHz sinusoidal carrier wave on its antenna, with enough energy to “tele-power” the SR176 device. The energy received on the SR176 antenna is transformed to a power supply voltage by a regulator, and to data bits through the ASK demodulator. To decode correctly the information sent to the SR176, the reader must use a 10% amplitude modulation of the 13.56 MHz wave, as represented (though not to scale) in *Figure 3*. The data transfer rate is 106 Kbit/second.

**Figure 3. Received wave using ASK modulation**



#### 3.2 Character transmission format for request frame

Data Bytes are transmitted and received by the SR176 as 10-bit characters, as shown in *Figure 4*, with the least significant bit ( $b_0$ ) transmitted first. These characters, with the addition of the Start Of Frame (SOF) and the End Of Frame (EOF), are grouped to form a Command Frame as shown in *Figure 10*. The frame includes an SOF, instructions, addresses, data, a CRC and an EOF as defined by ISO 14443-3 Type B. If an error is detected during the data transfer, no error frame is generated by the SR176, and the instruction is not executed.

Each bit duration is referred to as an ETU (Elementary Time Unit). One ETU is equal to  $9.44 \mu\text{s}$  ( $1/106 \text{ kHz}$ ).

#### 3.3 Request start of frame

The SOF, as shown in *Figure 5*, consists of:

- one falling edge
- followed by 10 ETUs at logic 0
- followed by one single rising edge
- followed by at least 2 ETUs (but no more than 3 ETUs) at logic 1.

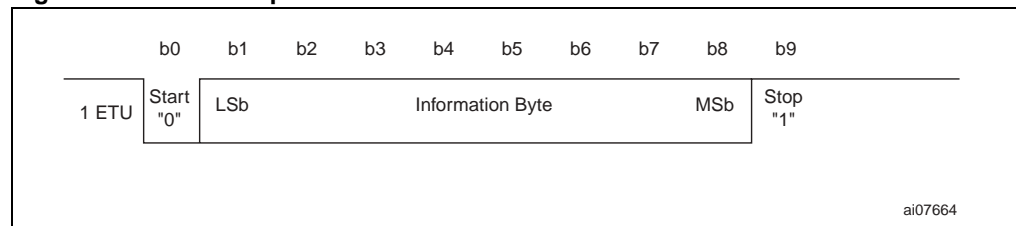


### 3.4 Request end of frame

The EOF, as shown in [Figure 6](#), consists of:

- one falling edge
- followed by 10 ETUs set to logic 0
- followed by one single rising edge

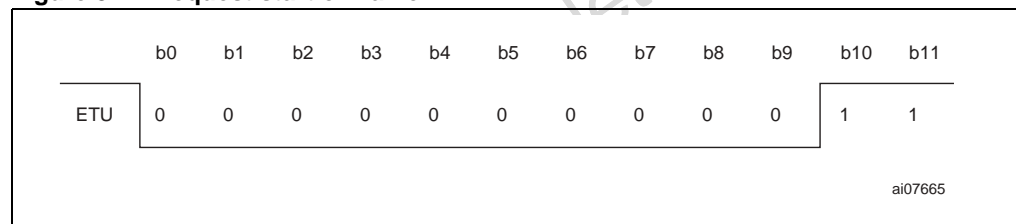
**Figure 4. SR176 request frame character format**



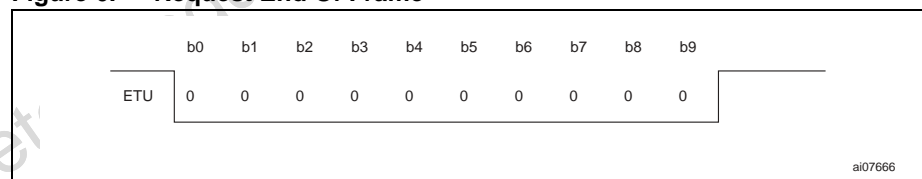
**Table 2. Bit description**

Bit	Description	Value
b <sub>0</sub>	Start bit used to synchronize the transmission	b <sub>0</sub> = 0
b <sub>1</sub> to b <sub>8</sub>	Information Byte (command, address or data or CRC)	Information Byte sent, least significant bit first
b <sub>9</sub>	Stop bit used to indicate the end of a character	b <sub>9</sub> = 1

**Figure 5. Request start of frame**



**Figure 6. Request End Of Frame**



### 3.5 Output data transfer from the SR176 to the Reader (answer frame)

The SR176 uses load modulation to return data to the reader. This modulation is achieved by modifying the SR176 current flow in its antenna. With appropriate detector circuitry, the reader is able to decode the information from the SR176. The data is transmitted using a BPSK coding of a 847.5 kHz subcarrier frequency,  $f_s$ , as specified in ISO 14443-2 Type B, and as shown in [Figure 7](#).

### 3.6 Character transmission format for answer frames

The character format is the same as for the input data transfer (Figure 4). The transmitted frames include an SOF, data, a CRC and an EOF (as shown in Figure 10). Like the input data transfer, in case of error, the reader does not emit any error code to the SR176, but must be able to detect and manage this situation. The data transfer rate is 106 Kbit/second.

### 3.7 Answer start of frame

The SOF, as shown in Figure 8, consists of:

- 10 ETUs at logic 0
- 2 ETUs at logic 1

### 3.8 Answer end of frame

The EOF, as shown in Figure 9, consists of:

- 10 ETUs at logic 0
- 2 ETUs at logic 1

Figure 7. Emitted wave using BPSK subcarrier modulation

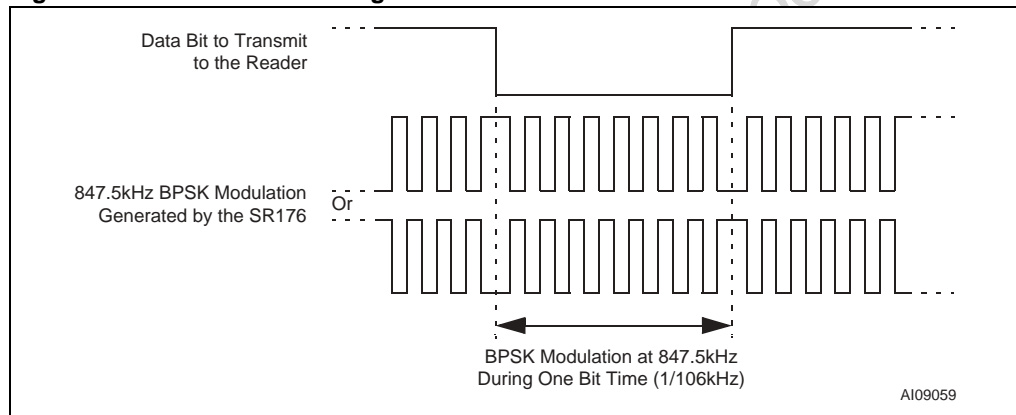


Figure 8. Answer start of frame

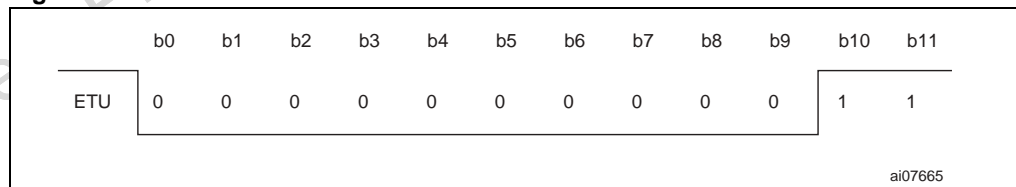
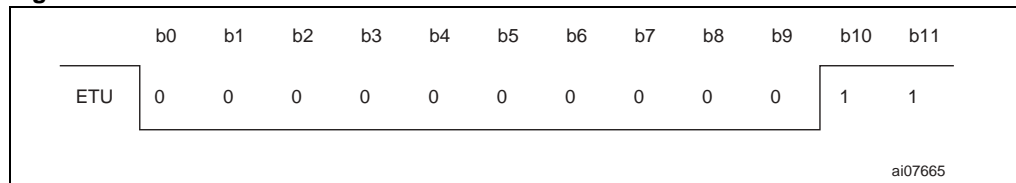


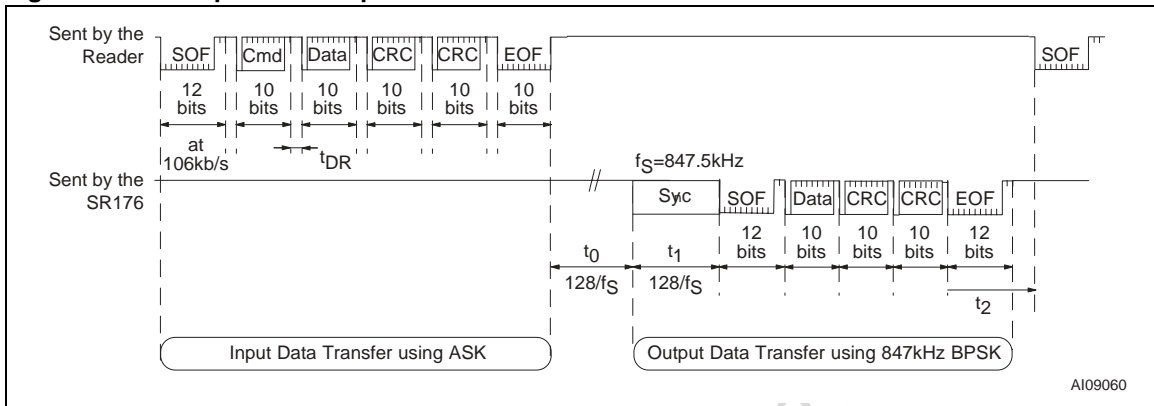
Figure 9. Answer end of frame



### 3.9 Transmission frame

Between the Request and the Answer data transfer, there is a guard time without ASK and BPSK modulation, for a minimum period of  $t_0 = 128/f_S$ . This delay allows the reader to switch from transmission to reception mode, and is applied after each frame. After  $t_0$ , the 13.56 MHz carrier frequency is modulated by the SR176 at 847.5 kHz for a period of  $t_1 = 128/f_S$ , to allow the reader to synchronize. After  $t_1$ , the first phase transition generated by the SR176 represent the start bit ('0') of the Answer SOF. After the falling edge of the Answer EOF, the reader has to wait for the minimum delay,  $t_2$ , before sending a new Request Frame to the SR176.

Figure 10. Example of a complete transmission frame



### 3.10 CRC

The 16-bit CRC that is used by the SR176 follows the ISO 14443 Type B recommendation. For further information, see [Appendix A](#). The initial register content is all ones: FFFFh.

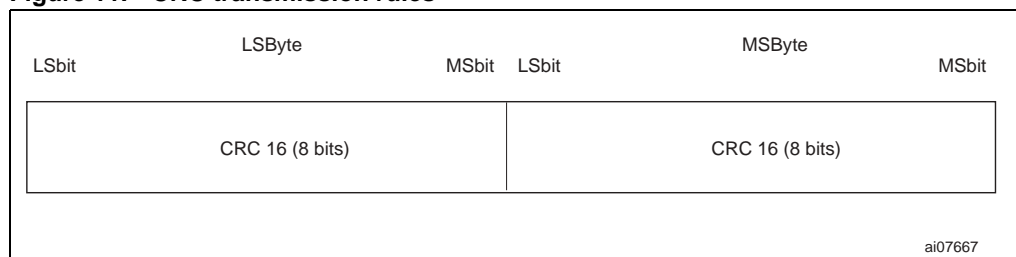
A two-byte CRC is appended to each Request and each Answer, within each frame, before the EOF. The CRC is calculated on all the Bytes after the SOF, up to the CRC field.

On reception of a Request from a reader, the SR176 verifies that the CRC value is valid. If it is invalid, it discards the frame and does not answer the reader.

On reception of an Answer from the SR176, it is recommended that the reader verify that the CRC value is valid. If it is invalid, that choice of actions that are to be performed are the responsibility of the reader designer.

The CRC is transmitted least significant byte first. Each byte is transmitted least significant bit first.

Figure 11. CRC transmission rules



## 4 Memory mapping

The SR176 is organized as 16 blocks of 16 bits, as shown in [Figure 12](#).

The first four blocks, from location 0 to 3, are used to store read-only data. They store the 64-bit UID. This value cannot be modified.

Blocks from locations 4 to 14 offer a 176-bit EEPROM user area in which the application can store its data values. Block 15 contains the OTP LOCK\_REG and the programmed Chip\_ID.

The PROTECT\_BLOCK command is used to lock write access to blocks 4 to 15 in groups of two blocks.

The GET\_PROTECTION command gives the status of the protection of blocks 4 to 15.

**Figure 12. SR176 memory mapping**

Block Address	MSb b15	16-bit block b8 b7	LSb b0	Description
0		UID0		64-bit UID ROM
1		UID1		
2		UID2		
3		UID3		
4		User Area		Lockable EEPROM
5		User Area		
6		User Area		Lockable EEPROM
7		User Area		
8		User Area		Lockable EEPROM
9		User Area		
10		User Area		Lockable EEPROM
11		User Area		
12		User Area		Lockable EEPROM
13		User Area		
14		User Area		Lockable EEPROM
15		OTP LOCK_REG	Reserved Chip_ID	

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### 4.1 Device identification

The SR176 has a 64-bit Unique Identifier (UID) which is written by STMicroelectronics during the manufacturing process. The UID is unique for each tag and cannot be altered. It is stored in a Read Only Memory area (ROM). In the SR176, the UID is stored in the first four blocks of the memory in blocks 0 to 3.

## 4.2 Device selection

After introducing the device in the reader's electromagnetic field, the SR176 has to be activated by a INITIATE command. After this command, the SR176 is in the ACTIVE state and waits for a SELECT command, as shown in [Figure 13](#). The SELECT command specifies a 4-bit Chip\_ID as a parameter. If the Chip-ID of the SR176 matches this parameter, the SR176 goes in the SELECTED state, and memory blocks become available for READ\_BLOCK and WRITE\_BLOCK commands up to the reception of a COMPLETION command. If the Chip\_ID does not match, the SR176 returns to, or stays in, the DESELECTED state. Write access rights are activated by the SELECT command.

After the Power On of the SR176, if the INITIATE command is not send or is not correctly generated, memory blocks will not be activated, and the SR176 will not respond to any command.

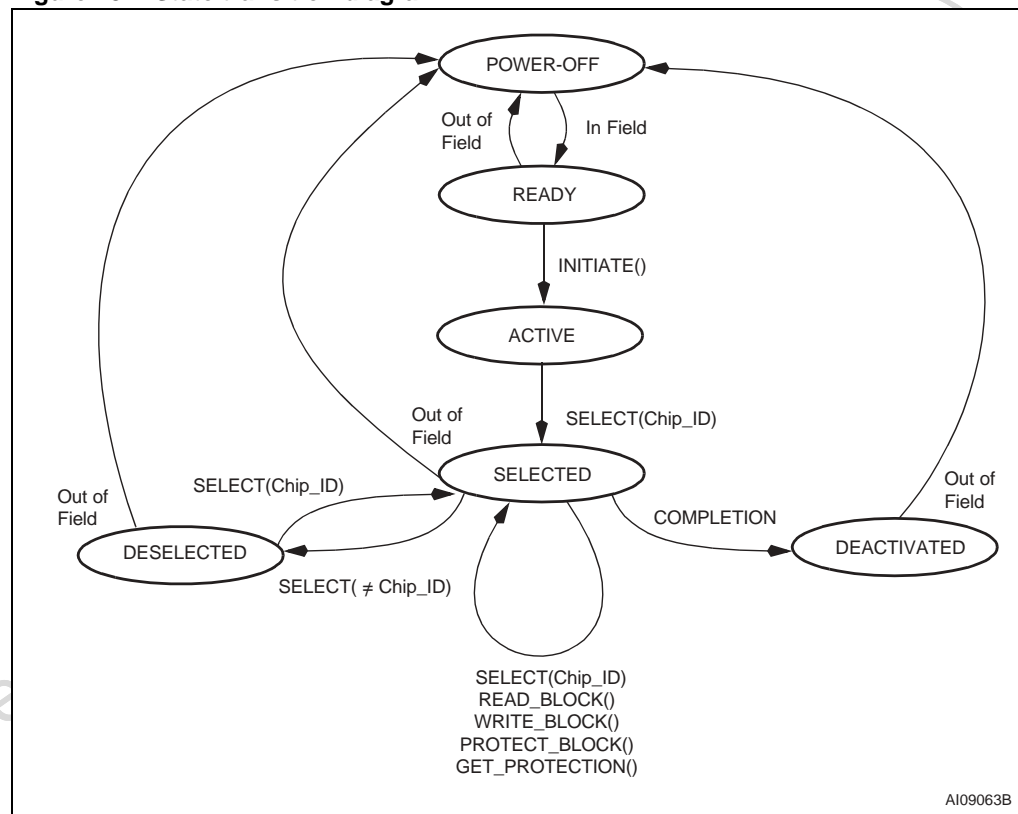
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## 5 Device operations (instructions)

All instructions, data and the CRC are transmitted to the SR176 in 10-bit character format using ASK modulation. The start bit ( $b_0$  of the 10 bits) is sent first. The command frame received by the SR176 on the antenna is demodulated by the 10% ASK demodulator, and is decoded by internal logic. Prior to any operation, the SR176 must have been previously activated by an INITIATE command (as shown in [Figure 13](#)). Each frame transmitted to the SR176 must start with a Start Of Frame, followed by one or more data characters, and is ended by two CRC bytes and the End Of Frame. When an invalid frame is decoded by the SR176 (because of a wrong instruction or CRC error), the memory does not send any error code.

When a valid frame is received, the SR176 may have to send back data to the reader. For this, it sends 10-bit characters back, with SOF, CRC and EOF, using the BPSK coding. The transfer is ended by the SR176 sending the EOF.

**Figure 13. State transition diagram**



## 5.1 INITIATE()

Command Code = 06h,00h

Prior to any other command, the SR176 must be activated by an INITIATE command. All other commands sent to the SR176 before the INITIATE are ignored. In response to receiving the INITIATE command, the SR176 sends back its Chip\_ID, using an 8-bit format (Figure 17).

Upon receiving a valid INITIATE command, the SR176 switches to the ACTIVE state, where it will not answer to any new INITIATE command. Once In the ACTIVE state, the SR176 will remain in this state until it receives a valid SELECT command.

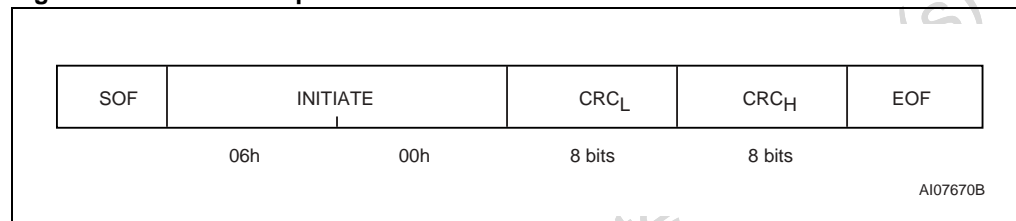
Request parameters (Figure 14):

- none

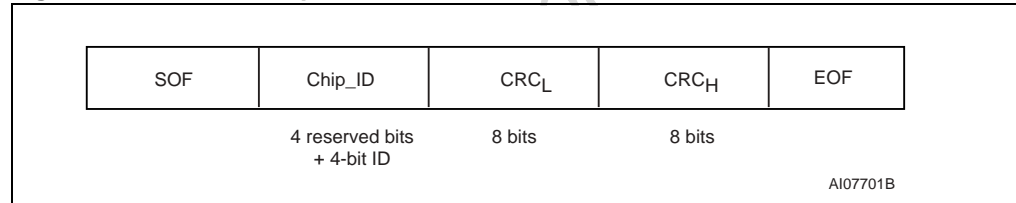
Response parameters (Figure 15):

- Chip\_ID (formatted as shown in Figure 16)

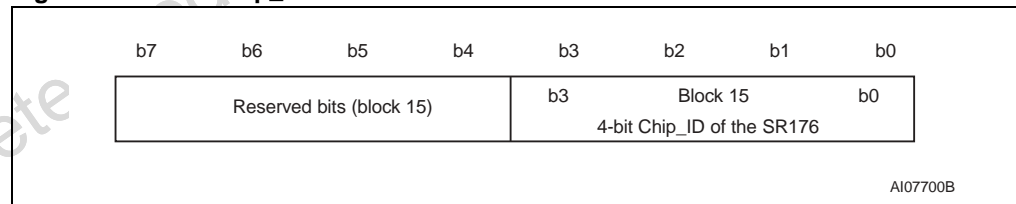
**Figure 14. INITIATE request format**



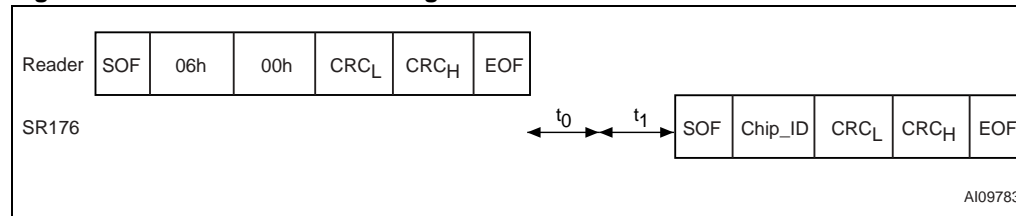
**Figure 15. INITIATE response format**



**Figure 16. 8-bit Chip\_ID format**



**Figure 17. INITIATE frame exchange between Reader and SR176**



## 5.2 SELECT(Chip\_ID)

Command Code = 0Eh,(X.ID)h

Prior to any memory access, the SR176 must have been set in the SELECTED state by a SELECT() command. All other commands sent to the SR176 before the SELECT(), except INITIATE(), are ignored. In response to receiving the SELECT() command, the SR176 sends back its Chip\_ID, using an 8-bit format (Figure 21).

Any SR176 that is already in the SELECTED state, and which receives a SELECT() command that does not match its Chip\_ID, is automatically put in the DESELECTED state. The SR176 stays in the SELECTED state up to the reception of a COMPLETION or a SELECT with a non-matching Chip\_ID.

After a PROTECT\_BLOCK command, it is necessary to send a new SELECT command in order to load enable the write access again in the internal logic. If a SELECT is not send, the SR176 keeps the previous write access rights.

Request parameters (Figure 18):

- Chip\_ID (formatted as shown in Figure 20)

Response parameters (Figure 19):

- Chip\_ID (formatted as shown in Figure 20)

Figure 18. SELECT request format

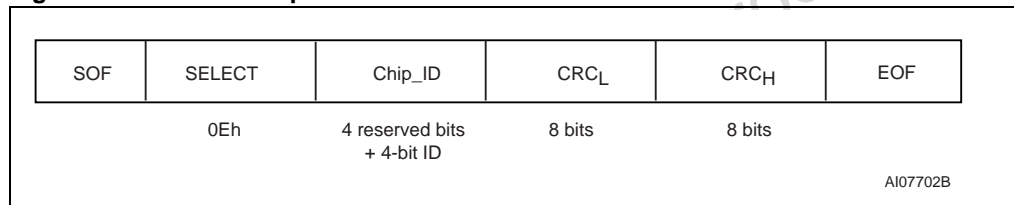


Figure 19. SELECT response format

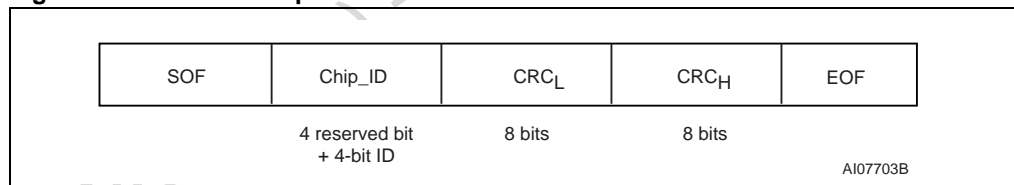
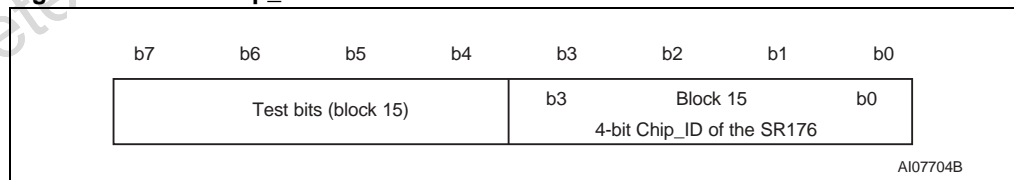
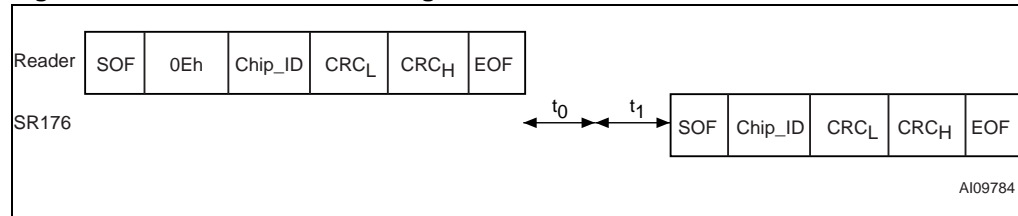


Figure 20. 8-bit Chip\_ID format





**Figure 21. SELECT frame exchange between Reader and SR176**

## 5.3 COMPLETION

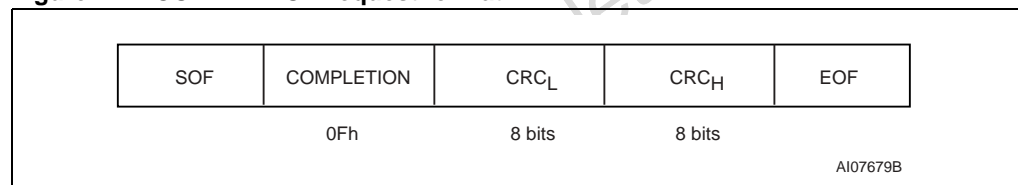
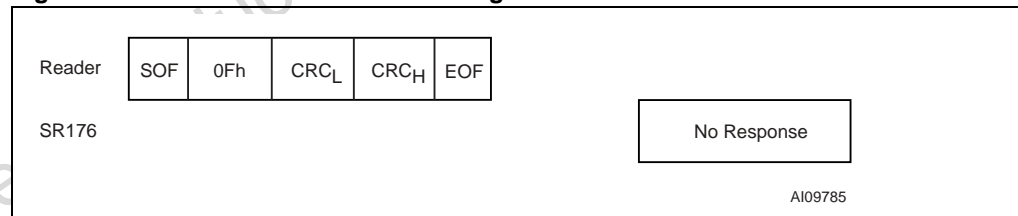
Command Code = 0Fh

When the COMPLETION command is received, the SR176 is put in the DEACTIVED state, and does not decode any new commands up to a Power-Off, and a new Power-On has occurred. This allows a new SR176 to be activated by an INITIATE command, without needing to remove the previous ones. The SR176 does not generate any response when it executes a COMPLETION command (*Figure 23*).

Prior to any COMPLETION command, the SR176 must have been put in the SELECTED mode by a SELECT command. A SR176 which was not selected does not interpret this command.

Request parameters (*Figure 22*):

- none

**Figure 22. COMPLETION request format****Figure 23. COMPLETION frame exchange between Reader and SR176**

## 5.4 READ\_BLOCK

Command Code = 08h,(X.AD)

When receiving the READ\_BLOCK command, the SR176 reads the requested block and sends back its 16-bit value in response (*Figure 26*). The AD value of the four least significant bits of the address code, (X.AD) ( $b_3$  to  $b_0$ ) represents the block address to be read. For example, address 06h sends back the value of block 6.

Prior to any READ\_BLOCK command, the SR176 must have been set into the SELECTED state.

Request parameters (*Figure 24*):

- ADDRESS: to specify an address block from 00h to 0Eh

Response parameters (*Figure 25*):

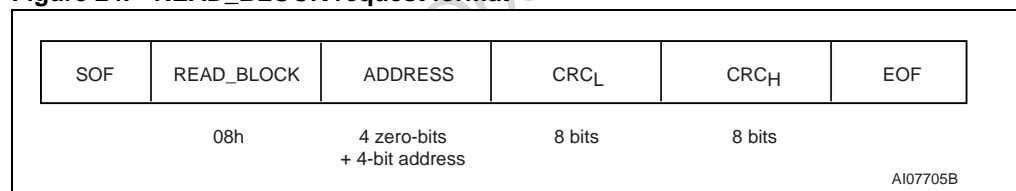
- DATA<sub>L</sub>: least significant Byte
- DATA<sub>H</sub>: most significant Byte

## 5.5 Read the 64-bit UID

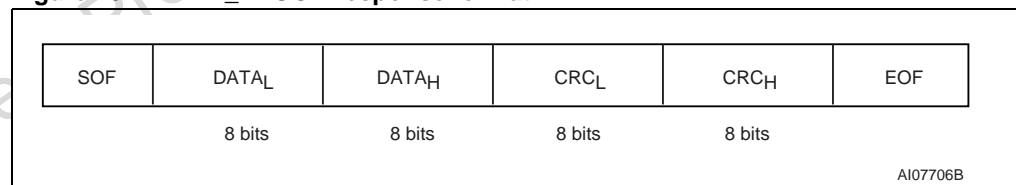
To read the complete 64-bit UID value from the SR176, the reader must provide a sequence of four READ\_BLOCK commands, in the following order (*Figure 27*):

- READ\_BLOCK @ 0 to get UID0
- READ\_BLOCK @ 1 to get UID1
- READ\_BLOCK @ 2 to get UID2
- READ\_BLOCK @ 3 to get UID3

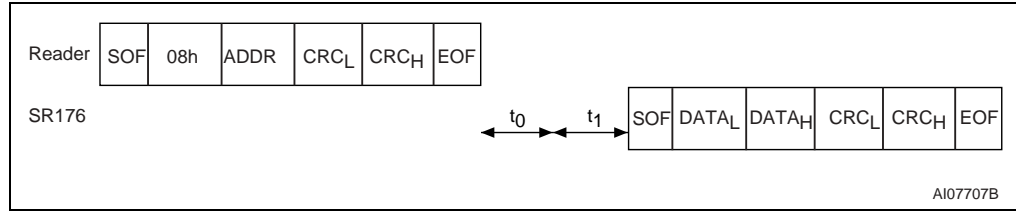
**Figure 24. READ\_BLOCK request format**



**Figure 25. READ\_BLOCK response format**

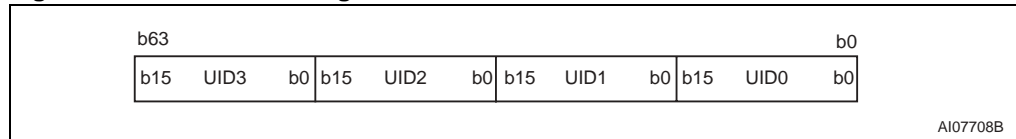


**Figure 26. READ\_BLOCK frame exchange between Reader and SR176**



AI07707B

**Figure 27. 64-bit UID storage format**



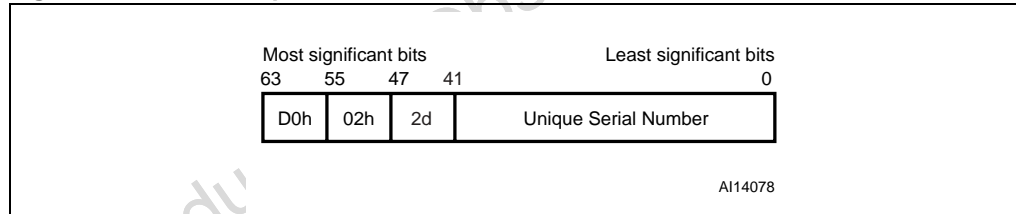
AI07708B

**Unique Identifier (UID)**

Members of the SR176 family are uniquely identified by a 64-bit Unique Identifier (UID). This is used for addressing each SR176 device uniquely after the anticollision loop. The UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. It is a read-only code, and comprises (as summarized in [Figure 28](#)):

- an 8-bit prefix, with the most significant bits set to D0h
- an 8-bit IC Manufacturer code (ISO/IEC 7816-6/AM1) set to 02h (for STMicroelectronics)
- a 6-bit IC code set to 00 0010b = 2d for SR176
- a 42-bit Unique Serial Number

**Figure 28. 64-bit unique identifier of the SR176**



AI14078

## 5.6 WRITE\_BLOCK

Command Code = 09h,(X.AD)

Prior to any WRITE\_BLOCK command, the SR176 must have been set into the SELECTED state.

When executing the WRITE\_BLOCK command, the SR176 overwrites the contents of the addressed block with the 16-bit value that was sent in the command, provided that the block is available and not write protected. The AD value of the four least significant bits of the address code (X.AD) ( $b_3$  to  $b_0$ ) represents the block address. For example, address 06h specifies that the data should be written in block 6. The SR176 does not generate any response when it executes a WRITE\_BLOCK command (Figure 30). The reader must check after the programming time,  $t_W$ , that the data bits were correctly programmed.

Block addresses between 0 to 3 cannot be accessed using the WRITE\_BLOCK command (the command has no effect on these blocks). Write access to block 15 is described in the section on the PROTECT\_BLOCK command.

Request parameters (Figure 29):

- ADDRESS: address block from 4 to 14
- DATA<sub>L</sub>: least significant Byte
- DATA<sub>H</sub>: most significant Byte

Figure 29. WRITE\_BLOCK request format

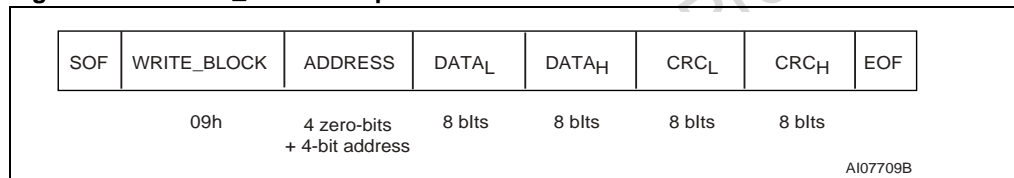
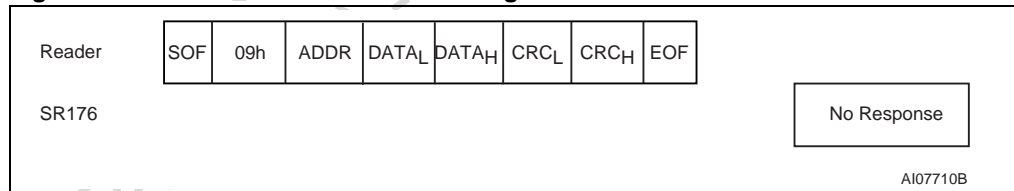


Figure 30. WRITE\_BLOCK frame exchange between Reader and SR176



## 5.7 PROTECT\_BLOCK

Command Code = 09h,0Fh,00h,LOCK\_REG

Prior to any PROTECT\_BLOCK command, the SR176 must have been set into the SELECTED state.

The PROTECT\_BLOCK command allows the write access to be blocked to memory blocks 4 to 15. It must be followed by a SELECT() command. This re-initializes the write protection conditions to blocks 4 to 15. Until then, the new protection setting is not taken into account by the SR176 logic. The SR176 does not generate any response when it executes a PROTECT\_BLOCK command (Figure 32). The reader must use the GET\_PROTECTION command to get the information on the protection status.

The OTP LOCK\_REG controls the write-protection on blocks 4 to 15, and is, itself, One-Time Programmable. Each '1' in the LOCK\_REG parameter indicates that the corresponding bit in the OTP LOCK\_REG should be set. Each '0' indicates that the corresponding bit should be left unchanged. Once a bit in the OTP LOCK\_REG has been set to '1', it is not possible to reset it to '0' and the corresponding memory blocks are forever write protected (and behaves like ROM).

Request parameters (Figure 31):

- LOCK\_REG (Table 3)

Figure 31. PROTECT\_BLOCK request format

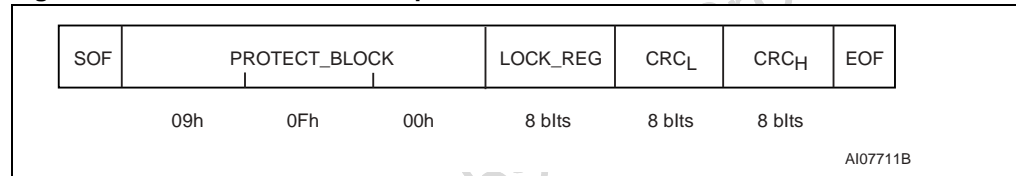
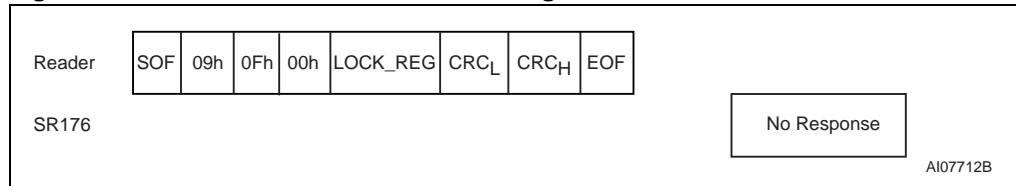


Table 3. Bits in the LOCK\_REG parameter, and in the OTP LOCK\_REG Register

Lock Reg Parameter Bit	Meaning	Block 15 Bit	Meaning
b <sub>7</sub>	1: set b <sub>15</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>15</sub>	1: Write-Protect Blocks 14 and 15 0: Allow write access
b <sub>6</sub>	1: set b <sub>14</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>14</sub>	1: Write-Protect Blocks 12 and 13 0: Allow write access
b <sub>5</sub>	1: set b <sub>13</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>13</sub>	1: Write-Protect Blocks 10 and 11 0: Allow write access
b <sub>4</sub>	1: set b <sub>12</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>12</sub>	1: Write-Protect Blocks 8 and 9 0: Allow write access
b <sub>3</sub>	1: set b <sub>11</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>11</sub>	1: Write-Protect Blocks 6 and 7 0: Allow write access
b <sub>2</sub>	1: set b <sub>10</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>10</sub>	1: Write-Protect Blocks 4 and 5 0: Allow write access
b <sub>1</sub>	1: set b <sub>9</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>9</sub>	1: Write-Protect Blocks 2 and 3 0: Allow write access
b <sub>0</sub>	1: set b <sub>8</sub> of Block 15 to '1' 0: leave it unchanged	b <sub>8</sub>	1: Write-Protect Blocks 0 and 1 0: Allow write access

**Figure 32. PROTECT\_BLOCK frame exchange between Reader and SR176**



## 5.8 GET\_PROTECTION

Command Code = 08h,0Fh

Prior to any GET\_PROTECTION, the SR176 must have been set into the SELECTED state.

GET\_PROTECTION allows the protection status of memory blocks 4 to 15 to be read. When receiving the GET\_PROTECTION command, the SR176 responds with the 16-bit value of block 15 (Figure 35). It gives the status of the LOCK\_REG and the Chip\_ID of the SR176.

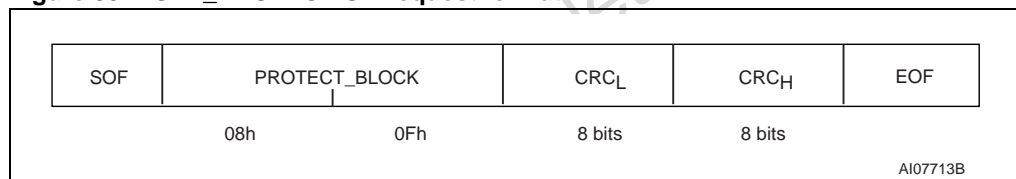
Request parameters (Figure 33):

- none

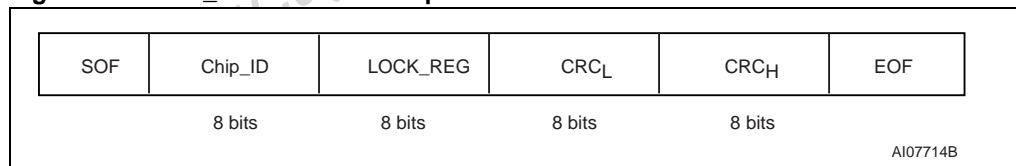
Response parameters (Figure 34):

- Chip\_ID: least significant Byte
- LOCK\_REG: most significant Byte

**Figure 33. GET\_PROTECTION request format**

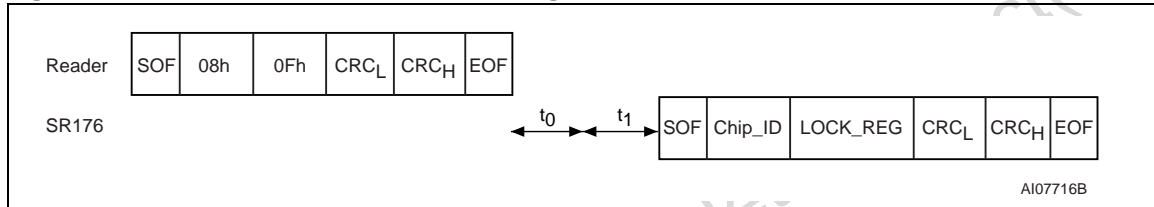


**Figure 34. GET\_PROTECTION response format**



**Table 4. Chip\_ID and LOCK\_REG**

Block 15 bits	Response parameter bits	Meaning
b <sub>15</sub>	LOCK_REG b <sub>7</sub>	1: Blocks 14 and 15 are write-protected (0: indicates that write-access is allowed)
b <sub>14</sub>	LOCK_REG b <sub>6</sub>	1: Blocks 12 and 13 are write-protected (0: indicates that write-access is allowed)
b <sub>13</sub>	LOCK_REG b <sub>5</sub>	1: Blocks 10 and 11 are write-protected (0: indicates that write-access is allowed)
b <sub>12</sub>	LOCK_REG b <sub>4</sub>	1: Blocks 8 and 9 are write-protected (0: indicates that write-access is allowed)
b <sub>11</sub>	LOCK_REG b <sub>3</sub>	1: Blocks 6 and 7 are write-protected (0: indicates that write-access is allowed)
b <sub>10</sub>	LOCK_REG b <sub>2</sub>	1: Blocks 4 and 5 are write-protected (0: indicates that write-access is allowed)
b <sub>9</sub>	LOCK_REG b <sub>1</sub>	1: Blocks 2 and 3 are write-protected (0: indicates that write-access is allowed)
b <sub>8</sub>	LOCK_REG b <sub>0</sub>	1: Blocks 0 and 1 are write-protected (0: indicates that write-access is allowed)
b <sub>4</sub> to b <sub>7</sub>	Chip_ID b <sub>4</sub> to b <sub>7</sub>	Reserved
b <sub>0</sub> to b <sub>3</sub>	Chip_ID b <sub>0</sub> to b <sub>3</sub>	Chip_ID (Value from 0h to Fh)

**Figure 35. GET\_PROTECTION frame exchange between Reader and SR176**

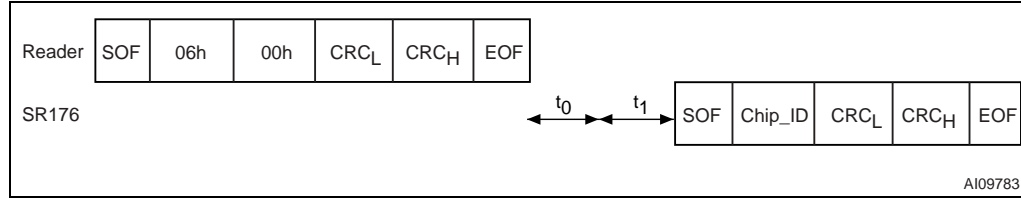
## 5.9 Power-on state

After Power-on, the SR176 is in the following state:

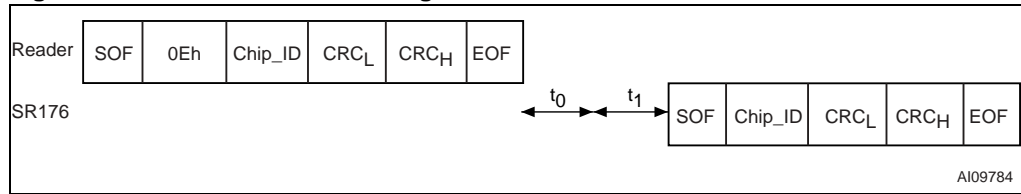
- The device is in the low power mode.
- The device is deselected.
- The device presents its highest impedance to the reader antenna field.
- It will not answer to any command except INITIATE.

## 6 SR176 command summary

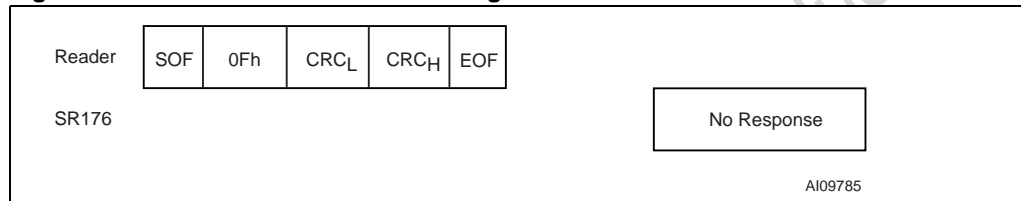
**Figure 36. INITIATE frame exchange between Reader and SR176**



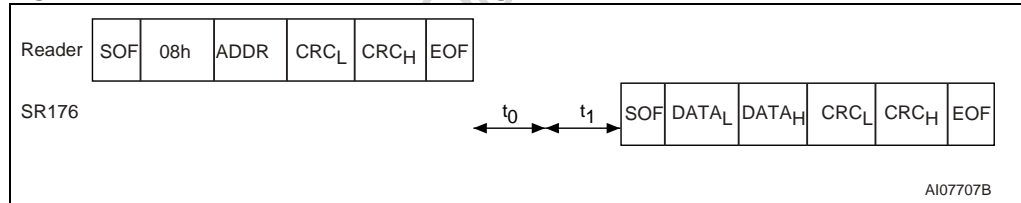
**Figure 37. SELECT frame exchange between Reader and SR176**



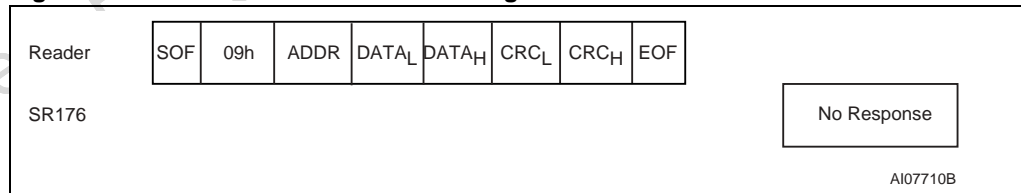
**Figure 38. COMPLETION frame exchange between Reader and SR176**



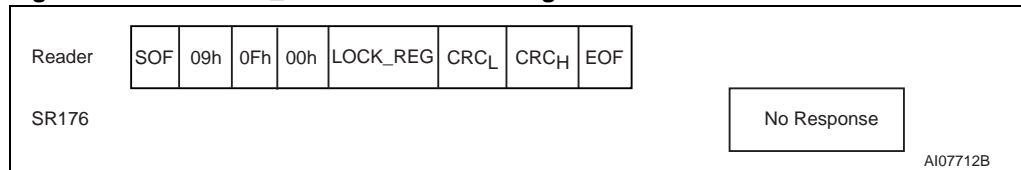
**Figure 39. READ\_BLOCK frame exchange between Reader and SR176**



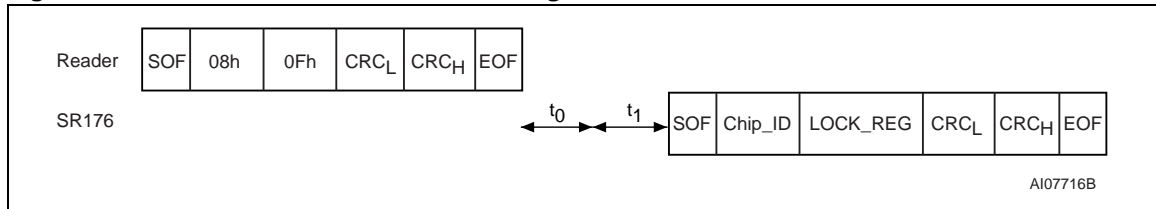
**Figure 40. WRITE\_BLOCK frame exchange between Reader and SR176**



**Figure 41. PROTECT\_BLOCK frame exchange between Reader and SR176**





**Figure 42. GET\_PROTECTION frame exchange between Reader and SR176**

Obsolete Product(s) - Obsolete Product(s)

## 7 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 5. Absolute maximum ratings**

Symbol	Parameter		Min.	Max.	Unit	
$T_{STG}$ , $h_{STG}$ , $t_{STG}$	Storage conditions	Wafer	15	25	°C	
				23	months	
		kept in its antistatic bag				
		A3, A4, A5	15	25	°C	
			40%	60%	RH	
			2	years		
$I_{CC}$	Supply current on AC0 / AC1		-20	20	mA	
$V_{MAX}$	Input voltage on AC0 / AC1		-7	7	V	
$V_{ESD}$	Electrostatic Discharge Voltage	Machine model <sup>(1)</sup>	-100	100	V	
		Human Body model <sup>(1)</sup>	-1000	1000	V	
		Human Body model <sup>(2)</sup>	-4000	4000	V	

1. Mil. Std. 883 - Method 3015.

2. ESD test: ISO 10373-6 for proximity cards.

## 8 DC and ac parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 6. Operating conditions**

Symbol	Parameter	Min.	Max.	Unit	
T <sub>A</sub>	Ambient operating temperature	Wafer	-20	85	°C
		A3, A4, A5	-20	85	°C

**Table 7. DC characteristics**

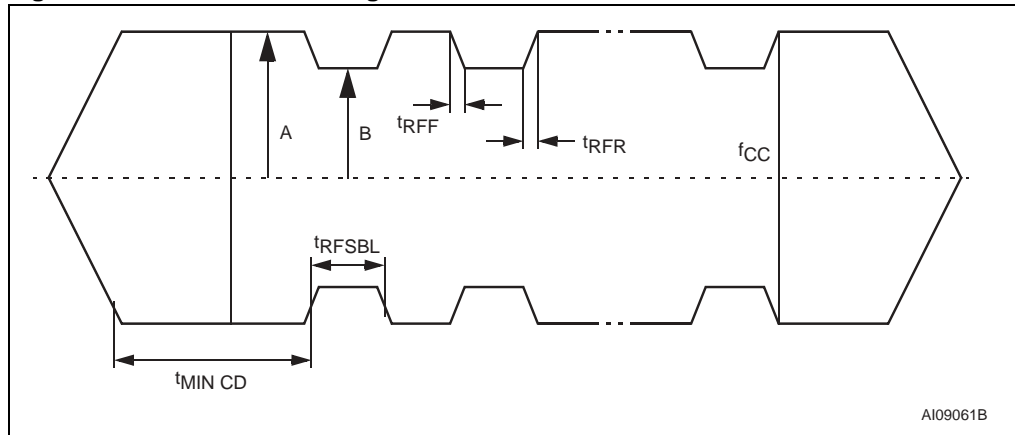
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>CC</sub>	Regulated voltage		2.5		3.5	V
V <sub>RET</sub>	Retromodulation induced voltage	ISO 10373-6	20			mV
C <sub>TUN</sub>	Internal tuning capacitor	13.56 MHz		64		pF

**Table 8. AC characteristics<sup>(1)</sup>**

Symbol	Parameter	Condition	Min	Max	Unit
f <sub>CC</sub>	External RF signal frequency		13.553	13.567	MHz
MI <sub>CARRIER</sub>	Carrier modulation index	MI=(A-B)/(A+B)	10	14	%
t <sub>RFR</sub> , t <sub>RFF</sub>	10% rise and fall time	10% to 90%	0.5	1.5	µs
t <sub>RFSBL</sub>	10% modulation pulse width	ETU = 128/f <sub>CC</sub>	9.44		µs
t <sub>JIT</sub>	ASK modulation data jitter	Coupler to SR176	- 2	+ 2	µs
t <sub>MIN CD</sub>	Minimum time from carrier generation to first data	From H-field Min	40		µs
f <sub>S</sub>	Subcarrier frequency	f <sub>CC</sub> /16	847.5		kHz
t <sub>0</sub>	Antenna reversal delay	128/f <sub>S</sub>	151		µs
t <sub>1</sub>	Synchronization delay	128/f <sub>S</sub>	151		µs
t <sub>2</sub>	Answer to new request delay	14 ETU	132		µs
t <sub>DR</sub>	Time between request characters	Coupler to SR176	0	57	µs
t <sub>DA</sub>	Time between answer characters	SR176 to Coupler	0		µs
t <sub>W</sub>	Programming time for WRITE			5	ms

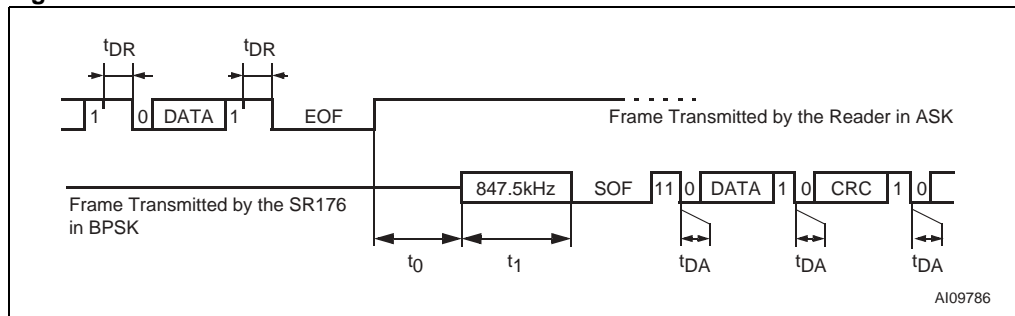
1. All timing measurements were performed on a reference antenna with the following characteristics:  
 External size: 75 mm x 48 mm  
 Number of turns: 3  
 Width of conductor: 1 mm  
 Space between 2 conductors: 0.4 mm  
 Value of the coil: 1.4 µH  
 Tuning Frequency: 14.4 MHz.

Figure 43. ASK modulated signal from the Reader to the contactless device



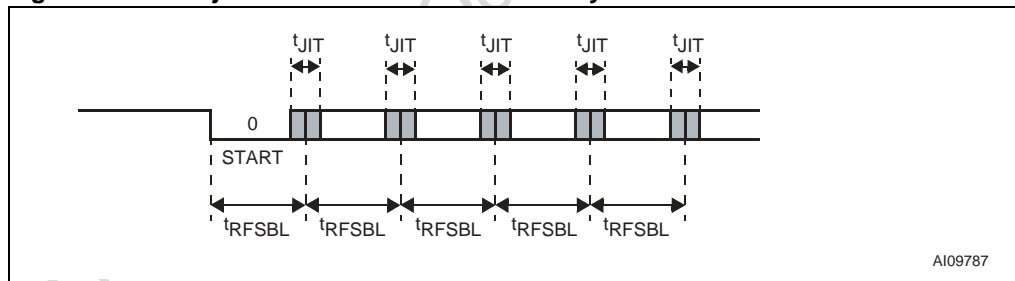
AI09061B

Figure 44. Frame transmission between the Reader and the contactless device



AI09786

Figure 45. Data jitter on the frame transmitted by the Reader in ASK



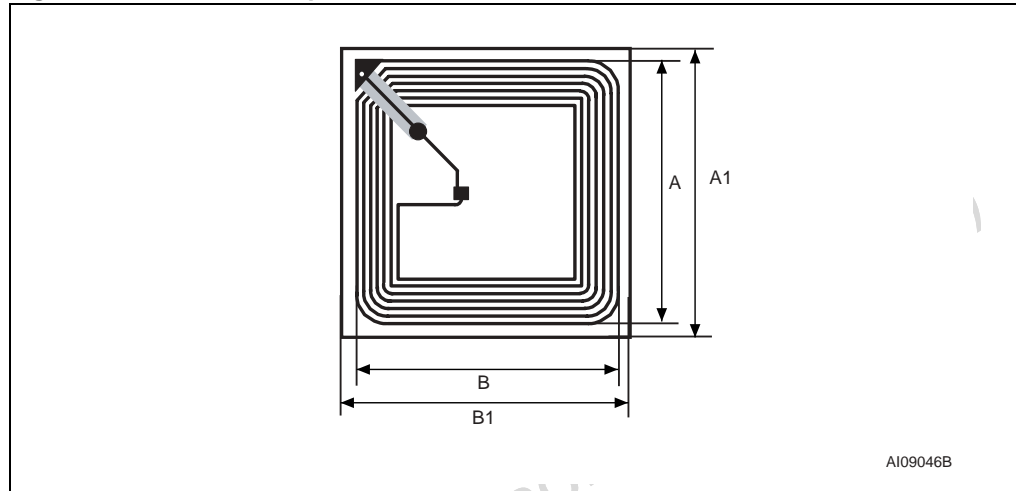
AI09787

## 9 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 46. A3 antenna specification**



**Table 9. A3 antenna specification**

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	38	37.5	38.5	mm
B	Coil length	38	37.5	38.5	mm
A1	Inlay width	43	42.5	43.5	mm
B1	Inlay length	43	42.5	43.5	mm
	Overall thickness of copper antenna coil	110	90	130	μm
	Silicon thickness	180	165	195	μm
Q	Unloaded Q value	40			
F <sub>NOM</sub>	Unloaded free-air resonance	15.1			MHz
P <sub>A</sub>	H-field energy for device operation		0.5		A/m
			114		dBμA/m

Figure 47. A4 antenna specification

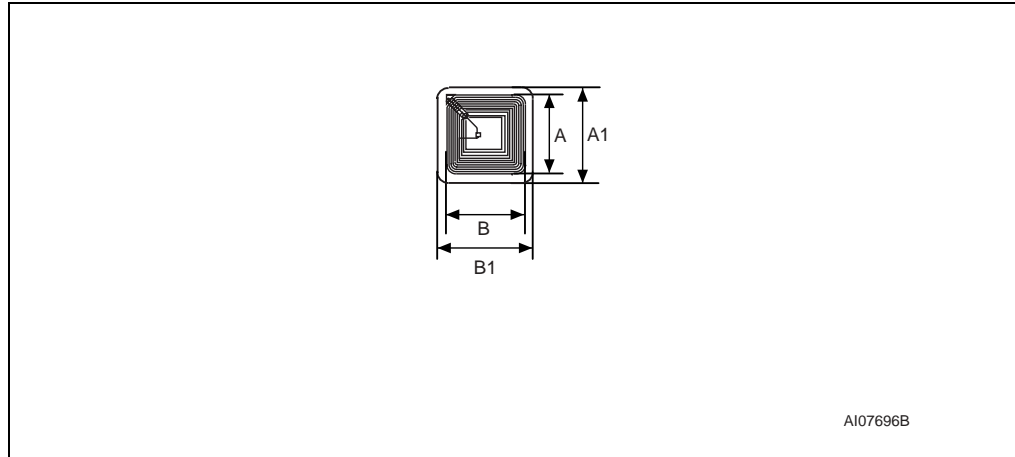


Table 10. A4 antenna specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	15	14.5	15.5	mm
B	Coil length	15	14.5	15.5	mm
A1	Inlay width	19	18.5	19.5	mm
B1	Inlay length	19	18.5	19.5	mm
	Overall thickness of copper antenna coil	110	90	130	μm
	Silicon thickness	180	165	195	μm
Q	Unloaded Q value	30			
F <sub>NOM</sub>	Unloaded free-air resonance	14.5			MHz
P <sub>A</sub>	H-field energy for device operation		1.5 123.5		A/m dBμA/m

Figure 48. A5 antenna specification

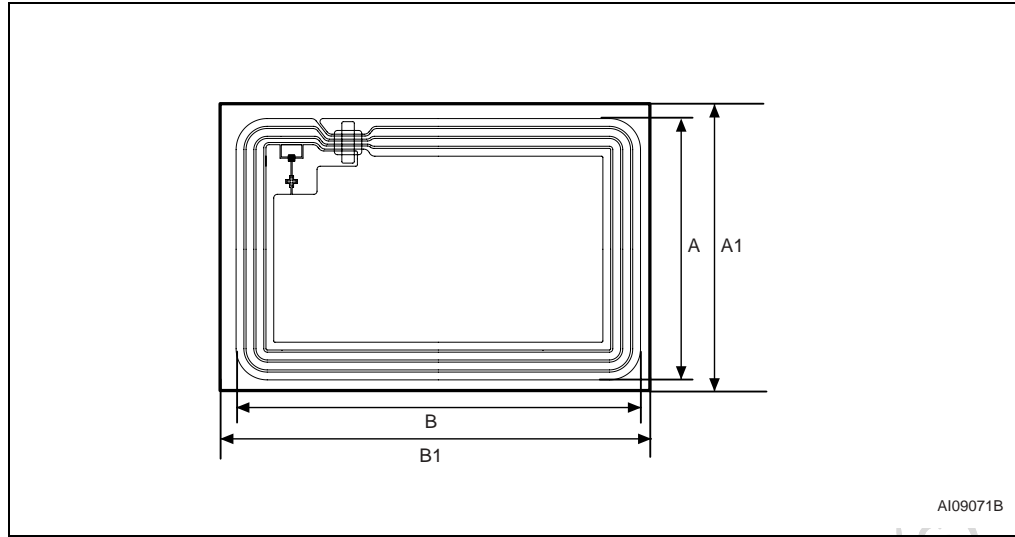


Table 11. A5 antenna specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	42	41.5	42.5	mm
B	Coil length	65	64.5	65.5	mm
A1	Inlay width	46	45.5	46.5	mm
B1	Inlay length	70	69.5	70.5	mm
	Overall thickness of copper antenna coil	140	130	150	$\mu\text{m}$
	Silicon thickness	180	165	195	$\mu\text{m}$
Q	Unloaded Q value	30			
$F_{\text{NOM}}$	Unloaded free-air resonance	14.8			MHz
$P_A$	H-field energy for device operation		0.25 108		A/m db $\mu$ A/m

## 10 Part numbering

**Table 12. Ordering information scheme**

Example:	SR176	–	W4 / XXX
<b>Device type</b>			
SR176			
<b>Package</b>			
W4 = 180 $\mu\text{m} \pm 15 \mu\text{m}$ UnsaWn Wafer			
SBN18 = 180 $\mu\text{m} \pm 15 \mu\text{m}$ Bumped and Sawn Wafer on 8-inch Frame			
A3T = 38 mm x 38 mm Copper Antenna on Continuous Tape			
A3S = 38 mm x 38 mm Copper Singulated Adhesive Antenna on Tape			
A4T = 15 mm x 15 mm Copper Antenna on Continuous Tape			
A4S = 15 mm x 15 mm Copper Singulated Adhesive Antenna on Tape			
A5T = 42 mm x 65 mm Copper Antenna on Continuous Tape			
A5S = 42 mm x 65 mm Copper Singulated Adhesive Antenna on Tape			
<b>Customer code</b>			
XXX = Given by STMicroelectronics			

**Note:** *Devices are shipped from the factory with the memory content bits erased to 1.*  
for a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.



## Appendix A ISO 14443 Type B CRC calculation

```

#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTE                unsigned char
#define USHORTunsigned short

unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
    ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
    ch = (ch^(ch<<4));
    *lpwCrc = (*lpwCrc >> 8)^(USHORT)ch << 8)^(USHORT)ch<<3)^(USHORT)ch>>4);
    return(*lpwCrc);
}

void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE *TransmitSecond)
{
    BYTE chBlock; USHORTt wCrc;
    wCrc = 0xFFFF; // ISO 3309
    do
    {
        chBlock = *Data++;
        UpdateCrc(chBlock, &wCrc);
    } while (--Length);
    wCrc = ~wCrc; // ISO 3309
    *TransmitFirst = (BYTE) (wCrc & 0xFF);
    *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
    return;
}

int main(void)
{
    BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
    printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1");
    printf("CRC_B of [ ");
    for(i=0; i<4; i++)
        printf("%02X ",BuffCRC_B[i]);
    ComputeCrc(BuffCRC_B, 4, &First, &Second);
    printf("] Transmitted: %02X then %02X.", First, Second);
    return(0);
}

```

## Revision history

**Table 13. Document revision history**

Date	Revision	Changes
23-Sep-2002	1.0	Document written
04-Oct-2004	2.0	First public release of full datasheet
29-Nov-2004	3.0	<i>INITIATE()</i> command specified.
10-Apr-2007	4	Document reformatted. Small text changes. Document status changed from Datasheet to Not For New Design. All antennas are ECOPACK® compliant. <i>Unique Identifier (UID) on page 19</i> added. $C_{TUN}$ min and max values removed, typical value added in <i>Table 7: DC characteristics</i> .

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