MN54F189-X REV 1A0

64-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

General Description

The F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

Industry Part Number	NS Part Numbers
54F189	54F189DLQB
	54F189FLQB
	54F189LLQB

Prime Die

M189

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp ($^{\circ}$C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-40
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-40
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-40
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-40

Features

- 3-State Outputs for Data Bus Applications
- Buffered Inputs Minimize Loading
- Diode Clamped Inputs Minimize Ringing
- Address Decoding On-Chip

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature
                                                          -65 C to +150 C
Ambient Temperature under Bias
                                                          -55 C to +125 C
Junction Temperature under Bias
                                                          -55 C to +175 C
Vcc Pin Potential to Ground Pin
                                                          -0.5V to +7.0V
Input Voltage
 (Note 2)
                                                          -0.5V to +7.0V
Input Current
 (Note 2)
                                                          -30 mA to +5.0mA
Voltage Applied to Output in HIGH State (with Vcc=0V)
    Standard Output   -0.5V to Vcc
    TRI-STATE Output   -0.5V to +5.5V
Current Applied to Output in LOW State (Max)
                                                          twice the rated Iol(mA)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or
         have its useful life impaired. Functional operation under these conditions is not
         implied.
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature
    Commercial   0 C to +70 C
    Military   -40 C to +125 C

Supply Voltage
    Military   +4.5V to +5.5V
    Commercial   +4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Limited Temp Range: -40C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input High Current	VCC=5.5V, VM=2.7V, VINH=5.5V	1, 3	INPUTS		20	uA	1, 2, 3
IBVI	Input High Current	VCC=5.5V, VM=7.0V, VINH=5.5V	1, 3	INPUTS		100	uA	1, 2, 3
IIL	Input LOW Current	VCC=5.5V, VM=0.5V	1, 3	An, Dn $\overline{WE}$		-0.6	mA	1, 2, 3
IIL2	Input LOW Current	VCC= 5.5V, VM=0.5V	1, 3	INPUTS $\overline{CS}$		-1.2	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIL=0.8V, IOL=20mA, VINH=5.5V	1, 3	OUTPUTS		0.5	V	1, 2, 3
VOH	Output High Voltage	VCC=4.5V, VINH=5.5, VINL=0.0V, IOH=-1.0mA	1, 3	OUTPUTS	2.5		V	1, 2, 3
VOH3	Output HIGH Voltage	VCC=4.5V, VINH=5.5V, VINL=0.0V, IOH3=-3.0mA, VIH=2.0V	1, 3	OUTPUTS	2.4		V	1, 2, 3
IOS	Short Circuit Current	VCC=5.5V, VINH=5.5V, VM=0.0V, VINL=0.0V	1, 3	OUTPUTS	-60	-150	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=5.5V	1, 3	INPUTS		-1.2	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINH=5.5V, VINL=0.0V	1, 3	VCC		55	mA	1, 2, 3
ICEX	Output HIGH Leakage Current	VCC=5.5V, VINH=5.5V, VINL=0.0V, VM=5.5V	1, 3	OUTPUTS		250	uA	1, 2, 3
IOZH	Output Leakage Current	VCC=5.5V, VM=2.7V, VINH=5.5V, VINL=0.0V, VIH=2.0V	1, 3	OUTPUTS		50	uA	1, 2, 3
IOZL	Output Leakage Current	VCC=5.5V, VM=0.5V, VINH=5.5V, VINL=0.0V, VIH=2.0V	1, 3	OUTPUTS		-50	uA	1, 2, 3

AC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Limited Temp Range: -40C to 125C   CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns   SEE AC FIGS

tpLH	Access Time, HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	An to $\overline{O}$n	11.0	26.0	ns	9
			2, 4	An to $\overline{O}$n	9.0	32.0	ns	10, 11
tpHL	Access Time, HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	An to $\overline{O}$n	8.0	19.0	ns	9
			2, 4	An to $\overline{O}$n	8.0	23.0	ns	10, 11

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Electrical Characteristics

AC PARAMETER(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Limited Temp Range: -40C to 125C   CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns   SEE AC FIGS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpZH(1)	Access Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	$\overline{CS}$ to $\overline{O}$n	3.5	8.5	ns	9
			2, 4	$\overline{CS}$ to $\overline{O}$n	3.5	10.5	ns	10, 11
tpZL(1)	Access Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	$\overline{CS}$ to $\overline{O}$n	5.0	13.5	ns	9
			2, 4	$\overline{CS}$ to $\overline{O}$n	5.0	15.0	ns	10, 11
tpHZ(1)	Disable Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	$\overline{CS}$ to $\overline{O}$n	2.0	6.0	ns	9
			2, 4	$\overline{CS}$ to $\overline{O}$n	2.0	8.0	ns	10, 11
tpLZ(1)	Disable Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	$\overline{CS}$ to $\overline{O}$n	3.0	8.0	ns	9
			2, 4	$\overline{CS}$ to $\overline{O}$n	2.5	10.0	ns	10, 11
tpZH(2)	Access Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4, 6	$\overline{WE}$ to $\overline{O}$n	6.5	28.0	ns	9
			2, 4, 6	$\overline{WE}$ to $\overline{O}$n	6.5	37.5	ns	10, 11
tpZL(2)	Access Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4, 6	$\overline{WE}$ to $\overline{O}$n	6.5	15.5	ns	9
			2, 4, 6	$\overline{WE}$ to $\overline{O}$n	6.5	17.5	ns	10, 11
tpHZ(2)	Disable Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4, 6	$\overline{WE}$ to $\overline{O}$n	4.0	10.0	ns	9
			2, 4, 6	$\overline{WE}$ to $\overline{O}$n	3.5	12.0	ns	10, 11
tpLZ(2)	Disable Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	2, 4	$\overline{WE}$ to $\overline{O}$n	4.0	13.0	ns	9
			2, 4	$\overline{WE}$ to $\overline{O}$n	4.0	15.0	ns	10, 11
ts(L/H)(1)	Setup Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	Dn to $\overline{WE}$	10.0		ns	9
			5	Dn to $\overline{WE}$	11.0		ns	10, 11
th(L/H)(1)	Hold Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	Dn to $\overline{WE}$	0		ns	9
			5	Dn to $\overline{WE}$	2.0		ns	10, 11

Electrical Characteristics

AC PARAMETER(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Limited Temp Range: -40C to 125C   CL=50pf, RL=500 OHMS, TR=2.5ns, TF=2.5ns   SEE AC FIGS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ts(L/H)(2)	Setup Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	An to $\overline{WE}$	0		ns	9, 10, 11
th(L/H)(2)	Hold Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	An to $\overline{WE}$	2.0		ns	9, 10, 11
ts(L)(3)	Setup Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	$\overline{CS}$ to $\overline{WE}$	0		ns	9, 10, 11
th(L)(3)	Hold Time HIGH or LOW	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C	5	$\overline{CS}$ to $\overline{WE}$	6.0		ns	9
			5	$\overline{CS}$ to $\overline{WE}$	7.5		ns	10, 11
tw(L)	Pulse Width	VCC=5.5V @25C, VCC=4.5 & 5.5V @ -40C/125C TR/TF=1.0ns	5	$\overline{WE}$	6.0		ns	9
			5	$\overline{WE}$	15.0		ns	10, 11

Note 1:   Screen tested 100% on each device at +25C, +125C & -40C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2:   Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3:   Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -40C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4:   Sample tested (Method 5005, Table 1) on each MFG. lot at +25C subgroup A9, and periodically at +125C & -40C temperature, subgroups 10 & 11.
Note 5:   GUARANTEED BUT NOT TESTED. (Design Characterization Data)
Note 6:   Spurious transitions may occur on the OX outputs prior to specified access time during the write enable cycles.