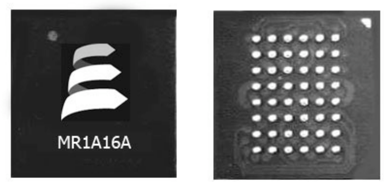
MR1A16A

128Kx16 MRAM Memory

Features

- Fast 35 ns Read/Write Cycle
- SRAM Compatible Timing and Pin-out Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to eliminate battery assembly, reliability, and liability issues
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Extended Temperatures
- RoHS-Compliant SRAM-compatible TSOPII Package
- RoHS-Compliant SRAM-compatible BGA Package Shrinks Board Area By Three Times

44-TSOP



48-BGA

RoHS

Introduction

The MR1A16A is a 2,097,152-bit magnetoresistive random access memory (MRAM) device organized as 131,072 words of 16 bits. The MR1A16A offers SRAM compatible 35 ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The MR1A16A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The MR1A16A is available in small footprint 400-mil, 44-lead plastic small-outline TSOP type-II package or 8 mm x 8 mm, 48-pin ball grid array (BGA) package with 0.75 mm ball centers. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The MR1A16A provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature (0 to +70˚C), industrial temperature (-40 to +85˚C), and extended temperature (-40 to +105˚C) range options.

Device Pin Assignment

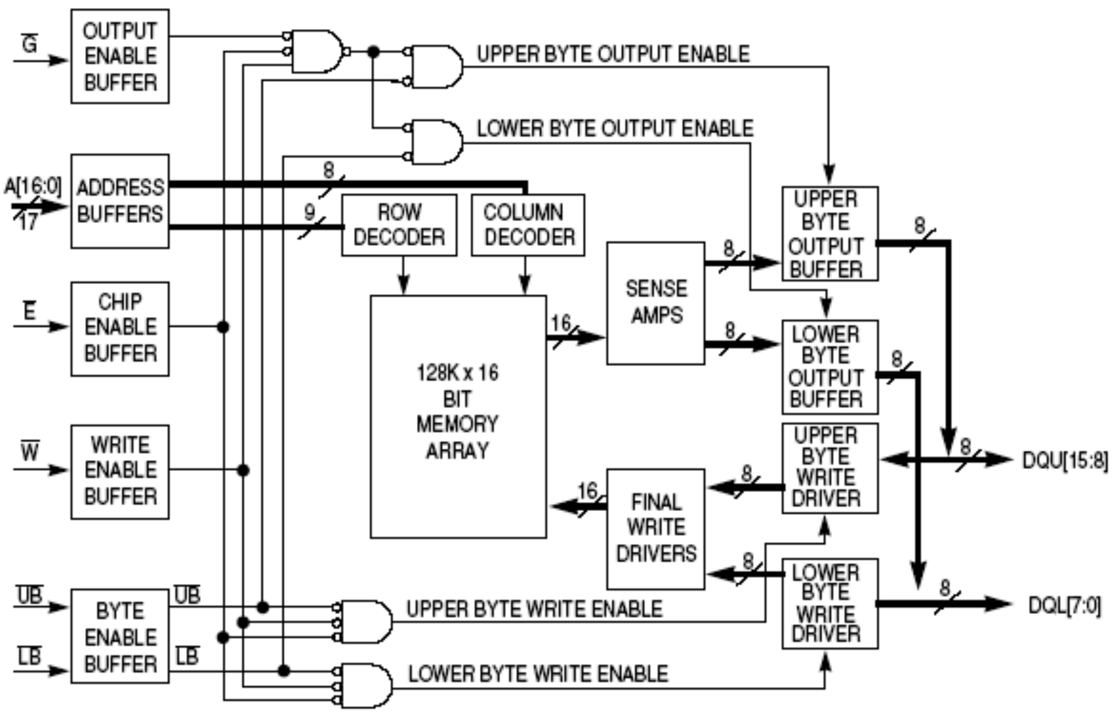
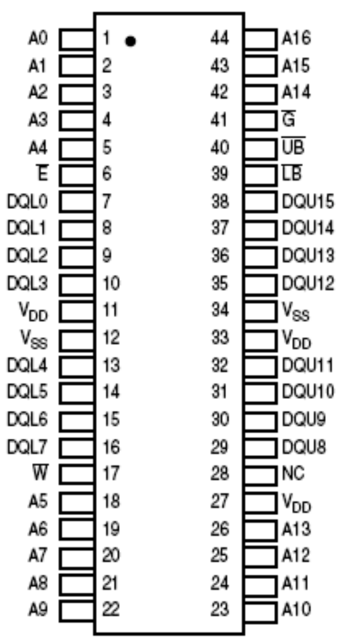


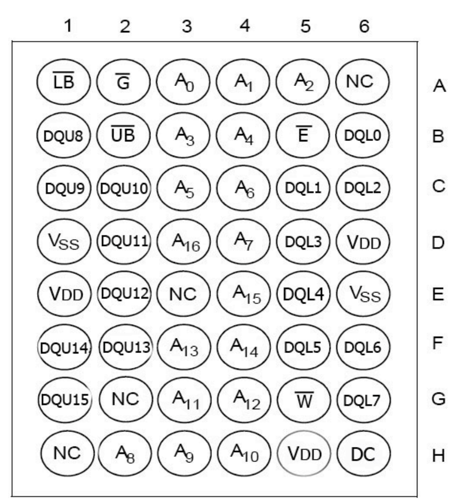
Figure 1. Block Diagram



44-Pin TSOP Type II

Table 1. Pin Functions

Signal Name	Function
A	Address input
$\overline{E}$	Chip enable
$\overline{W}$	Write enable
$\overline{G}$	Output enable
$\overline{UB}$	Upper byte select
$\overline{LB}$	Lower byte select
DQL	Data I/O, lower byte
DQU	Data I/O, upper byte
V_{DD}	Power supply
V_{SS}	Ground
NC	Do not connect this pin



48-Pin BGA

Table 2. Operating Modes

$\overline{E}$[1]	$\overline{G}$[1]	$\overline{W}$[1]	$\overline{LB}$[1]	$\overline{UB}$[1]	Mode	V_{DD} Current	DQL[7:0][2]	DQU[15:8][2]
H	X	X	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z	Hi-Z
L	H	H	X	X	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	X	X	H	H	Output disabled	I_{DDR}	Hi-Z	Hi-Z
L	L	H	L	H	Lower byte read	I_{DDR}	D_{Out}	Hi-Z
L	L	H	H	L	Upper byte read	I_{DDR}	Hi-Z	D_{Out}
L	L	H	L	L	Word read	I_{DDR}	D_{Out}	D_{Out}
L	X	L	L	H	Lower byte write	I_{DDW}	D_{In}	Hi-Z
L	X	L	H	L	Upper byte write	I_{DDW}	Hi-Z	D_{In}
L	X	L	L	L	Word write	I_{DDW}	D_{In}	D_{In}

NOTES:
1 H = high, L = low, X = don't care
2 Hi-Z = high impedance

Electrical Specifications

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 3. Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Supply voltage[2]	V_{DD}	–0.5 to 4.0	V
Voltage on any pin[2]	V_{In}	–0.5 to V_{DD} + 0.5	V
Output current per pin	I_{Out}	±20	mA
Package power dissipation[3]	P_D	0.600	W
Temperature under bias MR1A16A (Commercial Temperture) MR1A16AC (Industrial Temperature) MR1A16AV (Extended Temperature)	T_{Bias}	–10 to 85 –45 to 95 –45 to 110	˚C
Storage temperature	T_{stg}	–55 to 150	˚C
Lead temperature during solder (3 minute max)	T_{Lead}	260	˚C
Maximum magnetic field during write MR1A16A (All Temperatures)	H_{max_write}	2000	A/m
Maximum magnetic field during read or standby	H_{max_read}	8000	A/m

NOTES:
1 Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2 All voltages are referenced to V_{SS}.
3 Power dissipation capability depends on package characteristics and use environment.

Table 4. Operating Conditions

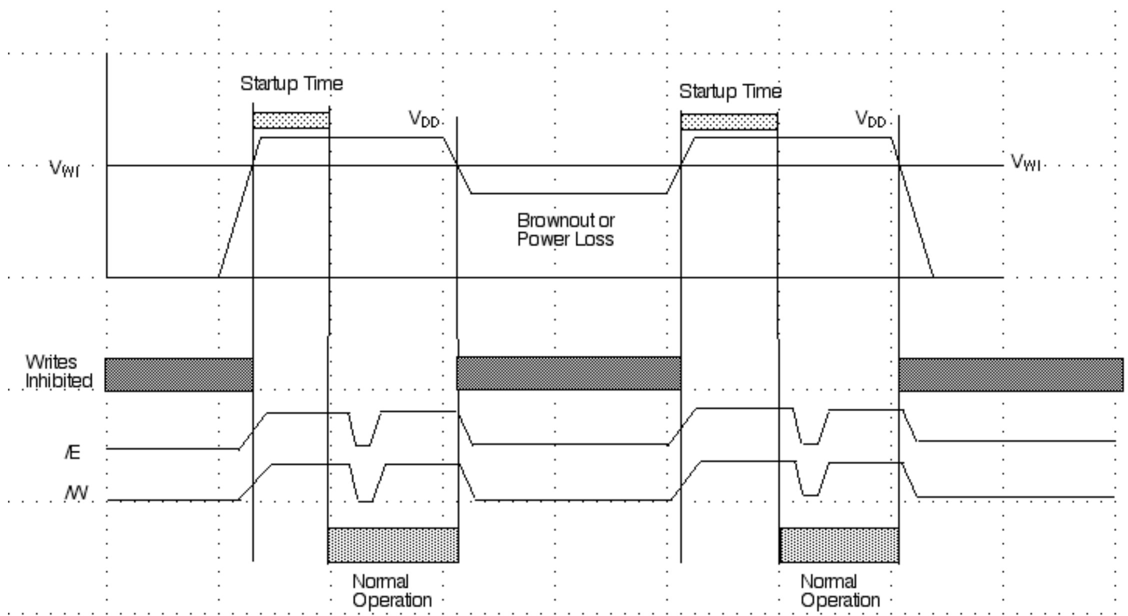
Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	3.0[1]	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0[1]	V
Input high voltage	V_{IH}	2.2	—	V_{DD} + 0.3[2]	V
Input low voltage	V_{IL}	–0.5[3]	—	0.8	V
Operating temperature MR1A16A (Commercial) MR1A16AC (Industrial) MR1A16AV (Extended)	T_A	0 -40 -40		70 85 105	°C

NOTES:

1 There is a 2 ms startup time once Vdd exceeds Vddmin. See Power up and Powerdown Sequencing section below

2 V_{IH} (max) = V_{DD} + 0.3 Vdc; V_{IH} (max) = V_{DD} + 2.0 Vac (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

3 V_{IL} (min) = –0.5 Vdc; V_{IL} (min) = –2.0 Vac (pulse width ≤ 10 ns) for I ≤ 20.0 mA.



Power Up and Power Down Sequencing

MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DDmin}, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The /E and /W control signals should track V_{DD} on power up to V_{DD}-0.2v or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /E and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DDmin}.

dc Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current	$I_{lkg(I)}$	—	—	±1	µA
Output leakage current	$I_{lkg(O)}$	—	—	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	—	—	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OH} = –4 mA) (I_{OH} = –100 uA)	V_{OH}	2.4 V_{DD} – 0.2	—	—	V

Power Supply Characteristics

Parameter	Symbol	Typ	Max	Unit
ac active supply current — read modes[1] (I_{Out} = 0 mA, V_{DD} = max)	I_{DDR}	55	80	mA
ac active supply current — write modes[1] (V_{DD} = max) MR1A16A (Commercial Temperature) MR1A16AC (Industrial Temperature) MR1A16AV (Extended Temperature)	I_{DDW}	105 105 105	155 165 165	mA
ac standby current (V_{DD} = max, $\overline{E} = V_{IH}$) (no other restrictions on other inputs)	I_{SB1}	18	28	mA
CMOS standby current ($\overline{E} \geq V_{DD} - 0.2$ V and $V_{In} \leq V_{SS} + 0.2$ V or $\geq V_{DD} - 0.2$ V) (V_{DD} = max, f = 0 MHz)	I_{SB2}	9	12	mA

NOTES:
1 All active current measurements are measured with one address transition per cycle and at minimum cycle time.

Timing Specifications

Table 7. Capacitance[1]

Parameter	Symbol	Typ	Max	Unit
Address input capacitance	C_{In}	—	6	pF
Control input capacitance	C_{In}	—	6	pF
Input/output capacitance	$C_{I/O}$	—	8	pF

NOTES:
[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, periodically sampled rather than 100% tested.

Table 8. ac Measurement Conditions

Parameter	Value
Logic input timing measurement reference level	1.5 V
Logic output timing measurement reference level	1.5 V
Logic input pulse levels	0 or 3.0 V
Input rise/fall time	2 ns
Output load for low and high impedance parameters	See Figure 3A
Output load for all other timing parameters	See Figure 3B

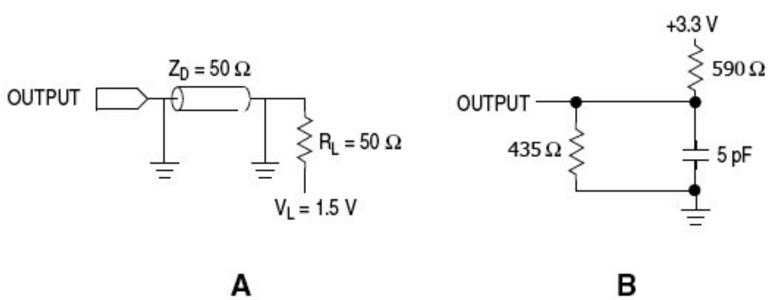


Figure 3. Output Load for ac Test

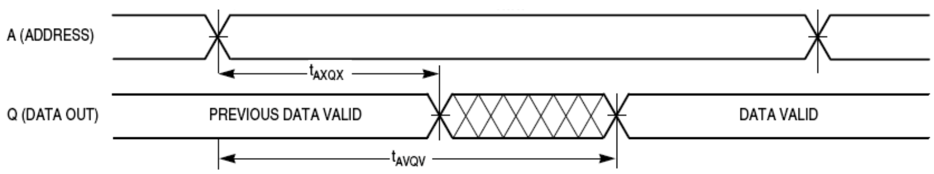
Timing Specifications

Read Mode

Table 9. Read Cycle Timing[1, 2]

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	—	ns
Address access time	t_{AVQV}	—	35	ns
Enable access time[3]	t_{ELQV}	—	35	ns
Output enable access time	t_{GLQV}	—	15	ns
Byte enable access time	t_{BLQV}	—	15	ns
Output hold from address change	t_{AXQX}	3	—	ns
Enable low to output active[4, 5]	t_{ELQX}	3	—	ns
Output enable low to output active[4, 5]	t_{GLQX}	0	—	ns
Byte enable low to output active[4, 5]	t_{BLQX}	0	—	ns
Enable high to output Hi-Z[4, 5]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[4, 5]	t_{GHQZ}	0	10	ns
Byte high to output Hi-Z[4, 5]	t_{BHQZ}	0	10	ns

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
3. Addresses valid before or at the same time $\overline{E}$ goes low.
4. This parameter is sampled and not 100% tested.
5. Transition is measured ±200 mV from steady-state voltage.



NOTES:
Device is continuously selected ($\overline{E} \leq V_{IL}$, $\overline{G} \leq V_{IL}$).

Figure 4. Read Cycle 1

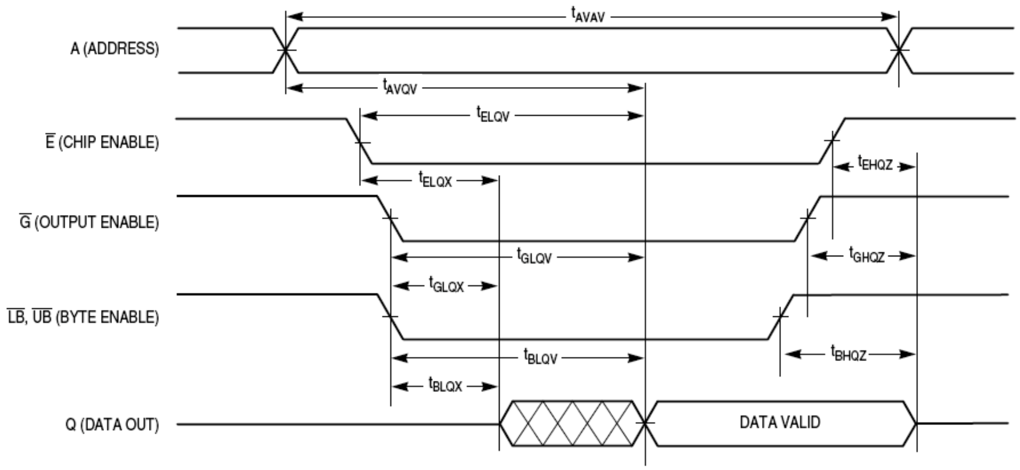


Figure 5. Read Cycle 2

Timing Specifications

Write Mode

Table 10. Write Cycle Timing 1 ($\overline{W}$ Controlled)[1, 2, 3, 4, 5]

Parameter	Symbol	Min	Max	Unit
Write cycle time[6]	t_{AVAV}	35	—	ns
Address set-up time	t_{AVWL}	0	—	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	18	—	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	—	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	15	—	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	15	—	ns
Data valid to end of write	t_{DVWH}	10	—	ns
Data hold time	t_{WHDX}	0	—	ns
Write low to data Hi-Z[7, 8, 9]	t_{WLQZ}	0	12	ns
Write high to output active[7, 8, 9]	t_{WHQX}	3	—	ns
Write recovery time	t_{WHAX}	12	—	ns

NOTES:

1 A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.

2 Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles

3 If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.

4 After $\overline{W}$, $\overline{E}$, or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.

5 The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

6 All write cycle timings are referenced from the last valid address to the first transition address.

7 This parameter is sampled and not 100% tested.

8 Transition is measured ±200 mV from steady-state voltage.

9 At any given voltage or temperature, t_{WLQZ} max < t_{WHQX} min.

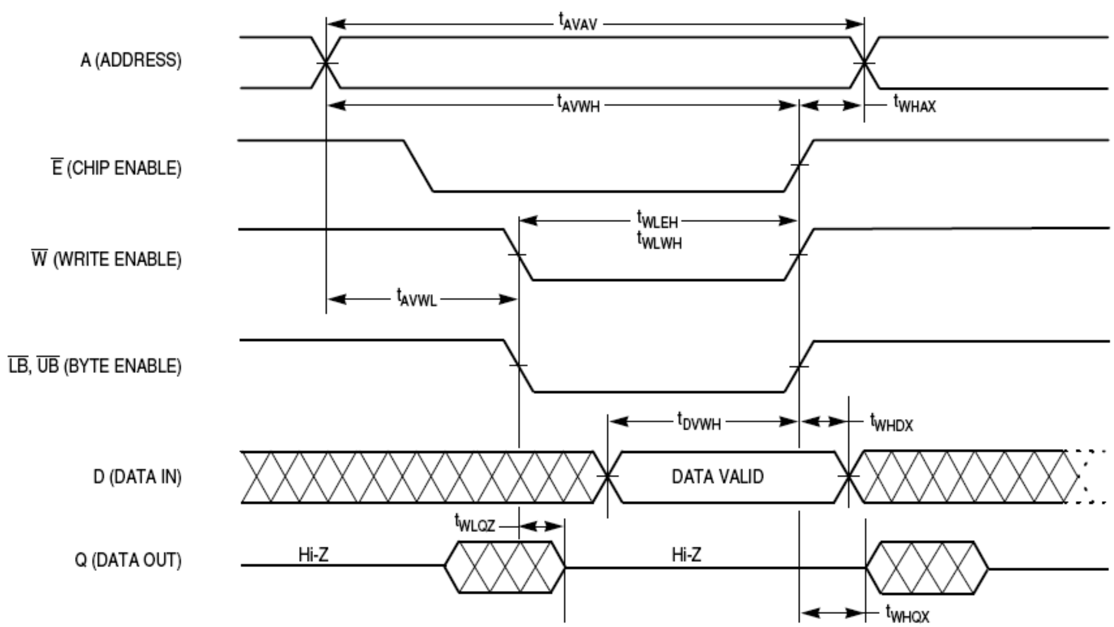


Figure 6. Write Cycle 1 ($\overline{W}$ Controlled)

Timing Specifications

Table 11. Write Cycle Timing 2 ($\overline{E}$ Controlled)[1, 2, 3, 4, 5]

Parameter	Symbol	Min	Max	Unit
Write cycle time[6]	t_{AVAV}	35	—	ns
Address set-up time	t_{AVEL}	0	—	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVEH}	18	—	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVEH}	20	—	ns
Enable to end of write ($\overline{G}$ high)	t_{ELEH} t_{ELWH}	15	—	ns
Enable to end of write ($\overline{G}$ low)[7, 8]	t_{ELEH} t_{ELWH}	15	—	ns
Data valid to end of write	t_{DVEH}	10	—	ns
Data hold time	t_{EHDX}	0	—	ns
Write recovery time	t_{EHAX}	12	—	ns

NOTES:

1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Power supplies must be properly grounded and decoupled, and bus contention must be minimized or eliminated during read and write cycles.
3. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. After $\overline{W}$, $\overline{E}$, or $\overline{UB}/\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
5. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
6. All write cycle timings are referenced from the last valid address to the first transition address.
7. If $\overline{E}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
8. If $\overline{E}$ goes high at the same time or before $\overline{W}$ goes high, the output will remain in a high-impedance state.

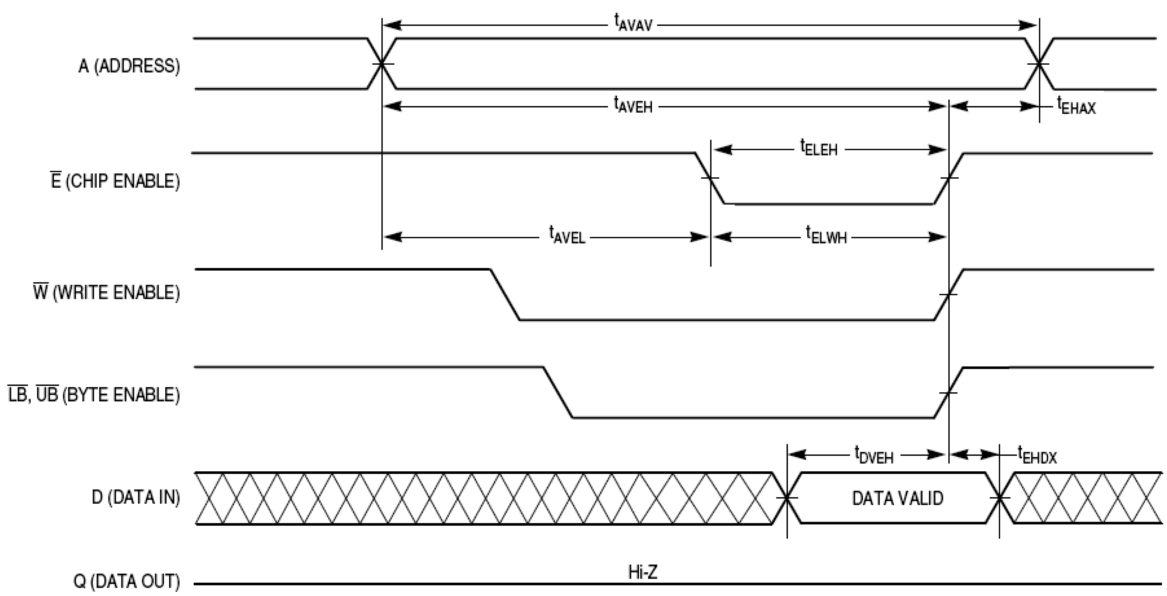


Figure 7. Write Cycle 2 ($\overline{E}$ Controlled)

Timing Specifications

Table 12. Write Cycle Timing 3 ($\overline{LB}$/$\overline{UB}$ Controlled)[1, 2, 3, 4, 5, 6]

Parameter	Symbol	Min	Max	Unit
Write cycle time[7]	t_{AVAV}	35	—	ns
Address set-up time	t_{AVBL}	0	—	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVBH}	18	—	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVBH}	20	—	ns
Byte pulse width ($\overline{G}$ high)	t_{BLEH} t_{BLWH}	15	—	ns
Byte pulse width ($\overline{G}$ low)	t_{BLEH} t_{BLWH}	15	—	ns
Data valid to end of write	t_{DVBH}	10	—	ns
Data hold time	t_{BHDX}	0	—	ns
Write recovery time	t_{BHAX}	12	—	ns

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read and write cycles.
3. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high-impedance state.
4. After $\overline{W}$, $\overline{E}$, or $\overline{UB}$/$\overline{LB}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns.
5. If both byte control signals are asserted, the two signals must have no more than 2 ns skew between them.
6. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.
7. All write cycle timings are referenced from the last valid address to the first transition address.

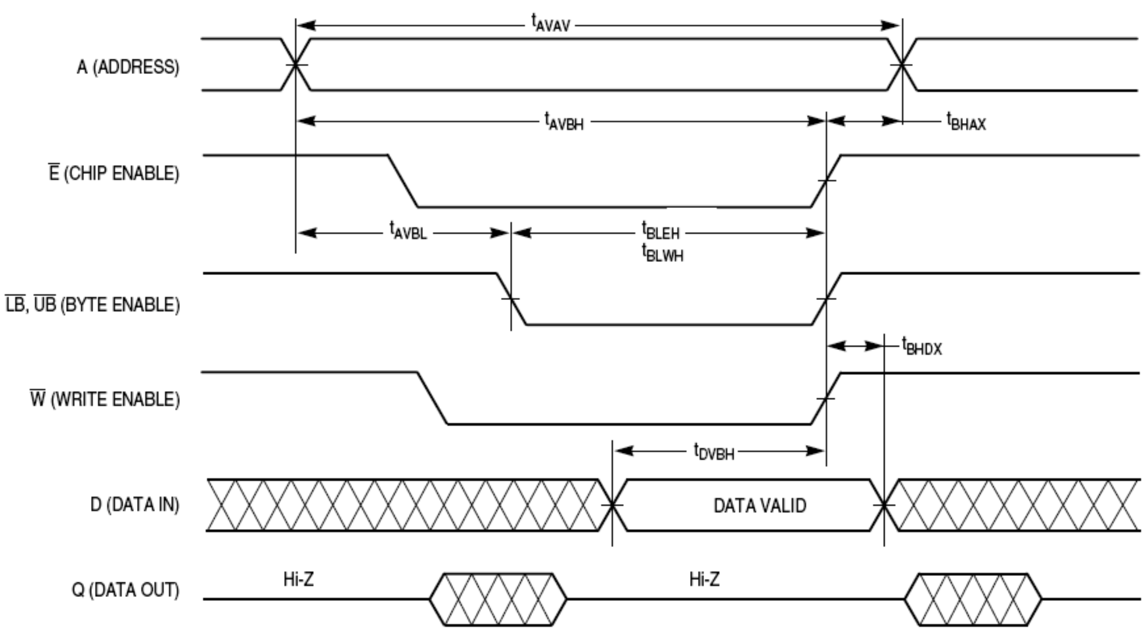
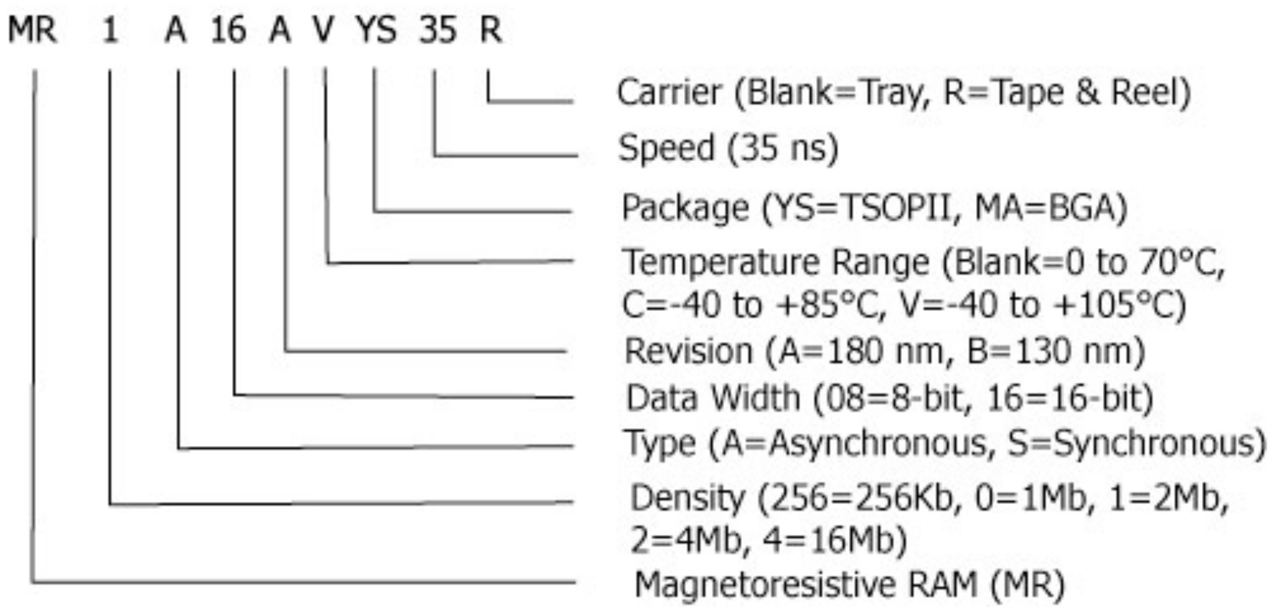


Figure 8. Write Cycle 3 ($\overline{LB}$/$\overline{UB}$ Controlled)

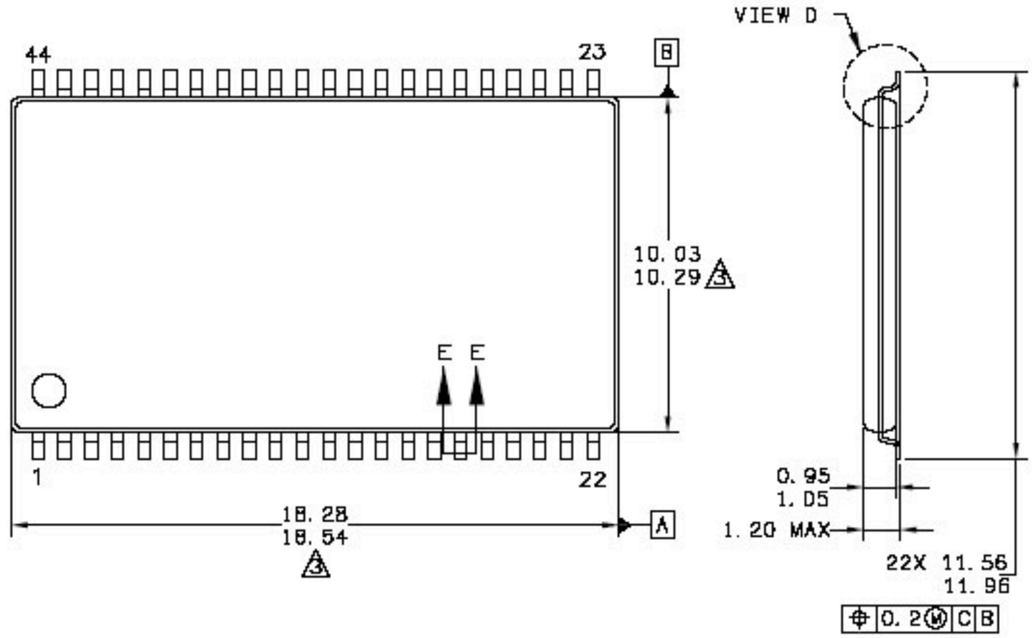
Ordering Information

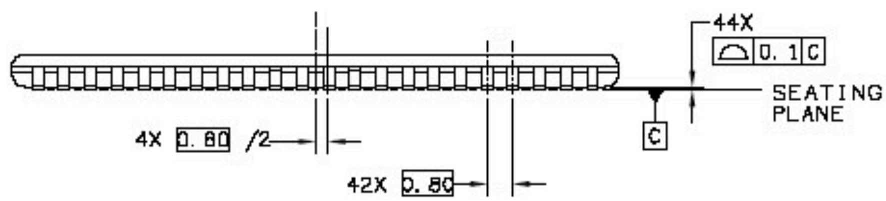
Part Numbering System

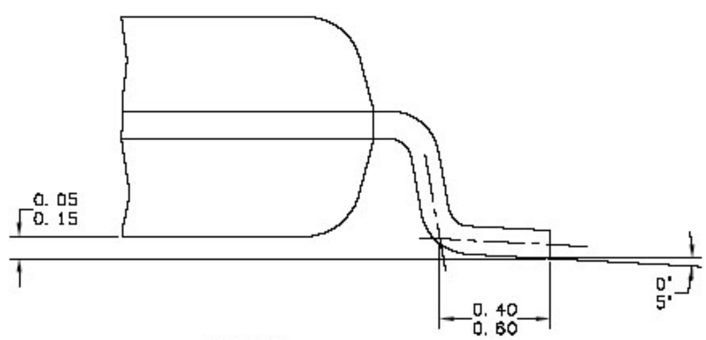


Part Number	Description	Temperature
MR1A16AYS35	3.3 V 128Kx16 MRAM 44-TSOP	Commercial
MR1A16ACYS35	3.3 V 128Kx16 MRAM 44-TSOP	Industrial
MR1A16AVYS35	3.3 V 128Kx16 MRAM 44-TSOP	Extended
MR1A16AYS35R	3.3 V 128Kx16 MRAM 44-TSOP T&R	Commercial
MR1A16ACYS35R	3.3 V 128Kx16 MRAM 44-TSOP T&R	Industrial
MR1A16AVYS35R	3.3 V 128Kx16 MRAM 44-TSOP T&R	Extended
MR1A16AMA35	3.3 V 128Kx16 MRAM 48-BGA	Commercial
MR1A16ACMA35	3.3 V 128Kx16 MRAM 48-BGA	Industrial
MR1A16AVMA35	3.3 V 128Kx16 MRAM 48-BGA	Extended

Mechanical Drawing (44-TSOP)

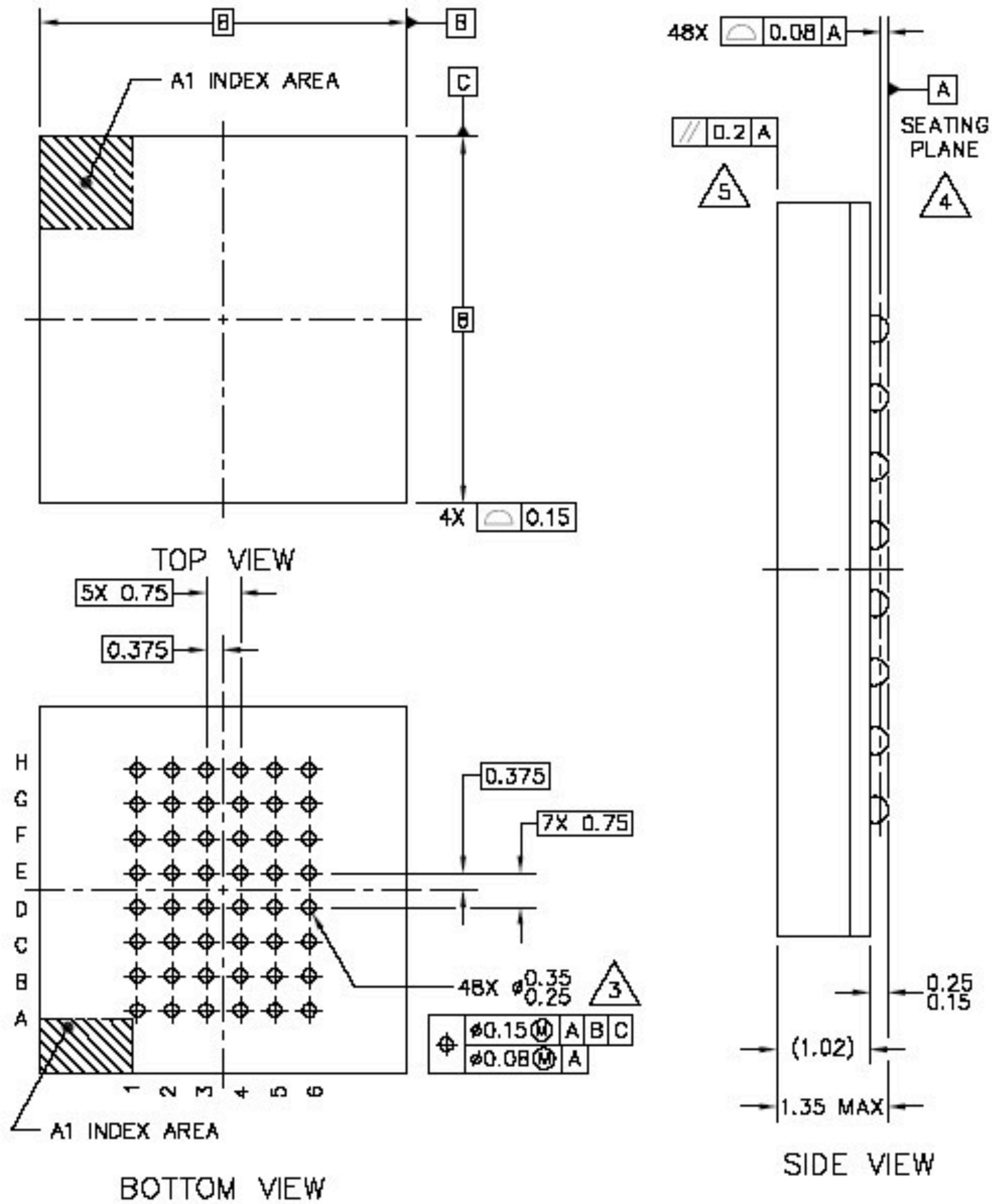






VIEW D
ROTATED 90° CW

Mechanical Drawing (48-BGA)



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Revision History

Revision	Date	Description of Change
1	August 10,2007	Initial Public Release Version
2	Sept 21, 2007	Table 6, Applied Values to TBD's in IDD Specifications
3	Nov 12, 2007	Table 2, Changed IDDA to IDDR or IDDW
4	Sep 12, 2008	Reformat Datasheet for EverSpin, Add BGA Packaging Information Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct I_{OH} spec of V_{OH} to -100 uA, Correct ac Test Conditions

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