128MB to 16GB
ATA PC Card

www.stec-inc.com

SLATAxxx(M/G)M1U(I)

Solid-State Memory Card
(No Moving Parts)

Capacity: 128MB - 16GB

ATA-5 Compatible

ATA Transfer modes:

- PIO 0-6, MWDMA 0-4
- PIO 0-6 only (for applications that require MWDMA access to be disabled)

Supports TrueIDE and PC Card Memory and I/O Modes

Form Factors:

- PC Card Type II

Endurance Guarantee of 2,000,000 Write/Erase Cycles

Card Information Structure (CIS) Programmed into 256 Bytes of Internal Memory

PC Card and Socket Services Release 2.1 or later compatible

5V or 3.3V Power Supply

Commercial and Industrial Operating Temperature Range

5-Byte Detection, 4-Byte Correction ECC Engine

10 Year Data Retention

RoHS-6 Compliant

5-Year Warranty

General Description

STEC's ATA PC Card is a small form factor memory card with no moving parts, available in capacities from 128MB to 16GB. The standard PC Card interface provides designers with a true plug-n-play storage device, allowing for short design cycles and fast time to market.

STEC's proprietary state-of-the-art flash memory controller is incorporated in the ATA PC Card, providing high data reliability and endurance. The built-in ECC engine can detect up to 5-byte errors and correct up to 4-byte errors, while sophisticated wear leveling algorithms guarantee 2,000,000 Write/Erase Cycles.

STEC's ATA PC Card is available in a PC Card Type II package.

STEC's ATA PC Card is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts, the STEC ATA PC Card is a reliable alternative to mechanical hard disk drives for mission critical applications.

Ordering Information

ATA PC Card

Part Number	CF Form Factor	Capacity
SLATA128MM1U(I)	Type II	128 Mbytes
SLATA256MM1U(I)	Type II	256 Mbytes
SLATA512MM1U(I)	Type II	512 Mbytes
SLATA1GM1U(I)	Type II	1 GByte
SLATA2GM1U(I)	Type II	2 GBytes
SLATA3GM1U(I)	Type II	3 GBytes
SLATA4GM1U(I)	Type II	4 GBytes
SLATA5GM1U(I)	Type II	5 GBytes
SLATA6GM1U(I)	Type II	6 GBytes
SLATA7GM1U(I)	Type II	7 GBytes
SLATA8GM1U(I)	Type II	8 GBytes
SLATA10GM1U(I)	Type II	10 GBytes
SLATA12GM1U(I)	Type II	12 GBytes
SLATA14GM1U(I)	Type II	14 GBytes
SLATA16GM1U(I)	Type II	16 GBytes

Legend:

- **(I) =** Industrial temperature range (-40ºC to +85 ºC).
- **Part numbers without (I) =** Commercial temperature range (0ºC to 70ºC).
- **(M/G)** indicates if proceeding capacity (xxx) is in Megabytes (M) or Gigabytes (G).
- **U =** RoHS-6 compliant lead-free.
- **-F** = media set to fixed storage for non-removable IDE applications. Use with operating systems, such as Windows XP, that require storage media to be identified as a fixed drive before it can be used as a bootable drive. Example: SLATAxxx(M/G)M1U(I)-F.
- **-P =** firmware programmed for PIO Modes 0-6 only for applications requiring MWDMA access to be disabled. Example: SLATAxxx(M/G)M1(T2)U(I)-P

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1.0 Product Specifications

1.1 Package Dimensions and Pin Locations

Table 1 and Figure 1show the mechanical dimensions of the PC Card Type II.

Table 1: Mechanical dimensions PC Card Type II

Parameter	Value
Length	85.60 ± 0.20 mm (3.370 ±. 0.008 in)
Width	54.00 ± 0.10 mm (2.126 ± 0.004 in)
Height (including label area)	5.00 mm (0.196 in) max

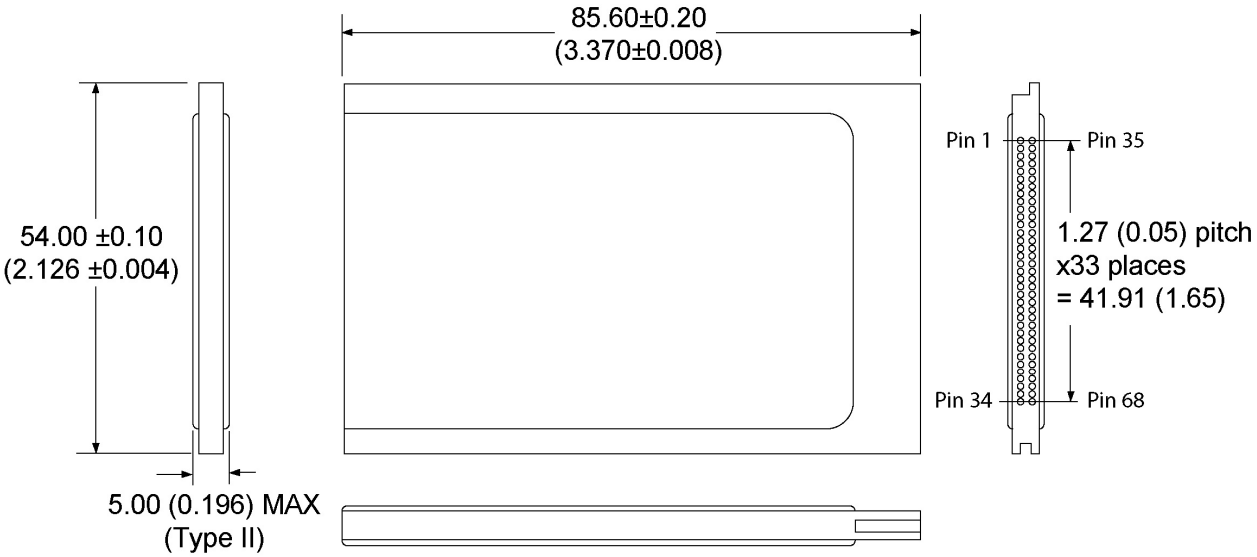

*Figure **1**: Mechanical dimensions PC Card Type II*

1.2 Pin Assignment

Table 2: ATA PC Card Pin Assignment

Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
1	GND	Ground	35	GND	Ground
2	D03	I/O	36	-CD1	O
3	D04	I/O	37	D11	I/O
4	D05	I/O	38	D12	I/O
5	D06	I/O	39	D13	I/O
6	D07	I/O	40	D14	I/O
7	-CE1	I	41	D15	I/O
8	A10	I	42	-CE2	I
9	-OE	I	43	-VS1	O
10	N/C		44	-IORD	I
11	A09	I	45	-IOWR	I
12	A08	I	46	N/C	
13	N/C		47	N/C	
14	N/C		48	N/C	
15	-WE	I	49	N/C	
16	RDY/-BSY, -IREQ, INTRQ	O	50	N/C	
17	VCC	Power	51	VCC	Power
18	N/C		52	N/C	
19	N/C		53	N/C	
20	N/C		54	N/C	
21	N/C		55	N/C	
22	A07	I	56	-CSEL	I
23	A06	I	57	-VS2	O
24	A05	I	58	RESET, -RESET	I
25	A04	I	59	-WAIT, IORDY	O
26	A03	I	60	-INPACK, DMARQ (not used for part numbers with P)	O
27	A02	I	61	-REG, -DMACK (not used for part numbers with P)	I
28	A01	I	62	BVD2, -SPKR, -DASP	I/O
29	A00	I	63	BVD1, -STSCHG, -PDIAG	I/O
30	D00	I/O	64	D08	I/O
31	D01	I/O	65	D09	I/O
32	D02	I/O	66	D10	I/O
33	WP, -IOIS16	O	67	-CD2	O
34	GND	Ground	68	GND	Ground

Legend: "-" = Low active

1.3 Signal Descriptions

Table 3: ATA PC Card Signal Descriptions

Signal Name	Type	Pin Number	Description
BVD2 (PC Card Memory Mode)	I/O	62	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product produces no audio.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	I/O	36, 67	These Card Detect pins are connected to ground on the card. They are used by the host to determine that the card is fully inserted into the socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same as Memory Mode.
-CD1, -CD2 (True IDE Mode)			These signals are not used in IDE Mode.
D15-D00 (PC Card Memory Mode)	I/O	37, 38, 39, 40, 41, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	These lines carry the data, commands, and host and the controller. D00 is the LSB of the LSB of the Odd Byte of the Word.
D15-D00 PC Card I/O Mode			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data onto the data bus and into the controller registers. The clocking occurs on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the ATA PC Card.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-WE (PC Card Memory Mode)	I	15	This is a signal driven by the host and used for strobing memory write data into the registers. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC.

Signal Name	Type	Pin Number	Description
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the ATA PC Card in PC Card Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-OE (True IDE Mode)			To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	16	In Memory Mode, this signal is set high when the ATA PC Card is ready to accept a new data transfer operation and held low when the ATA PC Card is busy. The host must provide a pull-up resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the ATA PC Card completes its power up or reset function. No access of any type should be made to the ATA PC Card during this time. The RDY/-BSY signal is held high (disabled from being busy) when the ATA PC Card is powered up with RESET continuously disconnected or asserted high.
-IREQ (PC Card I/O Mode)			After the ATA PC Card has been configured for I/O operation, this signal is used as the active low interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high interrupt request to the host.
A10-A0 (PC Card Memory Mode)	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	These address lines along with the -REG signal are used to select the following: the I/O port address registers within the ATA PC Card, the memory mapped port address registers within the ATA PC Card, a byte in the CIS and the Configuration Control and Status Registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE Mode)		27, 28, 29	In True IDE Mode only, A2:A0 are used to select the one of eight registers in the Task File. The remaining address lines should be grounded.
-CE1, -CE2 (PC Card Memory Mode Card Enable	I	7, 42	These input signals are used both to select the ATA PC Card and to indicate to the ATA PC Card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CE1, -CE2 (True IDE Mode)			In the True IDE Mode, -CE1 is the chip enable for the task file registers while -CE2 is used to select the Alternate Status Register and the ATA PC Card Control Register.

Signal Name	Type	Pin Number	Description
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This signal is used to configure this ATA PC Card as a Master or Slave. By default (ball not connected), the ATA PC Card is configured as a Master. To configure the ATA PC Card as a Slave, pull up ball to VCC through 0 to 470 ohm resistor.
-REG (PC Card Memory Mode) Attribute Memory Select	I	61	This signal distinguishes between accesses to Common Memory (high) and Register Attribute Memory (low).
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the bus.
-DMACK (not used for part numbers with P) (True IDE Mode)			In True IDE Mode this input signal is used by host in response to DMARQ to initiate DMA transfers.
WP (PC Card Memory Mode) Write Protect	O	33	The ATA PC Card does not have a write protect switch; therefore, this signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			Not defined in IDE Mode.
-INPACK (PC Card Memory Mode)	O	60	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the ATA PC Card when it is selected and responding to an I/O read cycle at the address that is on the bus. The host uses this signal to control the enable of any input data buffers between the ATA PC Card and the host's CPU.
DMARQ (Not used for part numbers with P) (True IDE Mode)			In True IDE Mode this signal is asserted by the ATA PC Card when it is ready to transfer data to/from the host. Data direction is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high as since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states. Its use is controlled by the Configuration and Status Register.
-PDIAG (True IDE Mode)			In True IDE Mode, this input/output signal is the Pass Diagnostic signal in the Master/Slave handshake protocol.

Signal Name	Type	Pin Number	Description
-WAIT (PC Card Memory Mode)	O	59	This signal is not used by the ATA PC Card, and is pulled up to VCC through a 4.7K ohm resistor.
-WAIT (PC Card I/O Mode)			This signal is not used by the ATA PC Card, and is pulled up to VCC through a 4.7K ohm resistor.
IORDY (True IDE Mode)			This signal is not used by the ATA PC Card, and is pulled up to VCC through a 4.7K ohm resistor.
GND (PC Card Memory Mode)	GND	1, 34, 35, 68	Ground
GND (PC Card I/O Mode)			Ground
GND (True IDE Mode)			Ground
VCC (PC Card Memory Mode)	VCC	17, 51	+5 V or 3.3V power
VCC (PC Card I/O Mode)			+5 V or 3.3V power
VCC (True IDE Mode)			+5 V or 3.3V power
RESET (PC Card Memory Mode)	I	58	When RESET is high, this signal resets the ATA PC Card. The ATA PC Card is reset only at power up if this signal is left high or open from power-up. The ATA PC Card can also be reset when the soft reset bit in the Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-VS1 *-VS2* (PC Card Memory Mode)	O	43, 57	-VS1 is grounded, and -VS2 is not connected so that the card CIS can be read at either 3.3 volts or 5.0 volts.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all models.
-VS1 -VS2 (True IDE Mode)			This signal is not used in IDE Mode.

1.4 Performance

Table 4: ATA PC Card Read/Write Performance

Parameter	Value
Data transfer rate to/from host	16.7 MBytes/s (burst)
Sustained read	up to 10 MBytes/s
Sustained write	up to 7 MBytes/s

1.5 CHS Parameters

Table 5: CHS Parameters per capacity

Capacity	Cylinder (C)	Head (H)	Sectors/Track (S)
128MB	980	8	32
256MB	980	16	32
512MB	993	16	63
1GB	1,986	16	63
2GB	3,970	16	63
4GB	7,964	16	63
5GB	10,038	16	63
6GB	12,046	16	63
7GB	14,054	16	63
8GB	16,062	16	63

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Table 6: ATA PC Card Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Commercial Operating Temperature	Ta	0	25	70	°C
Industrial Operating Temperature	Ta	-40	-	85	°C
VCC voltage	VCC	4.75	5.0	5.25	V
		3.18	3.3	3.465	V

2.2 Reliability

Table 7: ATA PC Card Endurance & Data Reliability

Parameter	Value
Endurance	2,000,000 Write/Erase Cycles
Data reliability	1 in 10^{14} bits, read
Data retention	10 years

2.3 Shock, Vibration, and Humidity

Table 8: ATA PC Card Shock, Vibration & Humidity

Parameter	Value
Shock	1K G, half-sine, 0.330 ms to 0.750 ms (per MIL-STD-202G Method 213B, Condition A)
Vibration	15 G 10Hz-2KHz (per MIL-STD-202G Method 204D 20 min/sweep, 12 sweeps/axis)
Humidity	85°C 95% RH, 5.5V, 500 hrs

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 9: ATA PC Card Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage	Vin, Vout	-0.5 to VCC +0.5	V
Storage temperature range	Tstg	-65 to +150	°C

3.2 DC Characteristics

Measurements at Recommended Operating Conditions unless otherwise specified.

Table 10: ATA PC Card DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VIL	Input LOW Voltage	-0.3	+0.8	V	VCC=3.3V or 5.0V
VIH	Input HIGH Voltage	2.0	VCC +0.3	V	VCC=3.3V or 5.0V
VOL	Output LOW Voltage		0.45	V	VCC=3.3V and IOL at 4mA
			0.8		VCC=5.0V and IOL at 4mA
VOH	Output HIGH Voltage	2.4		V	VCC=3.3V or 5.0V and IOH at 1mA
ICC	Sleep Mode		2	mA	ICC at VCC=3.3V or 5.0V
	Operating Current		75	mA	ICC at VCC=3.3V or 5.0V; Operating current measured with 2-way interleaving.
ILI	Input Leakage Current		10	µA	VCC=3.3V or 5.0V
ILO	Output Leakage Current		1	µA	VCC=3.3V
			2	µA	VCC= 5.0V
CI/O	Input/output Capacitance		25	pF	VCC=3.3V or 5.0V

3.3 AC Characteristics

Measurements at Recommended Operating Conditions, unless otherwise specified.

3.3.1 PC Card Memory Mode Attribute Memory Read

Table 11: PC Card Memory Mode Attribute Memory Read AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read Cycle Time	tc(R)	tAVAV	250	
Address Access Time	ta(A)	tAVQV		250
Card Enable Access Time	ta(CE)	tELQV		250
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from -CE	tdis(CE)	tEHQZ		100
Output Disable Time from -OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from -CE	ten(CE)	tELQNZ	5	
Output Enable Time from -OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Hold Time	th(A)	—	20	
-CE Setup Time	tsu(CE)	—	0	
-CE Hold Time	th(CE)	—	20	

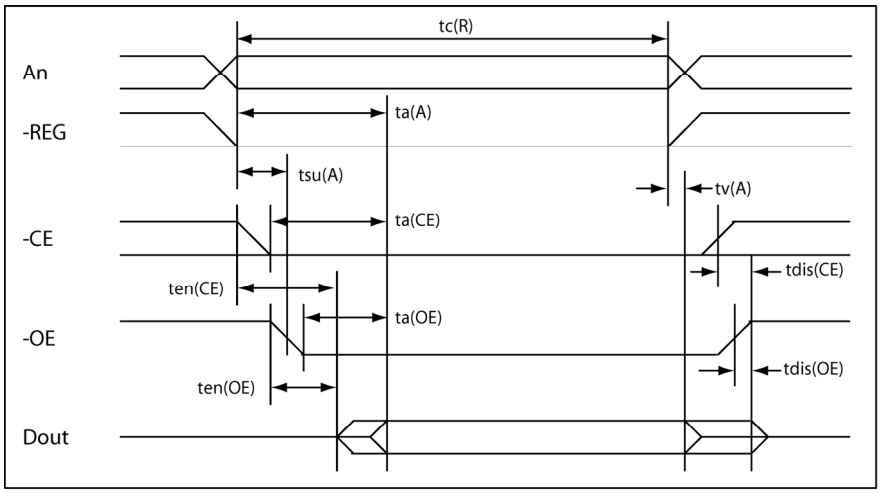

Figure 2: PC Card Memory Mode Attribute Memory Read Timing Diagram

3.3.2 PC Card Memory Mode Attribute Memory Write

Table 12: PC Card Memory Mode Attribute Memory Write AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Address Setup Time (-WE)	tsu(A-WEH)	—	180	
-CE Setup Time (-WE)	tsu(CE-WEH)	—	180	
Data Setup Time (-WE)	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Output Disable Time (-WE)	tdis(WE)	—		100
Output Disable Time (-OE)	tdis(OE)	—		100
Output Enable Time (-WE)	ten(WE)	—	5	
Output Enable Time (-OE)	ten(OE)	—	5	
Output Enable Setup Time (-WE)	tsu(OE-WE)	—	10	
Output Enable Hold Time (-WE)	th(OE-WE)	—	10	
-CE Setup Time	tsu(CE)	—	0	
-CE Hold Time	th(CE)	—	20	

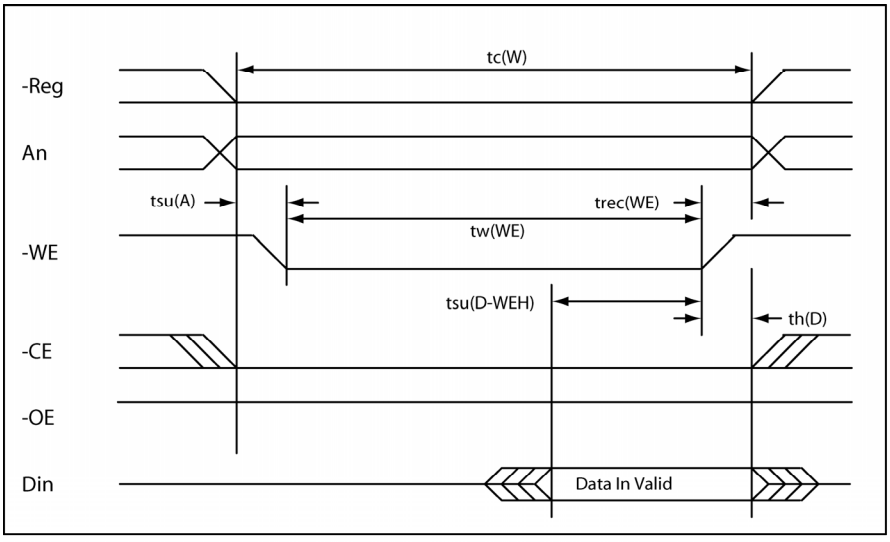

Figure 3: PC Card Memory Mode Attribute Memory Write Timing Diagram

3.3.3 PC Card Memory Mode Common Memory Read

Table 13: PC Card Memory Mode Common Memory Read AC Characteristics

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		N/A
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		N/A
Wait Width Time	tw(WT)	tWTLWTH		350		350		350		N/A

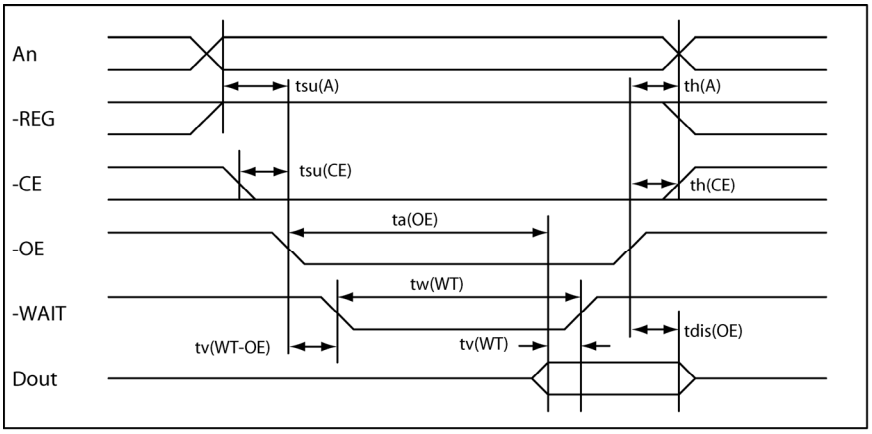

Figure 4: PC Card Memory Mode Common Memory Read Timing Diagram

3.3.4 PC Card Memory Mode Common Memory Write

Table 14: PC Card Memory Mode Common Memory Write AC Characteristics

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		15	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35		35		35		N/A
WE High from Wait Release	tv(WT)	tWTHWH	0		0		0		N/A	
Wait Width Time	tw(WT)	wWTLWTH		350		350		350		N/A

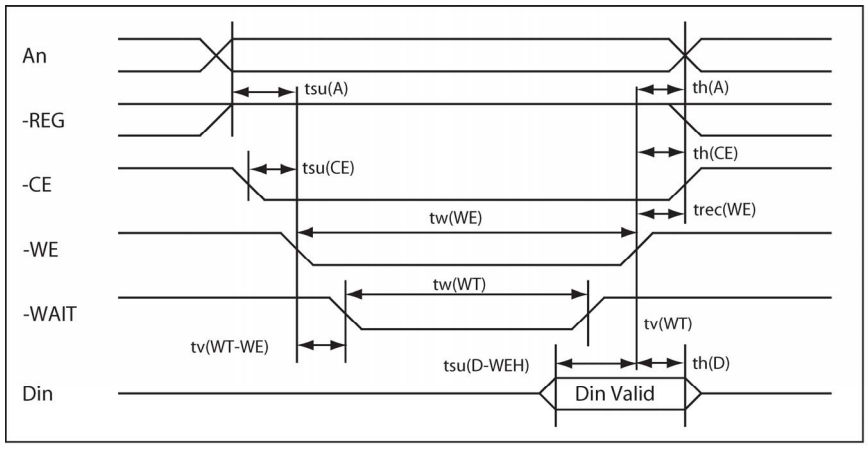

Figure 5: PC Card Memory Mode Common Memory Write Timing Diagram

3.3.5 PC Card I/O Mode Read AC Characteristics

Table 15: PC Card I/O Mode Read AC Characteristics

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after -IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following -IORD	th(IORD)	tIGHQX	0		5		5		5	
-IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before -IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following -IORD	thA(IORD)	tIGHAX	20		10		10		10	
-CE Setup before -IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
-CE Hold following -IORD	thCE(IORD)	tIGHEH	20		10		10		10	
-REG Setup before -IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
-REG Hold following -IORD	thREG(IORD)	tIGHRGH	0		0		0		0	

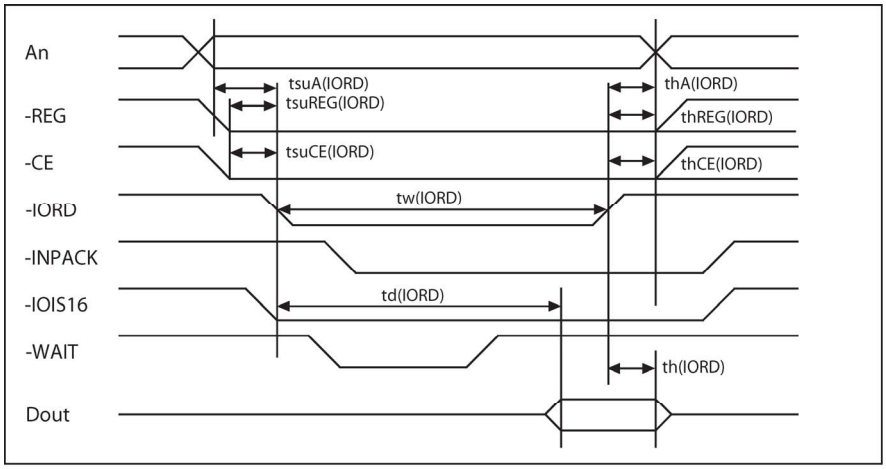

Figure 6: PC Card I/O Mode Read Timing Diagram

3.3.6 PC Card I/O Mode Write AC Characteristics

Table 16: PC Card I/O Mode Write AC Characteristics

Cycle Time Mode			250 ns		120 ns		100 ns		80 ns	
Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before -IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following -IOWR	th(IOWR)	tIWHDX	30		10		5		5	
-IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before -IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following –IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
-CE Setup before -IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
-CE Hold following -IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
-REG Setup before -IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
-REG Hold following -IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	

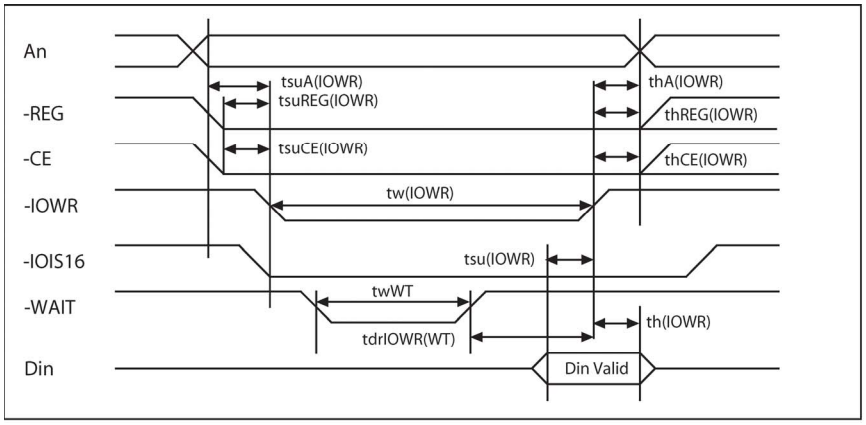

Figure 7: PC Card I/O Mode Read Timing Diagram

3.3.7 True IDE Mode Register Access

Table 17: True IDE Mode Register Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release (max)	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

3.3.8 True IDE Mode PIO Access

Table 18: True IDE Mode PIO Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

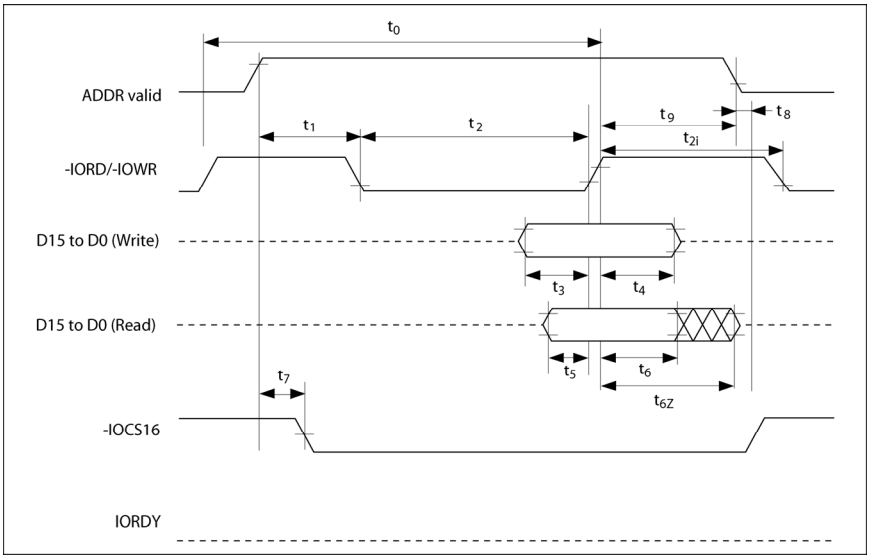

Figure 8: True IDE Mode PIO Access Timing Diagram

3.3.9 True IDE Mode Multiword DMA (not used for part numbers with P)

Table 19: True IDE Mode Multiword DMA AC Characteristics

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min)	t_0	480	150	120	100	80	ns
-IORD/-IOWR Asserted Pulse (min)	t_D	215	80	70	65	55	ns
-IORD data access (max)	t_E	150	60	50	50	45	ns
-IORD data hold (min)	t_F	5	5	5	5	5	ns
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10	ns
-IOWR data hold (min)	t_H	20	15	10	5	5	ns
DMACK to -IORD/-IOWR setup (min)	t_I	0	0	0	0	0	ns
-IORD/-IOWR to DMACK hold (min)	t_J	20	5	5	5	5	ns
-IORD negated pulse width (max)	t_{KR}	50	50	25	25	20	ns
-IOWR negated pulse width (min)	t_{KW}	215	50	25	25	20	ns
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35	ns
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35	ns

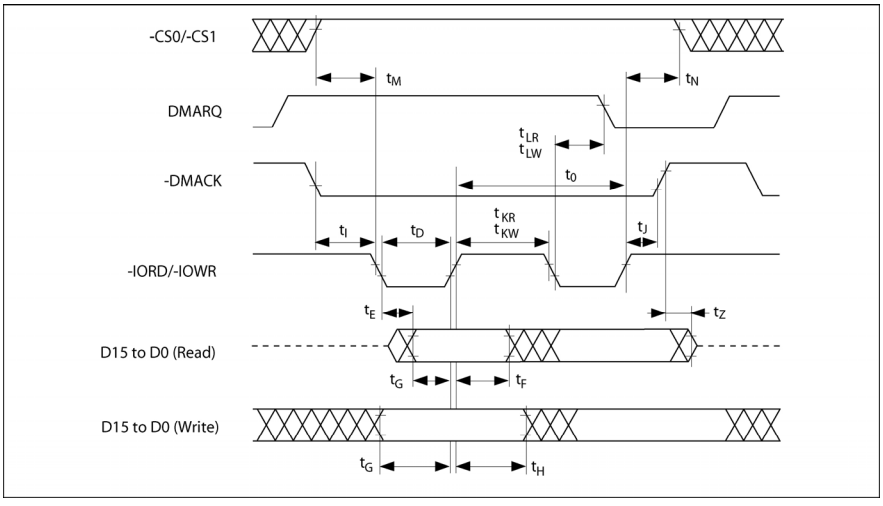

Figure 9: True IDE Mode Multiword DMA Timing Diagram

4.0 Host Access Specification

4.1 Task File Register and Byte/Word/Odd-Byte Mode Mappings

Please refer to the ATA PC Card standards for complete details on:

- Task File Register mapping for the interface modes
- Byte/Word/Odd-byte mode mapping within each of the interface modes

4.2 Host Access Interface Modes

The host can access the ATA PC Card by using the following interface modes with the Task Registers:

- *PC Card Memory Mode, Attribute Memory*
  The Card Information Structure (CIS) in Attribute Memory can be accessed by Byte/Word/Odd-byte modes in PC Card Memory Mode. The -REG signal must be asserted when accessing Attribute Memory. The ATA PC Card is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register. An example of a CIS is listed in *4.3, Card Information Structure (CIS).*

- *PC Card Memory Mode, Common Memory*.
  Common Memory can be accessed in the Byte/Word/Odd Byte modes in PC Card Memory Mode. The -REG signal must be de-asserted when accessing the Common Memory. The ATA PC Card is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register

- *PC Card I/O Mode*
  The ATA PC Card can be accessed by Byte/Word/Odd Byte modes in PC Card I/O Mode. The ATA PC Card is mapped to PC Card I/O Mode by the Index bits in the Configuration Option Reister. The Index bits also select Contiguous I/O, Primary I/O, or Secondary I/O mapping when using the PC Card I/O Mode.

- *True-IDE mode* with ATA Transfer Modes PIO 0-6 and MWDMA 0-4 (PIO 0-6 only for part numbers with P).
  The ATA PC Card is configured in a True IDE Mode of operation when the -OE input signal is asserted GND by the host at power up. In the True IDE Mode, Attribute Registers are not accessible from the host. The Data Register is accessed in word (16-bit) mode at power up. The ATA PC Card permits 8-bit accesses if the host issues a Set Feature Command to put the ATA PC Card in 8-bit mode. Parameter information that the ATA PC Card uses in True IDE mode is returned when the Identify Drive command (ECh) is invoked. Refer to *4.4*, *Identify Drive Parameter Information* for an example.

4.3 Card Information Structure (CIS)

The ATA PC Card uses a Card Information Structure (CIS) as outlined in the Table 20.

Table 20: Card Information Structure

0000: Code 01, link 03
D9 01 FF
Tuple CISTPL_DEVICE (01), length 3 (03) at offset 0
Device type is FUNCSPEC
Device speed is 250ns
Write protect switch is not in control
Device size is 2K bytes
0005: Code 1C, link 04
03 D9 01 FF
Tuple CISTPL_DEVICE_OC (1C), length 4 (04) at offset 5
Device conditions: minimum cycle with WAIT at Vcc = 3.3V
Device type is FUNCSPEC
Device speed is 250ns
Write protect switch is not in control
Device size is 2K bytes
000B: Code 18, link 02
DF 01
Tuple CISTPL_JEDEC_C (18), length 2 (02) at offset B
Device 0 JEDEC id: Manufacturer DF, ID 01
000F: Code 20, link 04
4D 01 00 01
Tuple CISTPL_MANFID (20), length 4 (04) at offset F
Manufacturer # 0x014D hardware rev 1.00
0015: Code 15, link 13
04 01 53 54 49 00 46 6C 61 73 68 20 37 2E 30 2E 30 00 FF
Tuple CISTPL_VERS_1 (15), length 19 (13) at offset 15
Major version 4, minor version 1
Product Information:
Manufacturer: "STI"
Product name: "Flash X.Y.Z"

002A: Code 21, link 02
04 01
Tuple CISTPL_FUNCID (21), length 2 (02) at offset 2A
Function code 04 (Fixed Disk), system init 01
002E: Code 22, link 02
01 01
Tuple CISTPL_FUNCE (22), length 2 (02) at offset 2E
This is an PC Card ATA Disk
0032: Code 22, link 03
02 0C 0F
Tuple CISTPL_FUNCE (22), length 3 (03) at offset 32
Vpp is not required
This is a silicon device
Identify Drive Model/Serial Number is guaranteed unique
Low-Power Modes supported: Sleep Standby Idle
Drive automatically minimizes power
All modes include 3F7 or 377
Index bit is not supported
-IOIS16 is unspecified in Twin configurations
0037: Code 1A, link 05
01 03 00 02 0F
Tuple CISTPL_CONFIG (1A), length 5 (05) at offset 37
Last valid configuration index is 3
Configuration Register Base Address is 200
Configuration Registers Present:
Configuration Option Register at 200
Card Configuration and Status Register at 202
Pin Replacement Register at 204
Socket and Copy Register at 206

003E: Code 1B, link 08
C0 C0 A1 01 55 08 00 20
Tuple CISTPL_CFTABLE_ENTRY (1B), length 8 (08) at offset 3E
Configuration Table Index is 00 (default)
Interface type is Memory
BVDs not active, WP not active, RdyBsy active
Wait signal support required
Vcc Power Description:
Nom V = 5.0 V
map 2048 bytes of memory to ATA PC Card address 0
Miscellaneous Features:
Max Twins 0, -Audio, -ReadOnly, +PowerDown
0048: Code 1B, link 06
00 01 21 B5 1E 4D
Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 48
Configuration Table Index is 00
Vcc Power Description:
Nom V = 3.30 V
Peak I = 45.0 mA
0050: Code 1B, link 0A
C1 41 99 01 55 64 F0 FF FF 20
Tuple CISTPL_CFTABLE_ENTRY (1B), length10 (0A) at offset 50 10 (0A) at offset 50
Configuration Table Index is 01 (default)
Interface type is I/O
BVDs not active, WP not active, RdyBsy active
Wait signal support not required
Vcc Power Description:
Nom V = 5.0 V
Decode 4 I/O lines, bus size 8 or 16
IRQ may be shared, pulse and level mode interrupts are supported
Interrupts in mask FFFF are supported
Miscellaneous Features:
Max Twins 0, -Audio, -ReadOnly, +PowerDown
Configuration Table Index is 01 (default)

005C: Code 1B, link 06
01 01 21 B5 1E 4D
Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 5C
Configuration Table Index is 01
Vcc Power Description:
Nom V = 3.30 V
Peak I = 45.0 mA
0064: Code 1B, link 0F
C2 41 99 01 55 EA 61 F0 01 07 F6 03 01 EE 20
Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 64
Configuration Table Index is 02 (default)
Interface type is I/O
BVDs not active, WP not active, RdyBsy active
Wait signal support not required
Vcc Power Description:
Nom V = 5.0 V
Decode 10 I/O lines, bus size 8 or 16
I/O block at 01F0, length 8
I/O block at 03F6, length 2
IRQ may be shared, pulse and level mode interrupts are supported
Only IRQ14 is supported
Miscellaneous Features:
Max Twins 0, -Audio, -ReadOnly, +PowerDown
Max Twins 0, -Audio, -ReadOnly, +PowerDown
Interface type is I/O
BVDs not active, WP not active, RdyBsy active
Wait signal support not required
Vcc Power Description:
0075: Code 1B, link 06
02 01 21 B5 1E 4D
Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 75
Configuration Table Index is 02
Vcc Power Description:
Nom V = 3.30 V
Peak I = 45.0 mA

007D: Code 1B, link 0F
C3 41 99 01 55 EA 61 70 01 07 76 03 01 EE 20
Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 7D
Configuration Table Index is 03 (default)
Interface type is I/O
BVDs not active, WP not active, RdyBsy active
Wait signal support not required
Vcc Power Description:
Nom V = 5.0 V
Decode 10 I/O lines, bus size 8 or 16
I/O block at 0170, length 8
I/O block at 0376, length 2
IRQ may be shared, pulse and level mode interrupts are supported
Only IRQ14 is supported
Miscellaneous Features:
Max Twins 0, -Audio, -ReadOnly, +PowerDown

008E: Code 1B, link 06
03 01 21 B5 1E 4D
Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 8E
Configuration Table Index is 03
Vcc Power Description:
Nom V = 3.30 V
Peak I = 45.0 mA
0096: Code 14, link 00
Tuple CISTPL_NO_LINK (14), length 0 (00) at offset 96
0098: Code FF
Tuple CISTPL_END (FF) at offset 98

4.4 Identify Drive Parameter Information

An example of the parameter information received from the ATA PC Card when invoking the Identify Drive command (ECh) is listed in Table 21 below.

Table 21: Identify Drive Parameter Information

Word Address	Data	Total Bytes	Description
0	848AH	2	Value fixed by CFA (value=044AH for part numbers with F suffix)
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per track
5	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 - 8	XXXXH	4	Number of sectors per ATA PC Card (word 7 = MSW, word 8 = LSW)
9	0000H	2	Reserved
10 - 19	Unique per card	20	Serial Number in ASCII (40 characters): STEC Proprietary (9 characters) Yr Day Hr Min Sec xxxxxxxxx yy ddd hh mm ss
20	XXXXH	2	Do not use this word. Before retirement, was buffer type
21	XXXXH	2	Do not use this word. Before retirement, was buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23 - 26	See description	8	Firmware revision in ASCII (8 characters): Rev8.0.0 52 65 76 38 2E 30 2E 30 hex
27 - 46	See description	40	Model Number in ASCII (40 characters): STI Flash 8.0.0 <left justified> 53 54 49 20 46 6C 61 73 68 20 38 2E 30 2E 30 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 hex
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0300H	2	DMA supported, LBA supported (0200H DMA not supported, LBA supported for part numbers with P)
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single word DMA data transfer cycle timing mode (not supported)
53	0003h	2	Words 54 - 58 and 64 - 70 are valid
54	XXXXH	2	Number of Current Cylinders
55	XXXXH	2	Number of Current Heads
56	XXXXH	2	Number of Current Sectors Per Track
57	XXXXH	2	LSW of the Current Capacity in Sectors
58	XXXXH	2	MSW of the Current Capacity in Sectors
59	010XH	2	Current Setting for Block Count=1 for R/W Multiple commands
60 - 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not supported
63	0407H	2	Multiword DMA modes supported (0000H Multiword DMA modes not supported for part numbers with P)
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum multiword DMA transfer cycle time per word (ns) (0000H for part numbers with P)
66	0078H	2	Recommended multiword DMA transfer cycle time per word (ns) (0000H for part numbers with P)
67	0078H	2	Minimum PIO transfer without flow control
68	0078H	2	Minimum PIO transfer with IORDY flow control
69 - 255	0000H	374	Reserved
XXXXH = These values depend on the specific ATA PC Card.			

5.0 Registers

This chapter lists the registers of the ATA PC Card. Refer to ATA PC Card standards for further details.

5.1 Configuration Registers

In PC Card Mode, four configuration registers, as listed in Table 22, are used.

Note: In True IDE Mode, these registers cannot be used.

Table 22: Configuration Registers

Configuration Register	Description
Configuration Option Register	This register is used to configure and observe the status of the ATA PC Card, and to issue soft resets to it. Also, the Index bits of this register are used to select the PC Card mapping mode that the ATA PC Card uses: 1) PC Card Memory, 2) PC Card Contiguous I/O, 3).PC Card Primary I/O, and 4) PC Card Secondary I/O
Configuration and Status Register	This register is used for observing the ATA PC Card state.
Pin Replacement Register	This register is used for providing the signal state of -IREQ when the ATA PC Card is configured in the PC Card I/O Mode.
Socket and Copy Register.	This read/write register is used to identify the ATA PC Card from other devices. This register should be set by the host before this Configuration Option register is set.

5.2 Task File Registers

Table 23: ATA PC Card Task File Registers

Task File Register	Description
Data Register	The Data Register is a 16-bit read/write register used for transferring data between the ATA PC Card and the host. This register can be accessed in word mode and byte mode.
Error Register	The Error Register is a read-only register that is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to “0” (Ready). Diagnostic Codes are returned in the Error Register after a Execute Drive Diagnostic command (code 90h). Extended Error Codes returned in the Error Register after an Request Sense command (code 03h).
Sector Count Register	This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the ATA PC Card. If the value in the register is 0, a count of 256 sectors is indicated.
Sector Number Register	When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.
Cylinder Low Register	In CHS mode (LBA=0), this register contains the low-order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.
Cylinder High Register	In CHS mode (LBA=0), this register contains the high-order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.
Drive/Head Register	This register selects the ATA PC Card address translation (CHS or LBA) and provides head address (CHS) or high-order address bits 27:24 for LBA.
Status Register	This read-only register indicates status of a command execution. When the BSY bit is “0”, the other bits are valid; when the BSY bit is “1”, the other bits are not valid. When the register is read, the interrupt pin, is cleared.
Alternate Status Register	This register is the same as the Status register, except that is not negated when the register is read.
Device Control Register	This write-only register is used for controlling the interrupt request and issuing an ATA soft reset to the ATA PC Card.
Drive Address Register	This read-only register is used for confirming the ATA PC Card’s status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host’s I/O space because of potential conflicts on bit 7.
Command Register	This write-only register is used for writing the command that executes the ATA PC Card’s operation. The command code is written in the command register after its parameters are written in the Task File during the ATA PC Card ready state.

6.0 Supported ATA Commands

The ATA commands used by the ATA PC Card are listed in Table 24 below. Refer to ATA PC Card standards for details.

Table 24: ATA PC Card Supported ATA Commands

Command Set	Code	Description
Check Power Mode	E5h or 98h	This command checks the power mode.
Execute Drive Diagnostic	90h	This command performs the internal diagnostic tests implemented by the ATA PC Card. The Diagnostic Code is returned in the Error Register.
Erase Sector(s)	C0h	This command is used to pre-erase and condition data sectors in advance.
Format Track	50h	This command writes the desired head and cylinder of the selected drive with a vender unique data pattern (typically 00h or FFh). This ATA PC Card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.
Identify Drive	ECh	This command lets the host receive parameter information from the ATA PC Card in the same protocol as Read Sector(s) command.
Idle	E3h or 97h	This command causes the ATA PC Card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
Idle Immediate	E1h or 95h	This command causes the ATA PC Card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt.
Initialize Drive Parameters	91h	This command enables the host to set the number of sectors per track and the number of heads per cylinder.
NOP	00h	No Operation.
Read Buffer	E4h	This command enables the host to read the current contents of the ATA PC Card's sector buffer.
Read DMA (Not used for part numbers with P)	C8h	This command is the sector read command used for Multiword DMA transfer.
Read Multiple	C4h	This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Read Long Sector	22h or 23h	This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
Read Sector(s)	20h (w/ retry) 21h (w/o retry)	This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

Command Set	Code	Description
Read Verify Sector(s)	40h (w/ retry) 41h (w/o retry	This command verifies one or more sectors on the ATA PC Card by transferring data from the flash media to the data buffer in the ATA PC Card and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
Recalibrate	1Xh	The ATA PC Card performs only the interface timing and register operations. When this command is issued, the ATA PC Card sets BSY and waits for an appropriate length of time, after which it clears BSY and issues an interrupt. When this command ends normally, the ATA PC Card is initialized.
Request Sense (Extended Error)	03h	This command requests an extended error code after a command ends with an error. The extended error code is returned in the Error Register
Seek	7Xh	This command is effectively a NOP command to the ATA PC Card although it does perform a range check.
Set Features	EFh	This command is used by the host to establish or select certain features.
Set Multiple Mode	C6h	This command enables the ATA PC Card to perform multiple read and write operations and establishes the block count for these commands.
Set Sleep Mode	E6h or 99h	This is the only command that allows the host to set the ATA PC Card into Sleep mode. When the ATA PC Card is set to sleep mode, the ATA PC Card clears the BSY line and issues an interrupt. The ATA PC Card enters sleep mode and the only method to make the ATA PC Card active again (back to normal operation) is by performing a hardware reset or a software reset.
Stand By	E2h or 96h	This command sets the ATA PC Card in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the ATA PC Card returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.
Stand By Immediate	E0h or 94h	This command causes the ATA PC Card to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
Translate Sector	87h	This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.
Wear Level	F5h	This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.
Write Buffer	E8h	This command enables the host to overwrite the contents of the ATA PC Card's sector buffer with any data pattern desired.
Write DMA (Not used for part numbers with P)	CAh	This command is the sector write command used for Multiword DMA transfer.

Command Set	Code	Description
Write Long Sector	32h or 33h	This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
Write Multiple	C5h	This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
Write Multiple w/o Erase	CDh	This command is similar to the Write Multiple command, except that an implied erase before the write operation is not performed. ***Note:*** *Before using this command, it is required to erase the respective sectors using the Erase Sectors command*
Write Sector(s)	30h (w/ retry) 31h (w/o retry)	This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
Write Sector(s) w/o Erase	38h	This command is similar to the Write Sector(s) command, except that an implied erase before the write operation is not performed. ***Note***: *Before using this command, it is required to erase the respective sectors using the Erase Sectors command*.
Write Verify	3Ch	This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

7.0 Revision History

Revision	*Date*	*Description*
-101	11/17/06	Product release.
-102	12/11/06.	P option added to Ordering Information Legend. Where MWDMA is documented, it is noted that N/A to part numbers with P.
-103	12/14/06	ID file Serial Number, Firmware Revision, and Model Number corrected in table.
-104	1/16/07	Logo updated. Disclaimer updated. Contact Information added.

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