Intel® Z-P140 PATA Solid State Drive

SSDPAPS0002G1, SSDPAPS0004G1

Product Manual

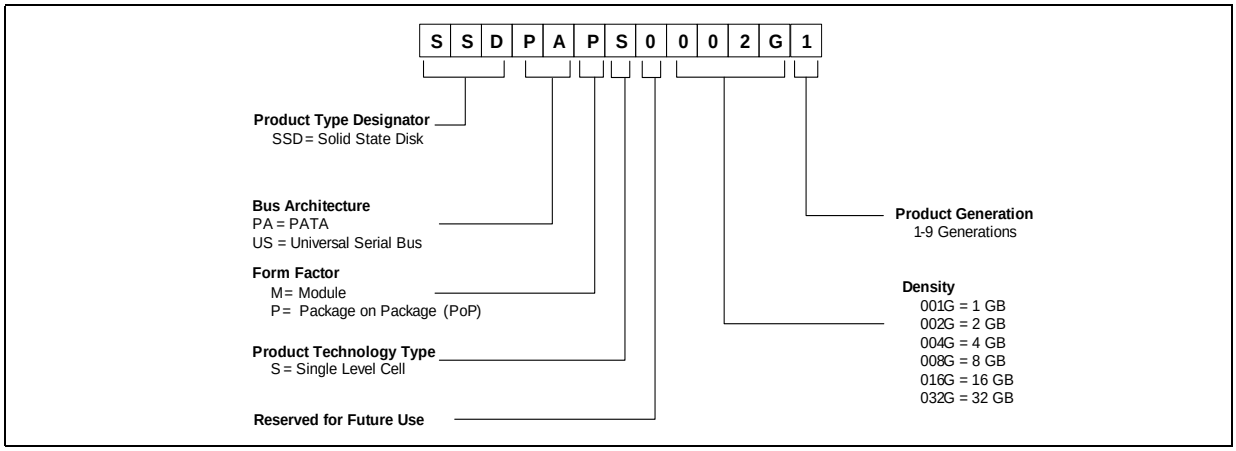
Product Features

- Capacities
  - — 2 GB (extensible to 4 GB using Intel SD54B NAND Flash Memory components)
  - — 4 GB (extensible to 16 GB using Intel SD58B NAND Flash Memory components)
- PATA Compatibility
  - — ATA-5 compatible
  - — PIO Mode 0-4 supported
  - — MWDMA Mode 0-2 supported
  - — UDMA Mode 0-4 supported
- Performance (SLC components)
  - — Sustained Sequential Read Bandwidth: 38 MB/s (TYP)
  - — Sustained Sequential Write Bandwidth: 29 MB/s (TYP)
- PATA Controller Flash Memory Interface
  - — Four Integrated 512 Byte buffers
  - — Dual Channel Flash Interface
  - — Flash Memory Power Down Logic
  - — Flash Memory Write Protect
- Form Factor: Package On Package Technology
  - — Total Package Volume: 12 x 18 x 1.8 mm
  - — Top NAND Package: 12 x 18 x 1.39 mm, using a 122 Ball Grid Array (BGA)
  - — Bottom PATA Controller: 12 x 12 mm, using a 168 Ball Grid Array (BGA)
- Compliances
  - — Halogen free
  - — Lead free
  - — RoHS
- Power Supply Voltage: 3.3 V
- Power Consumption (Vcc=3.3 V)
  - — SD54B Package on Package
    - • Standby: 340 µA; 1.12 mW (TYP)
    - • Active: 145 mA; 479 mW (TYP)
  - — SD58B Package on Package
    - • Standby: 385 µA; 1.27 mW (TYP)
    - • Active: 165 mA; 545 mW (TYP)
- Power Control Features
  - — Automatic Power down during wait periods
  - — Automatic Sleep Mode during host inactivity
- Power Loss Protection: both hardware and software help prevent data corruption in the event of a power down during a write cycle
- Operating Temperature
  - — SSDPAPS0002G1, PF29F16G32PANC1: $0^{o}C$ to $70^{o}C$
  - — SSDPAPS0004G1, PF29F32G32PANC1: $-40^{o}C$ to $85^{o}C$
- Non-operating: $-65^{o}C$ to $150^{o}C$
- Shock (Operating and non-operating): 1,500 G/0.5 ms
- Vibration: 3.13 G, 5-500 Hz
- NAND Management
  - — Error Correction Code (ECC): 4 symbol
  - — Active wear leveling algorithm (static and dynamic)
- Reliability
  - — Mean Time Between Failure (MTBF) 2,500,000 Hours
  - — 5 Years Useful Life

Order Number: 317505-003US
October 2008

Ordering Information

Intel Solid State Drive Decoder



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Intel Z-P140 PATA Solid State Drive Ordering Information

Part Number	MM# Tape & Reel (1000 Pieces)	MM # Tray Media (1 Piece)	Device Nomenclature
SSDPAPS0002G1	893478	893479	Intel PATA Value Solid State Drive, 2 GB, Package on package (PoP), Single-level cell (SLC)
SSDPAPS0004G1	893476	893477	Intel PATA Value Solid State Drive, 4 GB, Package on package (PoP), Single-level cell (SLC)
PF29F16G32PANC1	893459	893458	Intel NAND Flash Memory SD54B 16 Gb, x32, 3 V, Ball grid array (BGA)
PF29F32G32PANC1	893457	893460	Intel NAND Flash Memory SD58B 32 Gb, x32, 3 V, Ball grid array (BGA)

Contents

October 2008
Order Number: 318890-003US

1.0 Overview

The Intel® Z-P140 PATA Solid-State Drive (SSD) is an ultra-small, complete solution for mobile computing, digital entertainment, and embedded applications, offering low power, high-performance, and durability. Using the industry standard PATA (IDE) interface, the Intel Z-P140 PATA SSD delivers the storage capacity and performance to accelerate the trend towards greater mobility. Specifically designed to meet small form factor requirements, the Intel Z-P140 is an ideal solution for next generation mobile computing.

Using the standard PATA interface, chip-scale package-on-package (PoP) technology, and a form-factor significantly smaller than hard-disk drives, the Intel Z-P140 enables smaller industrial designs. With 2GB and 4GB capacities—expandable to 16GB—the Intel Z-P140 comfortably stores most computing or embedded operating systems, applications, and data, meeting mainstream capacity requirements for most ultra-mobile devices. Solid-state disk technology delivers fast boot, load, and execution of applications, with no moving parts, leading to faster system responsiveness, durability, and longer battery life.

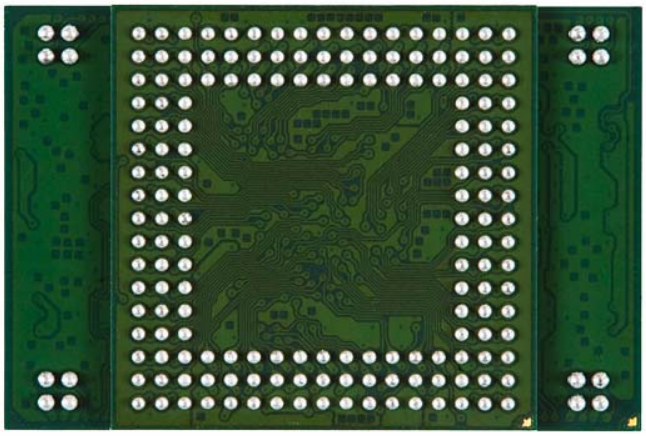
1.1 Product Overview

Offering flexible capacity of either 2 GB and 4 GB, the Intel Z-P140 PATA Solid State Drives (SSDs) utilize a stacked PoP configuration combining a Parallel Advanced Technology Attachment (PATA) controller with Intel high performance NAND Flash Memory for a compact, cost effective high performance SSD.

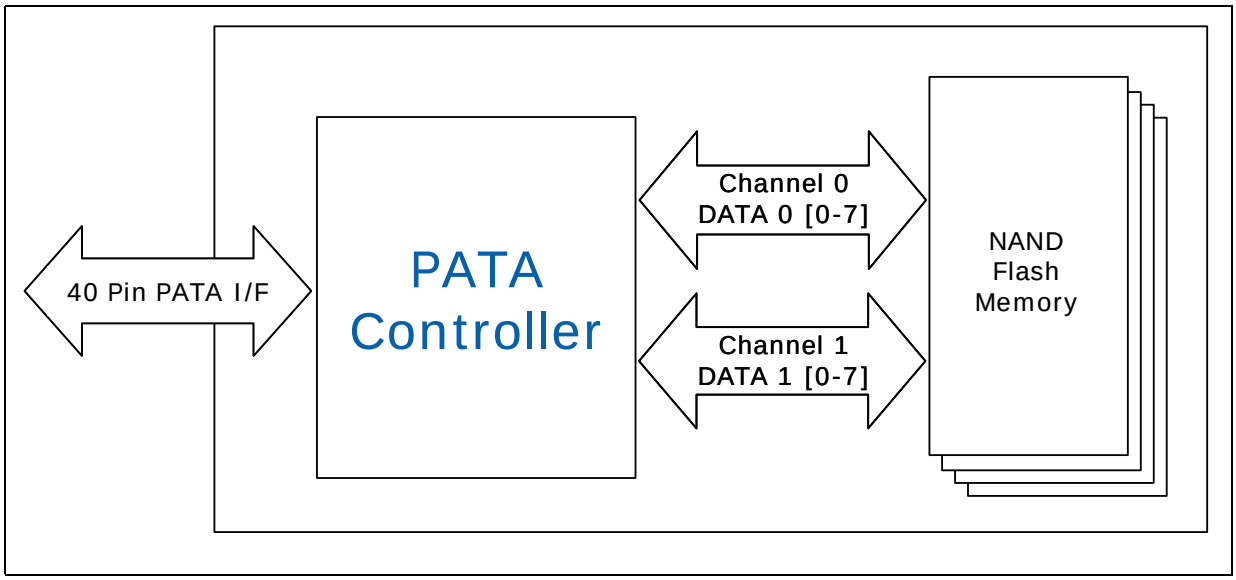
The Intel Z-P140 SSDs also feature flexible capacity options by adding additional Intel PF29F16G32PANC1 2 GB and PF29F32G32PANC1 4 GB NAND Flash Memory components all controlled by a single PoP controller. For example, a 2 GB PoP (SSDPAPS0002G1)can be combined with one PF29F16G32PANC1 devices for a total of 4 GB of contiguous SSD storage. Similarly, a 4 GB PoP (SSDPAPS0004G1)can be combined with one or three PF29F32G32PANC1 devices for a total of 8 or 16 GB of contiguous SSD storage. However, the Intel SD54B and SD58B NAND Flash Memory packages cannot be mixed because the PATA controller requires homogeneous memory that matches the PoP memory device. This flexible capacity feature allows system designers to allow stuffing options at time of manufacture to meet market demands.

Figure 1. Front View of the Intel Z-P140 PATA SSD

Figure 2. Back View of the Intel Z-P140 PATA SSD



1.2 Block Diagram



1.3 Architecture

The PATA controller in the Intel® Z-P140 PATA Solid State Drive utilizes a 32-bit RISC architecture which provides for direct connection of one, two or four NAND flash memory devices (2 per channel). An on-chip error correction code (ECC) and cyclic redundancy check (CRC) unit generates the required code bytes facilitating error detection and correction of up to four random bytes per 512 byte data sector. On the fly code byte generation for read and write operations minimizes ECC performance impacts.

Two 8-bit channels exist to interface to the flash memories that are managed through a direct flash access mechanism which alleviates the main controller from data transfer tasks. Both channels can operate in parallel and each channel has 512 byte sector buffers for data transfer between the host and flash memory.

Intel® Z-P140 PATA Solid State Drives use single level cell (SLC) Intel NAND Flash Memory devices. A PoP device consists of a NAND BGA component plus a PATA controller. The NAND packages not on the PoP are referred to as the BGA NAND packages in this document. SD54B based PoP device can connect with one additional 2GB NAND package to achieve up to 4GB of SSD storage space whereas SD58B based PoP can connect up to additional 1 or 3 NAND packages to achieve 8GB and 16GB of SSD storage space respectively. See Figure 3 and Figure 4 on page 8. The 2 GB Intel® Z-P140 PATA Solid State Drive uses Intel SD54B NAND Flash Memory, while the 4 GB Intel® Z-P140 PATA Solid State Drive uses Intel SD58B NAND Flash Memory. Combining 2 GB packages with 4 GB packages on a single SSD design is not allowed. Details about these NAND devices are available in their respective datasheets. Please see Section 8.0, “Additional Product Information and References” on page 24 for more information.

Figure 3. 2 GB Configuration Using Intel SD54B NAND Flash Memory

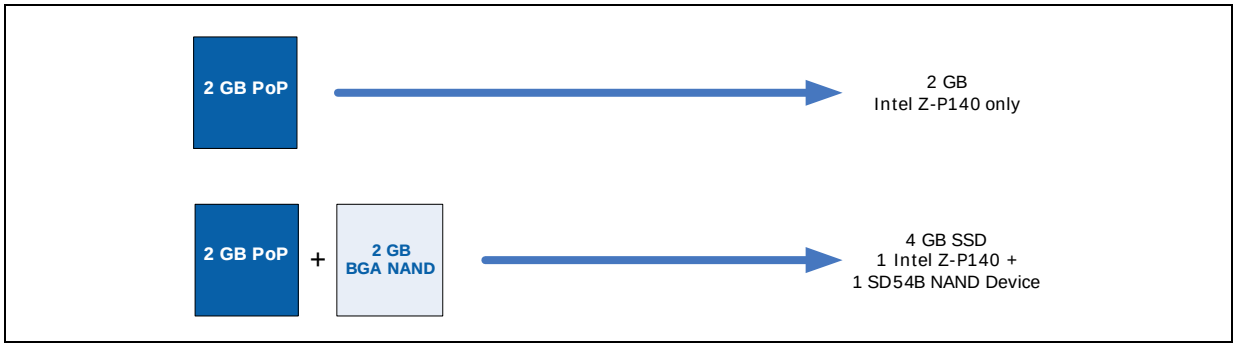
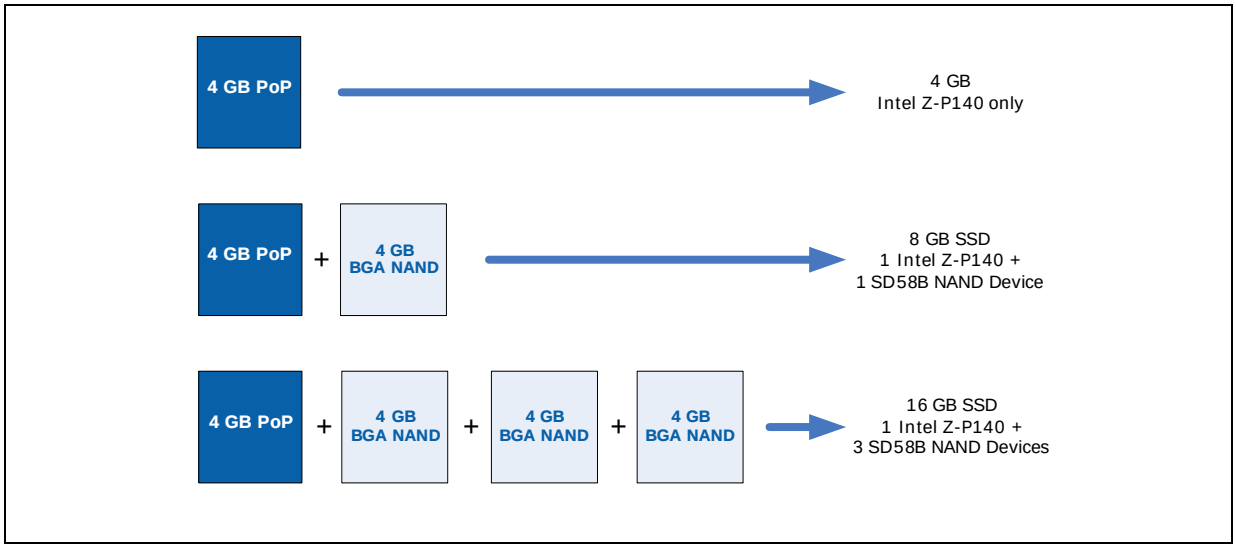


Figure 4. 4 GB Configuration Using Intel SD58B NAND Flash Memory



Intel SLC NAND uses an industry-standard basic NAND flash memory command set along with enhanced capabilities of program page cache mode, page read cache mode, two plane commands and interleaved die operations. The NAND write protect (WP#) feature is managed through the PATA Controller and can be brought out to a jumper pin for whole SSD system write protect.

A single NAND package has the maximum capability of four sets of 8-bit I/O. However, the Intel Z-P140 PATA SSD configuration only uses two sets. Each set is associated with its own set of control signals (ALE, CLE, etc.)

2.0 Compliance

Since the Intel Z-P140 PATA SSD is a component (or a set of components depending on the configuration) on the motherboard, system certifications are the responsibility of the OEM or ODM.

Table 1. Device Compliance

Compliance	Supported	Description
Pb Free	Yes	Components and materials are lead free.
Halogen Free	Yes	Components and materials are halogen free.
RoHS	Yes	Restriction of Hazardous Substance Directive

3.0 Operating Conditions

Table 2. Recommended Operating Voltage

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Vcc supply voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V

Table 3. DC Characteristics (PoP Configuration)

Symbol	Parameter		Min	Typ	Max	Units	Notes
V_{IL}	Input LOW Voltage		-0.3		+0.8	V	
V_{IH}	Input HIGH Voltage		2.0		3.6	V	
V_{OL}	Output LOW Voltage				0.45	V	1
V_{OH}	Output HIGH Voltage		2.4			V	2
I_{CC}	**Operating Current**						
	SD54B	Sleep / Standby mode		340		µA	4
		Active mode		133		mA	4
	SD58B	Sleep / Standby mode		385		µA	4
		Active mode		165		mA	4
I_{LI}	Input Leakage Current				±10	µA	4
I_{LO}	Output Leakage Current				±10	µA	4
$C_{I/O}$	Input/Output Capacitance				10	pF	4

Notes:
1. At 4 mA.
2. At 1 mA.
3. Sampled. Not tested.
4. Applies only to PoP design.

3.1 Capacity

Table 4. User Addressable Sectors

NAND Flash Component	Unformatted Capacity	Total User Addressable Sectors in LBA Mode
Intel SD54B NAND Flash Memory	2 GB	3,908,016
	4 GB	7,821,072
Intel SD58B NAND Flash Memory	4 GB	7,821,072
	8 GB	15,650,208
	16 GB	31,347,792

3.2 Performance

Table 5. Read and Write Bandwidth

Product	Access Type	Typ	Unit
SD54B	Sustained Sequential Read	37	MB/s
	Sustained Sequential Write	26	MB/s
SD58B	Sustained Sequential Read	38	MB/s
	Sustained Sequential Write	29	MB/s

Table 6. Power On Specification

Definition	Typ	Max	Condition
Time between 0 V to when the host can read the first data	100 ms + 450 ms	500 ms + 450 ms	In master configuration with no slave driver.*

Note: 450 ms is added for ATA specification compliance.

4.0 Electrical Characteristics

4.1 Power Consumption

Table 7. Typical Power Consumption

Mode	Configuration	Typ	Unit
Active Current*	SD54B PoP	145	mA
	SD54B PoP + 1 BGA NAND	170	
	SD58B PoP	165	mA
	SD58B PoP + 1 BGA NAND	185	
	SD58B PoP + 3 BGA NAND	185	

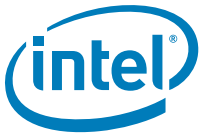


Table 7. Typical Power Consumption (Continued)

Mode	Configuration	Typ	Unit
Active Power*	SD54B PoP	479	mW
	SD54B PoP + 1 BGA NAND	561	
	SD58B PoP	545	mW
	SD58B PoP + 1 BGA NAND	611	
	SD58B PoP + 3 BGA NAND	611	
Sleep / Standby Current	SD54B PoP	340	uA
	SD54B PoP + 1 BGA NAND	380	
	SD58B PoP	385	uA
	SD58B PoP + 1 BGA NAND	415	
	SD58B PoP + 3 BGA NAND	505	
Sleep / Standby Power	SD54B PoP	1.12	mW
	SD54B PoP + 1 BGA NAND	1.25	
	SD58B PoP	1.27	mW
	SD58B PoP + 1 BGA NAND	1.37	
	SD58B Pop + 3 BGA NAND	1.66	

Note: Using UDMA 4 program mode, calculation based on worst casework load condition.

4.2 Environmental Conditions

4.2.1 Temperature

Table 8. Temperature Related Specifications

Mode	Part Number	Min	Max	Unit
Operating Temperature	SSDPAPS0002G1, PF29F16G32PANC1	0	70	^{o}C
	SSDPAPS0004G1, PF29F32G32PANC1	-40	85	^{o}C
Non-Operating Temperature	-	-65	150	^{o}C
Humidity	-	5	95	%

Notes:
1. Operating temperature gradient is 20^{o}C per hour without condensation.
2. Non-operating temperature gradient is 30^{o}C per hour without condensation.

4.2.2 Altitude

Since there are no moving parts, this device is not susceptible to a lack of air molecules and will operate correctly to 50,000 feet above sea level.

4.3 Shock and Vibration

Table 9. Shock and Vibration Specifications

	Mode	Timing	Max	Unit
Shock[1]	Operating	at .5 msec	1,500	G
	Non-Operating	at .5 msec	1,500	G
Vibration[2]	Operating		3.13 G	5-500 Hz
	Non-Operating		5 G	10-500 Hz[3]

Notes:
1. Shock specifications assumes that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Vibration may be applied in the X, Y or Z axis.
2. Vibration specifications assumes that the SSD is mounted securely with the input vibration applied to the drive mounting screws. Vibration may be applied in the X, Y or Z axis.
3. Sine wave sweeping 1 oct/min.

4.4 Acoustics

The drive has no moving or noise-emitting parts; therefore, it produces negligible sound (0 dB) in all modes of operation.

4.5 Electrostatic Discharge

Table 10. ESD Specifications

Test	Description	Performance Criteria	Reference Standard
• 2 kV	Human body model	B	JEDEC Standard JESD22-A114E
• 500 V	Charge device model	B	JEDEC Standard JES D22-C101C

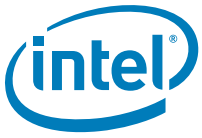
Notes:
1. **Performance Criteria A** = The device shall continue to operate as intended, i.e., normal unit operation with no degradation of performance.
2. **Performance Criteria B** = The device shall continue to operate as intended after completion of the test. However, during the test, some degradation of performance is allowed as long as there is no data loss operator intervention to restore device function.
3. **Performance Criteria C** = temporary loss of function is allowed. Operator intervention is acceptable to restore device function.

4.6 Reliability

Table 11. Reliability Specifications

Parameter	Value
Non-recoverable read errors	1 sector per 10^{15} bits read, max
Mean Time between Failure (MTBF)	2,500,000 hours
Useful Life	5 years*

Note: Based on a sequential workload of 5 GB/Day.



4.7 Error Correction Code (ECC) Retries

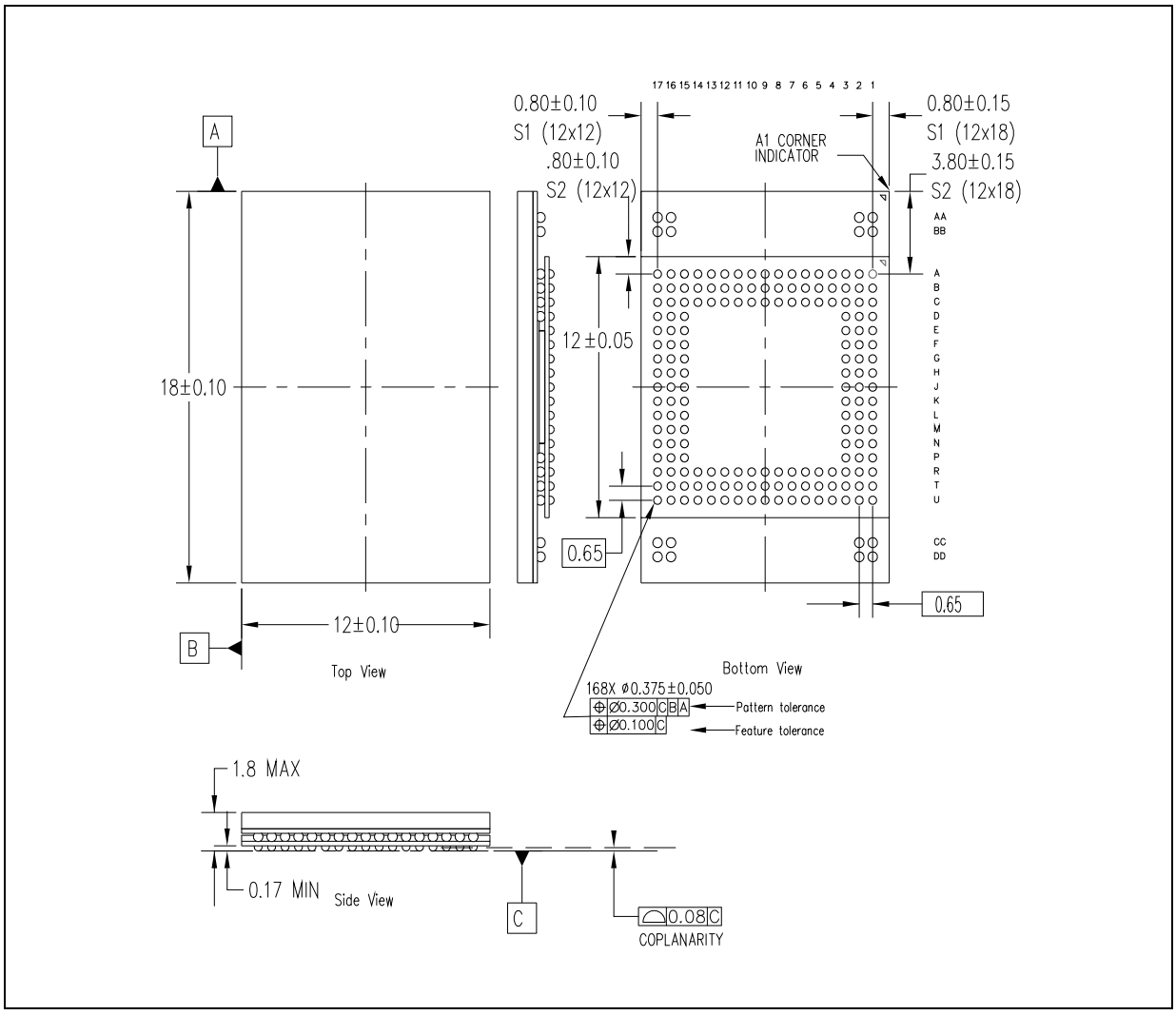
When the controller encounters an uncorrectable ECC error while reading data from the flash device, the controller will repeat the READ command to the flash device up to three times. If the process is unsuccessful, the ECC failure will be reported back to the host and both Aborted (ABRT) and Uncorrectable Data Error (UNC) bits will be set in the error register. This process enables the Intel Z-P140 PATA SSD device to recover from a single disturbance such as an ESD event, but not incorrectly report a block as bad. The device will still be able to manage ECC for true persistent uncorrectable errors.

4.8 Power Failure Protection

The device uses both hardware and software protection to prevent data corruption during power failures. A Flash Write Protect line activates hardware protection should the controller's V_{CC} voltage level fall below 2.7 V. A Flash Write Buffering scheme writes data to Flash Memory to provide software protection. A target user block writes all new data to an associated Flash Buffer Block. On power-up, the controller scans the buffer blocks (which could contain new data that is in the process of being written) for ECC errors to prevent data corruption. So, although a page written to during a power off could be lost, no data corruption occurs.

5.0 Mechanical Information

Figure 5. Combined Top and Bottom Mechanical Drawings



Note: All dimensions in millimeters.

6.0 Ball Assignments and Signal Descriptions

6.1 Bottom PATA Controller Ball Assignments and Locations

The following table depicts the ball out assignment and locations for the 168 BGA bottom controller, which includes 156 active balls and 12 outriggers. Due to space limitations the 12 outriggers are not shown. Please see Figure 5, "Combined Top and Bottom Mechanical Drawings" on page 14 to view the location of the outriggers.

Table 12. Ball Assignments and Locations Viewed From the Top

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	DNU	DNU	DQ01-0	DQ02-0	DQ03-0	WE#-0	ALE-0	CLE-0	CE0#-0	CE1#-0	RE#-0	R/B0#-0	DQ04-0	DQ05-0	DQ06-0	DNU	DNU
B	DNU	DQ00-0	DQ01-2	DQ02-2	DQ03-2	WE#-2	ALE-2	CLE-2	CE0#-2	CE1#-2	RE#-2	R/B0#-2	DQ04-2	DQ05-2	DQ06-2	DQ07-0	DNU
C	VSS	DQ00-2	VCCF	WP#-2	WP#-0	CFG-0	VCCF	VSS	CFG-4	VSS	VCCF	CFG-2	R/B1#-0	R/B1#-2	VCCF	DQ07-2	VSS
D	GND	DNU (BUSRQ#)	RFU	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	CFG-6	DNU (TEST)	GND
E	VDDF	XTALR (XTALSEL)	XTALIN (XTALI)	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DNU (UART_RX)	DNU (UART_TX)	VDDC
F	VDDF	XTALC (IO3)	IOCS16#	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	HRESET#	DNU (UART_CLK)	VDDC
G	FADJ (IBIAS)	PDIAG#	DASP#	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	RESET#	PWE#	CADJ (INT4)
H	VDDF_0	DA0	DMACK#	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	INTRQ	PSYNC_ CSEL#	VDDC_O
J	VDDF_0	DA1	DMARQ	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DIOW#	DIOR#	VDDC_O
K	GND	DA2	IORDY	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	CS3FX#	CS1FX#	GND
L	GND	DD11	DD3	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DD4	DD12	GND
M	VCC	DD10	DD2	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DD5	DD13	VCC
N	GND	DD9	DD1	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DD6	DD14	GND
P	VCC	DD8	DD0	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	DD7	DD15	VCC
R	VSS	DQ00-3	VCCF	WP#-3	WP#-1	CFG-1	VCCF	VSS	CFG-5	VSS	VCCF	CFG-3	R/B1#-1	R/B1#-3	VCCF	DQ07-3	VSS
T	DNU	DQ00-1	DQ01-3	DQ02-3	DQ03-3	WE#-3	ALE-3	CLE-3	CE0#-3	CE1#-3	RE#-3	R/B0#-3	DQ04-3	DQ05-3	DQ06-3	DQ07-1	DNU
U	DNU	DNU	DQ01-1	DQ02-1	DQ03-1	WE#-1	ALE-1	CLE-1	CE0#-1	CE1#-1	RE#-1	R/B0#-1	DQ04-1	DQ05-1	DQ06-1	DNU	DNU

Table 13. Signal Locator

Signal Name	BGA Location
ALE-0	A7
ALE-1	U7
ALE-2	B7
ALE-3	T7
CADJ / INT4	G17
CE0#-0	A9
CE0#-1	U9
CE0#-2	B9
CE0#-3	T9
CE1#-0	A10
CE1#-1	U10
CE1#-2	B10
CE1#-3	T10
CFG-0	C6
CFG-1	R6
CFG-2	C12
CFG-3	R12
CFG-4	C9
CFG-5	R9
CFG-6	D15
CLE-0	A8
CLE-1	U8
CLE-2	B8
CLE-3	T8
CS1FX#	K16
CS3FX#	K15
DA0	H2
DA1	J2
DA2	K2
DASP#	G3
DD0	P3
DD1	N3
DD2	M3
DD3	L3
DD4	L15
DD5	M15
DD6	N15
DD7	P15
DD8	P2
DD9	N2
DD10	M2
DD11	L2
DD12	L16
DD13	M16
DD14	N16
DD15	P16
DIOR#	J16
DIOW#	J15
DMACK#	H3
DMARQ	J3
DNU	A1, A2, A16, A17, B1, B17, T1, T17, U1, U2, U16, U17
DNU / BUSRQ#	D2
DNU / TEST	D16
DNU / UART_CLK	F16
DNU / UART_RX	E15
DNU / UART_TX	E16
DQ00-0	B2
DQ00-1	T2
DQ00-2	C2
DQ00-3	R2
DQ01-0	A3
DQ01-1	U3
DQ01-2	B3
DQ01-3	T3
DQ02-0	A4
DQ02-1	U4
DQ02-2	B4
DQ02-3	T4
DQ03-0	A5
DQ03-1	U5
DQ03-2	B5
DQ03-3	T5
DQ04-0	A13
DQ04-1	U13
DQ04-2	B13
DQ04-3	T13
DQ05-0	A14
DQ05-1	U14
DQ05-2	B14
DQ05-3	T14
DQ06-0	A15
DQ06-1	U15
DQ06-2	B15
DQ06-3	T15
DQ07-0	B16
DQ07-1	T16
DQ07-2	C16
DQ07-3	R16
FADJ / IBIAS	G1
GND	D1, D17, K1, K17, L1, L17, N1, N17
HRESET#	F15
INTRQ	H15
IOCS16#	F3
IORDY	K3
PDIAG#	G2
PSYNC_CSEL#	H16
PWE#	G16
R/B0#-0	A12
R/B0#-1	U12
R/B0#-2	B12
R/B0#-3	T12
R/B1#-0	C13
R/B1#-1	R13
R/B1#-2	C14
R/B1#-3	R14

Table 13. Signal Locator (Continued)

Signal Name	BGA Location
RE#-0	A11
RE#-1	U11
RE#-2	B11
RE#-3	T11
RESET#	G15
RFU	D3
VCC	M1, M17, P1, P17
VDDC	E17, F17

Signal Name	BGA Location
VDDC_0	H17, J17
VDDF	E1, F1
VDDF_0	H1, J1
VSS	C1, C8, C10, C17, R1, R8, R10, R17
WE#-0	A6
WE#-1	U6
WE#-2	B6
WE#-3	T6

Signal Name	BGA Location
WP#-0	C5
WP#-1	R5
WP#-2	C4
WP#-3	R4
XTALC / IO3	F2
XTALIN / XTALI	E3
XTALR / XTALSEL	E2

6.2 Signal Descriptions

6.2.1 BGA NAND Signals

Table 14. BGA NAND Signal Descriptions

Symbol	Type	Description
ALE-0, ALE-1 ALE-2, ALE-3	Input	Address latch enable (channels 0, 1, 2 and 3): During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE0#-0, CE1#-0 CE0#-1, CE1#-1 CE0#-2, CE1#-2 CE0#-3, CE1#-3	Input	Chip enable (Channels 0, 1, 2 and 3): Gates transfers between the host system and the NAND Flash device. After the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. For the 8 Gb configuration, CE0# controls the first 4 Gb of memory; CE1# controls the second 4 Gb of memory. For the 16 Gb configuration, CE0# controls the first 8 Gb of memory; CE1# controls the second 8 Gb. See the Bus Operation section, starting on page 15, for additional operational details.
CLE-0, CLE-1 CLE-2, CLE-3	Input	Command latch enable (channels 0, 1, 2 and 3): When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
RE#-0, RE#-1 RE#-2, RE#-3	Input	Read enable: Gates transfers from the NAND Flash device to the host system.
WE#-0, WE#-1 WE#-2, WE#-3	Input	Write enable: Gates transfers from the host system to the NAND Flash device.
WP#-0, WP#-1 WP#-2, WP#-3	Input	Write protect: Protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.
DQ[00...07]-0 DQ[00...07]-1 DQ[00...07]-2 DQ[00...07]-3	Input / Output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information between the PoP PATA controller and the additional BGA NAND devices. Data is output only during READ operations; at other times the I/Os are inputs.

Table 14. BGA NAND Signal Descriptions (Continued)

Symbol	Type	Description
R/B0#-0, R/B1#-0 R/B0#-1, R/B1#-1 R/B0#-2, R/B1#-2 R/B0#-3, R/B1#-3	Output	Ready/busy: An open-drain, active-LOW output. R/B# is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during READ operations to indicate when data is being transferred from the array into the serial data register. When these operations have completed, R/B# returns to the high-Z state. In the dual die per channel configurations, R/B0# is for the memory enabled by CE0#; R/B1# is for the memory enabled by CE1#.
VCCF	Supply	Power supply for Flash (NAND) that is regulated by the PATA controller.
VSS	Supply	Ground connection.

6.2.2 Controller Signals

Table 15. Controller Signal Descriptions

Symbol	Type	Description
CADJ / INT4		Not used.
CFG-0, CFG-1, CFG-2, CFG-3, CFG-4, CFG-5, CFG-6	Input	Configuration signals used by the controller to manage the configuration options on the BGA NAND devices. All configuration signals must be connected per the *Intel Z-P140 PATA SSD Reference Schematics*.
DNU		Do Not Use. Must be left unconnected.
GND	Supply	Ground connection.
RFU		Reserved for Future Use.
VCC	Supply	Power supply for PATA controller.
VDDC, VDDC_0	Supply	2.5 V core power supply for PATA controller. This voltage is generated internally by the controller, so there's not a need for an external supply.
VDDF, VDDF_0	Supply	Controller regulated Flash voltage supply. This voltage is generated internally by the controller, so there's not a need for an external supply.
FADJ / IBIAS	Input	IBIAS requires a 33 K Ω 1% resistor for unit to work properly.
XTALC / IO3	Input / Output	General purpose input and output.
XTALIN / XTALI	Input	Test clock input.
XTALR / XTALSEL	Output	Test clock select.

6.2.3 PATA Signals

Table 16. PATA Signal Descriptions

Symbol	Type	Description
CS1FX#	Input	Drive chip select 0 is used by host to select Command Block registers.
CS3FX#	Input	Drive chip select 1 is used by host to select Command Block registers.
DA0...2	Input	Drive address signals.
DASP#	Output	Drive active, Drive 1 present, or DMA request / True-IDE DASP.
DD0-15	Input / Output	Data and address bus.

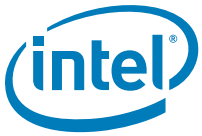


Table 16. PATA Signal Descriptions (Continued)

Symbol	Type	Description
DIOR#	Input	I/O Data Read Enable is the strobe signal asserted by the host to read device registers or the data port.
DIOW#	Input	I/O Data Write Enable is the strobe signal asserted by the host to write device registers or the data port. DIOW shall be negated by the host prior to the initiation of an Ultra DMA burst. STOP shall be negated by the host before the data is transferred in an Ultra DMA burst. The assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
DMACK#	Input	DMA Acknowledge, used by the host in response to DMARQ to either acknowledge that data has been accepted, or that the data is available.
DMARQ	Output	DMA request. This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. For multi word DMA transfers, the direction of data transfer is controller by DIOR# and DIOW#. This signal is used in a “handshake” manner with DMACK#. For example, the device shall wait until the host asserts DMACK# before negating DMARQ and re-asserting DMARQ if there is more data to transfer. When a DMS operation is enabled, CS0# and CS1# shall not be asserted and transfers shall be 16 bits wide. This signal shall be release when the device is not selected.
HRESET#	Input	Host reset.
IOCS16#	Output	16-bit I/O transfer.
INTRQ	Output	Drive interrupt request.
IORDY	Input / Output	I/O channel ready.
PDIAG#	Input / Output	Passed diagnostics.
PSYNC_CSEL#	Input	Cable Select for master/slave, spindle synch, or True-IDE chip.
PWE#	Input	Memory Write Enable or Service Mode Select.
RESET#	Input	Refers to the hardware reset that is used by the host to reset the device.

7.0 Command Sets

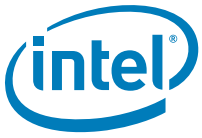
The Intel Z-P140 PATA SSD device supports all the mandatory ATA commands defined in the ATA/ATAPI-5 specification.

7.1 ATA General Feature Command Set

The Intel Z-P140 PATA SSD device supports the ATA General Feature command set (non-PACKET).

Table 17. ATA General Feature Commands

Command Name	Code
ERASE SECTOR(S)	C0h
EXECUTE DEVICE DIAGNOSTIC	90h
FORMAT TRACK	50h
FLUSH CACHE	E7h
IDENTIFY DEVICE	ECh
IDENTIFY DEVICE DMA	EEh
INITIALIZE DRIVE PARAMETERS	91h
MEDIA LOCK	DEh
MEDIA UNLOCK	DEh
NOP	00h
READ BUFFER	E4h
READ DMA	C8h, C9h
READ LONG	22h, 23h
READ MULTIPLE	C4h
READ SECTOR(S)	20h, 21h
READ VERIFY SECTOR(S)	40h, 41h
RECALIBRATE	1xh
REQUEST SENSE	03h
SEEK	7Xh
SET FEATURES	EFh
SET MULTIPLE MODE	C6h
TRANSLATE SECTOR	87h
WRITE BUFFER	E8h
WRITE DMA	CAh, CBh
WRITE LONG	32h, 33h
WRITE MULTIPLE	C5h
WRITE MULTIPLE without ERASE	CDh
WRITE SECTOR(S)	30h, 31h
WRITE SECTOR(S) without ERASE	38h
WRITE VERIFY	3Ch



7.1.1 IDENTIFY DEVICE DATA

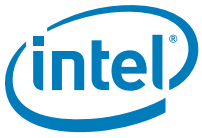
The following table details the data returned after issuing an IDENTIFY DEVICE command.

Table 18. Returned Sector Data

Word	SD54B Default Value	SD58B Default Value	Bytes	Description
0	045Ah	045Ah	2	General configuration bit-significant information: 848Ah = in PCMCIA mode 045Ah = in True-IDE mode
1	2 GB: 0E98h 4 GB: 1D3Ah	4 GB: 1E4Fh 8 GB: 3CA6h	2	Reserved
2	0000h	0000h	2	Unique configuration
3	0010h	0010h	2	Reserved
4	0000h	0000h	2	Reserved
5	0200h	0200h	2	Reserved
6	003Fh	003Fh	2	Reserved
7-8	2 GB: 0039h, 8250h 4 GB: 0073h, 1460h	4 GB: 0077h, 5710h 8GB: 00EEh, CDA0h	4	Reserved
9	0000h	0000h	2	Reserved
10-19	xxxxx	xxxxx	20	Intel Unique Identifier (Serial number): Reserved
20-21	0002h	0002h	4	Reserved
22	0004h	0004h	2	Reserved
23-26	3038h,3038h, 3139h,2E31h	3038h,3038h, 3139h,2E31h	8	Firmware revision (8 ASCII characters) 080819.1
27-46	2 GB: 5353h, 4450h, 4150h, 5330h, 3030h, 3247h, 3100h, 0000h, 0000h, 0000h	4 GB: 5353h, 4450h, 4150h, 5330h, 3030h, 3447h, 3120h, 2020h, 2020h, 2020h	40	Model number (40 ASCII characters) 2 GB: SSDPAPS0002G1 4 GB: SSDPAPS0004G1
47	8002h	8002h	2	Reserved
48	0000h	0000h	2	Reserved
49	0F00h	0F00h	2	Capabilities: DMA, LBA, IORDY supported
50	0000h	0000h	2	Reserved
51	0200h	0200h	2	Obsolete
52	0000h	0000h	2	Obsolete
53	0007h	0007h	2	Data fields 54 to 58, 64 to 70 and 88 are valid
54	2 GB: 0E9Bh 4 GB: 1D3Ah	4 GB: 1E4Fh 8 GB: 3CA6h	2	Reserved
55	0010h	0010h	2	Reserved
56	003Fh	003Fh	2	Reserved

Table 18. Returned Sector Data (Continued)

Word	SD54B Default Value	SD58B Default Value	Bytes	Description
57-58	2 GB: 8250h, 0039h 4 GB: 1460h, 0073h	4 GB: 5710h, 0077h 8 GB: CDA0h, 00EEh	4	Reserved
59	0102h	0102h	2	Reserved
60-61	2 GB: 8250h, 0039h 4 GB: 1460h, 0073h	4 GB: 5710h, 0077h 8 GB: CDA0h, 00EEh	4	Total number of user addressable logical sector
62	0000h	0000h	2	Reserved
63	0007h	0007h	2	Multi-word DMA transfer mode 2 and below are supported
64	0003h	0003h	2	Advanced PIO Modes: modes 3 and 4 supported
65	0078h	0078h	2	Minimum Multiword DMA transfer cycle time per word
66	0078h	0078h	2	Recommended Multiword DMA transfer cycle time
67	0078h	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69-70	0000h	0000h	4	Reserved
71-74	0000h	0000h	8	Reserved for IDENTIFY PACKET DEVICE command
75	0000h	0000h	2	Queue depth
76-79	0000h	0000h	8	Reserved for SATA
80	0020h	0020h	2	Major version number, ATA-5 support
81	0000h	0000h	2	Minor version number, not reported
82	7408h	7408h	2	Command sets supported: NOP, READ BUFFER, WRITE BUFFER, host protected area (HPA) and mandatory power management feature set
83	5000h	5000h	2	Command set supported: FLUSH CACHE
84	4000h	4000h	2	Command set/feature supported extension
85	7408h	7408h	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, host protected area (HPA) and mandatory power management feature set
86	1000h	1000h	2	Command set enabled: FLUSH CACHE
87	4000h	4000h	2	Command set/feature default
88	101Fh	101Fh	2	UDMA mode 4
89-92	0000h	0000h	8	Reserved
93	604Fh	604Fh	2	Hardware Reset Result
94-128	0000h	0000h	70	Reserved
129-159	XXXX	XXXX	62	Vendor specific
160-175	000hh	000hh	32	Reserved
176-254	0000h	0000h	158	Reserved
255	2 GB: 6AA5h 4 GB: 73A5h	2 GB: E9A5h 4 GB: FEA5h	2	Integrity Word (Checksum)



7.2 Host Protected Area Command Set

The Intel Z-P140 PATA SSD device supports the following Host Protected Area commands:

Table 19. Host Protected Area Commands

Command Name	Code
READ NATIVE MAX ADDRESS	F8h
SET MAX ADDRESS	F9h

7.3 Power Management Command Set

The Intel Z-P140 PATA SSD device supports the Power Management command set.

Table 20. Power Management Commands

Command Name	Code
CHECK POWER MODE	E5h, 98h
IDLE	E3h, 97h
IDLE IMMEDIATE	E1h, 95h
SET SLEEP MODE	E6h, 99h
STANDBY	E2h, 96h
STANDBY IMMEDIATE	E0h, 94h

8.0 Additional Product Information and References

For detailed information about a product mentioned in this document, please refer to the corresponding datasheet or application note.

Table 21. Addition Product Information

Order Number	Title	Type*
318531-003US	Intel® SD54B NAND Flash Memory Datasheet	Production
318906-002US	Intel® SD58B NAND Flash Memory Datasheet	Production
319743-001US	Intel® Z-P140 PATA Solid State Drive Configuration Tool	
319541-001US	Intel® Z-P140 PATA Solid State Drive Reference Schematic	

Note: Customers who request access to *Advanced* datasheets must have a a non-disclosure agreement (NDA) with Intel. We release *Advanced* datasheets prior to *Preliminary* datasheets, which are released around the time a product is sampled. *Production* datasheets become available when the part is mass produced. To obtain a copy of these documents, please contact your Intel field sales representative.

This document also references standards and specifications defined by a variety of organizations. Please use the following information to identify the location of an organization's standards information.

Table 22. Standards References

Date or Revision Number	Title	Location
February 2000	ATA-5	http://www.t13.org/Documents/UploadedDocuments/project/d1321r3-ATA-ATAPI-5.pdf
January 2007	JEDEC Standard: Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	http://www.jedec.org/download/search/default2.cfm
December 2004	JEDEC Standard JESD22-C101C: Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components	http://www.jedec.org/download/search/default2.cfm
1995	International Electrotechnical Commission ENV 50204 (Radiated electromagnetic field from digital radio telephones)	http://www.iec.ch
1995 1996 1995 1995 1997 1994	International Electrotechnical Commission EN 61000 4-2 (Personnel Electrostatic Discharge Immunity) 4-3 (Electromagnetic compatibility (EMC)) 4-4 (Electromagnetic compatibility (EMC)) 4-5 (Electromagnetic compatibility (EMC)) 4-6 (Electromagnetic compatibility (EMC)) 4-11 (Voltage Variations)	http://www.iec.ch
December 2006	Open NAND Flash Interface Specification (ONFI) 1.0	http://www.onfi.org/docs/ONFI_1_0_Gold.pdf

9.0 Glossary

This document incorporates many industry- and device-specific words. Use the following list to define a variety of terms and acronyms.

Table 23. Glossary of Terms and Acronyms

Term	Definition
ATA	Advanced Technology Attachment
CFA	CompactFlash Association
CPRM	Content Protection for Recordable Media
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
ECC	Error Correction Code
ESD	Electrostatic Discharge
HDD	Hard Disk Drive
HPA	Host Protected Area
IDE	Integrated Device Electronics
LBA	Logical Block Addressing
MTBF	Mean Time Between Failure
MWDMA	Multi-word DMA
ODM	Original Design Manufacturer
OEM	Original Equipment Manufacturer
PATA	Parallel ATA
PCMCIA	Personal Computer Memory Card International Association
PIO	Programmable Input / Output
PoP	Package on Package
SATA	Serial ATA
SSD	Solid state drive
UDMA	Ultra DMA, also know Ultra ATA

10.0 Revision History

Date	Revision	Description
October 2008	003	On the cover page, modified Performance and Power Consumption values, edited the values for Extended Temperature coverage on 4GB and 8 EGB. Updated values in Table 18, “Returned Sector Data” on page 21 Updated Figure Figure 1, “Front View of the Intel Z-P140 PATA SSD” on page 6 Modified the MM numbers for each product listed in the “Ordering Information” on page 2. Modified values LBA in Table 4, “User Addressable Sectors” on page 10 Modified values and notes in Table 3, “DC Characteristics (PoP Configuration)” on page 9 Modified values of current and power in Table 7, “Typical Power Consumption” on page 10.

Date	Revision	Description
June 2008	002	On the cover page, modified the total number of extensible memory from 8 GB to 4 GB when using 2 GB configuration, modified Performance and Power Consumption values, inserted the values for Extended Temperature and added a reference for Halogen Free compliance. Update the MM numbers for each product listed in the "Ordering Information" on page 2. Modified content in the following sections: • Section 1.0, "Overview" on page 5 • Section 1.1, "Product Overview" on page 5 Removed the PoP + 3 BGA NAND configuration from Figure 3, "2 GB Configuration Using Intel SD54B NAND Flash Memory" on page 8. Added "Halogen Free" to Table 1, "Device Compliance" on page 9. Added the values for "Ground" to Table 2, "Recommended Operating Voltage" on page 9. Modified values and notes in Table 3, "DC Characteristics (PoP Configuration)" on page 9. Updated values in Table 4, "User Addressable Sectors" on page 10 and Table 5, "Read and Write Bandwidth" on page 10. Removed former Table 7, Operating Voltage because information already contained in Table 2, "Recommended Operating Voltage" on page 9. Modified values and format of current Table 7, "Typical Power Consumption" on page 10. Modified Table 8, "Temperature Related Specifications" on page 11 and Notes. Added note to Figure 5, "Combined Top and Bottom Mechanical Drawings" on page 14. Added definition of Useful Life to Table 11, "Reliability Specifications" on page 12. Updated the following tables: • Table 12, "Ball Assignments and Locations Viewed From the Top" on page 15 • Table 13, "Signal Locator" on page 16 Modified description for Ready/Busy (R/B#) in Table 14, "BGA NAND Signal Descriptions" on page 17 Merged the content from former Table 18, F3-Specific Signal Descriptions with Table 15, "Controller Signal Descriptions" on page 18. Updated the following tables • Table 16, "PATA Signal Descriptions" on page 18 • Table 18, "Returned Sector Data" on page 21 Added Section 8.0, "Additional Product Information and References" on page 24. Added the ordering information for the Intel Z-P140 PATA SSD Configuration Tool and updated the ordering number for Intel Z-P140 PATA SSD Reference Schematic in Table 21, "Addition Product Information" on page 24. Added MWDMA, HPA and corresponding definitions to Section 9.0, "Glossary" on page 25.
December 2007	001	Initial Pre-Release