W86L157

WINBOND
MMC CARD CONTROLLER

Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	-	2/2004	0.5		First published.
2	16	4/6/2004	0.6		Add 48-pin LQFN package
3	18, 19	12/2/2004	0.7		Update schematic description
4					
5					
6					
7					
8					
9					
10					

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LIFE SUPPORT APPLICATIONS

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W86L157 Preliminary

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Table of Contents-

1. GENERAL DESCRIPTION

MutiMediaCard (MMC) is flash-based memory card, widely used as storage in mobile & consumer devices. The W86L157 is MMC memory card controller, which supports 8 bit NAND type flash memory or ROM (8/16bit). Support 4xNAND flash memory maxium capacity up to 4GB or 4xROM up to1GB. W86L157 is a powerful and intelligent controller, which has high transferring performance and Smart Flash Diagnosis Circuits. Support MMC commands in MMC and SPI mode.

2. FEATURES

- Compliant with MMC Spec. Version 3.3

- Support MMC and SPI mode.

- Access NAND flash memory up to 4GBytes and ROM up to 1GB.

- Support 4x NAND Flash (8bit) or 4x ROM (256M address with 8/16 bit).

- Built-in 512Bytes data buffer for data transmit between MMC bus and Flash/ ROM.

- Block and partial block read supported, stream read also supported.

- Read block size programmable between 1 and 512 bytes

- Flexible valid data blocks setting for different defect rate of Flash.

- Support card lock/un-lock command.

- Built-in 2bit EDC & 1bit ECC diagnosis circuits for data correction.

- Power low autodetect and damage free for card insertion/removal.

- High integration with no external component needed.

- Interface operating voltage: 2.0 to 3.6V.

- Flash operating voltage: 2.7 to 3.6V.

- Support 64-ELGA, 48-LQFN package and die form.

- 48-LQFN supports 4xNAND Flash, not support ROM.

Ordering Information

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W86L157Y	64-ELGA 9 x 9 x 0.7mm	Commercial, 0 ^{o}C to +70 ^{o}C
W86L157SY	48-LQFN 7 x 7 x 0.7mm	Commercial, 0 ^{o}C to +70 ^{o}C

3. PIN CONFIGURATION

3.1 W86L157 Pin Assignment (64-pin)
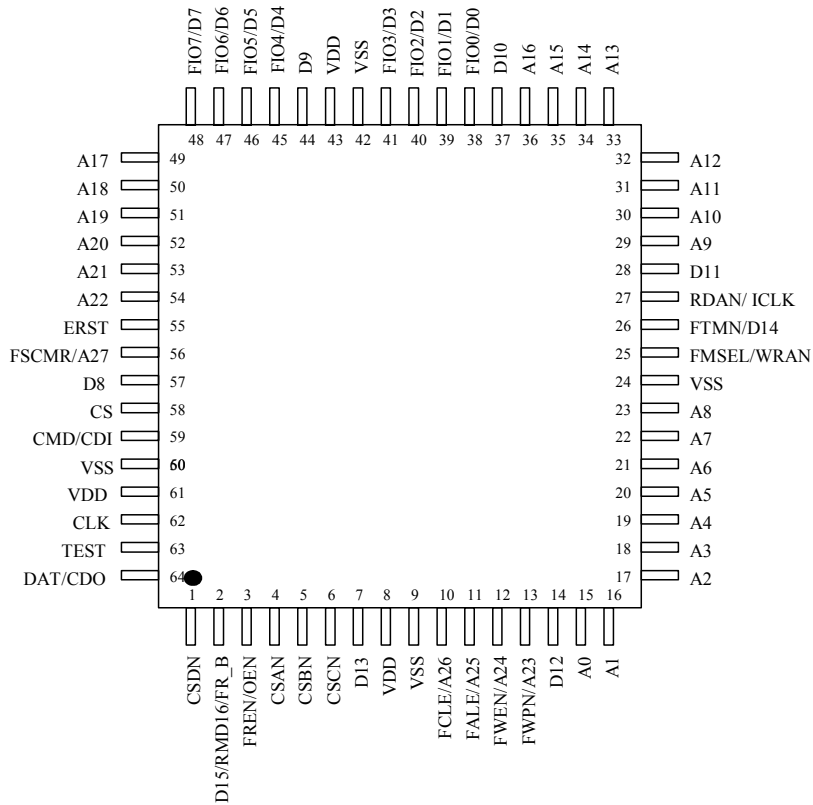

Fig. 3-1 W86L157 Pin Assignment (64-pin)
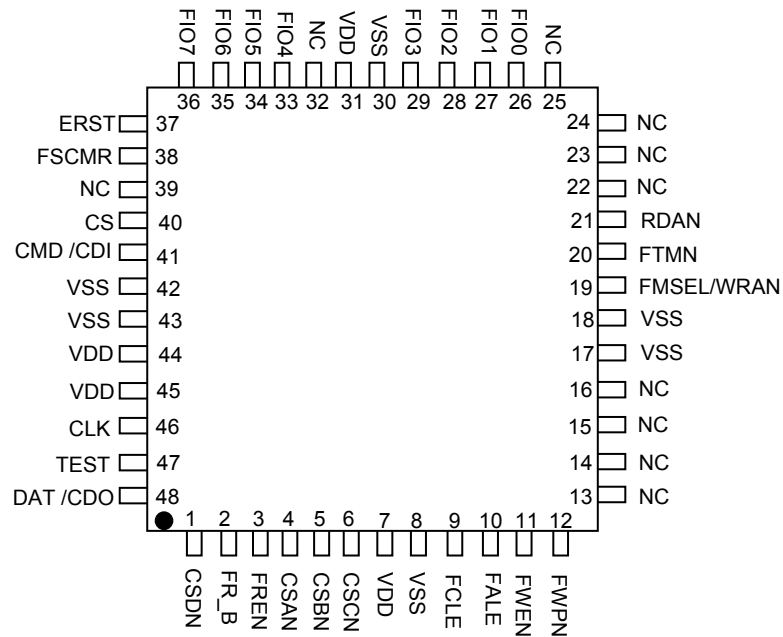
3.2 W86L157 Pin Assignment (48-pin)

Fig. 3-2 W86L157 Pin Assignment (48-pin)

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4. PIN DESCRIPTIONS

4.1 W86L157Y Pin Descriptions (64-pin)

PIN	NAME	TYPE	DESCRIPTION
MMC Interface:			
64	DAT/CDO	DB/DO	MMC mode: Data line SPI mode: Card data output.
58	CS	DI	SPI mode: Card select input, active low.
59	CMD/CDI	DB/DI	MMC mode: Command response. SPI mode: Card data input.
62	CLK	DI	Clock input signal of MMC card.
Flash Memory or ROM Interface Signal:			
56	FSCMR/A27	DI/DO	Flash Single ComMand Read set in flash memory, Address line 27 of ROM. If the flash ID number can not recognized, flash memory is single command read if this pin is high and is two command read if low. *Always input when flash memory select.*
10	FCLE/A26	DO/DIO	Command Latch Enable of flash memory, Address line 26 of ROM.
11	FALE/A25	DO/DIO	Address Latch Enable of flash memory, Address line 25 of ROM.
12	FWEN/A24	DO/DIO	Write Enable of flash memory, Address line 24 of ROM.
13	FWPN/A23	DO/DIO	Write Protect of flash memory, Address line 23 of ROM.
15~23	A[0:8]	DO/DIO	Address line [0:8] of ROM.
29~36	A[9:16]	DO/DIO	Address line [9:16] of ROM.
49~54	A[17:22]	DO/DIO	Address line [17:22] of ROM.
4	CSAN	DO/DIO	Chip select output pin of flash memory A or ROM A, active low.
5	CSBN	DO/DI	Chip select output pin of flash memory B or ROM B, active low and input during reset. This pin is disable and single flash or ROM is connected if input low during reset. *Weak pull high is drive and will change to weak pull low when single flash or ROM is used.*
6	CSCN	DO/DI	Chip select output pin of flash memory C or ROM C, active low and input during reset. *Weak pull high is drive and will change to weak pull low when 4 flashs or ROMs are used.*
1	CSDN	DO/DI	Chip select output pin of flash memory D or ROM D, active low and input during reset. *Weak pull hign is drive and will change to weak pull low when 4 flashs or ROMs are used.*

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W86L157Y Pin Descriptions (64-pin), continued

PIN	NAME	TYPE	DESCRIPTION
Flash Memory or ROM Interface Signal:			
3	FREN/OEN	DO/DIO	Read Enable of flash memory or output enable of ROM.
48, 47, 46, 45, 41, 40, 39, 38	FIO[7:0]/ D[7:0]	DB/DI	Command, Address or Data lines of flash memory, Data line [7:0] of ROM. *Weak pull high or low is driven when no accessing*.
2	D15/RMD16/ FR_B	DI/DI/ DI/DIO	Data line 15 of ROM, ROM data size 16, Ready/Busy state output of flash memory. High byte data of ROM is disabled if RMD16 input low during reset, internal 10K pull high when flash memory selected. *10K pull high is driven and will turn off wheh read high byte data bus of ROM is read or RMD16 is low during reset.*
26	*FTMN*/D14	DI/DIO	*Force memory in Transparency Mode,* High byte data line 14 of ROM. This pin is low during reset will force flash memory into transparency mode, High byte data is disabled if RMD16 input low during reset. *Weak pull high is drive during reset and will change to weak pull high or low when no accessing.*
7,14, 28,37,44,57	D[13:8]/ *TMB[5:0]*	DI/DIO	High byte data line [13:8] of ROM. High byte data is disabled if RMD16 input low during reset. *Bit [5:0] of test mode settingduring reset and test mode enable. Weak pull high or low is driven when no accessing. D[12] power low detect output in test mode after reset.*
25	FMSEL/ WRAN	DI/DO	Flash memory select during reset, left open or pull high for flash memory, low for ROM, write access indicate output (active low) if flash memory card selected.
Other Signal:			
27	RDAN /ICLK	DO /DIO	Read access indicate output (active low) *or internal operation clock output*.
55	ERST	DI	External Reset input, hardware reset input, internal pull high and active low, should left open in normal operation.
63	TEST	DI	Test input, should left open in normal operation. Always input High in test mode. *Weak pull low is driven*.
Power:			
8,43,61	VDD x3	DP	Power supply 3.3V (3 pins).
9, 24, 42, 60	VSS x4	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output, DB is Digital Bi-direction.

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4.2 W86L157SY Pin Descriptions (48-pin)

PIN	NAME	TYPE	DESCRIPTION
MMC Interface:			
48	DAT/CDO	DB/DO	MMC mode: Data line SPI mode: Card data output.
40	CS	DI	SPI mode: Card select input, active low.
41	CMD/CDI	DB/DI	MMC mode: Command response. SPI mode: Card data input.
46	CLK	DI	Clock input signal of MMC card.
Flash Memory Interface Signal:			
38	FSCMR	DI/DO	Flash Single ComMand Read set in flash memory, If the flash ID number can not recognized, flash memory is single command read if this pin is high and is two command read if low. *Always input when flash memory select.*
9	FCLE	DO/DIO	Command Latch Enable of flash memory
10	FALE	DO/DIO	Address Latch Enable of flash memory
11	FWEN	DO/DIO	Write Enable of flash memory
12	FWPN	DO/DIO	Write Protect of flash memory
4	CSAN	DO/DIO	Chip select output pin of flash memory A, active low.
5	CSBN	DO/DI	Chip select output pin of flash memory B, active low and input during reset. This pin is disable and single flash is connected if input low during reset. *Weak pull high is drive and will change to weak pull low when single flash is used.*
6	CSCN	DO/DI	Chip select output pin of flash memory C, active low and input during reset. *Weak pull high is drive and will change to weak pull low when 4 flashs are used.*
1	CSDN	DO/DI	Chip select output pin of flash memory D, active low and input during reset. *Weak pull hign is drive and will change to weak pull low when 4 flashs are used.*
3	FREN	DO/DIO	Read Enable of flash memory.
36, 35, 34, 33, 29, 28, 27, 26	FIO[7:0]	DB/DI	Command, Address or Data lines of flash memory.
2	FR_B	DI/DI/ DI/DIO	Ready/Busy state output of flash memory.
20	*FTMN*	DI/DIO	*Force memory in Transparency Mode.*

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W86L157SY Pin Descriptions (48-pin), contined

PIN	NAME	TYPE	DESCRIPTION
Flash Memory Interface Signal:			
19	FMSEL/ WRAN	DI/DO	Flash memory select during reset, left open or pull high for flash memory, low for ROM, write access indicate output (active low) if flash memory card selected.
Other Signals:			
21	RDAN /ICLK	DO /DIO	Read access indicate output (active low) *or internal operation clock output*.
37	ERST	DI	External Reset input, hardware reset input, internal pull high and active low, should left open in normal operation.
47	TEST	DI	Test input, should left open in normal operation. Always input High in test mode. *Weak pull low is driven*.
Power:			
7, 31, 44, 45	VDD x 4	DP	Power supply 3.3V (3 pins).
8, 17, 18, 30, 42, 43	VSS x 6	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output, DB is Digital Bi-direction.
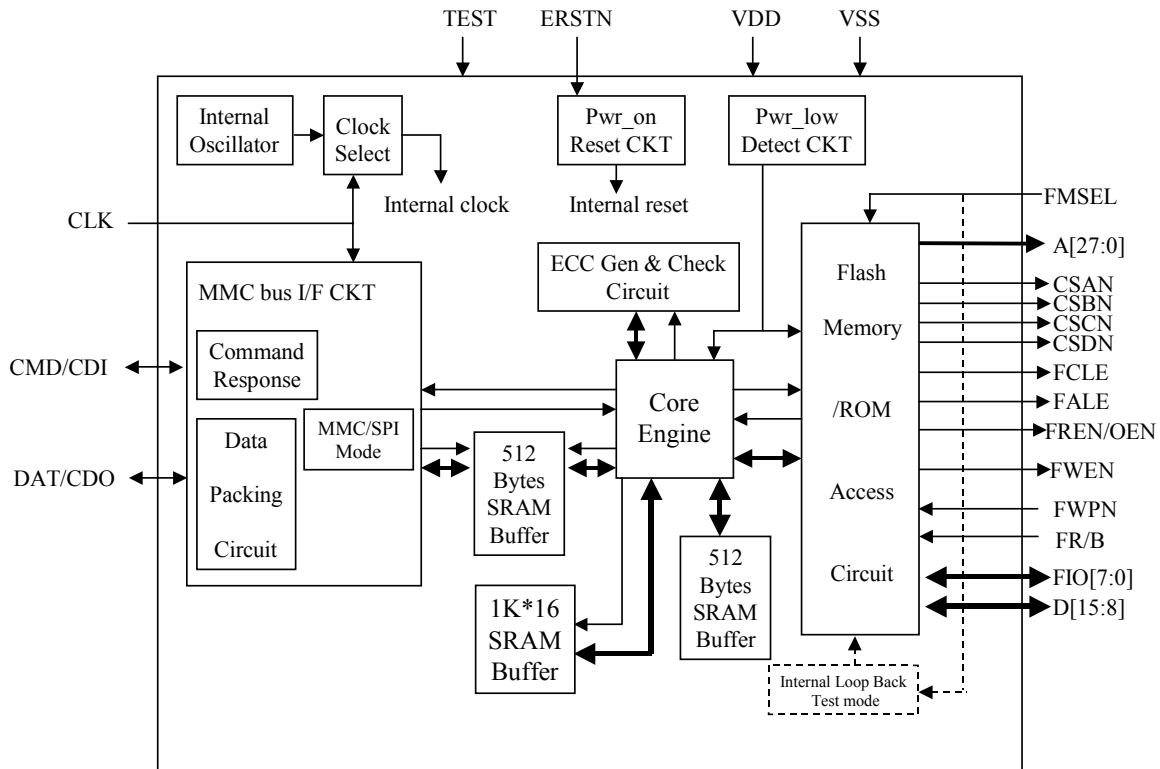
5. BLOCK DIAGRAM

Fig. 5-1 Block Diagram of W86L157.

6. FUNCTION DESCRIPTION

6.1 MMC Bus

6.1.1 MMC Memory Card Registers

- **CID register**, 16 bytes. Card identification number, default value is all 0x00, can be set in boot block of flash memory or ROM.
- **RCA register**, 2 bytes. Relative card address, local system address of a card, dynamically assigned by the host during initialization.
- **DSR register**, not support.
- **CSD register**, 16 bytes. Card specific data register, default is all 0x00 and can be set in boot block of flash memory or ROM.
- **OCR register**, 4 bytes. Operation condition register, fixed at 2.0 to 3.6V of operation voltage and un-configurable.

7. ELECTRICAL CHARACTERISTICS

7.1 Maximum Ratings*

PARAMETER	SYMBOL	RATING	UNITS
Supply Voltage differentials (Vss_1, Vss_2)		-0.5 to 0.5	V
Current at any pin other than supplies		0 to 10	mA
Storage Temperature	T_{st}	-65 to 150	°C

Note: * Exceeding these values may cause permanent damage.

7.2 Recommended Operating Conditions

CHARACTERISTICS	SYMBOL	RATING	UNIT
Operation Voltage (referenced to V_{SS} pin)	V_{VDD}	2.0 to 3.6	V
Clock Frequency at CLK pin	f_{CLK}	20	MHz
Operation Temperature	T_{op}	0 to 70	°C

7.3 Power Supply Characteristics

PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	TEST
Standby Supply Current	Power Supply	I_S		20	40	uA	Test 1
Operating Supply Current	(V_{VDD} = 3.3V)	I_{VDD}		TBD	TBD	mA	Test 2

‡: Typical figure are at V_{VDD} = 3.3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{VDD} or V_{VSS}, configured as power down mode, output without loading and no clock input on the CLK pin.

Test 2: 20 MHz clock input on the CLK pin, output without loading.

7.4 Ring Oscillator Characteristics

PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	NOTES
Oscillator frequency	(V_{VDD} = 3.3V)	f_{QSC}		25	28	MHz	

‡: Typical figure are at V_{VDD} = 3.3V and temperature = 25 °C and subject to production testing.

7.5 Power Low Detection Characteristics (Temperatur: 25°C)

PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	NOTES
Detection Voltage		V_{DET}	2.1	2.3	2.6	V	
Hysteresis		V_{DHY}		50		mV	

‡: Typical figure are at temperature = 25 °C and subject to production testing.

7.6 Digital Characteristics

PARAMETER	CONDITION	SYMBOL	MIN.	TYP‡	MAX.	UNITS	NOTES
Output High Voltage	2mA load	V_{OH}	0.9			V_{DD}	
Output Low Voltage	2mA sink	V_{OL}			0.1	V_{DD}	
High Level Input Voltage		V_{IH}	0.7			V_{DD}	
Low Level Input Voltage		V_{IL}			0.3	V_{DD}	
Input Current		Iin			1	uA	
Input Capacitance		Cin		10		pF	

‡: Typical figure are at V_{DVDD} = 3.3V and temperature = 25 °C and are for design aid only, not guaranteed and not subject to production testing.
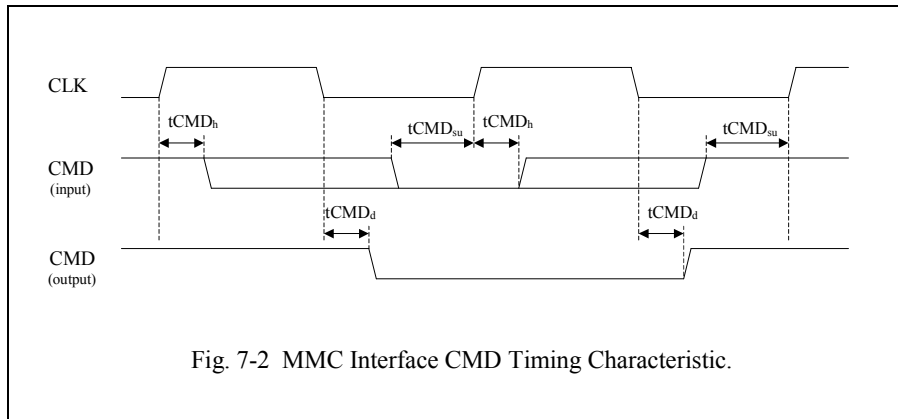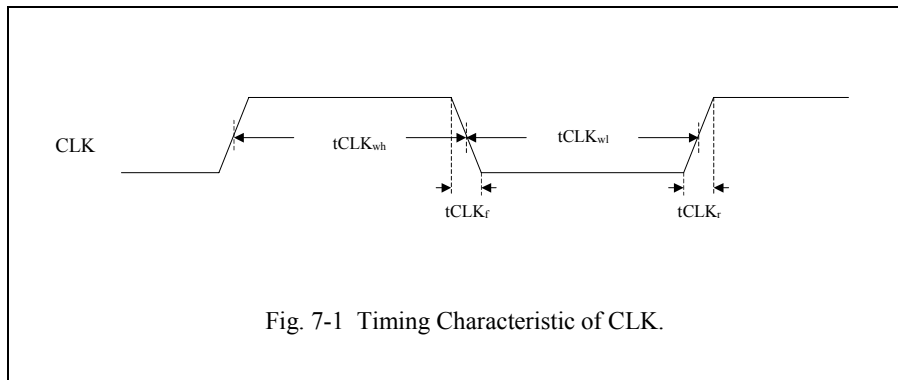
7.7 Timing Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock (figure 7-1)						
CLK	fCLK		-	400	KHz	
CLK	fCLK		-	20	MHz	C_L <=100PF
CLK high pulse width	tCLK$_{wh}$	10	-	-	ns	C_L <=100PF
CLK low pulse width	tCLK$_{wl}$	10	-	-	ns	C_L <=100PF
CLK rise time	tCLK$_r$	-	-	10	ns	C_L <=100PF
CLK fall time	tCLK$_f$	-	-	10	ns	C_L <=100PF

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Timing Characteristics,continued

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Serial Interface Signals *(figure 7-2, 7-3)*						
CMD output delay	$tCMD_d$	5	-	15	nS	1
CMD input setup time	$tCMDD_{su}$	3	-	-	nS	
CMD input hold time	$tCMD_h$	3	-	-	nS	
DAT output delay time	$tDAT_d$	-	-	15	nS	1
DAT input setup time	$tDAT_{su}$	3	-	-	nS	
DAT input hold time	$tDAT_h$	3	-	-	nS	
Flash Memory Interface Signals *(figure 7-4)*						
FIO[7:0] output delay time	$tDAT_d$	-	-	15	nS	1
FIO[7:0] input setup time	$tDAT_{su}$	15	-	-	nS	
FIO[7:0] input hold time	$tDAT_h$	5	-	-	nS	
ROM Interface Signals *(figure 7-5)*						
D[7:0] output delay time	tD_d	-	-	150	nS	1
D[7:0] input hold time	tD_h	0	-	-	nS	

Note 1: 20 pF output loading.

Fig. 7-1 Timing Characteristic of CLK.

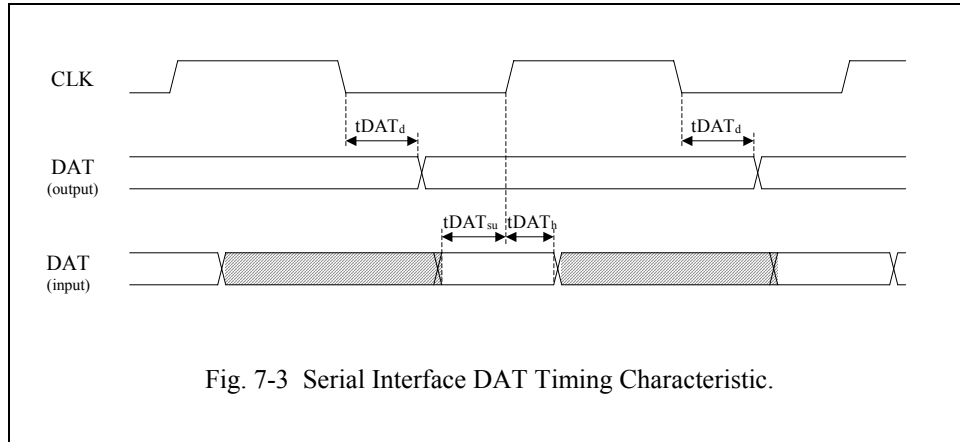Fig. 7-2 MMC Interface CMD Timing Characteristic.

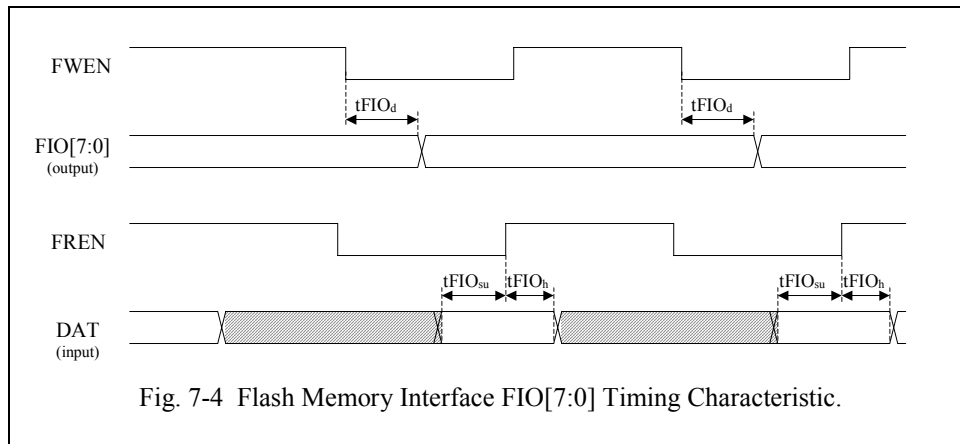Fig. 7-3 Serial Interface DAT Timing Characteristic.

Fig. 7-4 Flash Memory Interface FIO[7:0] Timing Characteristic.

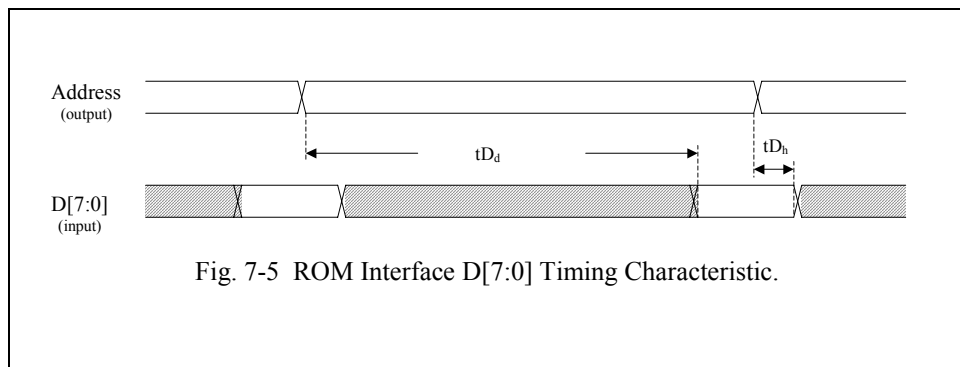Fig. 7-5 ROM Interface D[7:0] Timing Characteristic.

8. HOW TO READ THE TOP MARKING

The top marking of W86L157Y

SMART @ IO
W86L157Y
413AABA
2217970320

○

1st line: Winbond logo and SMART@IO Mark

2nd line: Part number of W86L157Y

3rd line: Tracking code   413 A A BA

        413: Packages made in '04, week 13

        A: Assembly house ID; A means ASE, O means OSE, G means GR

        A: IC revision; A means version A, B means version B
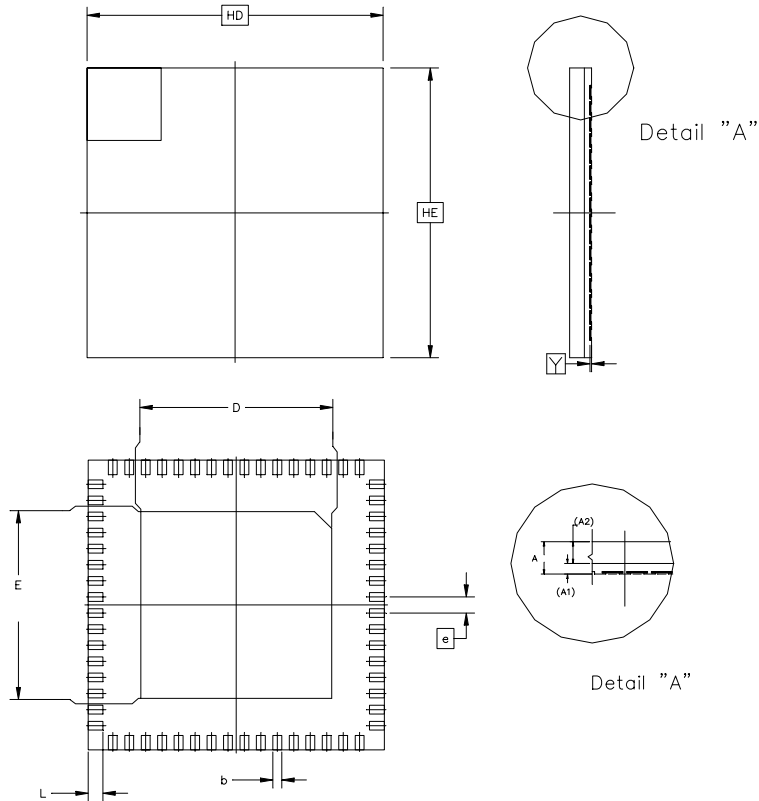
        BA: for internal use

4th line: Tracking code

9. PACKAGE DIMENSIONS

9.1 W86L157Y Package Dimensions

ELGA 64L 9X9 MM^2, Thickness: 0.7 MM

Detail "A"

Detail "A"

Controlling Dimension : Millimeters

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	0.7	-----	-----	0.028
A1	0.22 REF.			0.0087REF.		
A2	0.45 REF.			0.0177 REF.		
HP	9 BSC			0.3543BSC		
HE	9 BSC			0.3543BSC		
L	0.4	0.45	0.55	0.0157	0.0177	0.0217
D	5.65	5.8	5.95	0.2224	0.2283	0.2343
E	5.65	5.8	5.95	0.2224	0.2283	0.2343
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
e	0.5 BSC			0.0197BSC		
Y	0.08BSC			0.003BSC		

*D,*E:By die size difference.

9.2 W86L157SY Package Dimensions

LQFN 48L 7X7 MM^2, Thickness: 0.7 MM

TOP VIEW   BOTTOM VIEW
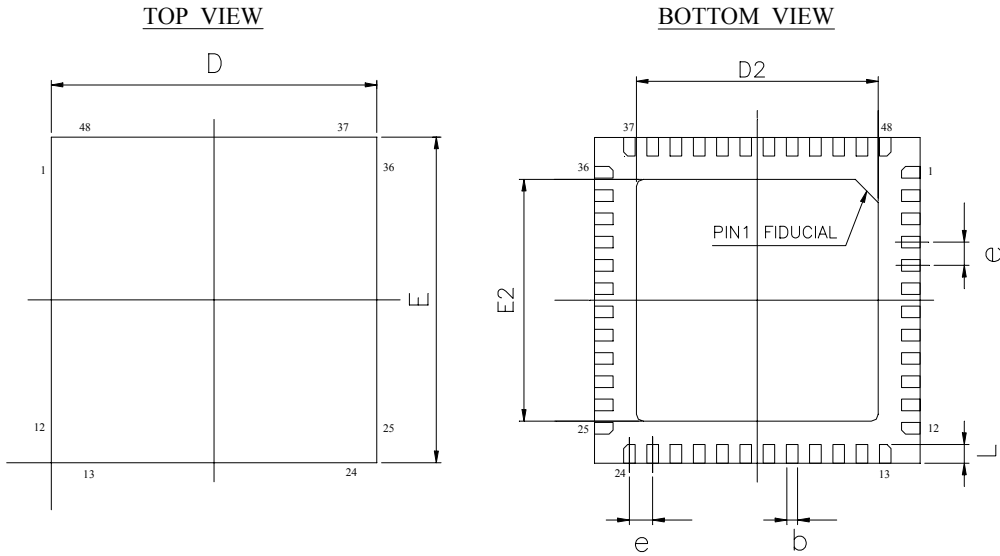
Controlling Dimension :Millimeters

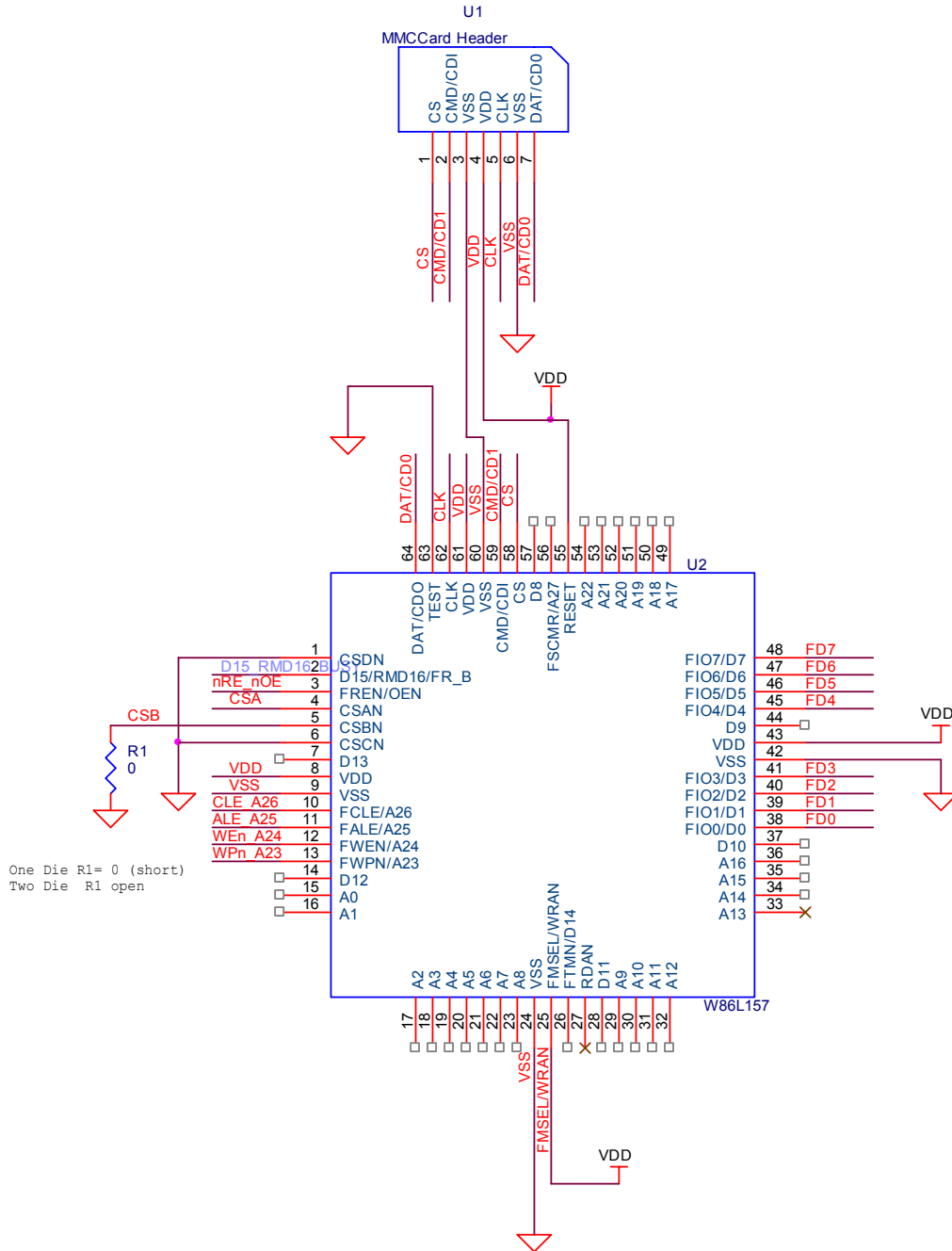| SYMBOL	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.61	0.66	0.70	0.024	0.026	0.028
A1	0	0.02	0.05	0	0.001	0.002
A3	0.127 REF			0.005 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	7.00 BSC			0.276 BSC		
D2	2.25	4.70	5.25	0.089	0.185	0.207
E	7.00 BSC			0.276 BSC		
E2	2.25	4.70	5.25	0.089	0.185	0.207
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.08			0.003		
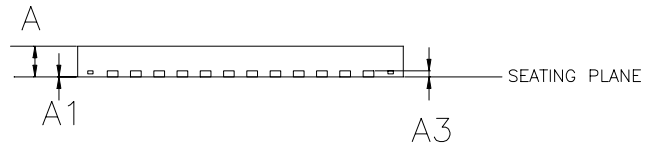
*D2,*E2 :By die size difference

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10. REFERENCE SCHEMATIC

10.1 W86L157Y Reference Schematic

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U3

Pin	Left Label		Right Label	Pin	Net

```
                    U3
         1 ┤ NC              NC ├ 48
         2 ┤ NC              NC ├ 47
         3 ┤ NC              NC ├ 46
         4 ┤ NC              NC ├ 45
         5 ┤ NC             I/O7 ├ 44    FD7
         6 ┤ NC             I/O6 ├ 43    FD6
D15_RMD16_BUSY  7 ┤ R/B     I/O5 ├ 42    FD5
    nRE_nOE    8 ┤ RE       I/O4 ├ 41    FD4
       CSA     9 ┤ CE         NC ├ 40
       CSB    10 ┤ NC/CE2     NC ├ 39
VDD          11 ┤ NC        PRE ├ 38         VDD
             12 ┤ VCC       VCC ├ 37
             13 ┤ VSS       VSS ├ 36
             14 ┤ NC         NC ├ 35
             15 ┤ NC         NC ├ 34
   CLE_A26   16 ┤ CLE        NC ├ 33
   ALE_A25   17 ┤ ALE      I/O3 ├ 32    FD3
   WEn_A24   18 ┤ WE       I/O2 ├ 31    FD2
   WPn_A23   19 ┤ WP       I/O1 ├ 30    FD1
             20 ┤ NC       I/O0 ├ 29    FD0
             21 ┤ NC         NC ├ 28
             22 ┤ NC         NC ├ 27
             23 ┤ NC         NC ├ 26
             24 ┤ NC         NC ├ 25
                 K9F1G08U0M-Y
```
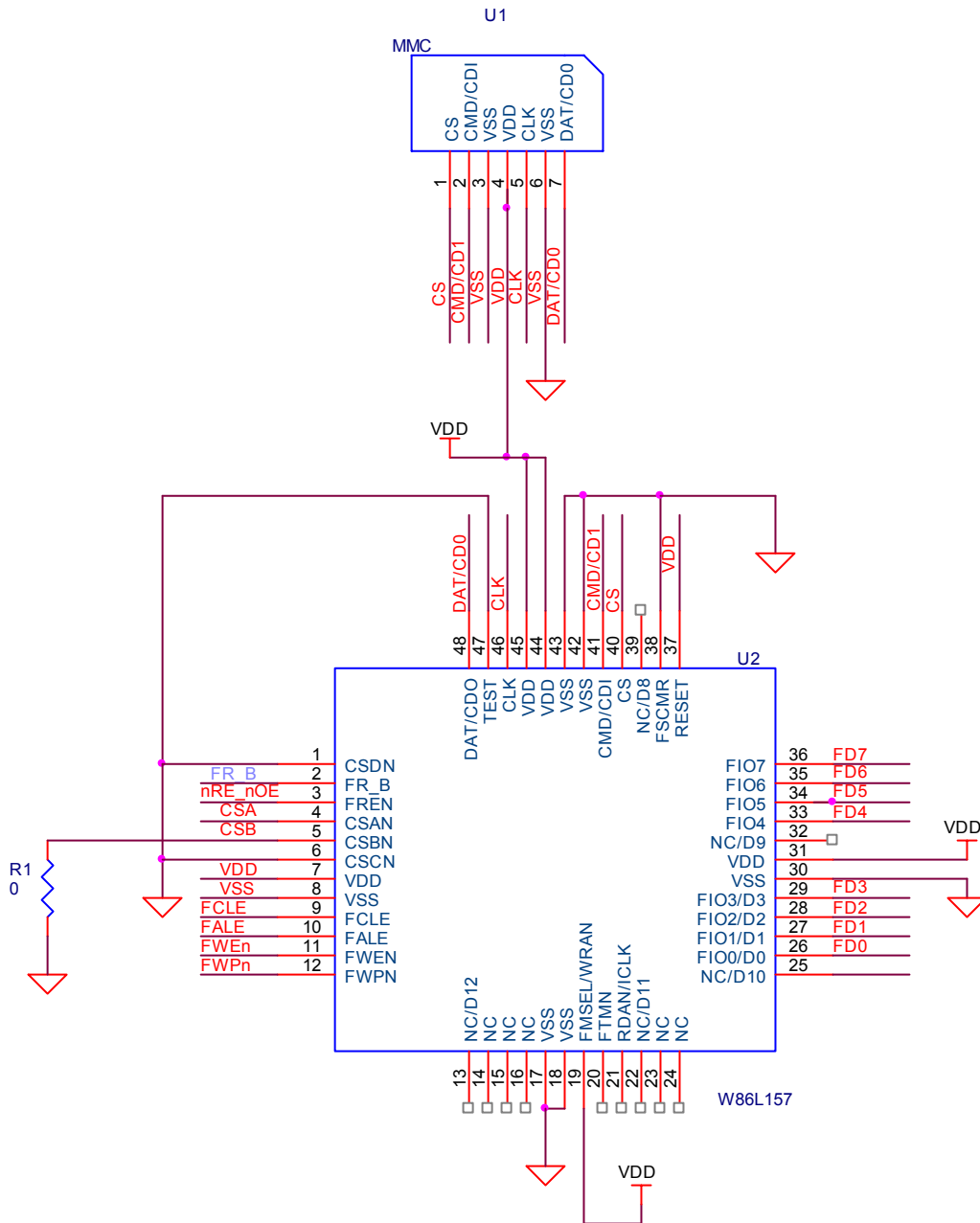
10.2 W86L157SY Reference Schematic

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```
                                    U3
        1  ┌─────────────────────────────┐  48
        2  │ NC                       NC  │  47
        3  │ NC                       NC  │  46
        4  │ NC                       NC  │  45
        5  │ NC                       NC  │  44    FD7
        6  │ NC                      I/O7 │  43    FD6
 FR_B   7  │ NC                      I/O6 │  42    FD5
nRE_nOE 8  │ R/B                     I/O5 │  41    FD4
 CSA    9  │ RE                      I/O4 │  40
 CSB    10 │ CE                       NC  │  39
        11 │ NC/CE2                   NC  │  38
VDD     12 │ NC                      PRE  │  37    VDD
        13 │ VCC                     VCC  │  36
        14 │ VSS                     VSS  │  35
        15 │ NC                       NC  │  34
 FCLE   16 │ NC                       NC  │  33
 FALE   17 │ CLE                      NC  │  32    FD3
 FWEn   18 │ ALE                     I/O3 │  31    FD2
 FWPn   19 │ WE                      I/O2 │  30    FD1
        20 │ WP                      I/O1 │  29    FD0
        21 │ NC                      I/O0 │  28
        22 │ NC                       NC  │  27
        23 │ NC                       NC  │  26
        24 │ NC                       NC  │  25
           └─────────────────────────────┘
                    Samsung
```
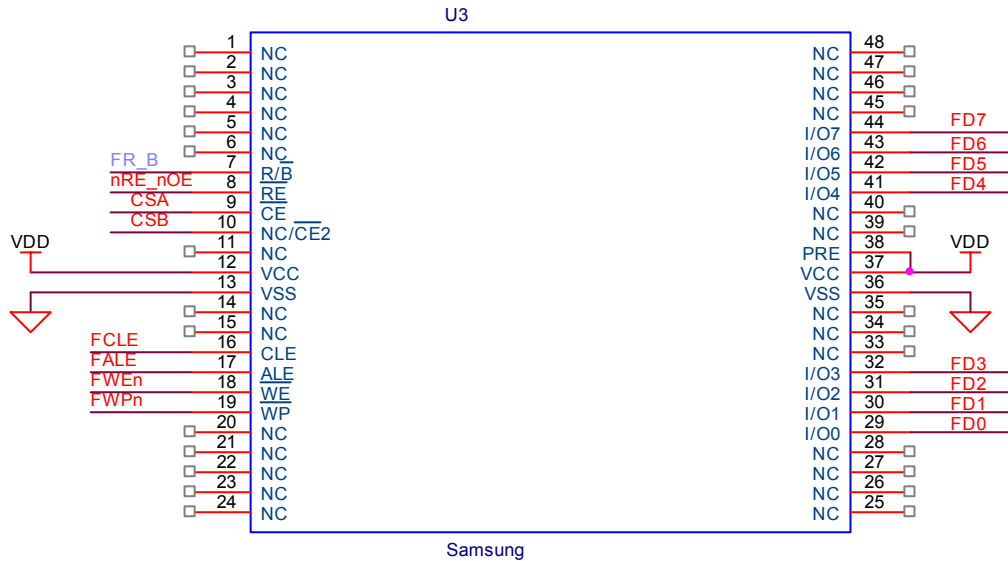
Categlory	One CE pin	Two CE pins
Schematic discription	CSBN connet to GND (R1: Short)	CSBN connect to Flash CE2 (Flash chip enable2) (R1: open)
Samsung Flash list	K9K4G08U0M,K9K2G08U0M, K9F2G08U0M,K9F1G08U0M, K9F1G08U0A,K9K1G08U0M, K9K1G08U0A,K9F1208U0M, K9F1208U0A, K9F5608U0C.	K9W8G08U1M K9W4G08U1M

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