128 MB to 8 GB ATA Flash PC Cards

FEATURES

- ATA-4 Compatibility
- Support for PCMCIA I/O, Memory and True-IDE Interfaces
- Form Factors: PC Card Type II
- Endurance Guarantee of 2,000,000 Write/Erase Cycles
- CIS (Card Information Structure) Programmed into 256 Bytes of Internal Memory
- Compatible with PC Card and Socket Services (Release 2.1 or later)
- 5V or 3.3V Power Supply
- Completely Solid-State (No Moving Parts)
- Standard ECC Engine
- 7 Year Warranty
- Other Features Available *(inquire for more information)*
  - *Power Down Protection.* A built-in feature that protects the card from losing data during a write operation when a lost of power or an unexpected removal from the host system occurred.
  - *Endurance Status Monitor.* A firmware option that allows applications to estimate the remaining life span of the device.
  - *Password Protection/Write Protection.* A custom utility software that allows the administrator and user to set passwords for up to four partitions.

GENERAL DESCRIPTION

The SimpleTech SLATAFLxxxJ(U)(I)-(F)(S) are Type II ATA Flash PC Cards with 128MB to 8GB of nonvolatile storage. The cards use a flash memory controller that provides a fully compatible ATA Flash PC Card interface for the flash memory.

SimpleTech OEM ATA Flash PC Cards are the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, ATA Flash PC Cards are reliable alternatives to mechanical hard disk drives for high availability and mission critical applications.

While the inherent ruggedness and reliability of solid state storage relative to rotating hard drives is intuitive, new applications for OEM ATA Flash PC Cards are emerging due to the low cost per usable megabyte. Most applications using embedded operating systems such as VxWorks™, Windows XP/embedded™, and Linux™ don't have multi-gigabyte data storage requirements, and therefore a cost savings can be realized when using this robust media.

ORDERING INFORMATION

Part Number	PC Card Form Factor	Capacity
• SLATAFL128J	Type II	128 MBytes
• SLATAFL256J	Type II	256 MBytes
• SLATAFL512J	Type II	512 MBytes
• SLATAFL1GBJ	Type II	1 GBytes
• SLATAFL2GBJ	Type II	2 GBytes
• SLATAFL3GBJ	Type II	3 GBytes
• SLATAFL4GBJ	Type II	4 GBytes
• SLATAFL5GBJ	Type II	5 GBytes
• SLATAFL6GBJ	Type II	6 GBytes
• SLATAFL7GBJ	Type II	7 GBytes
• SLATAFL8GBJ	Type II	8 GBytes

Option Designators

Options can be selected by using the Option Designators in the part number in the following format:

SLATAFLxxxJ(U)(I)-(F)(S)
where

U RoHS compliant lead free product

I Commercial Operating Temperature range: 0 to 70°C *(designator is BLANK)*
Industrial Operating Temperature range: -40 to 85°C *(designator=I)*

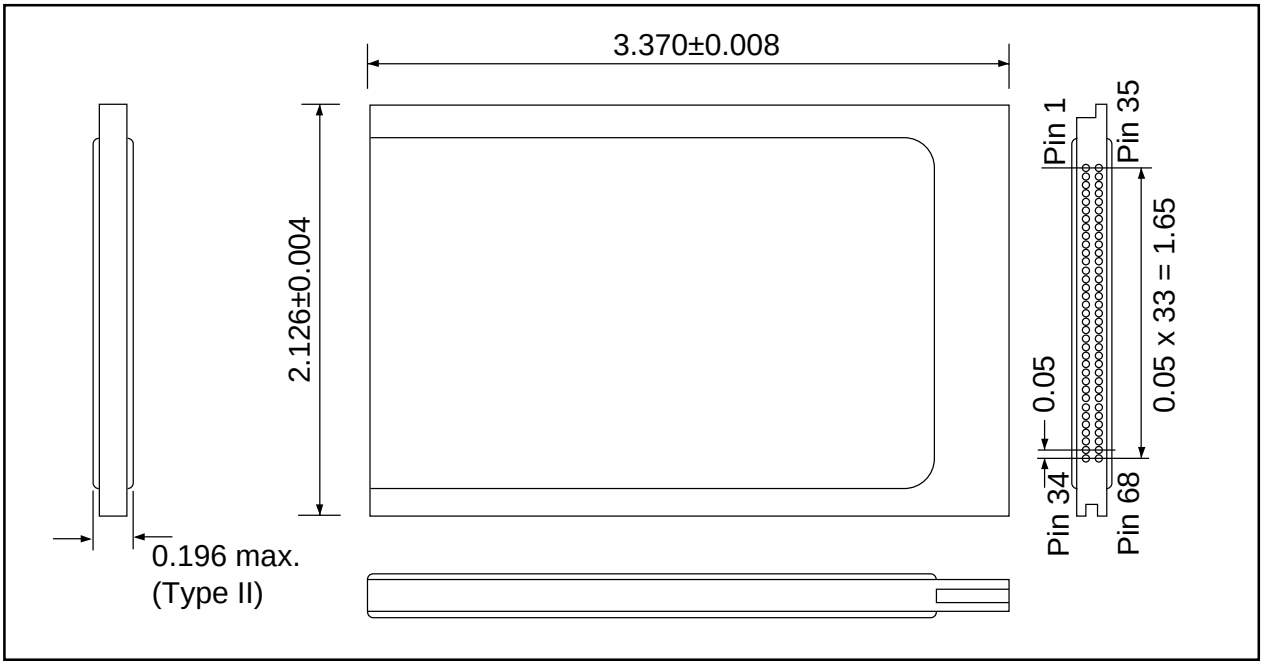
F Media set to fixed storage for non-removable IDE applications, e.g operating systems that require fixed device before the device can be used as a bootable drive.

S Optimized for applications that store small (1-4 sector) data packets e.g. transactional data acquisition.

PACKAGE DIMENSIONS AND PIN LOCATIONS

PC Card Type II

Length	3.370±0.008 in (85.60±0.20 mm)
Width	2.126±0.004 in (54.00±0.10 mm)
Thickness (including Label Area)	0.196 in max. (5.00 mm max.) (PC Card Type II)



PIN ASSIGNMENTS

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pint Type	Pin Num	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10	I
9	-OE	I	9	-OE	I	9	-SELATA	I
10	N/C		10	N/C		10	N/C	
11	A09	I	11	A09	I	11	A09	I
12	A08	I	12	A08	I	12	A08	I
13	N/C		13	N/C		13	N/C	
14	N/C		14	N/C		14	N/C	
15	-WE	I	15	-WE	I	15	-WE	I
16	RDY/-BSY	O	16	IREQ	O	16	INTRQ	O
17	VCC	Power	17	VCC	Power	17	VCC	Power
18	N/C		18	N/C		18	N/C	
19	N/C		19	N/C		19	N/C	
20	N/C		20	N/C		20	N/C	
21	N/C		21	N/C		21	N/C	
22	A07	I	22	A07	I	22	A07*	I
23	A06	I	23	A06	I	23	A06*	I
24	A05	I	24	A05	I	24	A05*	I
25	A04	I	25	A04	I	25	A04*	I
26	A03	I	26	A03	I	26	A03*	I
27	A02	I	27	A02	I	27	A02	I
28	A01	I	28	A01	I	28	A01	I
29	A00	I	29	A00	I	29	A00	I
30	D00	I/O	30	D00	I/O	30	D00	I/O
31	D01	I/O	31	D01	I/O	31	D01	I/O
32	D02	I/O	32	D02	I/O	32	D02	I/O
33	WP	O	33	-IOIS16	O	33	-IOCS16*	O
34	GND	Ground	34	GND	Ground	34	GND	Ground
35	GND	Ground	35	GND	Ground	35	GND	Ground
36	-CD1	O	36	-CD1	O	36	-CD1	O
37	D11	I/O	37	D11	I/O	37	D11	I/O
38	D12	I/O	38	D12	I/O	38	D12	I/O
39	D13	I/O	39	D13	I/O	39	D13	I/O
40	D14	I/O	40	D14	I/O	40	D14	I/O
41	D15	I/O	41	D15	I/O	41	D15	I/O
42	-CE2	I	42	-CE2	I	42	-CS1	I
43	-VS1	O	43	-VS1	O	43	-VS1*	O
44	-IORD	I	44	-IORD	I	44	-IORD	I
45	-IOWR	I	45	-IOWR	I	45	-IOWR	I
46	N/C		46	N/C		46	N/C	
47	N/C		47	N/C		47	N/C	
48	N/C		48	N/C		48	N/C	
49	N/C		49	N/C		49	N/C	
50	N/C		50	N/C		50	N/C	

(continued)

PIN ASSIGNMENTS *(continued)*

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin Num	**Signal Name**	**Pin Type**	**Pin Num**	**Signal Name**	**Pint Type**	**Pin Num**	**Signal Name**	**Pin Type**
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	N/C		52	N/C		52	N/C	
53	N/C		53	N/C		53	N/C	
54	N/C		54	N/C		54	N/C	
55	N/C		55	N/C		55	N/C	
56	-CSEL	I	56	-CSEL	I	56	-CSEL	I
57	-VS2	O	57	-VS2	O	57	-VS2*	O
58	RESET	I	58	RESET	I	58	-RESET	I
59	-WAIT	O	59	-WAIT	O	59	IORDY	O
60	-INPACK	O	60	-INPACK	O	60	Not Used	O
61	-REG	I	61	-REG	I	61	Not Used	I
62	BVD2	I/O	62	-SPKR	I/O	62	-DASP	I/O
63	BVD1	I/O	63	-STSCHG	I/O	63	-PDIAG	I/O
64	D08	I/O	64	D08	I/O	64	D08	I/O
65	D09	I/O	65	D09	I/O	65	D09	I/O
66	D10	I/O	66	D10	I/O	66	D10	I/O
67	-CD2	O	67	-CD2	O	67	-CD2	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

* Signals marked with an asterisk are not used in IDE mode.

SIGNAL DESCRIPTIONS

Signal Name	Dir	Pin	Description
BVD2 (PC Card Memory Mode)	I/O	62	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product produces no audio.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	36, 67	These Card Detect pins are connected to ground on the card. They are used by the host to determine that the card is fully inserted into the socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same as Memory Mode.
-CD1, -CD2 (True IDE Mode)			These signals are not used in IDE Mode.
D15-D00 (PC Card Memory Mode)	I/O	37, 38, 39, 40, 41, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	These lines carry the data, commands, and status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15-D00 (PC Card I/O Mode			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode)	I	45	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data onto the data bus and into the card controller registers. The clocking occurs on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IORD (PC Card Memory Mode)	I	44	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the card.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-WE (PC Card Memory Mode)	I	15	This is a signal driven by the host and used for strobing memory write data into the registers. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC.

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SIGNAL DESCRIPTIONS *(continued)*

Signal Name	Dir	Pin	Description
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-OE (True IDE Mode)			To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	16	In Memory Mode this signal is set high when the card is ready to accept a new data transfer operation and held low when the card is busy. The host memory card socket must provide a pull-up resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the card has completed its power up or reset function. No access of any type should be made to the card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: the card has been powered up with RESET continuously disconnected or asserted high.
-IREQ (PC Card I/O Mode)			After the card has been configured for I/O operation, this signal is used as the active low interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high interrupt request to the host.
A10-A0 (PC Card Memory Mode)	I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	These address lines along with the -REG signal are used to select the following: the I/O port address registers within the card, the memory mapped port address registers within the card, a byte in the card's information structure and the card's configuration control and status registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE Mode)		27, 28, 29	In True IDE Mode only, A2:A0 are used to select the one of eight registers in the Task File. The remaining address lines should be grounded.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 42	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS2 is used to select the Alternate Status Register and the Device Control Register.

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SIGNAL DESCRIPTIONS *(continued)*

Signal Name	Dir	Pin	Description
-CSEL (PC Card Memory Mode)	I	56	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure the card as a Master or a Slave. When the pin is grounded, the card is configured as a Master. When the pin is open, the card is configured as a Slave.
-REG (PC Card Memory Mode) Attribute Memory Select	I	61	This signal is distinguishes between accesses to Common Memory (high) and Register Attribute Memory (low).
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the bus.
Not Used (True IDE Mode)			This signal is not used in this mode.
WP (PC Card Memory Mode) Write Protect	O	33	The card does not have a write protect switch; therefore, this signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			Not defined in IDE Mode.
-INPACK (PC Card Memory Mode)	O	60	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the card when it is selected and responding to an I/O read cycle at the address that is on the bus. The host uses this signal to control the enable of any input data buffers between the card and the host's CPU.
Not Used (True IDE Mode)			This signal is not used in this mode.
BVD1 (PC Card Memory Mode)	I/O	63	This signal is asserted high as since a battery is not used with this product.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states. Its use is controlled by the Card Configuration and Status Register.
-PDIAG (True IDE Mode)			In True IDE Mode, this input/output signal is the Pass Diagnostic signal in the Master/Slave handshake protocol.

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SIGNAL DESCRIPTIONS *(continued)*

Signal Name	Dir	Pin	Description
-WAIT (PC Card Memory Mode)	O	59	This signal is not used by the card, and is pulled up to VCC through a 4.7K ohm resistor.
-WAIT (PC Card I/O Mode)			This signal is not used by the card, and is pulled up to VCC through a 4.7K ohm resistor.
IORDY (True IDE Mode)			This signal is not used by the card, and is pulled up to VCC through a 4.7K ohm resistor.
GND (PC Card Memory Mode)	—	1, 34, 35, 68	Ground
GND (PC Card I/O Mode)			Ground
GND (True IDE Mode)			Ground
VCC (PC Card Memory Mode)	—	17, 51	+5 V or 3.3V power
VCC (PC Card I/O Mode)			+5 V or 3.3V power
VCC (True IDE Mode)			+5 V or 3.3V power
RESET (PC Card Memory Mode)	I	58	When RESET is high, this signal resets the card. The card is reset only at power up if this signal is left high or open from power-up. The card can also be reset when the soft reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-VS1 -VS2 (PC Card Memory Mode)	O	43 57	-VS1 is grounded, and -VS2 is not connected so that the card CIS can be read at either 3.3 volts or 5.0 volts.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all models.
-VS1 -VS2 (True IDE Mode)			This signal is not used in IDE Mode.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin w.r.t. Vss	Vin, Vout	-0.5 to VCC+0.5	V
Storage Temperature range	Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Commercial operating temperature	Ta	0	25	70	°C
Industrial operating temperature	Ta	-40	—	85	°C
VCC voltage	VCC	4.75 3.18	5.0 3.3	5.25 3.465	V

PERFORMANCE

Item	Performance
Data Transfer Rate To/From Host	16.7 MBytes/s (burst)
Sustained Read	up to 5 MBytes/s
Sustained Write	up to 5 MBytes/s

RELIABILITY

Item	Value
Data Write/Erase Endurance	2 million cycles min.
Data reliability	1 in 10^{14} bits, read
Data retention	10 years

CHS PARAMETERS

Standard CHS Values			
Capacity	C	H	S
128MB	980	8	32
256MB	980	16	32
512MB	993	16	63
1GB	1986	16	63
2GB	3970	16	63
3GB	6022	16	63
4GB	7964	16	63
5GB	10038	16	63
6GB	12046	16	63
7GB	14054	16	63
8GB	16062	16	63
C=cylinders; H=heads; S=sectors/track			

CHS Values with -S optimized option			
Capacity	C	H	S
128MB	937	8	32
256MB	938	16	32
512MB	953	16	63
1GB	1908	16	63
2GB	3816	16	63
3GB	5725	16	63
4GB	7633	16	63
5GB	9542	16	63
6GB	11450	16	63
7GB	13359	16	63
8GB	15268	16	63
C=cylinders; H=heads; S=sectors/track			

ENVIRONMENTAL CHARACTERISTICS

Leaded Cards (without the "U" option)	
Shock:	2K G, half-sine, 0.330 ms to 0.750 ms (per MIL-STD-202G Method 213B, Condition A)
Vibration:	30 G 10Hz-2KHz (per MIL-STD-202G Method 204D 20 min/sweep, 12 sweeps/axis)
Humidity:	85°C 95% RH, 5.5V, 500 hrs
RoHS Compliant Lead Free Cards (with the "U" option)	
Shock:	1K G, half-sine, 0.330 ms to 0.750 ms (per MIL-STD-202G Method 213B, Condition A)
Vibration:	15 G 10Hz-2KHz (per MIL-STD-202G Method 204D 20 min/sweep, 12 sweeps/axis)
Humidity:	85°C 95% RH, 5.5V, 500 hrs

DC CHARACTERISTICS-1

(Ta= 0°C to 70°C for commercial temperature parts, or Ta = –40°C to 85°C for industrial temperature parts; VCC = 3.3V +5% or –3.6%)

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input LOW Voltage	-0.3	+0.8	V	
VIH	Input HIGH Voltage	2.0	VCC+0.3	V	
VOL	Output LOW Voltage		0.45	V	at 4mA
VOH	Output HIGH Voltage	2.4		V	at 1mA
ICC	Operating Current Sleep mode Operating		 800 30	 µA mA	
ILI	Input Leakage Current		10	µA	
ILO	Output Leakage Current		1	µA	
CI/O	Input/output Capacitance		25	pF	

DC CHARACTERISTICS-2

(Ta= 0°C to 70°C for commercial temperature parts, or Ta = –40°C to 85°C for industrial temperature parts; VCC = 5V±5%)

Symbol	Parameter	Min	Max	Units	Notes
VIL	Input LOW Voltage	-0.3	+0.8	V	
VIH	Input HIGH Voltage	2.0	VCC+0.3	V	
VOL	Output LOW Voltage		0.8	V	at 4mA
VOH	Output HIGH Voltage	4.0		V	at 1mA
ICC	Operating Current, VCC=5.0V Sleep mode Operating		 1200 30	 µA mA	
ILI	Input Leakage Current		10	µA	
ILO	Output Leakage Current		2	µA	
CI/O	Input/output Capacitance		25	pF	

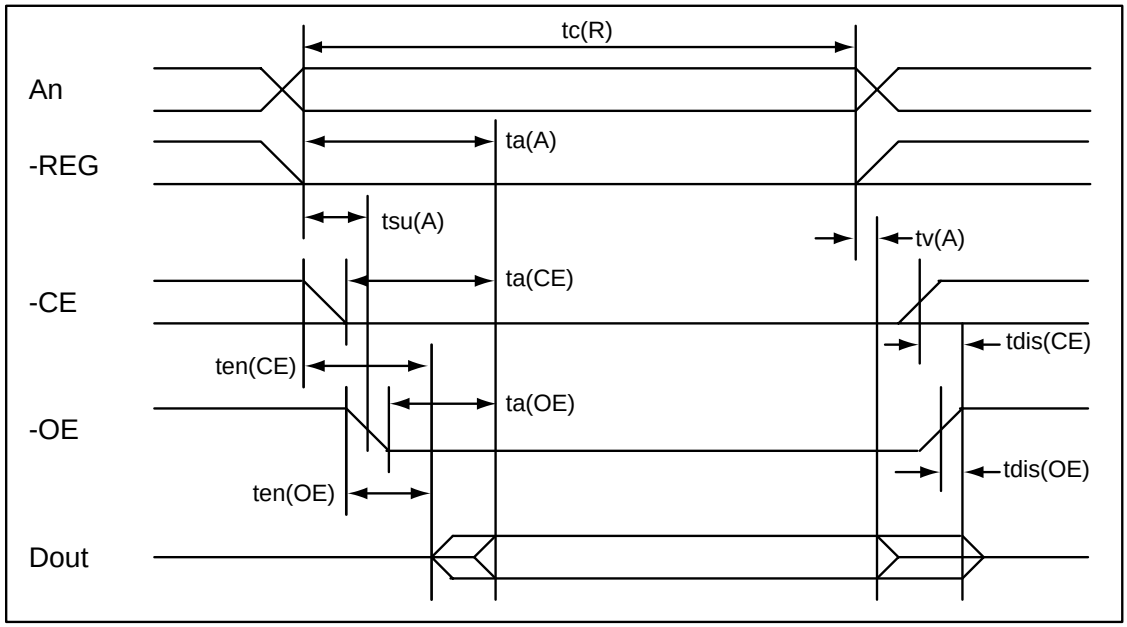
AC CHARACTERISTICS

(Ta = 0°C to 70°C for commercial temperature parts, or Ta = –40°C to 85°C for industrial temperature parts;
VCC = 5V±5% or VCC = 3.3V +5% or -3.6%)

Attribute Memory Read AC Characteristics

Speed Version:			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Read Cycle Time	tc(R)	tAVAV	250	
Address Access Time	ta(A)	tAVQV		250
Card Enable Access Time	ta(CE)	tELQV		225
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from -CE	tdis(CE)	tEHQZ		100
Output Disable Time from -OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from -CE	ten(CE)	tELQNZ	5	
Output Enable Time from -OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Attribute Memory Read Timings

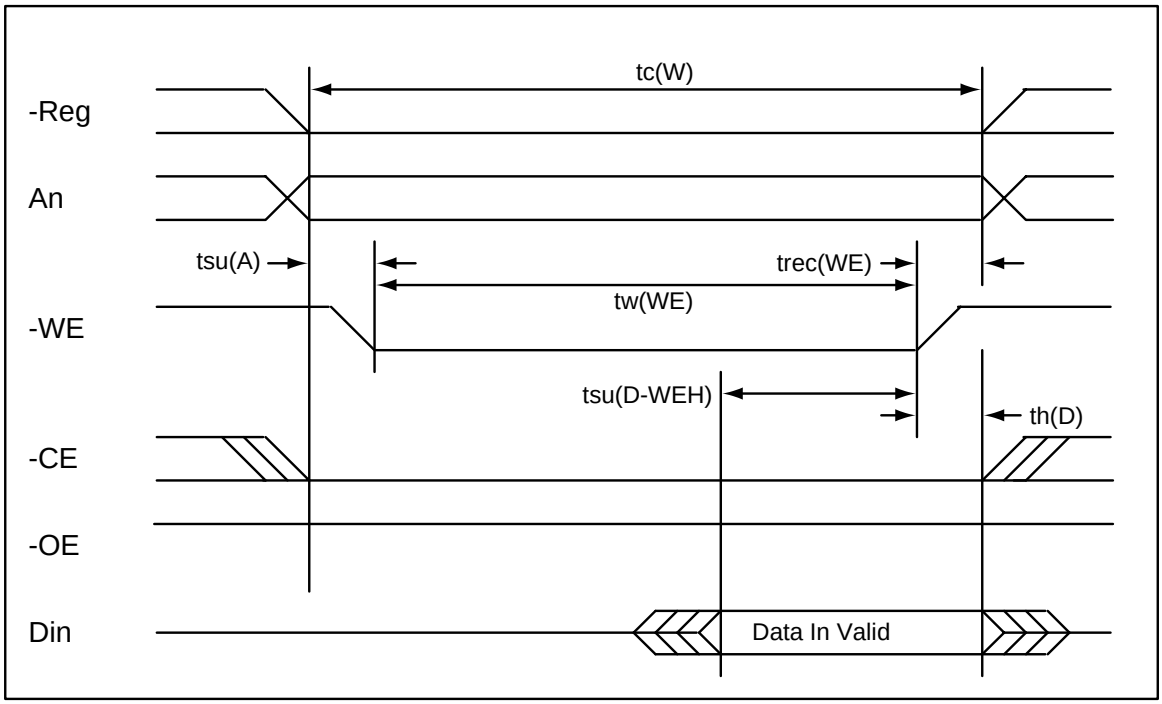


AC CHARACTERISTICS *(continued)*

Attribute Memory Write AC Characteristics

Speed Version:			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Data Setup Time for -WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	

Attribute Memory Write Timings



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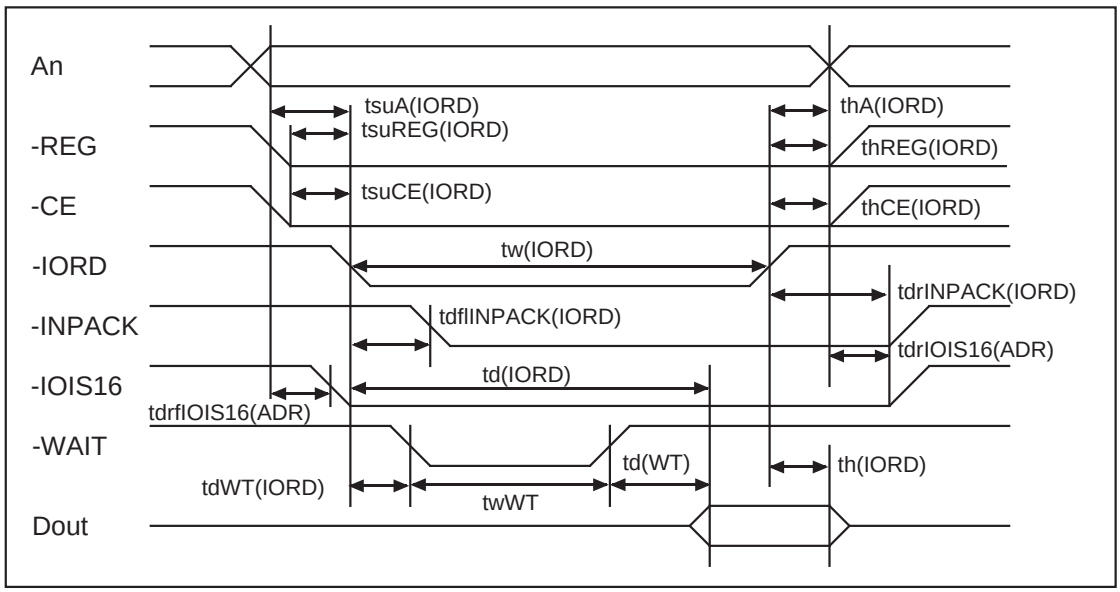
AC CHARACTERISTICS *(continued)*

I/O Access Read AC Characteristics

Cycle Time Mode:			250ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Data Delay after -IORD	td(IORD)	tIGLQV		100
Data Hold following -IORD	th(IORD)	tIGHQX	0	
-IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before -IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following -IORD	thA(IORD)	tIGHAX	20	
-CE Setup before -IORD	tsuCE(IORD)	tELIGL	5	
-CE Hold following -IORD	thCE(IORD)	tIGHEH	20	
-REG Setup before -IORD	tsuREG(IORD)	tRGLIGL	5	
-REG Hold following -IORD	thREG(IORD)	tIGHRGH	0	
-INPACK Delay Falling from -IORD	tdfINPACK(IORD)	tIGLIAL	0	45
-INPACK Delay Rising from -IORD	tdrINPACK(IORD)	tIGHIAH		45
-IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
-Wait Delay Falling from -IORD	tdWT(IORD)	tGLWTL		35
Data Delay from -Wait Rising	td(WT)	tWTHQV		0
-Wait Width Time	tw(WT)	tWTLWTH		350

I/O Access Read Timings



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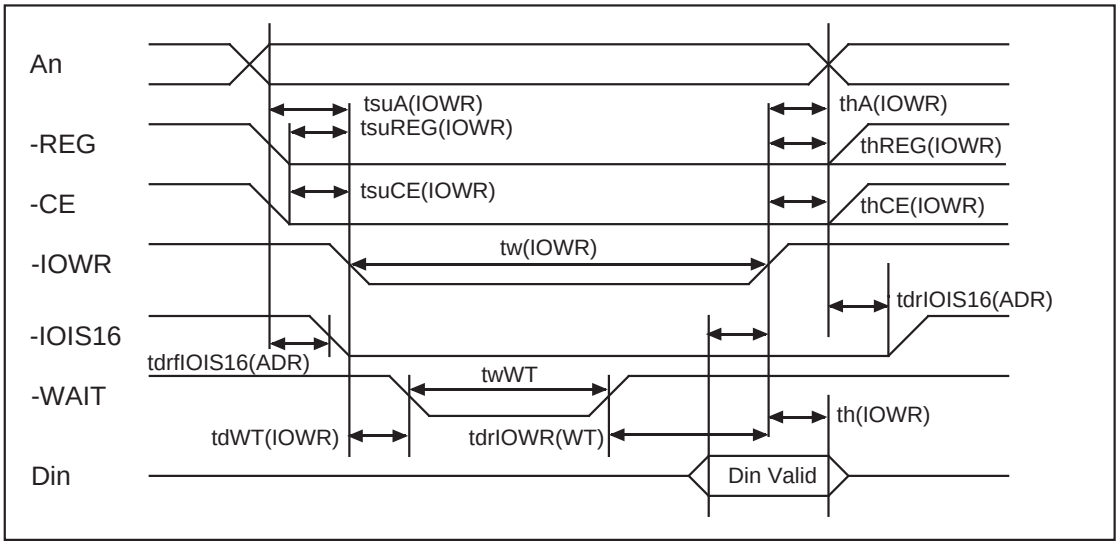
AC CHARACTERISTICS *(continued)*

I/O Access Write AC Characteristics

Cycle Time Mode:			255ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Data Setup before -IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following -IOWR	th(IOWR)	tIWHDX	30	
-IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before -IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following -IOWR	thA(IOWR)	tIWHAX	20	
-CE Setup before -IOWR	tsuCE(IOWR)	tELIWL	5	
-CE Hold following -IOWR	thCE(IOWR)	tIWHEH	20	
-REG Setup before -IOWR	tsuREG(IOWR)	tRGLIWL	5	
-REG Hold following -IOWR	thREG(IOWR)	tIWHRGH	0	
-IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
-IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
-Wait Delay Falling from -IOWR	tdWT(IOWR)	tIWLWTL		35
-IOWR high from -Wait high	tdrIOWR(WT)	tWTJIWH	0	
-Wait Width Time	tw(WT)	tWTLWTH		350

I/O Access Write Timings



(continued)

AC CHARACTERISTICS *(continued)*

Register Access AC Characteristics for True IDE

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time (min)	t_0	600	383	330	180	120	ns
Address valid to -IORD/-IOWR setup (min)	t_1	70	50	30	30	25	ns
-IORD/-IOWR pulse width 8bit (min)	t_2	290	290	290	80	70	ns
-IORD/-IOWR recovery time (min)	t_{2i}	—	—	—	70	25	ns
-IOWR data setup (min)	t_3	60	45	30	30	20	ns
-IOWR data hold (min)	t_4	30	20	15	10	10	ns
-IORD data setup (min)	t_5	50	35	20	20	20	ns
-IORD data hold (min)	t_6	5	5	5	5	5	ns
-IORD data tristate (max)	t_{6z}	30	30	30	30	30	ns
Address valid to -IOCS16 assert. (max)	t_7	90	50	40	n/a	n/a	ns
Address valid to -IOCS16 release (max)	t_8	60	45	30	n/a	n/a	ns
-IORD/-IOWR to address valid hold	t_9	20	15	10	10	10	ns

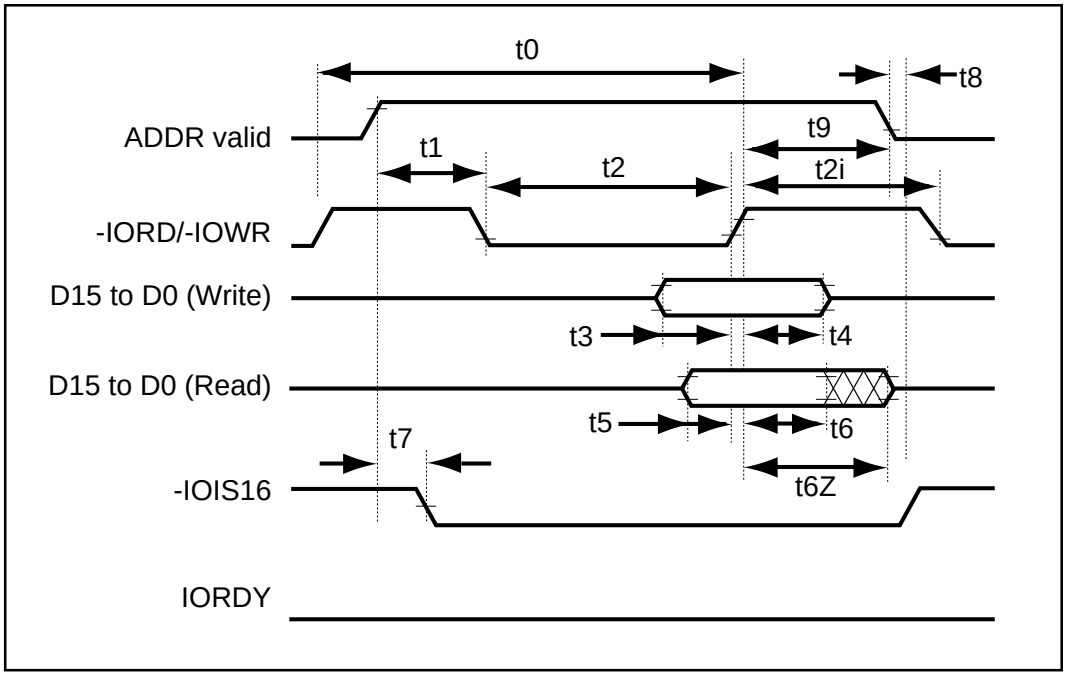
PIO Mode Access AC Characteristics for True IDE

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
Cycle time (min)	t_0	600	383	240	180	120	ns
Address valid to -IORD/-IOWR setup (min)	t_1	70	50	30	30	25	ns
-IORD/-IOWR pulse width 16bit (min)	t_2	165	125	100	80	70	ns
-IORD/-IOWR recovery time (min)	t_{2i}	-	-	-	70	25	ns
-IOWR data setup (min)	t_3	60	45	30	30	20	ns
IOWR data hold (min)	t_4	30	20	15	10	10	ns
-IORD data setup (min)	t_5	50	35	20	20	20	ns
-IORD data hold (min)	t_6	5	5	5	5	5	ns
-IORD data tristate (max)	t_{6z}	30	30	30	30	30	ns
Address valid to -IOCS16 assert. (max)	t_7	90	50	40	n/a	n/a	ns
Address valid to -IOCS16 release (max)	t_8	60	45	30	n/a	n/a	ns
-IORD/-IOWR to address valid hold	t_9	20	15	10	10	10	ns

(continued)

AC CHARACTERISTICS *(continued)*

True IDE Mode Access Read/Write Timings



HOST ACCESS SPECIFICATION

Attribute Access Specifications

The CIS can be accessed by Byte/Word/Odd-byte modes which are defined by PC Card card standard specifications. The -REG signal must be low when accessing the CIS.

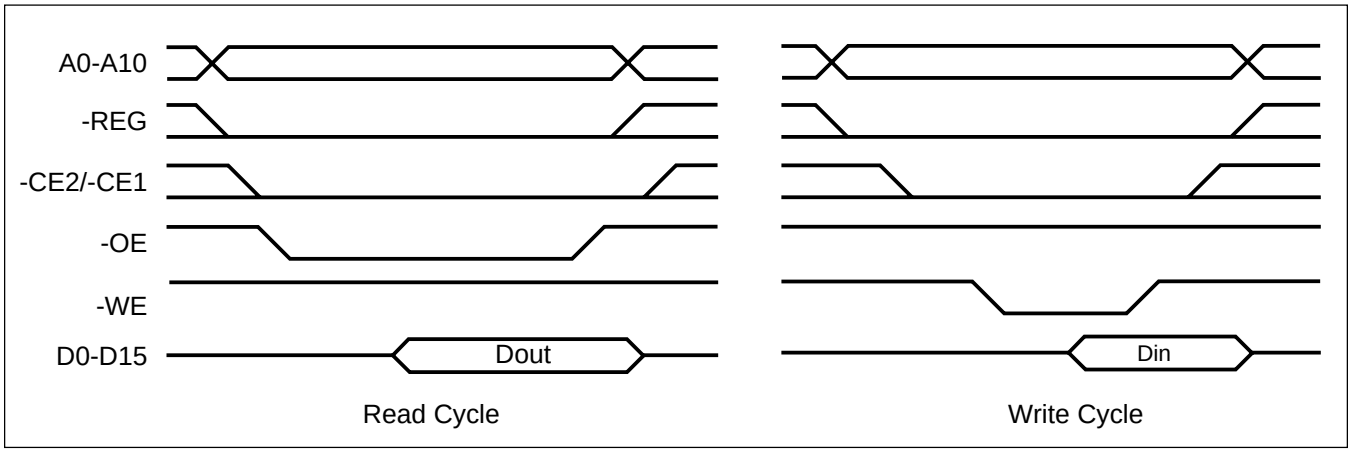
Attribute Read Access Mode

Function Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Access (8-bit)	L L	H H	L L	L H	L L	H H	High Z High Z	Even Byte Invalid
Word Access (16-bit)	L	L	L	x	L	H	Invalid	Even Byte
Odd Byte Access (8-bit)	L	L	H	x	L	H	Invalid	High Z
x: L or H								

Attribute Write Access Mode

Function Mode	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	Don't Care	Don't Care
Byte Access (8-bit)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Don't Care
Word Access (16-bit)	L	L	L	x	H	L	Don't Care	Even Byte
Odd Byte Access (8-bit)	L	L	H	x	H	L	Don't Care	Don't Care
x: L or H								

Attribute Access Timing Example



Task File Register Access Specifications

There are two cases of Task File register mapping, one is the mapped I/O address area, the other is mapped Memory address area. Task File register read and write operations are described in the charts below. The Task File register can be accessed by Byte/Word/Odd Byte mode which are defined by PC Card card standard specifications.

I/O Address Map

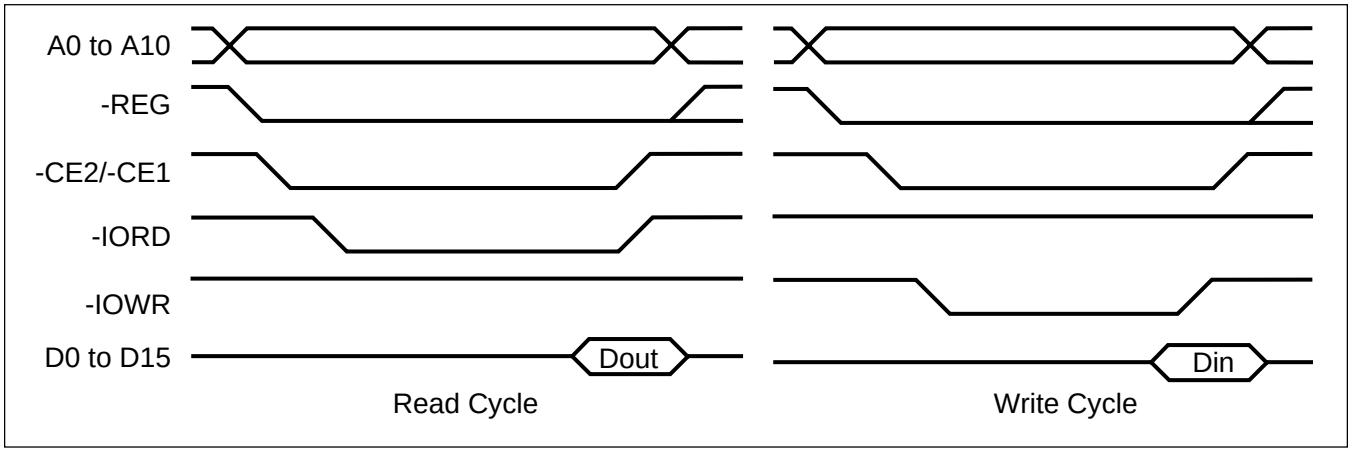
Task File Register Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D15-D8	D7-D0
Standby Mode	x	H	H	x	x	x	x	x	High Z	High Z
Byte Access (8 bit)	L L	H H	L L	L H	L L	H H	H H	H H	High Z High Z	Even-Byte Odd-Byte
Word Access (16-bit)	L	L	L	x	L	H	H	H	Odd-Byte	Even Byte
I/O Inhibit	H	x	x	x	L	H	H	H	High-Z	High-Z
Odd Byte Access (8-bit)	L	L	H	x	L	H	H	H	Odd-Byte	High-Z
x: L or H										

Task File Register Write Acess Mode

Mode	-REG	-CE2	-CE1	A0	-IORD	-IOWR	-OE	-WE	D15-D8	D7-D0
Standby Mode	x	H	H	x	x	x	x	x	Don't Care	Don't Care
Byte Access (8 bit)	L L	H H	L L	L H	H H	L L	H H	H H	Don't Care Don't Care	Even-Byte Odd-Byte
Word Access (16-bit)	L	L	L	x	H	L	H	H	Odd-Byte	Even Byte
I/O Inhibit	H	x	x	x	H	L	H	H	High-Z	High-Z
Odd Byte Access (8-bit)	L	L	H	x	H	L	H	H	Odd-Byte	Don't Care
x: L or H										

Task File Register Access Timing Example



Memory Address Map

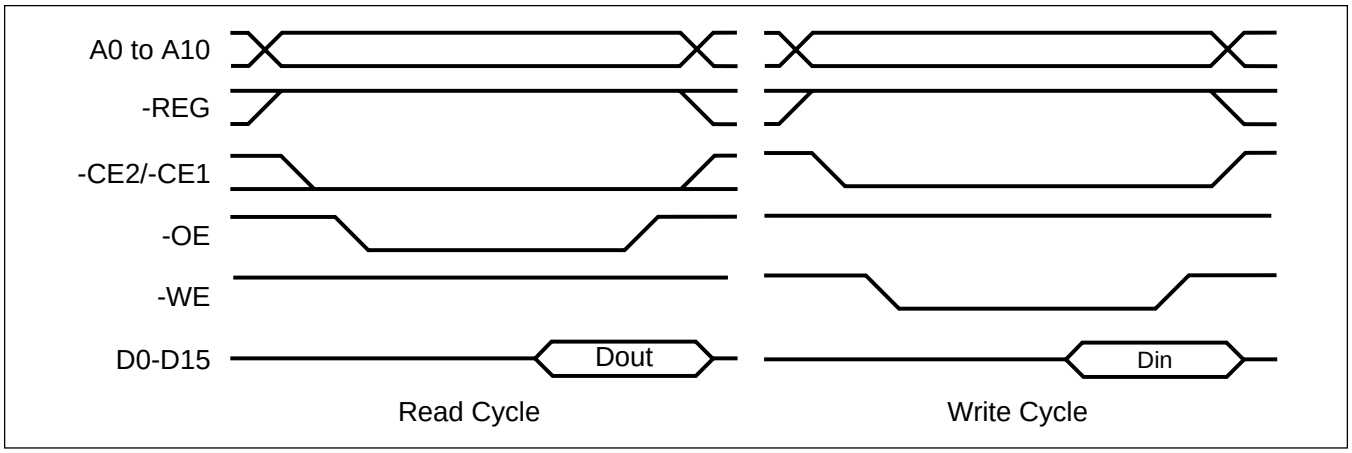
Task File Register Read Access Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	x	H	H	x	x	x	x	x	High Z	High Z
Byte Access (8 bit)	H H	H H	L L	L H	L L	H H	H H	H H	High Z High Z	Even-Byte Odd-Byte
Word Access (16-bit)	H	L	L	x	L	H	H	H	Odd-Byte	Even Byte
Odd Byte Access (8-bit)	H	L	H	x	L	H	H	H	Odd-Byte	High-Z
x: L or H										

Task File Register Write Acess Mode

Mode	-REG	-CE2	-CE1	A0	-OE	-WE	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	x	H	H	x	x	x	x	x	Don't Care	Don't Care
Byte Access (8 bit)	H H	H H	L L	L H	H H	L L	H H	H H	Don't Care Don't Care	Even-Byte Odd-Byte
Word Access (16-bit)	H	L	L	x	H	L	H	H	Odd-Byte	Even Byte
Odd Byte Access (8-bit)	H	L	H	x	H	L	H	H	Odd-Byte	Don't Care
x: L or H										

Task File Register Access Timing Example



True IDE Mode

The card is configured in a True IDE mode of operation when the -OE input signal is asserted GND by the host at power up. In the True IDE mode, Attribute Registers are not accessible from the host. The data register is accessed in word (16-bit) mode at power up. The card permits 8-bit accesses if the host issues a Set Feature Command to put the device in 8-bit mode.

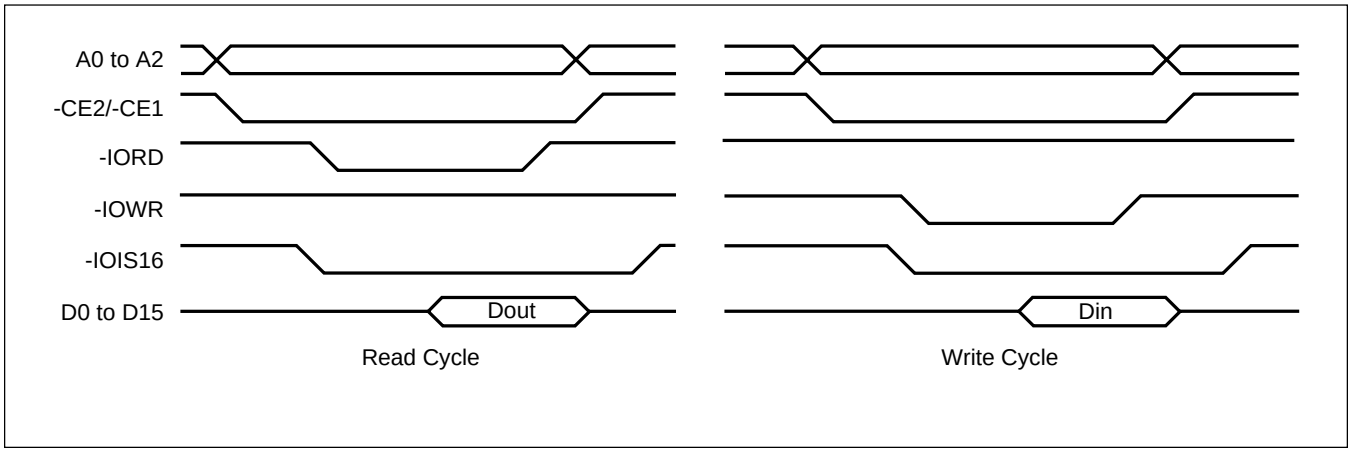
True IDE Mode Read I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	x	x	x	High Z	High Z
Standby Mode	H	H	x	x	x	High Z	High Z
Data Register Access	H	L	0	L	H	Odd-Byte	Even-Byte
Alternate Status Access	L	H	6h	L	H	High Z	Status Out
Other Task File Access	H	L	1-7h	L	H	High Z	Data
x: L or H							

True IDE Mode Write I/O Function

Mode	-CE2	-CE1	A0 to A2	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	x	x	x	Don't Care	Don't Care
Standby Mode	H	H	x	x	x	Don't Care	Don't Care
Data Register Access	H	L	0	H	L	Odd-Byte	Even-Byte
Control Register Access	L	H	6h	H	L	Don't Care	Control In
Other Task File Access	H	L	1-7h	H	L	Don't Care	Data
x: L or H							

True IDE Mode I/O Access Timing Example



CIS INFORMATION (TYPICAL)

0000: Code 01, link 03

D9 01 FF

Tuple CISTPL_DEVICE (01), length 3 (03) at offset 0

Device type is FUNCSPEC

Device speed is 250ns

Write protect switch is not in control

Device size is 2K bytes

0005: Code 1C, link 04

03 D9 01 FF

Tuple CISTPL_DEVICE_OC (1C), length 4 (04) at offset 5

Device conditions: minimum cycle with WAIT at Vcc = 3.3V

Device type is FUNCSPEC

Device speed is 250ns

Write protect switch is not in control

Device size is 2K bytes

000B: Code 18, link 02

DF 01

Tuple CISTPL_JEDEC_C (18), length 2 (02) at offset B

Device 0 JEDEC id: Manufacturer DF, ID 01

000F: Code 20, link 04

4D 01 00 01

Tuple CISTPL_MANFID (20), length 4 (04) at offset F

Manufacturer # 0x014D hardware rev 1.00

0015: Code 15, link 13

04 01 53 54 49 00 46 6C 61 73 68 20 37 2E 30 2E

30 00 FF

Tuple CISTPL_VERS_1 (15), length 19 (13) at offset 15

Major version 4, minor version 1

Product Information:

Manufacturer: "STI"

Product name: "Flash 7.0.0"

002A: Code 21, link 02

04 01

Tuple CISTPL_FUNCID (21), length 2 (02) at offset 2A

Function code 04 (Fixed Disk), system init 01

002E: Code 22, link 02

01 01

Tuple CISTPL_FUNCE (22), length 2 (02) at offset 2E

This is an PC Card ATA Disk

0032: Code 22, link 03

02 0C 0F

Tuple CISTPL_FUNCE (22), length 3 (03) at offset 32

Vpp is not required

This is a silicon device

Identify Drive Model/Serial Number is guaranteed unique

Low-Power Modes supported: Sleep Standby Idle

Drive automatically minimizes power

All modes include 3F7 or 377

Index bit is not supported

-IOIS16 is unspecified in Twin configurations

0037: Code 1A, link 05

01 03 00 02 0F

Tuple CISTPL_CONFIG (1A), length 5 (05) at offset 37

Last valid configuration index is 3

Configuration Register Base Address is 200

Configuration Registers Present:

Configuration Option Register at 200

Card Configuration and Status Register at 202

Pin Replacement Register at 204

Socket and Copy Register at 206

003E: Code 1B, link 08

C0 C0 A1 01 55 08 00 20

Tuple CISTPL_CFTABLE_ENTRY (1B), length 8 (08) at offset 3E

Configuration Table Index is 00 (default)

Interface type is Memory

BVDs not active, WP not active, RdyBsy active

Wait signal support required

Vcc Power Description:

Nom V = 5.0 V

map 2048 bytes of memory to card address 0

Miscellaneous Features:

Max Twins 0, -Audio, -ReadOnly, +PowerDown

0048: Code 1B, link 06

00 01 21 B5 1E 4D

Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 48

Configuration Table Index is 00

Vcc Power Description:

Nom V = 3.30 V

Peak I = 45.0 mA

0050: Code 1B, link 0A

C1 41 99 01 55 64 F0 FF FF 20

Tuple CISTPL_CFTABLE_ENTRY (1B), length 10 (0A) at offset 50

Configuration Table Index is 01 (default)

Interface type is I/O

BVDs not active, WP not active, RdyBsy active

Wait signal support not required

Vcc Power Description:

Nom V = 5.0 V

Decode 4 I/O lines, bus size 8 or 16

IRQ may be shared, pulse and level mode interrupts are supported

Interrupts in mask FFFF are supported

Miscellaneous Features:

Max Twins 0, -Audio, -ReadOnly, +PowerDown

005C: Code 1B, link 06

01 01 21 B5 1E 4D

Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 5C

Configuration Table Index is 01

Vcc Power Description:

Nom V = 3.30 V

Peak I = 45.0 mA

0064: Code 1B, link 0F

C2 41 99 01 55 EA 61 F0 01 07 F6 03 01 EE 20

Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 64

Configuration Table Index is 02 (default)

Interface type is I/O

BVDs not active, WP not active, RdyBsy active

Wait signal support not required

Vcc Power Description:

Nom V = 5.0 V

Decode 10 I/O lines, bus size 8 or 16

I/O block at 01F0, length 8

I/O block at 03F6, length 2

IRQ may be shared, pulse and level mode interrupts are supported

Only IRQ14 is supported

Miscellaneous Features:

Max Twins 0, -Audio, -ReadOnly, +PowerDown

0075: Code 1B, link 06

02 01 21 B5 1E 4D

Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 75

Configuration Table Index is 02

Vcc Power Description:

Nom V = 3.30 V

Peak I = 45.0 mA

007D: Code 1B, link 0F

C3 41 99 01 55 EA 61 70 01 07 76 03 01 EE 20

Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 7D

Configuration Table Index is 03 (default)

Interface type is I/O

BVDs not active, WP not active, RdyBsy active

Wait signal support not required

Vcc Power Description:

Nom V = 5.0 V

Decode 10 I/O lines, bus size 8 or 16

I/O block at 0170, length 8

I/O block at 0376, length 2

IRQ may be shared, pulse and level mode interrupts are supported

Only IRQ14 is supported

Miscellaneous Features:

Max Twins 0, -Audio, -ReadOnly, +PowerDown

008E: Code 1B, link 06

03 01 21 B5 1E 4D

Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 8E

Configuration Table Index is 03

Vcc Power Description:

Nom V = 3.30 V

Peak I = 45.0 mA

0096: Code 14, link 00

Tuple CISTPL_NO_LINK (14), length 0 (00) at offset 96

0098: Code FF

Tuple CISTPL_END (FF) at offset 98

CONFIGURATION REGISTER SPECIFICATION

This card supports four configuration registers for the purpose of the configuration and observation of the card. These registers can be used in memory card mode and I/O card mode. In True IDE mode, these registers can not be used.

Configuration Option Register (Address 200h)

This register is used to configure and observe the status of the card, and to issue soft resets to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRESET	LevlREQ	INDEX (bits 0-5)					
Initial Value: 00h							

Name	R/W	Function
SRESET (HOST->)	R/W	Setting this bit to "1" places the card in the reset state. This operation is equal to a hard reset, except this bit is not cleared.
LevlREQ (HOST->)	R/W	This bit is set to "0" when pulse mode interrupt is selected, and to "1" when level mode interupt is selected.
INDEX (HOST->)	R/W	These bits are used to select the operation mode of the card. (See table below.) At power on, hard reset, and soft reset, this data is "000000" for the purpose of Memory card interface recognition, and access to CIS.

INDEX bit								
5	4	3	2	1	0	Card Mode	Task File Register Address	Mapping Mode
0	0	0	0	0	0	Memory Card	0h to Fh, 400h to 7FFh	Memory Mapped
0	0	0	0	0	1	I/O Card	xx0h to xxFh	Contiguous I/O Mapped
0	0	0	0	1	0	I/O Card	1F0h to 1F7h, 3F6h to 3F7h	Primary I/O Mapped
0	0	0	0	1	1	I/O Card	170h to 177h, 376h to 377h	Secondary I/O Mapped

Configuration and Status Register (Address 202h)

This register is used for observing the card state.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
CHGED	SIGCHG	IOIS8	0	0	PWD	INTR	0
Initial Value: 00h							

Name	R/W	Function
CHGED (CARD->)	R	This bit indicates that CRDY/-BSY bit on Pin Replacement register is set to “1”. When the CHGED bit is set to “1”, the -STSCHG pin is held low if the SIGCHG bit is also set to “1” and the card configured for the I/O interface.
SIGCHG (HOST->)	R/W	This bit is set or reset by the host for enabling and disabling the status change signal (-STSCHG pin). When the card is configured to I/O card interface and this bit is set to “1”, -STSCHG pin is controlled by CHGED bit. If this bit is set to “0”, -STSCHG pin is kept high when the card is configured for I/O.
IOIS8 (HOST->)	R/W	The host sets this field to “1” when it can provide I/O cycles only with an 8 bit data bus (D7 to D0).
PWD (HOST->)	R/W	When this bit is set to “1”, the card enters sleep state (power down mode). When this bit is reset to “0”, the card transfers to idle state (active mode).
INTR (CARD->)	R	This bit indicates the internal state of the interrupt request. The bit is available whether the I/O card interface has been configured or not. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero.

Pin Replacement Register (Address 204h)

This register is used for providing the signal state of -IREQ when the card is configured as the I/O card interface.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	CRDY/-BSY	CWProt	1	1	RRDY/-BSY	RWProt
Initial Value: 0Ch							

Name	R/W	Function
CRDY/-BSY (HOST->)	R/W	This bit is set to "1" when the RRDY/-BSY bit changes state. This bit may also be written by the host.
CWProt (HOST->)	R	This bit is set to "1" when the RWProt changes state. This bit may also be written by the host.
RRDY/-BSY (HOST->)	R/W	This bit is used to determine the internal state of the RDY/BSY signal. This bit may be used to determine the state of the Ready/Busy as this pin has been reallocated for use as interrupt request on an I/O card.
RWProt (HOST->)	R	This bit indicates the write protect status. When set, indicates write protect. When cleared, indicates that write is enabled.

Socket and Copy Register (Address 206h)

This read and write register is used to identify the card from other cards. This register should be set by the host before this card's Configuration Option register is set.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	0	DRV#	1	1`	0	0
Initial Value: 00h							

Name	R/W	Function
DRV# (HOST->)	R/W	These fields are used to configure mulitple cards. When the host configures multiple cards, the card's copy number is written in this field. In this way, the host can perform the card's master/slave organization.

TASK FILE REGISTER SPECIFICATION

These registers are used for reading and writing data to the card. These registers are mapped four types by the configuration of INDEX in Configuration Option register. A fifth mapping, True IDE, is configured at power up if -OE is held low.

Memory Map (INDEX=0)

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=L	-WE=L
1	0	X	0	0	0	0	0	Data register	Data register
1	0	X	0	0	0	1	1	Error register	Feature register
1	0	X	0	0	1	0	2	Sector Count register	Sector Count register
1	0	X	0	0	1	1	3	Sector No. register	Sector No. register
1	0	X	0	1	0	0	4	Cylinder Low register	Cylinder Low register
1	0	X	0	1	0	1	5	Cylinder High register	Cylinder High register
1	0	X	0	1	1	0	6	Drive Head register	Drive Head register
1	0	X	0	1	1	1	7	Status register	Command register
1	0	X	1	0	0	0	8	Dup. Even RD Data reg.	Dup. Even WR Data reg.
1	0	X	1	0	0	1	9	Dup. Odd RD Data reg.	Dup. Odd WR Data reg.
1	0	X	1	1	0	1	D	Dup. Error register	Dup. Feature register
1	0	X	1	1	1	0	E	Alt Status register	Device Ctl register
1	0	X	1	1	1	1	F	Drive Address register	Reserved
1	1	X	X	X	X	0	8	Even Data register	Even Data register
1	1	X	X	X	X	1	9	Odd Data register	Odd Data register

Contiguous I/O Map (INDEX=1)

-REG	A10-A4	A3	A2	A1	A0	Offset	-IORD=L	-IOWR=L
0	X	0	0	0	0	0	Data register	Data register
0	X	0	0	0	1	1	Error register	Feature register
0	X	0	0	1	0	2	Sector Count register	Sector Count register
0	X	0	0	1	1	3	Sector No. register	Sector No. register
0	X	0	1	0	0	4	Cylinder Low register	Cylinder Low register
0	X	0	1	0	1	5	Cylinder High register	Cylinder High register
0	X	0	1	1	0	6	Drive Head register	Drive Head register
0	X	0	1	1	1	7	Status register	Command register
0	X	1	0	0	0	8	Dup. Even RD Data reg.	Dup. Even WR Data reg.
0	X	1	0	0	1	9	Dup. Odd RD Data reg.	Dup. Odd WR Data reg.
0	X	1	1	0	1	D	Dup. Error register	Dup. Feature register
0	X	1	1	1	0	E	Alt Status register	Device Ctl register
0	X	1	1	1	1	F	Drive Address register	Reserved

Primary I/O Map (INDEX=2)

-REG	A10	A9-A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	1Fh	0	0	0	0	Data register	Data register
0	X	1Fh	0	0	0	1	Error register	Feature register
0	X	1Fh	0	0	1	0	Sector Count register	Sector Count register
0	X	1Fh	0	0	1	1	Sector No. register	Sector No. register
0	X	1Fh	0	1	0	0	Cylinder Low register	Cylinder Low register
0	X	1Fh	0	1	0	1	Cylinder High register	Cylinder High register
0	X	1Fh	0	1	1	0	Drive Head register	Drive Head register
0	X	1Fh	0	1	1	1	Status register	Command register
0	X	1Fh	0	1	1	0	Alt Status register	Device Ctl register
0	X	1Fh	0	1	1	1	Drive Address register	Reserved

Secondary I/O Map (INDEX=3)

-REG	A10	A9-A4	A3	A2	A1	A0	-IORD=L	-IOWR=L
0	X	17h	0	0	0	0	Data register	Data register
0	X	17h	0	0	0	1	Error register	Feature register
0	X	17h	0	0	1	0	Sector Count register	Sector Count register
0	X	17h	0	0	1	1	Sector No. register	Sector No. register
0	X	17h	0	1	0	0	Cylinder Low register	Cylinder Low register
0	X	17h	0	1	0	1	Cylinder High register	Cylinder High register
0	X	17h	0	1	1	0	Drive Head register	Drive Head register
0	X	17h	0	1	1	1	Status register	Command register
0	X	37h	0	1	1	0	Alt Status register	Device Ctl register
0	X	37h	0	1	1	1	Drive Address register	Reserved

True IDE Mode I/O Map (-OE held low at power up)

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	Data register	Data register
1	0	0	0	1	Error register	Feature register
1	0	0	1	0	Sector Count register	Sector Count register
1	0	0	1	1	Sector No. register	Sector No. register
1	0	1	0	0	Cylinder Low register	Cylinder Low register
1	0	1	0	1	Cylinder High register	Cylinder High register
1	0	1	1	0	Drive Head register	Drive Head register
1	0	1	1	1	Status register	Command register
0	1	1	1	0	Alt Status register	Device Control register
0	1	1	1	1	Drive Address register	Reserved

Data Register

The Data Register is a 16 bit read/write register used for transferring data between the card and the host. This register can be accessed in word mode and byte mode.

bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
D0 to D15															

Error Register

This read only register is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to "0" (Ready).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

bit	Name	Function
7	BBK (Bad Block Detected)	This bit is set when a Bad Block is detected in requested ID field—not supported
6	UNC (Data ECC Error)	This bit is set when an Uncorrectable error has occurred when reading the card.
4	IDNF (ID Not Found)	The requested sector ID is in error or cannot be found.
2	ABRT (ABoRTed Command)	Drive status error or Aborted invalid command
0	AMNF (Address Mark Not Found)	This bit is set in case of a general error.

Diagnostic Code	Description
01h	No error detected
02h	Formatting error
03h	Sector buffer error
04h	ECC error
05h	Microprocessor error
8xh	Drive 1 failed (not used)

Feature Register

This write only register provides information regarding the features of the card which the host wishes to utilize. See details under the SET FEATURE command.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Byte							

Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in the register is 0, a count of 256 sectors is indicated.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector Count Byte							

Sector Number Register

When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Sector Number Byte or bits 7:0 of the LBA							

Cylinder Low Register

In CHS mode (LBA=0), this register contains the low order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder Low Byte or bits 15:8 of the LBA							

Cylinder High Register

In CHS mode (LBA=0), this register contains the high order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Cylinder High Byte or bits 23:16 of the LBA							

Drive/Head Register

This register select the device address translation (CHS or LBA) and provides head address (CHS) or high order address bits 27:24 for LBA.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1	LBA	1	DRV	Head No. or LBA bits 27:24			

bit	Name	Function
7	1	This bit is set to “1”.
6	LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows: LBA07-LBA00: Sector Number Register D7-D0 LBA15-LBA08: Cylinder Low Register D7-D0 LBA23-LBA16: Cylinder High Register D7-D0 LBA27-LBA24: Drive/Head Register bits HS3-HS0
5	1	This bit is set to “1”.
4	DRV (DRiVe select)	This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register.
3-0	Head Number (HS3-HS0)	These bits are used for selecting the Head number. Bit 3 is MSB. In LBA mode, these bits represent the LBA address 27:24.

Status Register

This read only register indicates status of a command execution. When the BSY bit is "0", the other bits are valid; when the BSY bit is "1", the other bits are not valid. When the register is read, the interrupt (-IREQ pin) is cleared.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

bit	Name	Function
7	BSY (BuSY)	This bit is set when the card internal operation is executing. When this bit is set to "1", other bits in this register are invalid.
6	DRDY (Drive ReaDY)	If this bit and DSC bit are set to "1", the card is capable of receiving the read and write or seek requests. If this bit is set to "0", the card prohibits these requests. On error, DRDY changes only after the host reads the Status Register.
5	DWF (Drive Write Fault)	This bit is set if a fault occurs during the write process.
4	DSC (Drive Seek Complete)	This bit is set when the requested sector was found.
3	DRQ (Data ReQuest)	This bit is set when information can be transferred between the host and data register.
2	CORR (CORRected data)	This bit is set when a correctable data error has occurred and the data has been corrected.
1	IDX (InDeX)	This bit is always set to "0".
0	ERR (ERRor)	This bit is set when the previous command has ended in some type of error. The error information is set in the Error register.

Alternate Status Register

This register is the same as the Status register except that -IREQ is not negated when data is read.

Command Register

This write only register is used for writing the command that executes the card's operation. The command code is written in the command register after its parameters are written in the Task File during the card ready state. See details under the ATA COMMAND SPECIFICATIONS.

Device Control Register

This write only register is used for controlling the interrupt request and issuing an ATA soft reset to the card.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	x	1	SRST	nIEN	0

bit	Name	Function
7-4	x	Don't care.
3	1	This bit is set to "1".
2	SRST (Software ReSeT)	This bit is set to "1" in order to force the card to perform an AT disk control soft reset operation.
1	nIEN (Interrupt ENable)	When set to "0", it enables interrupts to the host (using the -IREQ tri-state pin). When inactive (set to "1") or drive is not selected, it disables all pending interrupts (-IREQ in high-Z). This bit is ignored in memory mode.
0	0	This bit is set to "0".

Drive Address Register

This read only register is used for confirming the card's status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host's I/O space because of potential conflicts on bit 7.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
High-Z	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

bit	Name	Function
7	x	This bit is unused.
6	nWTG (WriTing Gate)	This bit is unused.
5-2	nHS3-0 (Head Select 3-0)	These bits are the negative value of the Head Select bits (bit 3 to 0) in the Drive/Head register
1	nDS1 (Drive Select 1)	When set to "0", drive 1 is active and selected.
0	nDS0 (Drive Select 0)	When set to "0", drive 0 is active and selected.

ATA COMMAND SPECIFICATIONS

This table with the following paragraphs summarizes the ATA command set.

No.	Command set	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check Power Mode	E5h or 98h	—	Y	—	—	Y	—	—
2	Execute Drive Diagnostic	90h	—	—	—	—	Y**	—	—
3	Erase Sector(s)	C0h	—	Y	Y	Y	Y	Y	Y
4	Format Track	50h	—	Y	—	Y	Y	Y	Y
5	Identify Drive	ECh	Y	—	—	—	Y	—	—
6	Idle	E3h or 97h	—	Y	—	—	Y	—	—
7	Idle Immediate	E1h or 95h	—	—	—	—	Y	—	—
8	Initialize Drive Parameters	91h	—	Y	—	—	Y	Y	—
9	Read Buffer	E4h	—	—	—	—	Y	—	—
10	Read Multiple	C4h	—	Y	Y	Y	Y	Y	Y
11	Read Long Sector	22h or 23h*	—	—	Y	Y	Y	Y	Y
12	Read Sector(s)	20h or 21h*	—	Y	Y	Y	Y	Y	Y
13	Read Verify Sector(s)	40h or 41h*	—	Y	Y	Y	Y	Y	Y
14	Recalibrate	1Xh	—	—	—	—	Y	—	—
15	Request Sense	03h	—	—	—	—	Y	—	—
16	Seek	7Xh	—	—	Y	Y	Y	Y	Y
17	Set Features	EFh	—	Y	Y	Y	Y	Y	—
18	Set Multiple Mode	C6h	—	Y	—	—	Y	—	—
19	Set Sleep Mode	E6h or 99h	—	—	—	—	Y	—	—
20	Stand By	E2h or 96h	—	Y	—	—	Y	—	—
21	Stand By Immediate	E0h or 94h	—	—	—	—	Y	—	—
22	Translate Sector	87h	—	Y	Y	Y	Y	Y	Y
23	Wear Level	F5h	—	—	—	—	Y	Y	—
24	Write Buffer	E8h	—	—	—	—	Y	—	—
25	Write Long Sector	32h or 33h*	—	Y	Y	Y	Y	Y	Y
26	Write Multiple	C5h	—	Y	Y	Y	Y	Y	Y
27	Write Multiple w/o Erase	CDh	—	Y	Y	Y	Y	Y	Y
28	Write Sector(s)	30h or 31h*	—	Y	Y	Y	Y	Y	Y
29	Write Sector(s) w/o Erase	38h	—	Y	Y	Y	Y	Y	Y
30	Write Verify	3Ch	—	Y	Y	Y	Y	Y	Y

FR=Features Register, SC=Sector Count Register (00h to FFh), SN=Sector Number Register (01h to 20h), CY=Cylinder Registers, DR=Drive bit of Drive/Head Register, HD=Head no. (0 to 3) of Drive/Head Register, LBA=Logical Block Address Mode Supported.

Y—Set up.

"—" —Not set up.

* First command code=with retry, Second command code=without retry.

** Address to drive 0. Both drives execute command

Check Power Mode (code: E5h or 98h)

This command checks the power mode.

Execute Drive Diagnostic (code: 90h)

This command performs the internal diagnostic tests implemented by the card. See ERROR register for dianostic codes.

Erase Sector(s) (code: C0h)

This command is used to pre-erase and condition data sectors in advance.

Format Track (code: 50h)

This command writes the desired head and cylinder of the selected drive with a vender unique data pattern (typically 00h or FFh). This card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.

Identify Drive (code: ECh)

This command enables the host to receive parameter information from the card. (See tables on the next page.)

Idle (code: E3h or 97h)

This command causes the card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

Idle Immediate (code: E1h or 95h)

This command causes the card to set BSY, enter the Idle (Read) mode, clear BSY, and generate an interrupt.

Initialize Drive Parameters (code: 91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

Read Buffer (code: E4h)

This command enables the host to read the current contents of the card's sector buffer.

Read Multiple (code: C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Read Long Sector (code: 22h or 23h)

This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

Read Sector(s) (code: 20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

Read Verify Sector(s) (code: 40h or 41h)

This command verifies one or more sectors on the card by transferring data from the flash media to the data buffer in the card and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

Recalibrate (code: 1Xh)

The card performs only the interface timing and register operations. When this command is issued, the card sets BSY and waits for an appropriate length of time after which it clears BSY and issues an interrupt. When this command ends normally, the card is initialized.

Identify Drive Information (Typical)

Word Address	Data	Total Bytes	Description
0	848AH	2	General configuration bit-significant information (value=044AH for versions with the -F suffix)
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per track
5	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7-8	XXXXH	4	Number of sectors per card (word 7 = MSW, word 8 = LSW)
9	0000H	2	Reserved
10-19	XXXXH	20	Serial Number (see table below for definition)
20	XXXXH	2	Do not use this word. Before retirement, was buffer type
21	XXXXH	2	Do not use this word. Before retirement, was buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23-46	XXXXH	48	Firmware revision and model number in ASCII (see table below for definition)
47	0001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0200H	2	DMA not supported, LBA supported
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single word DMA data transfer cycle timing mode (not supported)
53	0003h	2	Words 54 - 58 and 64 - 70 are valid
54	XXXXH	2	Number of Current Cylinders
55	XXXXH	2	Number of Current Heads
56	XXXXH	2	Number of Current Sectors Per Track
57	XXXXH	2	LSW of the Current Capacity in Sectors
58	XXXXH	2	MSW of the Current Capacity in Sectors
59	010XH	2	Current Setting for Block Count=1 for R/W Multiple commands
60-61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not supported
63	0000H	2	Multiword DMA modes not supported
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0000H	2	Minimum multiword DMA transfer cycle time per word (ns)
66	0000H	2	Recommended multiword DMA transfer cycle time per word (ns)
67	0078H	2	Minimum PIO transfer without flow control
68	0078H	2	Minimum PIO transfer with IORDY flow control
69-255	0000H	388	Reserved

XXXXH: These values are dependent upon the the specific card.

Identify Drive Information (continued)

(Serial Number, Firmware Revision, and Model Number)

Serial Number Format (typical): Words 10-19

SimpleTech Proprietary	Yr	Day	Hr	Min	Sec
STI_J13C0	*04*	*224*	*09*	*27*	*50*

Firmware Revision: Words 23-26

mm/dd/yy

Model Number: Words 27-46

STI Flash X.Y.Z

Request Sense (code: 03h)

This command requests an extended error code after a command ends with an error. Refer to table below.

Code	Description
00H	No error detected
01H	Self test OK (No error)
09H	Miscellaneous Error - N/A
20H	Invalid Command
21H	Invalid Address (requested Head or Sector invalid)
2FH	Address Overflow (address too large)
35H, 36H	Supply or generate Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Correctable ECC Error - N/A
05H, 30H-34H, 37H, 3EH	Self Test Diagnostic Failed
10H, 14H	ID Not Found - N/A
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format - N/A
03H	Write / Erase Failed - N/A
22H	Power Level 1 Disabled

Seek (code: 7Xh)

This command is effectively a NOP command to the Card although it does perform a range check.

Set Features (code: EFh)

This command is used by the host to establish or select certain features.

Feature	Description
01H	Enable 8-bit data transfers
55H	Disable Read Look Ahead
66H	Disable Power on Reset (POR) establishment of defaults at Soft Reset
81H	Disable 8-bit data transfers
BBH	4bytes of data apply on Read/Write Long commands
CCH	Enable Power on Reset (POR) establishment of default at Soft Reset

Set Multiple Mode (code: C6h)

This command enables the card to perform Read and Write Multiple operations and establishes the block count for these commands.

Set Sleep Mode (code: E6h or 99h)

This is the only command that allows the host to set the card into Sleep mode. When the card is set to sleep mode, the card clears the BSY line and issues an interrupt. The card enters sleep mode and the only method to make the card active again (back to normal operation) is by performing a hardware reset or a software reset.

Stand By (code: E2h or 96h)

This command is sets the card in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the card returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.

Stand By Immediate (code: E0h or 94h)

This command causes the card to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

Translate Sector (code: 87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.

Wear Level (code: F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.

Write Buffer (code: E8h)

This command enables the host to overwrite the contents of the card's sector buffer with any data pattern desired.

Write Long Sector (code: 32h or 33h)

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

Write Multiple (code: C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

Write Multiple without Erase (code: CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before the write operation is not performed. Note that before using this command, it is required to erase the repective sectors using the Erase Sectors command.

Write Sector(s) (code: 30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

Write Sector(s) without Erase (code: 38h)

This command is similar to the Write Sector(s) command with the exception that an implied erase before the write operation is not performed. Note that before using this command, it is required to erase the repective sectors using the Erase Sectors command.

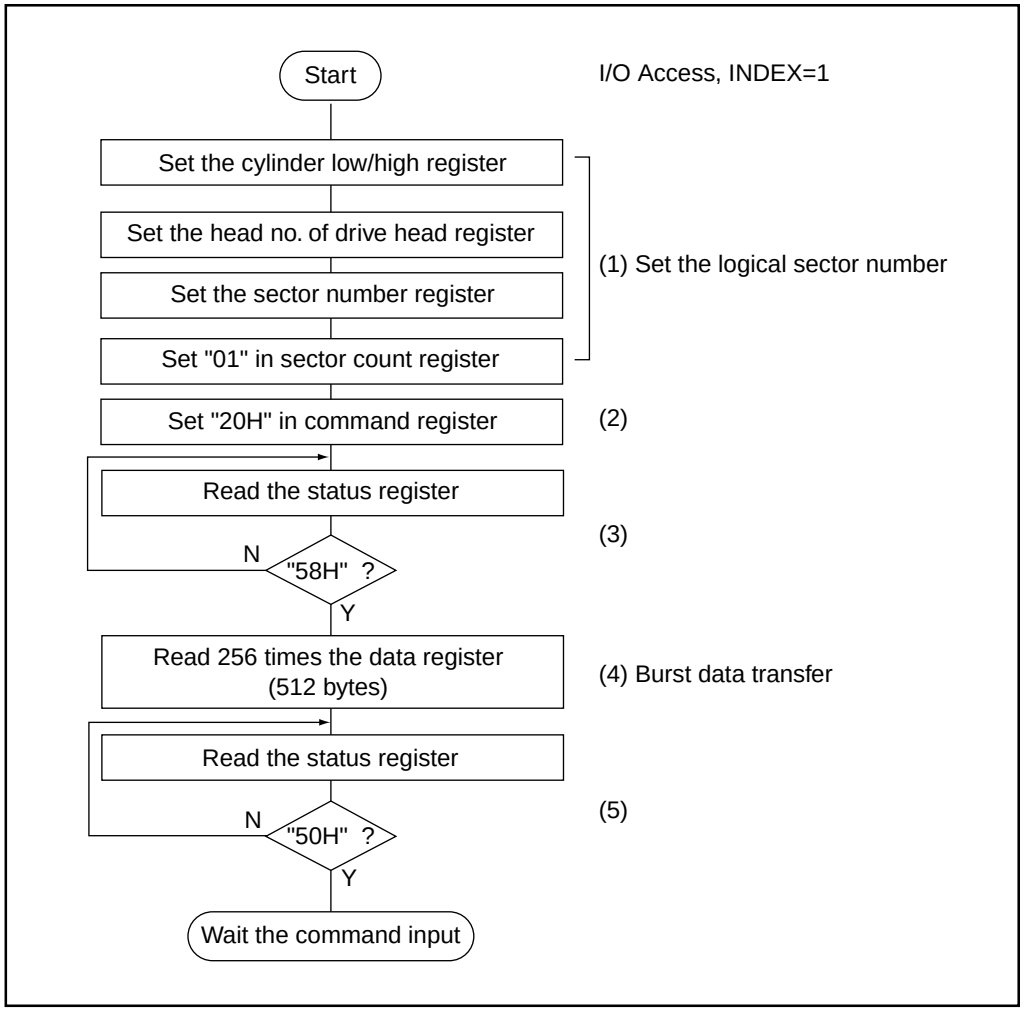
Write Verify (code: 3Ch)

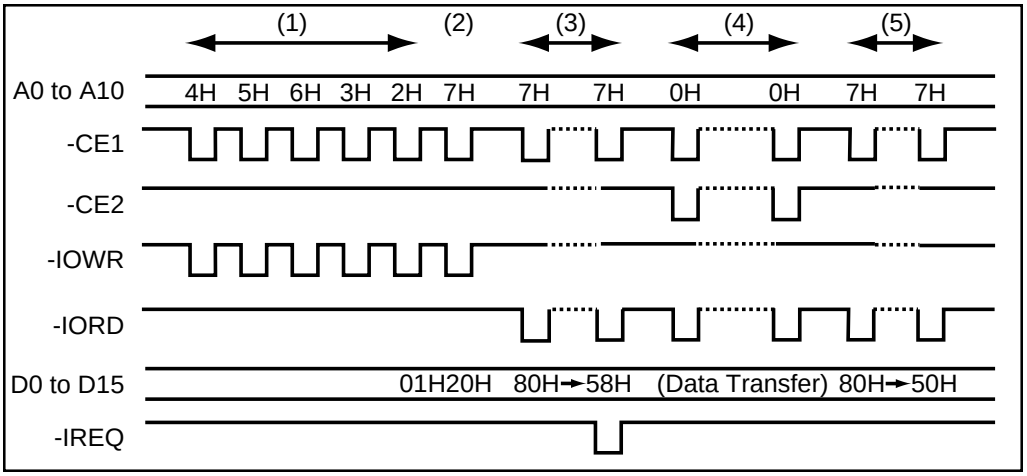
This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

SECTOR TRANSFER PROTOCOL

Sector Read

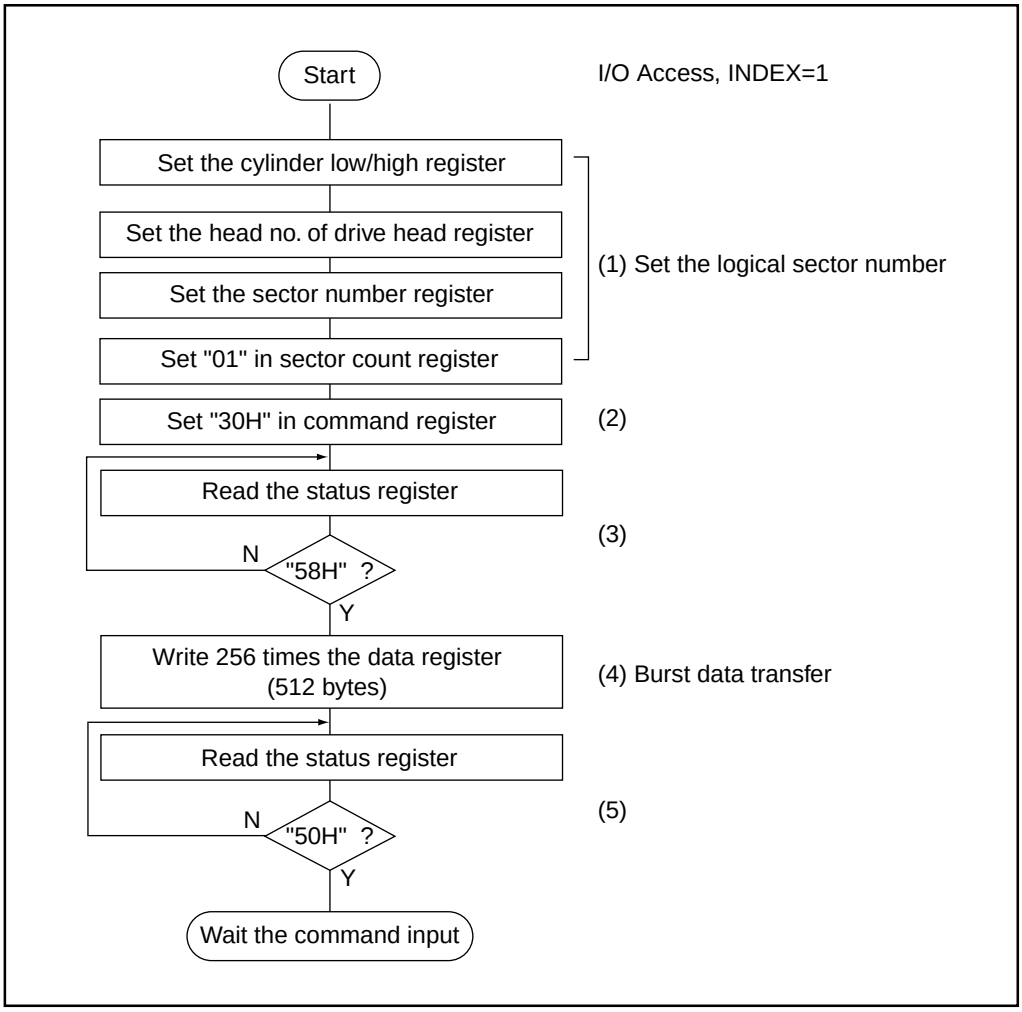
One sector read procedure after the card is configured to I/O interface is shown in the following charts.

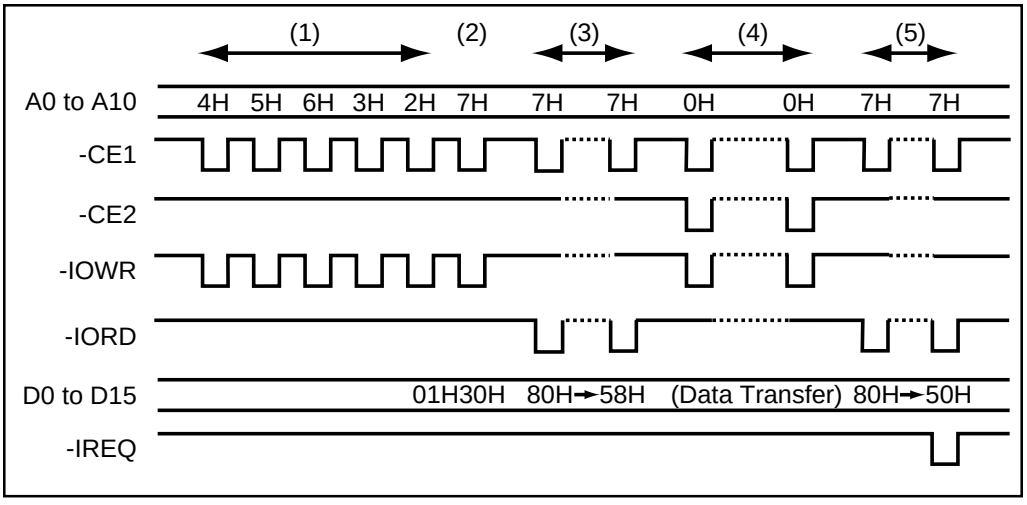




Sector Write

One sector write procedure after the card is configured to I/O interface is shown in the following charts.





REVISION HISTORY

Rev.	Change Description from Previous Revision
-101	2/1/04. Initial Release.
-102	5/26/04. Sleep mode current at 3.3V corrected to 80µA from 80mA. The operating current at 3.3V corrected to 30mA from 3mA. IOL/IOH condition at 5.0V is removed. Showpiece photo replaces Block Diagram. General Description updated with new marketing copy. R/W speeds updated from 5.4/5.5MB/s to 5/5MB/s. 64MB option removed. CHS Parameter table added. VCC(min) changed to 3.18V from 3.135V. VCC 5V tolerance changed to 5% from 10%. Preliminary notice removed. Disclaimer notice added. CIS Information corrected.
-103	6/18/04. Features bullets on page 1 updated. Pin Assignments for IDE Mode corrected to indicate which pins are not used in IDE Mode. . Pin Description changes: -CD1 and -CD2 not used in IDE mode; -IOIS16 not used in IDE mode; -WAIT description corrected to not used by card and pulled up by 4.7K ohm resistor. Performance rates for read and write described as sustained read and sustained write. AC Characteristics VCC 3.3V operating tolerances restated as +5% and -3.6% tolerances. Error register bit 0 Function “not supported” phrase removed. DMA commands removed. (Paper only error indicated that DMA was supported). Identify Drive Information table updated to reflect DMA not supported. “-F” p/n suffix selection added to notes of the Ordering Information. ATA-4 compatiblility added to Features. DC Characterists Sleep Mode values changed from 80uA to 800uA for 3.3V power supply, and 120uA to 1200uA for 5V power supply.
-104	7/9/04. Endurance increased from 300,000 cycles min to 2 million cycles min.
-105	7/22/04. “up to” added to sustained read and write data rate performance.
-106	8/23/04. Definition for Serial #, Firmware Rev., and Model # in the Identify Drive Information table added in callout. Words 0, 4-5, 20-21, 49 and 63 of Drive ID table corrected.
-107	10/14/04. Standard ECC, Endurance, and Warranty bullets added to Features on page 1.
-108	2/14/05. Shock parameter changed to 0.330ms to 0.750ms from 11ms. 3/14/05. Humidity parameter updated to 95% from 85%. CHS values updated. 4/22/05. U and S options added.
-109	2/14/05. MWDMA Mode 2 support added for this rev of spec only. 3/14/05. Humidity parameter updated to 95% from 85%. CHS values updated. 4/22/05. S and U options added. 7/20/05. For higher revs of this spec, the MWDMA support has been removed. Product with MWDMA has been given a P/N of SLATAFLxxxJ2(U)(I)-(F)(S).
-110	7/20/05. Separate shock and vibration for U option added.