M-Systems
Flash Disk Pioneers

Data Sheet

July 2001

DiskOnChip® 2000 TSOP 16MB
MD2211-D16-V3

Features

General

- **Flash Disk – full hard disk emulation**
- **16Mbyte (128Mbit) capacity**
- **Single-chip, based on state-of-the-art NAND flash technology**
- **Small form factor - standard 48-pin TSOP-I package**
- **High reliability - on the fly EDC/ECC**

Software Integration

- **Easily integrated plug-n-play flash disk**
- **Support for all major OS: Windows CE, Linux, VxWorks, Windows Embedded NT 4.0, BE, pSOS+, QNX, LynxOS, ATI Nucleus, DOS and others (also OS-less environment support)**
- **Small memory window size – 8KB for the entire DiskOnChip product line and all capacities**
- **The TrueFFS® driver supports 8-bit, 16-bit, and 32-bit bus architectures**

Hardware Integration

- **Simple SRAM-like hardware interface**
- **Compatible with major processors: x86, MediaGX, PowerPC, 68K, MIPS, SHx, StrongARM, and others**
- **Easy scalability - pinout compatible with various capacities of DiskOnChip TSOP-I products**
- **Low power - single 3.3V power supply**
- **Supports 3.3V and 5V host interface - all I/Os are 5V tolerant**

Advanced Features

- **Boot ROM replacement (BIOS in PC architectures) capability with an auto-loading XIP boot block – can be the only non-volatile device in the system**

TrueFFS® Technology

- **Full hard-disk read/write emulation and boot capability**
- **Third-generation wear leveling**
- **Automatic bad block management**
- **Power loss recovery**

Applications

- **Internet access devices**
- **Set-top boxes or Interactive TV's (ITV)**
- **WBT, thin clients, network computers**
- **Embedded systems**
- **Routers, switchers, networking equipment**
- **Web phones, car PC's, DVD's, Hand-held PC's**
- **Point-of-sale terminals, industrial PCs**
- **PDA's & Smart phones**

1 General Description

The DiskOnChip 2000 TSOP 16MB (MD2211-D16-V3) is based on M-Systems' patented DiskOnChip technology. DiskOnChip is a flash disk that provides full hard disk emulation using solid-state flash memory technology. DiskOnChip technology combines a disk controller with flash memory in a single chip providing a complete, easily integrated, flash disk solution. In addition, the DiskOnChip is a multi-function device. It provides both mass data storage and code storage with eXecute In Place (XIP) capabilities.

The DiskOnChip is based on state-of-the-art NAND flash technology. NAND flash features exceptional write and erase performance, providing the optimal data storage solution. Additionally, NAND technology is known for its high density and small die size. Thus providing a cost effective solution.

A programmable boot block (1KB) provides XIP capability. This means, that the DiskOnChip can replace the boot ROM, functioning as the only non-volatile memory on board. Eliminating the need for an additional boot ROM on the motherboard not only reduces cost, but also saves programming effort, reduces logistics costs, reduces board real estate, simplifies PCB layout and more. Although the XIP area is only 1KB, larger boot code images can be executed by swapping in multiple code pages from the flash memory.

The DiskOnChip is a member of M-Systems' DiskOnChip 2000 product line. It is available in a standard 48-pin TSOP-I plastic package, providing an SMT solution in addition to the traditional 32-pin DIP package of the other DiskOnChip 2000 products (MD220x-Dxx). The DiskOnChip is optimized for use where minimal weight, space, and low power consumption are essential. Typical applications include: information appliances, set-top boxes, car PCs, thin clients, thin servers, embedded systems such as avionics systems, industrial applications and more.

By using the DiskOnChip, physical space requirements are reduced. Unlike standard IDE drives, no cables or extra space for mounting brackets are required. The TSOP package is well suited for mass production because it does not require a socket or any kind of manual handling. Further, the DiskOnChip has no moving parts, resulting in significantly decreased power consumption and increased reliability. It is easy to use and reduces integration overhead. This makes the DiskOnChip a very attractive alternative to conventional hard and floppy disk drives and modules that require much more space, weight and assembly labor.

Greater capacities can be achieved by cascading up to four devices with no additional glue logic. This upgrade path can easily provide a flash disk of 32MB, 48MB or 64MB while remaining totally transparent to the file system and user.

2 Detailed Feature List

2.1 TrueFFS Technology

To emulate a hard disk, a flash disk requires a software management layer. TrueFFS is M-Systems' patented flash file system management technology that allows flash components to fully emulate hard disks, so they can be read from and written to like any other hard disk.

TrueFFS software simplifies and enhances flash memories by:

- Using third-generation wear leveling to ensure that all blocks are erased an equal number of times. This dramatically increases the life of the product. Refer to our online life expectancy calculator on the M-Systems Web site (www.m-sys.com). It can help you calculate the life expectancy of the DiskOnChip in your specific application.
- Using virtual blocking of the flash device to make erasure of large blocks transparent to the operator.
- Offering automatic bad block management and retirement.
- Implementing a robust, power-loss recovery mechanism to guarantee protection of data.

The TrueFFS driver supports 8-bit, 16-bit, and 32-bit bus architectures. Support for the 16-bit and 32-bit bus architectures, typically used in RISC processors, is achieved by using the LSB of the data bus as follows:

- For a 16-bit data bus, shift the address lines by *one*. For example: host address line A1 should be connected to address A0 of the DiskOnChip, host address line A2 should be connected to address A1 of the DiskOnChip, and so on.
- For a 32-bit data bus, shift the address lines by *two*. For example: host address line A2 should be connected to A0 of the DiskOnChip, host address line A3 should be connected to A1 of the DiskOnChip, and so on.

2.2 Full Boot Solution

The DiskOnChip provides full boot capability. In many cases, this allows the system engineer to remove the boot ROM/flash device from the motherboard. The CPU can fetch and execute boot code directly from the 1KB XIP boot block of the DiskOnChip. It can then load the remainder of the boot code from the NAND flash into the system's RAM and continue to execute from RAM.

2.3 Small Form Factor and Low Power

Integration of a flash disk in a single chip gives the DiskOnChip unique features including:

- Small footprint - 48-pin TSOP-I package.
- Low-power consumption – internal functions are synchronized with the CPU's read and write strobes. This innovation eliminates the need for an external clock and provides a fully static device.
- Single 3.3V power supply.

These features make the DiskOnChip the best cost-performance solution for computers that require minimal weight, space and power consumption.

Future DiskOnChip TSOP-I products will allow an easy and convenient upgrade path while also using the same 48-pin TSOP-I package and pinout.

2.4 Capacity

The DiskOnChip is available as a 16MB (128Mbits) flash disk. The capacity can be easily expanded to 32MB, 48MB, and 64MB, by cascading up to four devices without any additional glue logic.

The TrueFFS software automatically detects the number of cascaded devices, so that it appears to the user as one large disk drive. Where space permits, it is recommended that printed circuit boards be laid out with pads to support additional devices in order to facilitate upgrading the flash disk capacity in the future.

2.5 Easy Integration

The following features ensure fast integration:

- Compatible with standard SRAM/Flash interface.
- Supports local bus and ISA bus interface options.
- Includes 1KB programmable boot block for boot code storage.
- Small memory window size – only 8KB for the entire DiskOnChip family and all capacities.
- Static operation – no clock required.

2.6 Robust Error Correction

The DiskOnChip family utilizes a Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), providing the following error handling capabilities for each 512-byte block of data:

- Corrects up to two 10-bit symbols including two random bit errors.
- Corrects single bursts up to 11 bits.
- Detects up to four 10-bit symbols including four random bit errors.
- Detects single bursts up to 31 bits and double bursts up to 11 bits.

2.7 High Reliability

The DiskOnChip can be soldered directly onto the motherboard, eliminating the need for mechanical disk drives, bulky ribbon cables and connectors. The single chip design of the DiskOnChip ensures the highest level of reliability, even when subjected to levels of shock, vibration and temperature changes, which would destroy a conventional magnetic disk drive. In addition, TrueFFS is designed to prevent data inconsistency during a power failure.

2.8 High Speed

The DiskOnChip implements a tightly coupled pipelined architecture for data transfers. By using this architecture, it offers the following advantages over competitive alternatives:

- Eliminates bottlenecks typical in this area.
- Doubles the performance.
- Significantly improves write performance.

The DiskOnChip can sustain a system write speed of over 550KB per second and a read speed of more than 1.4MB per second (measured in ISA no wait state environment). Burst read/write transfer rates exceeding 14MB per second can be achieved.

2.9 Broad Support for Operating Systems and Processors

The DiskOnChip family of products is supplied with TrueFFS software, which supports a wide range of operating systems (OS), including: DOS, Windows CE, BE, Windows Embedded NT, as well as real-time operating systems (RTOS) such as QNX, VxWorks, pSOS, Linux, FreeBSD, LynxOS, NucleusOS and others.

In addition, leading operating systems such as Windows CE and Tornado offer native support for the DiskOnChip family of products for easy integration.

For OS-less applications and customized solutions, M-Systems offers its TrueFFS Software Development Kit (SDK), an ANSI-C source code kit designed specifically to support proprietary OS integration or OS-less environments.

Compatible with most major processors, the DiskOnChip family of products supports all popular processors including x86, 68K, MediaGx, Geode SCxxxx, PowerPC, MIPS, SHx, StrongARM and many others. For a complete and updated listing of TrueFFS OS compatibility, refer to M-Systems' web site: www.m-sys.com

2.10 Portable Solution – Shorter Time-to-Market

Development and integration time for implementing a flash disk is greatly reduced by the DiskOnChip standard software interface, which shortens time-to-market and provides portability to other operating systems and processors.

2.11 Complete Solution

The DiskOnChip series offers a full flash disk solution that includes different voltage and temperature options, software drivers tailored to your operating system, data sheets, application support, and online email support. DiskOnChip evaluation boards (EVB) provide a platform for software development prior to target hardware availability. In all, DiskOnChip offers a complete set of tools for delivering a complete solution whenever your application can use a flash disk.

3 Pin List and Description

Table 1: Pin List

Pin Name	Pin Number		Pin Number	Pin Name
RSTIN#	1		48	GND
CE#	2		47	Reserved
WE#	3		46	NC / D[15]
OE#	4		45	NC / D[14]
A[12]	5		44	NC / D[13]
A[11]	6		43	NC / D[12]
A[10]	7		42	NC / D[11]
A[9]	8		41	NC / D[10]
A[8]	9		40	NC / D[9]
A[7]	10		39	NC / D[8]
A[6]	11		38	Reserved
VCC	12		37	VCC
GND	13		36	GND
A[5]	14		35	D[7]
A[4]	15		34	D[6]
A[3]	16		33	D[5]
A[2]	17		32	D[4]
A[1]	18		31	D[3]
A[0]	19		30	D[2]
Reserved	20		29	D[1]
Reserved	21		28	D[0]
Reserved	22		27	BUSY#
Reserved	23		26	ID[1]
ID[0]	24		25	GND

Note: The MD2211-D16-V3 footprint is compatible with other DiskOnChip TSOP-I products.

3.1 Pins Description

Table 2: Pin List Description

Pin Name	Description	Direction
A[12:0]	**Address bus**	INPUT
D[7:0]	**Data bus**	INPUT/OUTPUT
CE#	**Chip Enable**, active low	INPUT
OE#	**Output Enable**, active low	INPUT
WE#	**Write Enable**, active low	INPUT
RSTIN#	**Reset input**, active low	INPUT
ID[1:0]	**Configuration control** inputs to support multiple chips cascaded in the same memory window. First chip - ID1, ID0 = GND, GND (0,0); used for single-chip configurations Second chip - ID1, ID0 = GND, VCC (0,1) Third chip - ID1, ID0 = VCC, GND (1,0) Forth chip - ID1, ID0 = VCC, VCC (1,1)	INPUT
BUSY#	**BUSY** - Open drain; active low output indicates that the DiskOnChip is initializing and should not be accessed. A pull-up resistor is required even if the pin is not used.	OPEN DRAIN OUTPUT
VCC	**Device supply** - All VCC pins must be connected.	SUPPLY
GND	**Ground** - All GND pins must be connected.	SUPPLY
RESERVED	**Reserved** – must be left floating.	
NC / D[15:8]	**Not Connected** - Current DiskOnChip 2000 TSOP 16MB is an 8-bit device therefore these pins are not connected internally. **Data bus high byte** – It is recommended that these pins be connected to D[15:8] of the data bus for compatibility with DiskOnChips supporting the 16-bit bus interface (e.g., DiskOnChip Millennium Plus 32MB).	

3.2 Compatibility with 32MB DiskOnChip Millennium Plus

DiskOnChip 2000 TSOP 16MB is pin compatible with DiskOnChip Millennium Plus 32MB. Both devices are packed in a 48-pin TSOP-I package and the pin location is designed for an easy drop in replacement.

Some of the reserved pins of the DiskOnChip 2000 TSOP 16MB are utilized in the DiskOnChip Millennium Plus 32MB. Please refer to the DiskOnChip Millennium Plus 32MB data sheet for a detailed description of the additional functionality of the DiskOnChip Millennium Plus (e.g., 16-bit interface, security and data protection features).

4 Designing with the DiskOnChip 2000 TSOP 16MB

4.1 Theory of Operation

Upon the negation of the RSTIN# input, the DiskOnChip downloads the boot code into the 1024 byte XIP boot block from the flash memory. As a failsafe mechanism, the DiskOnChip uses its internal EDC/ECC (Error Detection and Correction) logic to verify the integrity of this data. If an error is detected, then the DiskOnChip downloads the redundant copy of the boot code that is stored in subsequent pages of the flash memory. The entire download process takes less than 1ms. The DiskOnChip will not respond to accesses until the download process has completed.

At the completion of the download process, the host system can execute the boot code from the XIP boot block. This code can load the TrueFFS software or any other code from the NAND flash into the host's memory. This area is normally used to hold an x86 BIOS extension. Most non-x86 platforms do not use this area.

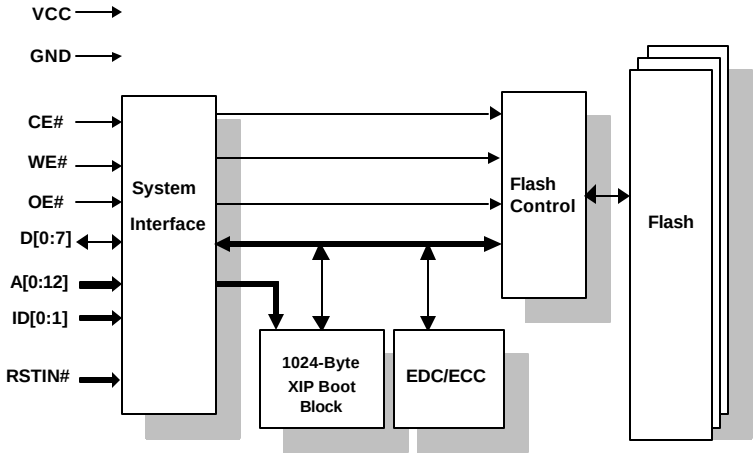

Figure 1: DiskOnChip 2000 TSOP 16MB Simplified Block Diagram

4.2 Hardware

The DiskOnChip is connected as a standard memory device, similar to SRAM. Typically, the DiskOnChip may be mapped to any free 8KB memory space. In PC-compatible platform it is usually mapped into the BIOS expansion area. If the allocated memory window is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once during the ROM expansion search. Figure 2 illustrates a typical system interface of the DiskOnChip 2000.

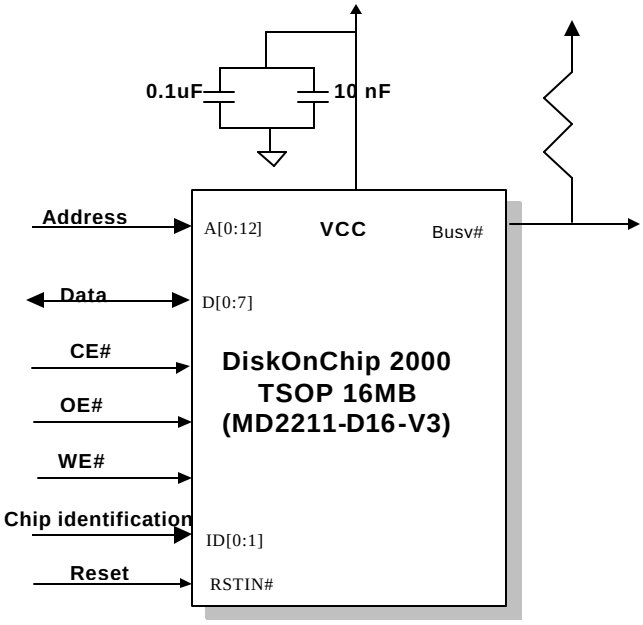

Figure 2: Simplified I/O Diagram

Note 1: The 0.1µF and the 10nF low-inductance high-frequency capacitors must be attached to each of the device's VCC and GND pins. These capacitors must be placed as close as possible to the package leads.

Note 2: CE#, OE# and WE# are edge-sensitive inputs and must be properly routed and terminated to avoid ringing.

4.3 Disk Capacity

Table 3: Disk Capacities

Product	Formatted Capacity (bytes)	Sectors	Formatted Capacity (bytes) (DOS 6.22)	Sectors (DOS 6.22)
DiskOnChip 2000 TSOP 16MB	16,375,808	31,984	16,324,608	31,884

4.4 Device Cascading

Up to four DiskOnChip 2000 TSOP devices may be cascaded. Figure 3 illustrates the cascading of four DiskOnChip devices to the host bus (not all signals are shown – all other signals must be connected as well). No external decoding circuitry is required. All the pins of the cascaded devices must be wired in common, except for the ID0 and ID1 pins. The ID input pins are strapped to Vcc or GND according to each DiskOnChip's device location, as described in Table 2.

The ID pin value determines the identity of each DiskOnChip. For example, the first device is defined by connecting the ID pins to '00', and the last device is defined by connecting the ID pins to '11'. Systems that use only one DiskOnChip must connect the ID pins as {00}. Additional devices must be configured consecutively as {01}, {10} and {11}.

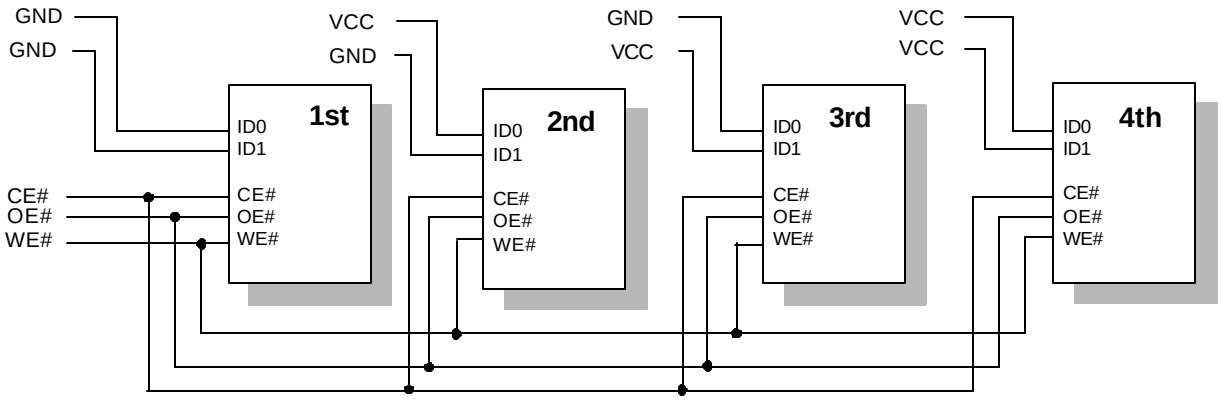

Figure 3: Cascaded Configuration

4.5 Software

TrueFFS the industry standard for flash disk emulation, is implemented into most major operating systems. Proprietary operating systems are supported with the DiskOnChip SDK. The DiskOnChip software integration is straightforward and configuration is quickly accomplished. For specific configuration instructions, refer to documentation from M-Systems and from the relevant OS vendors.

Features

- Similar to other block devices, the DiskOnChip 2000 TSOP is accessed using standard file system calls.
- Applications can write to and read from any sector on the DiskOnChip. The DiskOnChip is compatible with most diagnostic utilities, applications and file systems.
- TrueFFS accesses the flash memory within the DiskOnChip through an 8KB window in the CPU's memory space.
- TrueFFS handles the paging of this window in the flash array, and provides flash disk emulation that includes wear leveling, bad block management and retirement, and garbage collection.

4.6 Integration of DiskOnChip into PC-like Platforms

When used in PC-compatible architectures, the DiskOnChip should be allocated an 8KB memory window in the BIOS expansion memory range, typically located between 0C8000H and 0EFFFFH. During the boot process, the BIOS code loads the TrueFFS firmware into the PC's memory and installs the DiskOnChip as a disk drive in the system. When the operating system is loaded, the DiskOnChip is recognized as a standard disk. No external software is required in order to boot from the DiskOnChip. Figure 4 illustrates the DiskOnChip 2000 TSOP 16MB memory window in relation to the PC memory map.

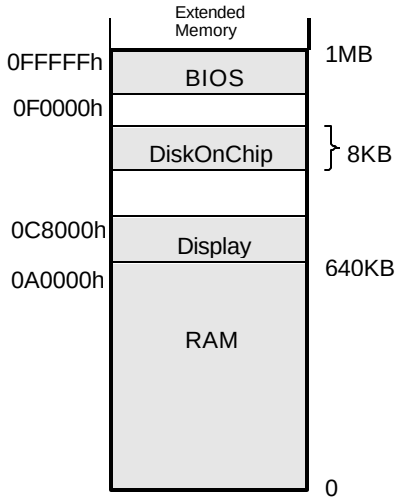

Figure 4: PC Memory Map

After reset, the BIOS code first executes the POST (Power On Self-Test) and then searches for all expansion ROM devices. When the DiskOnChip is found, the BIOS code executes the IPL code (Initial Program Loader) from the XIP boot block located in the DiskOnChip. This code loads the TrueFFS driver into system memory, installs the DiskOnChip as a disk in the system, and then returns control back to the BIOS code. The operating system subsequently identifies the disks that are available and the DiskOnChip software (TrueFFS) responds by emulating a hard disk.

From this point forward, the DiskOnChip appears as a standard disk drive. It is assigned a drive letter and it can be used by any application. The DiskOnChip 2000 TSOP does not require any modifications to either the BIOS set-up or the autoexec.bat/config.sys files.

The DiskOnChip can be used as the only disk in the system. In this case, the system boots directly from the DiskOnChip and is accessed as drive C:. It can work with or without a floppy drive, or with additional hard disks.

- When working with a hard disk, the DiskOnChip can be configured as the last drive (the default configuration). In this case, the hard disk will be C: and the DiskOnChip will be D:.
- Alternatively, it can be configured as the first drive. In this case, the hard disk will be D: and the DiskOnChip will be C:.
- DiskOnChip can be used as the OS boot device when configured as drive C:. In this configuration, the DiskOnChip must be formatted as a bootable device by copying the OS files onto the disk. When running DOS, you can use the SYS command to do this.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units	Notes
DC Supply Voltage	V_{CC}	-0.5 to 3.9	V	
Input Pin Voltage	V_{IN}	-0.5 to 6.0	V	2
Storage Temperature	T_{STG}	-65 to 150	°C	

Note 1: Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The voltage on any pin may undershoot to -2.0V or overshoot to 6.6V for periods less than 20ns.

5.2 Capacitance

Table 5: DiskOnChip Capacitance

Parameter	Symbol	Conditions[1,2]	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IN} = 0V	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF

Note 1: Vcc = 3.3V, Tj = 25°C, f = 1 MHz

Note 2: Capacitance is not 100% tested.

5.3 DC Electrical Characteristics Over Operating Range

Table 6: DiskOnChip DC Operating Range

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
System Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High-level Input Voltage	V_{IH}		2.0			V
Low-level Input Voltage	V_{IL}				0.8	V
High-level Output Voltage	V_{OH}	I_{OH} = -8 mA; Vcc=Vcc min	2.1			V
Low-level Output Voltage	V_{OL}	I_{OL} = 8 mA; Vcc=Vcc min			0.4	V
Input Leakage Current	I_{IL}				±10	µA
Output Leakage Current	I_{OZ}				±10	µA
Active Supply Current	I_{CC}	150 ns Cycle Time Outputs open		17	30	mA
Standby Supply Current	I_{CCS}	V_{IN} = 0V or Vcc		45	100	µA

5.4 Signal Integrity

The DiskOnChip derives its internal clock signal from the CE#, OE# and WE# inputs. These signals must have clean rising and falling edges, free from noise and ringing that can be misinterpreted as multiple edges. PC board traces for these three signals must either be kept short or suitably terminated to guarantee proper operation

5.5 Temperature Ranges

Commercial operating temperature…….. 0 °C to +70 °C

5.6 Humidity

10% to 90% relative, non-condensing.

5.7 Endurance

DiskOnChip is based upon NAND flash technology, which has a guaranteed minimum endurance of 100,000 erase cycles. TrueFFS' wear leveling algorithm significantly enhances the endurance of the flash. The typical expected life span is increased by an order of magnitude. For more information refer to the life expectancy calculator that is available on M-Systems' web site (www.m-sys.com).

5.8 AC Operating Conditions

Timing specifications are based on the conditions as defined in Table 7.

Table 7: AC Test Conditions

Item	Value	Units
Temperature (T_A)	0 to +70	^{0}C
Input Pulse Levels	0 to 3.0	V
Input Rise and Fall Times (20% - 80%)	3	ns
Input Timing Levels	1.5	V
Output Timing Levels	1.5	V
Output Load	140	pF

6 Timing Specifications

6.1 Power-up Timing

DiskOnChip 2000 TSOP devices are reset by the RSTIN# input. When the reset signal is negated, the DiskOnChip initiates the download procedure from the flash memory into the internal XIP boot block.

Hosts may employ any of the following methods to guarantee the timing requirements of the first access to the DiskOnChip 2000 TSOP:

a) Use a software loop to wait at least TP (BUSY1) before accessing the DiskOnChip after the reset signal is negated.

b) Poll the state of the BUSY# output.

c) Use the BUSY# output to hold the host before first access.

Host systems that boot from the DiskOnChip 2000 TSOP must employ option c), or use another method to guarantee the required timing of the first access. (Refer to Figure 5 and Table 8).

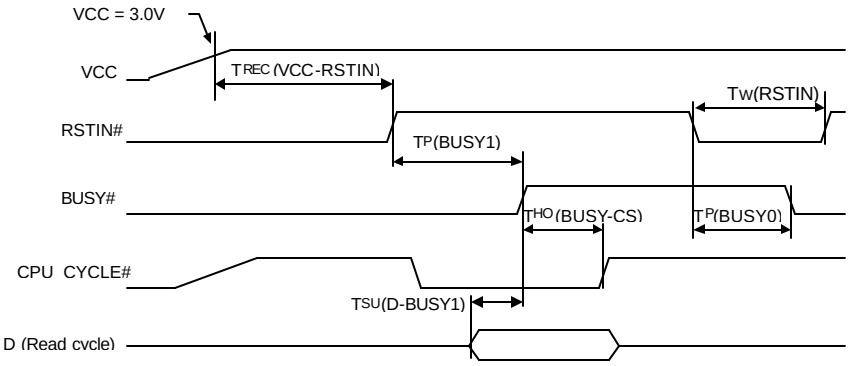

Figure 5: Reset Timing

Note: CPU_CYCLE# is an imaginary signal that is low during a CPU write or read cycle. It is equivalent to: !(!CE# & (!WE# | !OE#)).

Table 8: Timing Specifications

Parameter	Description	Min	Max	Units	Notes
VCC_RISE	VCC rise time	0.01	32.7	ms	1
Trec(VCC-RSTIN)	VCC stable to RSTIN# ↑	100		ns	2
Tw(RSTIN#)	RSTIN# asserted pulse width	30		ns	
Tp(BUSY0)	RSTIN# ↓ to BUSY# ↓		50	ns	
Tp(BUSY1)	RSTIN# ↑ to BUSY# ↑		1	ms	3
Tho(BUSY-CS)	BUSY# ↑ to CE#/OE#/WE# ↑	0		ns	4
Tsu(D-BUSY1)	Data valid to BUSY# ↑	0		ns	4

Note 1: Max value is specified from the first positive crossing above 2.15V to the final positive crossing above 3.0V. Min value is specified from 0V to 2.7V. Slew rate not to exceed 0.33 V/uS at any time.

Note 2: Specified from the final positive crossing of Vcc above 3.0V.

Note 3: If the assertion of RSTIN# occurs during a flash erase cycle this time could be extended by up to 500 µs.

Note 4: Normal read/write cycle timing applies. This parameter applies only to the case when the cycle is extended until the negation of the BUSY# signal.

6.2 Read Cycle Timing

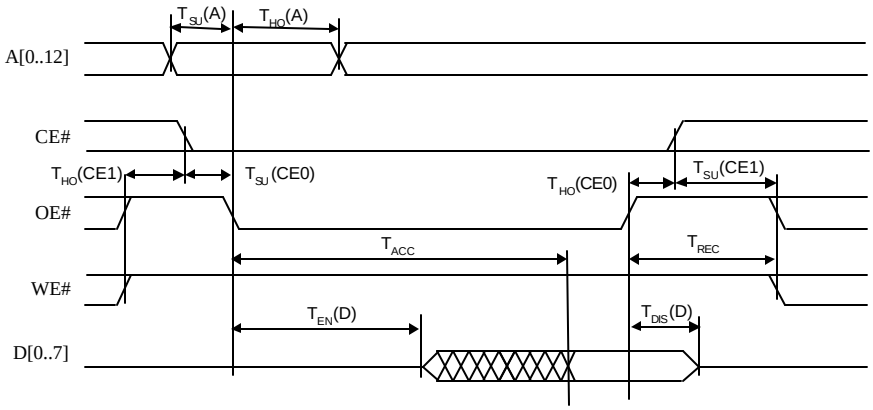

Figure 6: Read Cycle Timing

Table 9: Read Cycle Timing Definitions

Symbol	Description	Min (ns)	Max (ns)	Notes
T_{SU}(A)	Address to OE# ↓ setup	2		
T_{HO}(A)	OE#↓ to Address hold	18		
T_{SU}(CE0)	CE# ↓ to OE# ↓ setup	0		1
T_{HO}(CE0)	OE#↑ to CE# ↑ hold	0		2
T_{HO}(CE1)	OE# or WE#↑ to CE# ↓ hold	4		
T_{SU}(CE1)	CE#↑ to WE# or OE# ↓ setup time	4		
T_{REC}	OE#↑ to start of next cycle	17		
T_{ACC}	Read access time (boot block)		69	3,4
	Read access time (all other registers)		45	3
T_{EN}(D)	OE#↓ to D active delay	11	69	
T_{DIS}(D)	OE#↑ to D Hi-Z delay		11	

Note 1: CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to when OE# was asserted will be referenced instead to the time CE# was asserted.

Note 2: CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to when OE# was negated will be referenced instead to the time CE# was negated.

Note 3: The boot block is located at addresses 0000~07FFH and 1800H~1FFFH. Registers located at addresses 0800H~17FFH have a faster access time than the boot block. Access to the boot block is not required after the boot process has completed.

Note 4: Systems that do not access the boot block may implement only the read access timing for “all other registers”. This will increase the systems performance, however it will prevent access to the boot block.

6.3 Write Cycle Timing

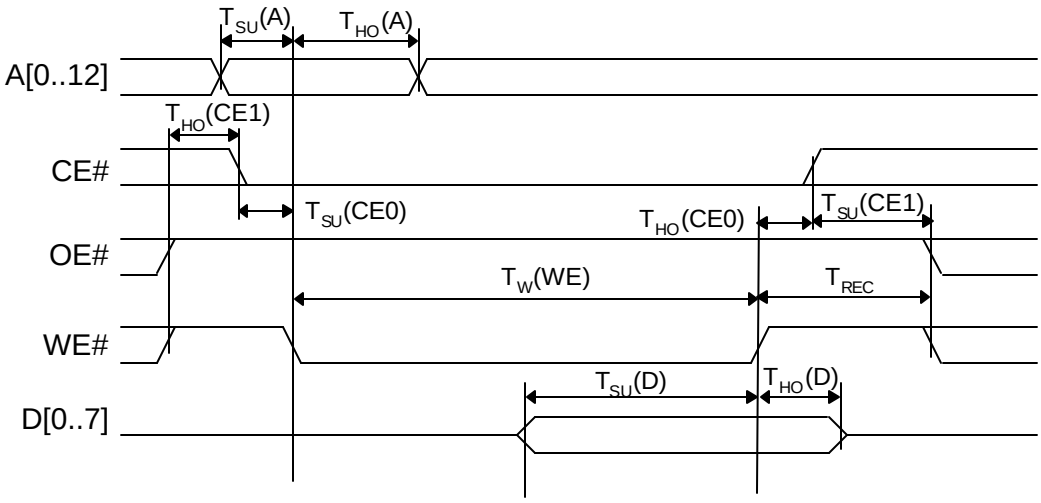

Figure 7: Write Cycle Timing

Table 10: Write Cycle Timing Definitions

Symbol	Description	Min (ns)	Max (ns)	Notes
T_{SU}(A)	Address to WE#↓ setup time	2		
T_{HO}(A)	WE#↓ to Address hold time	18		
T_W(WE)	WE# asserted width	50		
T_{SU}(CE0)	CE#↓ to WE#↓ setup time	0		1
T_{HO}(CE0)	WE#↑ to CE#↑ hold time	0		2
T_{HO}(CE1)	OE# or WE#↑ to CE#↓ hold time	4		
T_{SU}(CE1)	CE#↑ to WE# or OE#↓ setup time	4		
T_{REC}	WE#↑ to start of next cycle	17		
T_{SU}(D)	D to WE#↑ setup time	17		
T_{HO}(D)	WE#↑ to D hold time	0		

Note 1: CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to when WE# was asserted will be referenced instead to the time CE# was asserted.

Note 2: CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to when WE# was negated will be referenced instead to the time CE# was negated.

7 Mechanical Dimensions

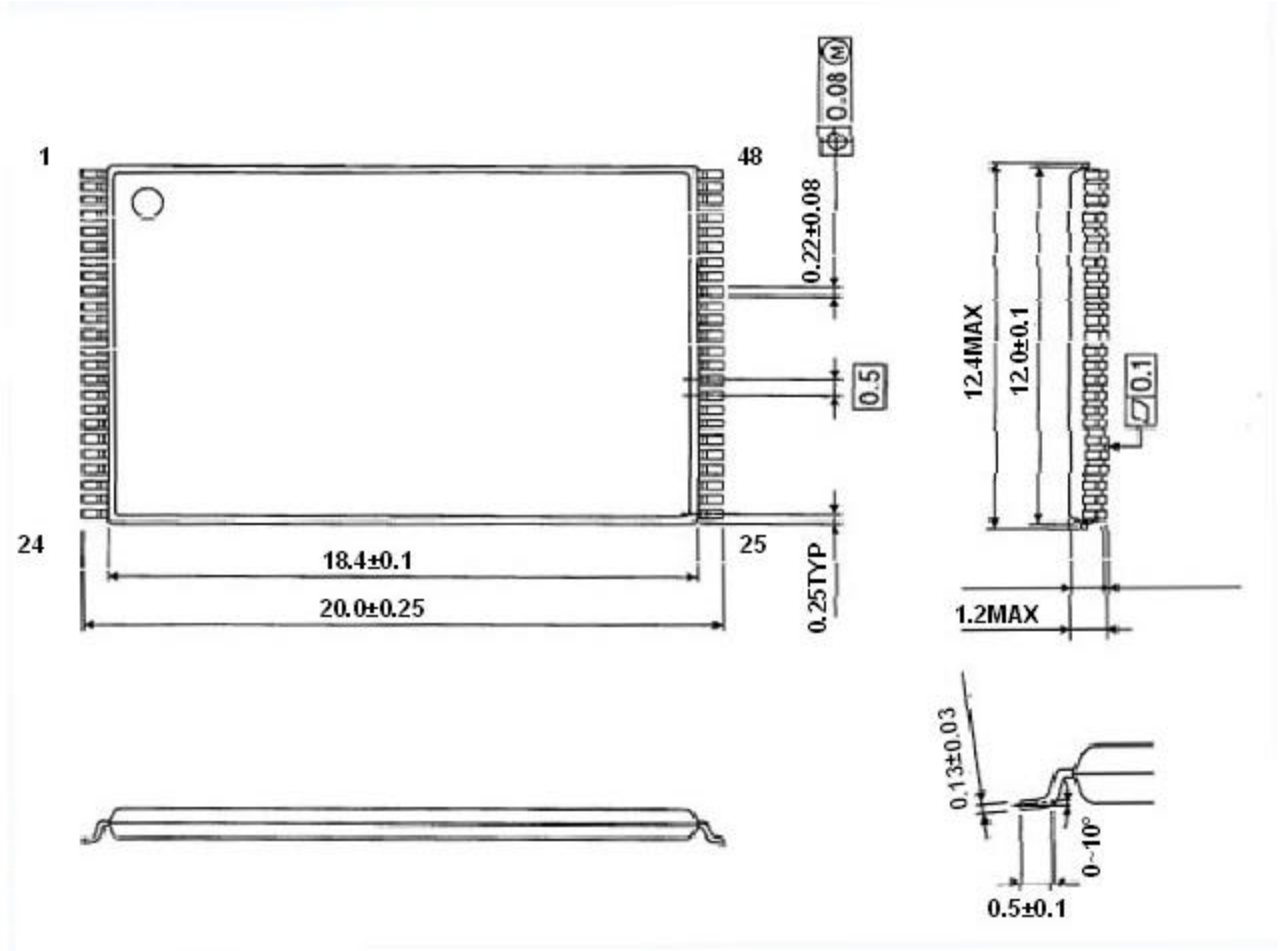

Figure 8: DiskOnChip 2000 TSOP 16MB Mechanical Dimensions

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