128MB to 1GB
Industrial Grade microSD Cards

Preliminary

www.stec-inc.com

SLSDMxxxB(I)U

General Description

The Industrial Grades microSD is the smallest removable flash card on the market, measuring only 11mm x 15mm x 1.00mm.

The microSD can be accessed trough 2 serial interfaces. The card can operate in SD mode or in SPI mode. While the SD interface provides high performance 4 bit data transfer, the SPI mode allows easy integration in any type of application at lower performance.

STEC's Industrial Grade microSD cards are specifically designed, manufactured and tested to withstand extreme environmental conditions and to improve system reliability and endurance.

At the heart of each card is an advanced microcontroller that performs elaborate Flash management including 5-Bytes on-the-fly Error Detection and 4-Bytes Correction (EDC/ECC), bad block management (BBM) and extensive wear leveling.

STEC's Industrial grade microSD utilizes only the highest reliability Single Level Cell (SLC) Flash for its superior endurance.

This combination allows achieving 2,000,000 logical program/erase cycles.

The microSD has no moving parts inside. As such, it is made to withstand extreme shock and vibration.

STEC manufacturing process and test methodology makes the card even more robust. In fact, to assure that the cards shipped meets the rigorous threshold set by the OEM customers, each card is extensively tested at STEC's manufacturing facility to guarantee perfect functionality in any conditions. STEC provides rigorous bill of material control as an additional guarantee for the customer, ensuring long term product stability and availability.

Ordering Information

microSD Card

Part Number	Capacity
SLSDM128B(I)U	128 Mbytes
SLSDM256B(I)U	256 Mbytes
SLSDM512B(I)U	512 Mbytes
SLSDM1GBB(I)U	1 GBytes

Legend:

- **(I) =** Industrial temperature range (-40ºC to +85 ºC).
- **Part numbers without (I) =** Commercial temperature range (0ºC to 70ºC).

Compliant to Specifications

- SD Memory Card Specification Part 1, Physical Layer Specification V1.1
  - microSD addendum version 1.1
- SD Memory Card Specification Part 2, File System Specification V1.01
- SD Memory Card Specification Part 3 Security Specification V1.01 (CPRM)

Supports SD and SPI Modes

Variable Clock Rate:

- Low frequency: 0 to 25MHz
- High frequency: 26Mhz to 50MHz

Voltage Range

- Basic communication : 2.0V to 3.6V (CMD0, CMD15, CMD55, ACMD41)
- Normal operating status: 2.7 to 3.6V

Low Power Consumption

Extended Data Write/Erase Endurance

- Optimized wear leveling algorithm
- Hardware ECC to automatically detect and correct errors
- 2,000,000 cycles (Preliminary)

Data Retention: 10 years

Power-on damage free card insertion and removal

Two Operating Temperature Ranges available:

- Commercial: 0 to 70°C
- Industrial: -40 to 85°C

RoHS compliant lead-free

Table of Contents

1.0 Product Specifications

1.1 Package Dimensions and Pin Locations

Refer to the Table 1, Figure 1, and Figure 2 for package dimensions and pin locations of the card. Units are in millimeters, and tolerances are ±0.15mm unless otherwise specified.

Table 1: Mechanical Dimensions microSD Card

Parameter	Value
Length	15.0±0.15mm
Width	11.0±0.15mm
Height	1.00±0.1mm

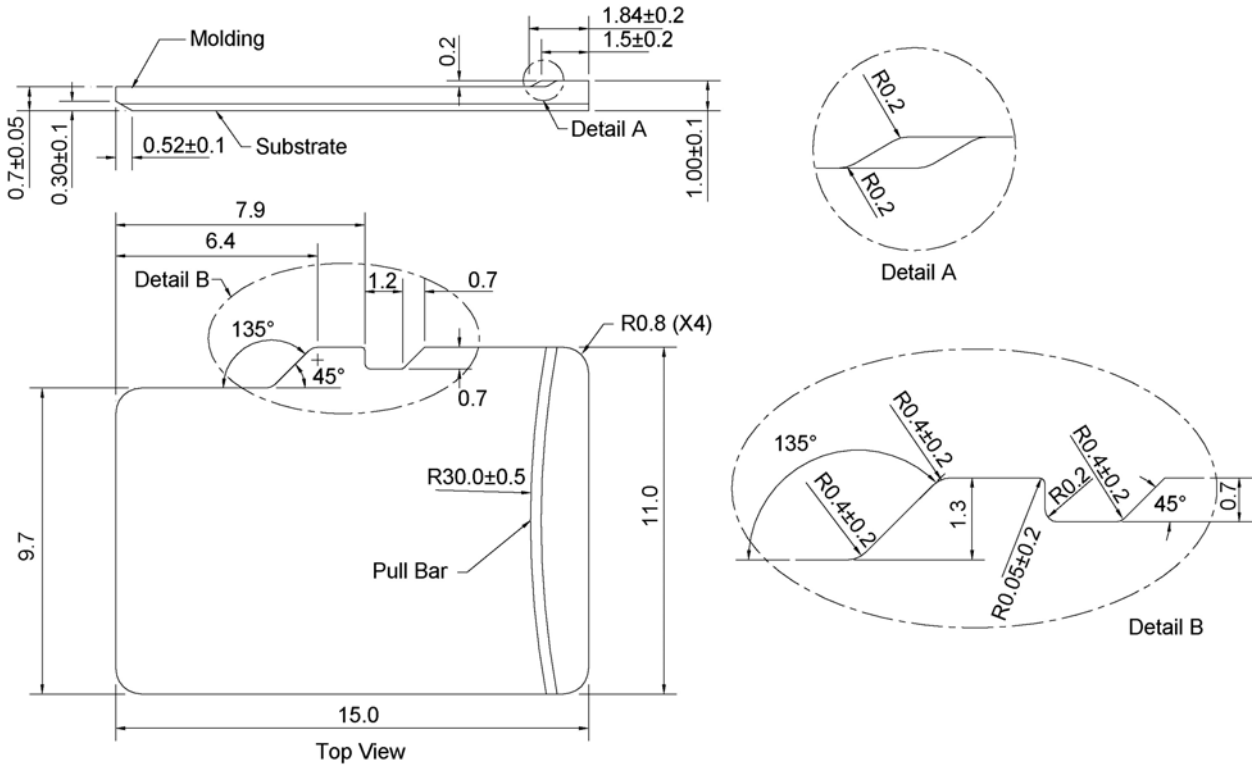

Figure 1: Mechanical Dimensions microSD Card

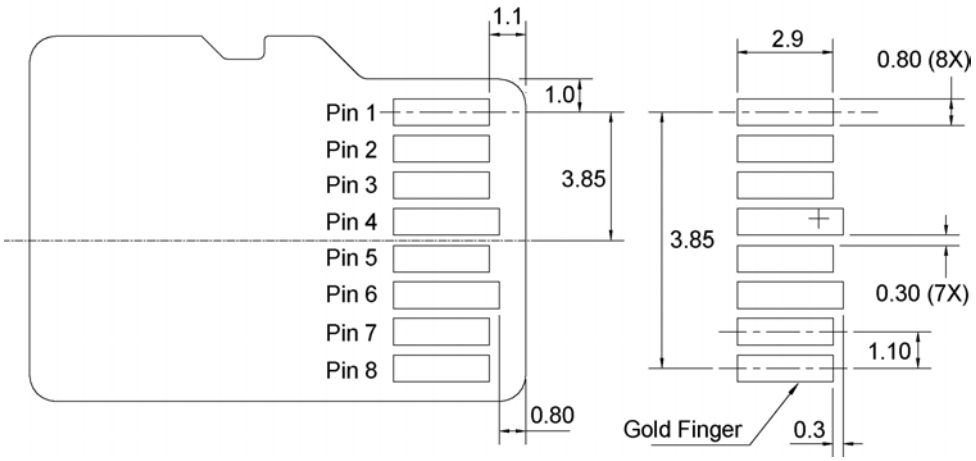

Figure 2: Mechanical Dimensions microSD Card (continued)

1.2 Pin Assignment and Signal Description

Table 2: microSD Card Pin Assignment and Signal Description

microSD Mode			
Pin	**Signal Name**	**Pin Type**	**Description**
1	DAT2	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 2. For read only cards, DAT2 is output only.
2	CD, DAT3	Bi-directionally I/O, I/O using Push-Pull Drivers	Card Detect, Data line bit 3. See Notes 1 and 2.
3	CMD	I/O using Push-Pull Drivers	Command/Response
4	VDD	Supply	Supply voltage
5	CLK	Input	Clock
6	VSS	Supply	Supply voltage ground
7	DAT0	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 0. For read only cards, DAT0 is output only.
8	DAT1	Bi-directionally I/O, I/O using Push-Pull Drivers	Data line bit 1. For read only cards, DAT1 is output only.
SPI Mode			
Pin	**Signal Name**	**Pin Type**	**Description**
1	—	—	Reserved for future use. Host should pull up with 10 to 100K ohm resistance.
2	/CS	Input	Chip select (“/” indicates low active)
3	DI	Input	Data in
4	VDD	Supply	Supply voltage
5	CLK	Input	Clock
6	VSS	Supply	Supply voltage ground
7	DO	Output, I/O using Push Pull Drivers	Data out
8	—	—	Reserved for future use. Host should pull up with 10 to 100K ohm resistance.

Notes:

1. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

2. After power up the CD line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

1.3 Performance

Measurements are in SD bus mode using HB Bench test.

Table 3: microSD Card Read/Write Performance

Parameter	128MB	256MB	512MB	1GB	Unit
Sequential Read	Up to 11.6	Up to 11.3	Up to 12.1	Up to 11.6	Mbytes/s
Sequential Write	Up to 5.8	Up to 4.6	Up to 7.8	Up to 9.5	Mbytes/s
Random Read	Up to 11.1	Up to 10.8	Up to 11.7	Up to 11.1	Mbytes/s
Random Write	Up to 2.0	Up to 1.3	Up to 2.2	Up to 1.1	Mbytes/s

Test conditions: Main Board: MSI865PE Neo2, CPU: Intel Pentium 4 2.4GHz, DDR memory: 256MBytes, OS: Windows 2000 with SP4, Software: FD Bench Ver3.4, USB Card reader (GL819)

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Table 4: microSD Card Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Commercial Operating Temperature	0	25	70	°C
	Industrial Operating Temperature	-40	-	85	°C
VDD	Supply Voltage	2.7	-	3.6	V
VSS1 VSS2	Supply Voltage Differentials	-0.3	-	0.3	V
-	Power Up Time (from 0V to VDD min)	-	-	250	ms

2.2 Reliability

Table 5: microSD Card Endurance & Data Retention

Parameter	Value
Endurance	2,000,000 Write/Erase Cycles
Data retention	10 years

2.3 Humidity & ESD

Table 7: microSD Card Humidity & ESD

Parameter		Value
Humidity	Operating	25 °C/95% RH
	Storage	40°C/93% RH 500 hours
ESD	Contact Pad, Human Body Model IEC61000-4-2: Charge C=100pF; Discharge R=1.5 K ohm	±4KV
	Non Contact Pad area, Human Body Model Coupling plane discharge Air discharge	 ±8KV ±15KV

3.0 Electrical Specifications

3.1 DC Characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 9: microSD Card DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
	Peak Voltage on all Lines	-0.3	Vcc + 0.3	V	
VIL	Input LOW Voltage	Vss - 0.3	0.25 x Vcc	V	
VIH	Input HIGH Voltage	0.625 x Vcc	Vdd + 0.3	V	
VOL	Output LOW Voltage		0.125 x Vcc	V	I_{OL} = -100uA @ Vcc min
VOH	Output HIGH Voltage	0.75 x Vcc		V	I_{OH} = -100uA @ Vcc min
IDD	Operating Current		45	mA	
	Standby Current		150	µA	
ILI	Input Leakage Current	-10	10	µA	
ILO	Output Leakage Current	-10	10	µA	

3.2 Signal Loading

The total capacitance C_L the CLK line of the SD memory card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line: $C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$ where N is the number of connected cards.

Requiring the sum of the host and bus capacitances not to exceed 30pF for up to 10 cards, and 40 pF for up to 30cards, the values shown in Table 6 must not be exceeded:

Note: the total capacitance of CMD and DAT lines will be consist of C_{HOST} , C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Table 6: microSD Card Signal Loading

Parameter	Symbol	Min	Max	Unit	Notes
Pull up resistance for CMD	R_{CMD}	10	100	K ohms	To prevent bus floating
Pull up resistance for DAT	R_{DAT}	10	100	K ohms	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	Fpp<5MHz, 21 cards
Bus signal line capacitance	C_L		100	pF	Fpp<20MHz, 7 cards
Signal card capacitance	C_{CARD}		10	pF	Single card
Signal line inductance			16	nH	
Pull up resistance inside card (Pin 1)	R_{DAT3}	10	90	K ohms	May be used for card detection

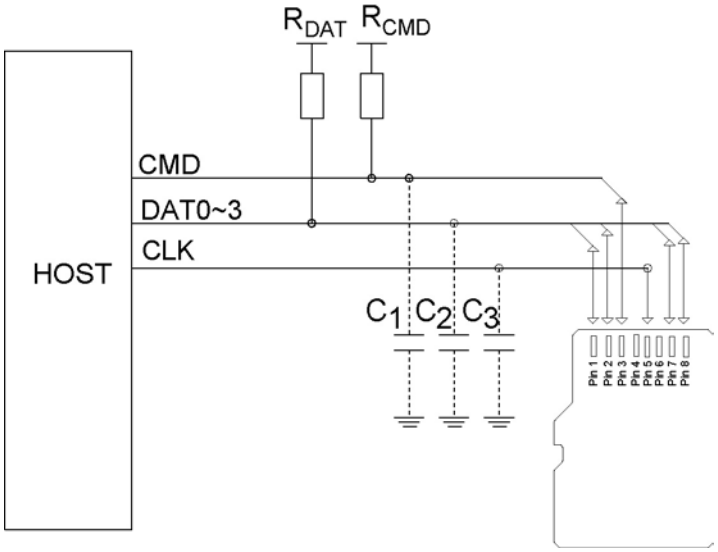

Figure 3: microSD Card Signal Loading

3.3 AC Characteristics

Table11: AC Characteristics Low Speed Mode

Parameter	Symbol	Min	Max	Unit	Notes
Clock frequency in data transfer mode	Fpp	0	25	MHz	C_L≤100pF (7 cards)
Clock frequency in card id mode	Fod	0	400	KHz	C_L≤250pF (21 cards)
Clock low time	tWL	10		ns	C_L≤100pF (7 cards)
Clock high time	tWH	10		ns	C_L≤100pF (7 cards)
Clock rise time	tTLH		10	ns	C_L≤100pF (7 cards)
Clock fall time	tTHL		10	ns	C_L≤100pF (7 cards)
Clock low time	tWL	50		ns	C_L≤250pF (21 cards)
Clock high time	tWH	50		ns	C_L≤250pF (21 cards)
Clock rise time	tTLH		50	ns	C_L≤250pF (21 cards)
Clock fall time	tTHL		50	ns	C_L≤250pF (21 cards)
CMD, DAT input setup time	tISU	5		ns	CMD,DAT Reference to CLK
CMD, DAT input hold time	tIH	5		ns	CMD,DAT Reference to CLK
Output delay time during Data Transfer Mode	tODLY	0	14	ns	CMD,DAT Reference to CLK
Output delay time during Identification Mode	tODLY	0	50	ns	CMD,DAT Reference to CLK

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

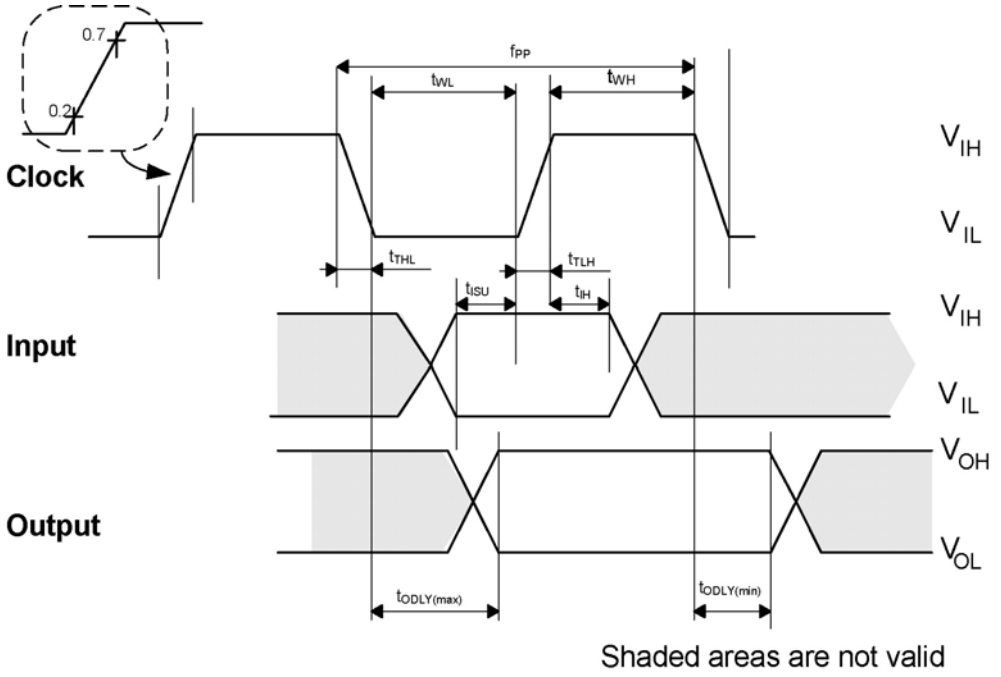

Figure 4: AC Characteristics Low Speed Mode

Table 12: AC Characteristics High Speed Mode

Parameter	Symbol	Min	Max	Unit
Clock frequency in data transfer mode	Fpp	0	50	MHz
Clock low time	tWL	7		ns
Clock high time	tWH	7		ns
Clock rise time	tTLH		3	ns
Clock fall time	tTHL		3	ns
CMD, DAT input setup time	tISU	6		ns
CMD, DAT input hold time	tIH	2		ns
CMD, DAT output hold time	tOH	2.5		ns
Output delay time during Data Transfer Mode	tODLY		14	ns

Notes:

1. Rise and fall times are measured from 10% to 90% of voltage level.
2. CLK referenced to VIH min and VIL max.
3. CMD and DAT inputs and outputs referenced to CLK.
4. 0Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.
5. In order to satisfy severe timing, the host shall drive only one card. $C_L \leq 30pF$

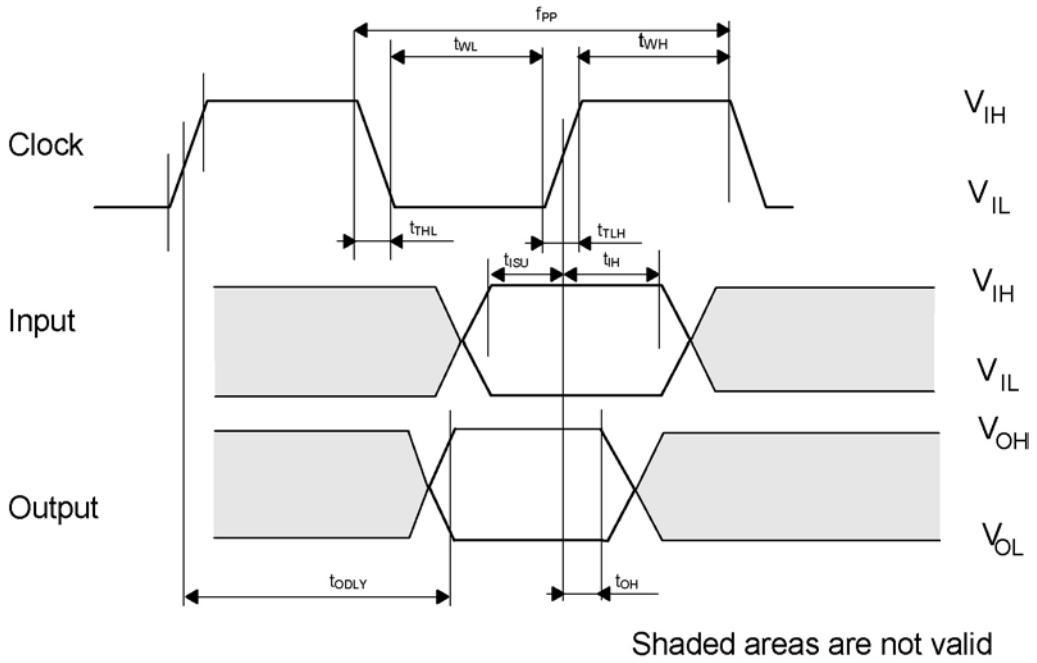

Figure 5: AC Characteristics High Speed Mode

4.0 Host Access Specifications

The following chapters summarize how the host accesses the card:

- The block diagram in *Chapter 4.1* shows how the SD and SPI buses interact with the registers via the controller.
- *Chapter 4.2* summarizes the SD and SPI buses.
- *Chapter 4.3* summarizes the registers.

4.1 Functional Block Diagram

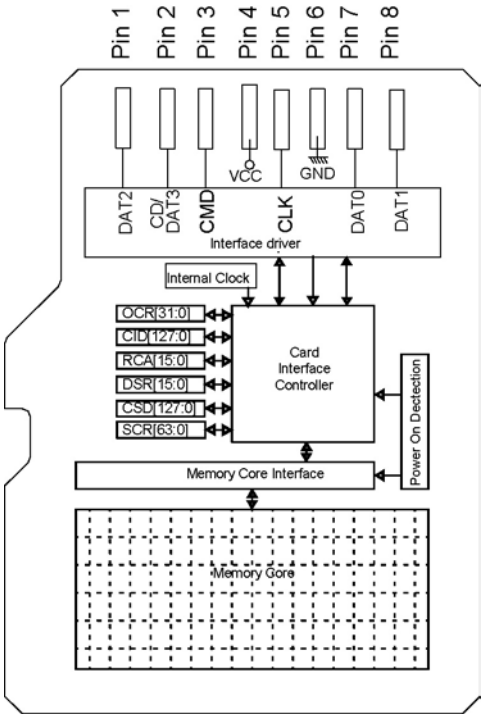

Figure 6: microSD Card Function Block Diagram

4.2 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

4.2.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

The SD bus signals are listed Table and the SD bus topology is illustrated in Figure 7.

Table13: SD Bus Signals

Signal	Description
CLK	Host to card clock signal
CMD	Bidirectional Command/Response signal
DAT0-DAT3	4 Bidirectional data signals
Vdd, Vss	Power and Ground

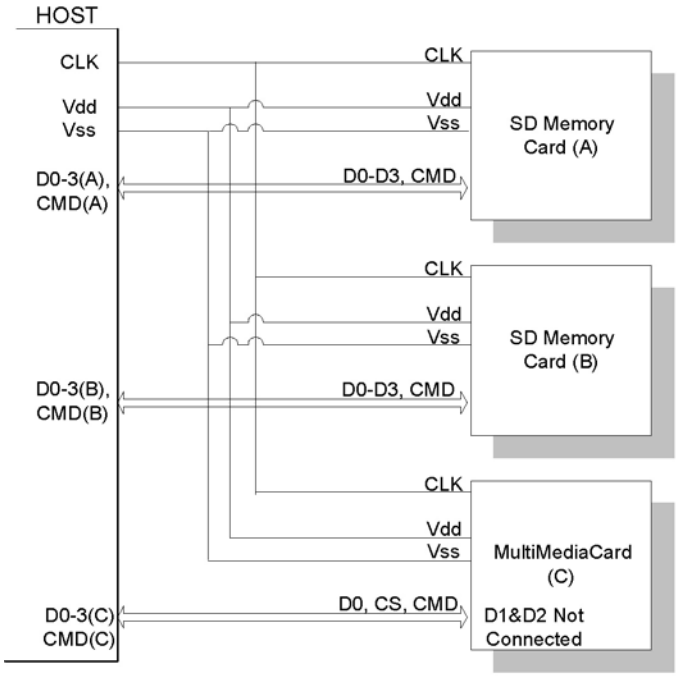

Figure 7: SD Bus Topology

4.2.2 SPI Bus Mode Protocol

The Serial Parallel Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.

While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

The SPI bus signals are listed Table and the SPI bus topology is illustrated in Figure 8.

Table14: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

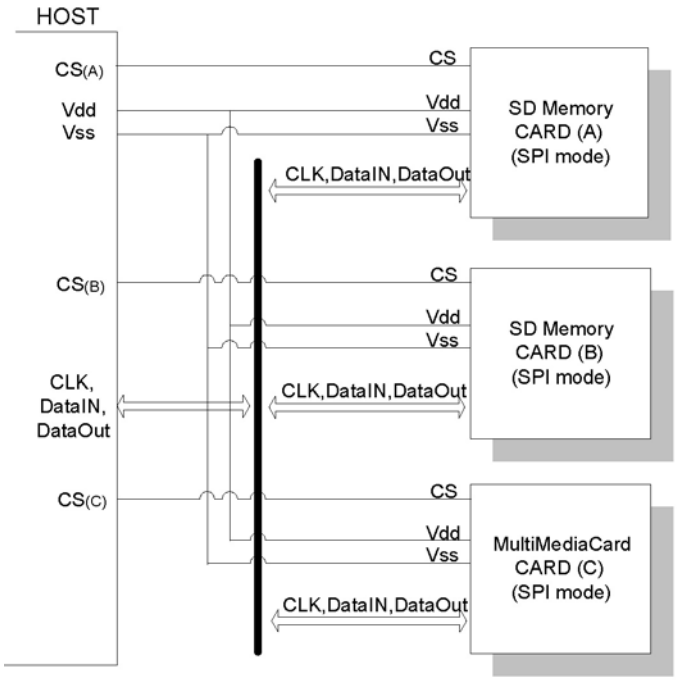

Figure 8: SPI Bus Topology

4.2.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.

During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is MultiMediaCard. In that case it should re-start the card as MultiMediaCard using CMD0 and CMD1.

4.3 Card Registers

The microSD Card has six registers. Refer to Table to Table for detail.

Table 15: microSD Card Registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD(CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address in SD Card mode.
DSR	16	Driver Stage Register	This register provides an optional function for the output driver condition.

Table16: CID Register

Register Name	Bit Width	CID-slice	Description
MID	8	[127:120]	Manufacture ID
OID	16	[119:104]	OEM/Application ID
PNM	40	[103:64]	Product Name
PRV	8	[63:56]	Product Version
PSN	32	[55:24]	Product Serial Number
—	4	[23:20]	Reserved
MDT	12	[19:8]	Manufacture Date
CRC	7	[7:1]	Check sum of CID contents
—	1	[0:0]	Not used; always=1

Table17: OCR Register

OCR bit position	VDD voltage window	Value	OCR bit position	VDD voltage window	Value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	1
13	2.5-2.6	0	31	Card power up status bit (busy)	0=busy; 1=ready
14	2.6-2.7	0			

Table18: CSD Register

Register Name	Bit Width	Cell Type	CSD slice	Value	Description
CSD_STRUCTURE	2	R	[127:126]	00	CSD structure
—	6	R	[125:120]	000000	Reserved
TAAC	8	R	[119:112]	01011110	Data read access time 1
NSAC	8	R	[111:104]	000000000	Data read access time 2 (CLK cycle)
TRAN_SPEED	8	R	[103:96]	00110010	Data transfer rate
CCC	12	R	[95:84]	010101110101	Card command classes
READ_BL_LEN	4	R	[83:80]	1001	Read data block length
READ_BL_PARTIAL	1	R	[79:79]	1	Partial blocks for read allowed
WRITE_BLK_MISALIGN	1	R	[78:78]	0	Write block misalignment
READ_BLK_MISALIGN	1	R	[77:77]	0	Read block misalignment
DSR_IMP	1	R	[76:76]	0	DSR implemented
—	2	R	[75:74]	00	Reserved
C_SIZE	12	R	[73:62]	F27h (128MB) F3Fh (256MB) F4Bh (512MB) F41h (1GB)	Device size
VDD_R_CURR_MIN	3	R	[61:59]	101	VDD min read current
VDD_R_CURR_MAX	3	R	[58:56]	101	VDD max read current
VDD_W_CURR_MIN	3	R	[55:53]	101	VDD min write current
VDD_W_CURR_MAX	3	R	[52:50]	101	VDD max write current
C_SIZE_MULT	3	R	[49:47]	100 (128MB) 101 (256MB), 110 (512MB) 111 (1GB)	Device size multiplier
ERASE_BLK_EN	1	R	[46:46]	1	Erase single block enable
SECTOR_SIZE	7	R	[45:39]	1111111	Erase sector size
WP_GRP_SIZE	7	R	[38:32]	0000011 (128MB,) 0000111 (256MB), 0001111 (512MB), 0011111 (1GB)	Write protect group size
WP_GRP_ENABLE	1	R	[31:31]	1	Write protect group enable
—	2	R	[30:29]	00	Reserved
R2W_FACTOR	3	R	[28:26]	101	Write speed factor
WRITE_BL_LEN	4	R	[25:22]	1001	Write data block length
WRITE_BL_PARTIAL	1	R	[21:21]	0	
—	5	R	[20:16]	00000	Reserved
FILE_FORMAT_GRP	1	R/W(1)	[15:15]	0	File format group
COPY	1	R/W(1)	[14:14]	0	Copy flag
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0	Permanent write protection
TMP_WRITE_PROTECT	1	R/W	[12:12]	0	Temporary write protection
FILE_FORMAT	2	R/W(1)	[11:10]	00	File format
—	2	R/W	[9:8]	00	Reserved
CRC	7	R/W	[7:1]	(CRC)	Checksum of CSD contents
—	1	-	[0:0]	1	Always=1

Table 19: SCR Register

Field	Bit Width	CID-slice	Value
SCR_STRUCTURE	4	[63:60]	0
SD_SPEC	4	[59:56]	1
DATA_STAT_AFTER_ERASE	1	[55:55]	0
SD_SECURITY	3	[54:52]	010
SD_BUS_WIDTHS	4	[51:48]	0101
Reserved	16	[47:32]	0
Reserved	32	[31:0]	0

5.0 Revision History

Revision	*Date*	*Description*
-101	1/5/07	Initial release.
-102	2/22/07	STEC Logo
-103	2/27/07	Added description of the SD bus protocol and SPI protocol, removed durability, corrected ESD, removed absolute maximum rating, added preliminary
-104	7/05/07	Correct stand-by current

Worldwide Headquarters
3001 Daimler Street
Santa Ana, California
92705 USA
Tel: (949) 476-1180
Fax: (949) 476-1209
www.stec-inc.com

STEC Europe
Donau-City-Strasse 1
1220 Vienna, Austria
Tel: +43 1 263 38 08
Fax: +43 1 263 37 65
www.stec-inc.com

STEC Hong Kong
Unit 01-02, 10/F
88 Hing Fat Street
Causeway Bay,
Hong Kong
Tel: +852-3150-8398
Fax: +852-3150-8399
www.stec-inc.cn

STEC Japan
Landmark Tower
20/F 2-2-1, Minato-Mirai,
Nishi-ku
YOKOHAMA, 220-8120,
Japan
Tel: +81(0) 45-670-7030
Fax: +81(0) 45-670-7001
www.stec-inc.jp

STEC Taiwan
4F, No. 3, Lane 91,
Dongmei Road
Hsinchu City Taiwan
Tel: +886-3-5733233
Fax: +886-3-5733633
www.stec-inc.com