1GB to 8GB
CompactFlash Card

STEC

www.stec-inc.com

SLCFxGM2U

Solid-State Memory Card
(No Moving Parts)

Capacity: 1GB - 8GB

CFA 4.0 and ATA-5 Compatible

ATA Transfer modes:

UDMA 0-5, MWDMA 0-4, PIO 0-6

Supports TrueIDE and PC Card Memory and I/O Modes

Form Factors:

- CompactFlash Type I
- CompactFlash Adapter

Advanced Wear-Leveling for Greater Flash Endurance

Card Information Structure (CIS) Programmed into Internal Memory

PC Card and Socket Services Release 2.1 or later compatible

5V or 3.3V Power Supply

Commercial Operating Temperature Range

4-Symbol Reed-Solomon ECC Engine

10 Year Data Retention

RoHS-6 Compliant

General Description

STEC's flash storage adheres to the latest industry compliance and regulatory standards including UL, FCC, RoHS, and various compliance associations. Each device incorporates a proprietary state-of-the-art flash memory controller that provides the greatest flexibility to customer-specific applications while supporting key flash management features resulting in the industry's highest reliability and endurance. Key features include:

- Built-in 4-symbol Reed-Solomon ECC engine detects and corrects errors
- Sophisticated block management and wear leveling algorithms dramatically enhance flash memory endurance
- Lifecycle management feature allows users to monitor the device's block management

STEC's CF Card is the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, ESD, and temperature. The rugged industrial design combined with temperature testing and adherence to rigid JEDEC JESD22 standards ensures flawless execution in the harshest environments.

In addition to custom hardware and firmware designs, STEC also offers value-added services including:

- Custom labeling and packaging
- Custom software imaging and ID strings
- Full BOM control and product change notification
- Total supply-chain management to ensure continuity of supply
- In-field application engineering to help customers through product design-ins

Ordering Information: CompactFlash Card

Note: The card automatically configures itself as fixed device when used as an IDE device. When used as a CF card, the card is removable.

Part Number	CF Form Factor	Capacity
SLCF1GM2U	Type I	1 GByte
SLCF2GM2U	Type I	2 GBytes
SLCF4GM2U	Type I	4 GBytes
SLCF8GM2U	Type I	8 GBytes

Legend:

- **SLCF =** STEC standard CompactFlash card part number prefix.
- **G =** proceeding capacity (x) is in Gigabytes.
- **M2 =** Mach 2 controller
- **U =** RoHS-6 compliant lead-free.

Table of Contents

1.0 Product Specifications

1.1 Labeling

STEC CF Cards can be manufactured with standard labeling, or customer-specific, custom labeling. Standard labeling is shown in Figure 1.

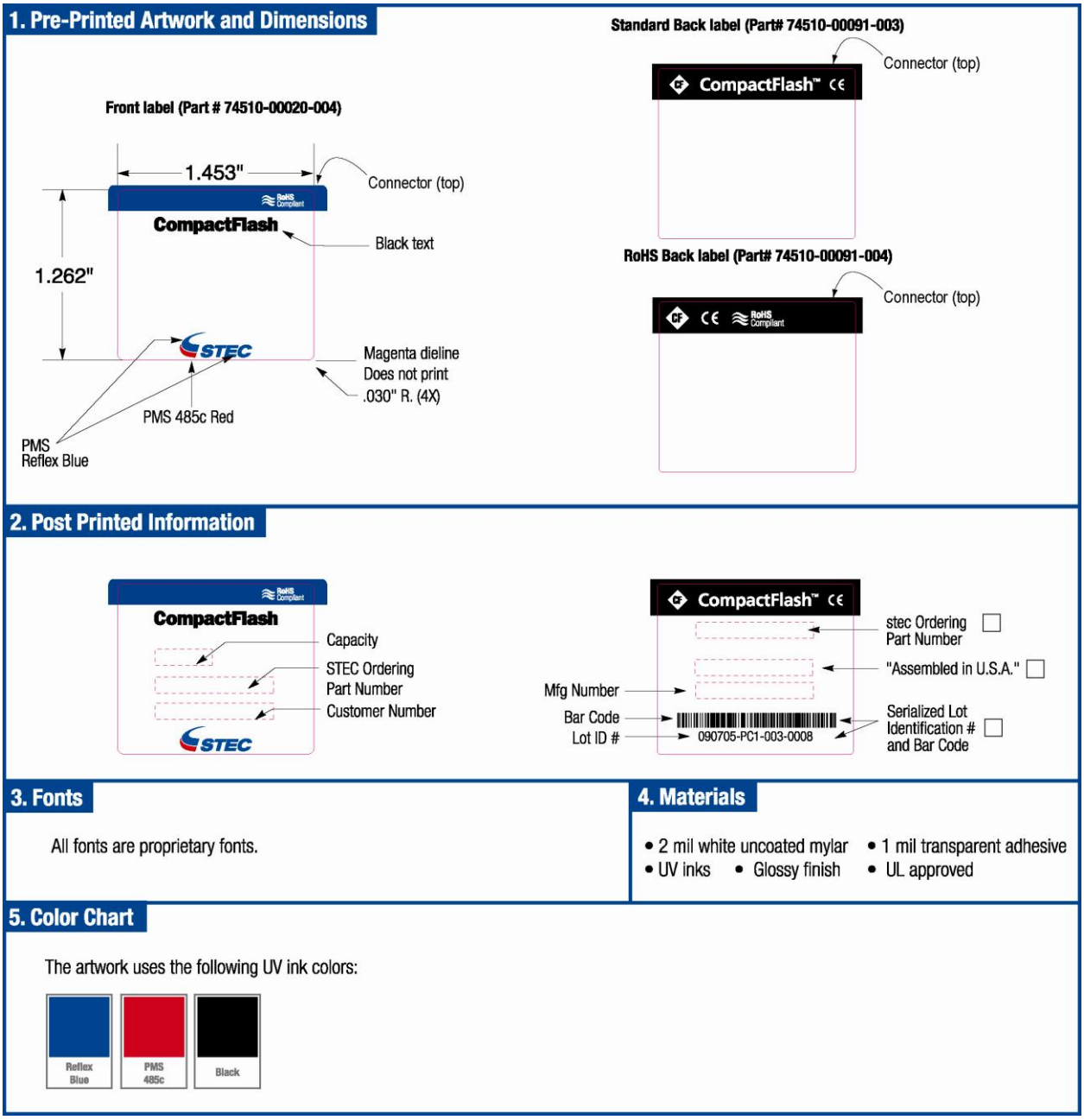


Figure 1: Standard Labeling

1.2 Package Dimensions and Pin Locations

Table 1 and Figure 2 show the mechanical dimensions of the CF Card Type I.

Table 1: Mechanical dimensions CF Card Type I

Parameter	Value
Length	36.40 ± 0.15 mm (1.433 ±. 0.006 in)
Width	42.80 ± 0.10 mm (1.685 ± 0.004 in)
Height (including label area)	3.30 ± 0.10 mm (0.130 ± 0.004 in)

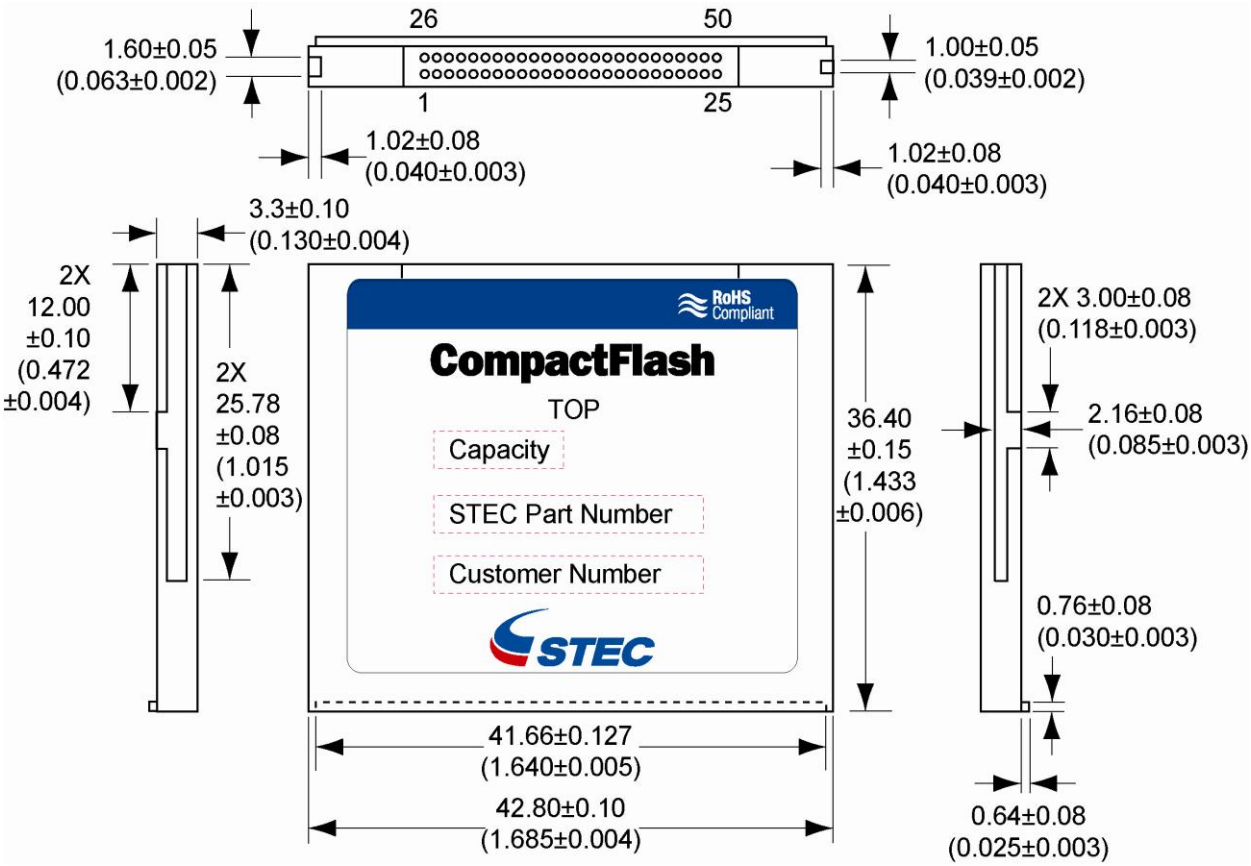


Figure 2: Mechanical dimensions CF Card Type I

1.3 Pin Assignments

Table 2: CF Card Pin Assignment

Pin Number	Signal Name	Pin Type	Pin Number	Signal Name	Pin Type
1	GND	Ground	26	-CD1	O
2	D03	I/O	27	D11	I/O
3	D04	I/O	28	D12	I/O
4	D05	I/O	29	D13	I/O
5	D06	I/O	30	D14	I/O
6	D07	I/O	31	D15	I/O
7	-CE1 -CS0	I	32	-CE2 -CS1	I
8	A10	I	33	-VS1	O
9	-OE -ATASEL	I	34	-IORD HSTROBE (-)HDMARDY	I
10	A09	I	35	-IOWR STOP	I
11	A08	I	36	-WE	I
12	A07	I	37	RDY/-BSY -IREQ INTRQ	O
13	VCC	Power	38	VCC	Power
14	A06	I	39	-CSEL	I
15	A05	I	40	-VS2	O
16	A04	I	41	(-)RESET	I
17	A03	I	42	-WAIT IORDY -DDMARDY DSTROBE	O
18	A02	I	43	-INPACK (-)DMARQ	O
19	A01	I	44	-REG (-)DMACK	I
20	A00	I	45	BVD2 -SPKR -DASP	I/O
21	D00	I/O	46	BVD1 -STSCHG -PDIAG	I/O
22	D01	I/O	47	D08	I/O
23	D02	I/O	48	D09	I/O
24	WP -IOIS16 -IOCS16	O	49	D10	I/O
25	-CD2	O	50	GND	Ground

Legend: “-“ = Low active

1.4 Signal Description

Table 3: CF Card Signal Description

Signal Name	Type	Pin Number	Description
BVD2 (PC Card Memory Mode)	I/O	45	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (PC Card I/O Mode)			This output line is always driven to a high state in I/O Mode since this product produces no audio.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	I/O	26, 25	These Card Detect pins are connected to ground on the card. They are used by the host to determine that the card is fully inserted into the socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same as Memory Mode.
-CD1, -CD2 (True IDE Mode)			These signals are not used in IDE Mode.
D15-D00 (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	These lines carry the data, commands, and host and the controller. D00 is the LSB of the LSB of the Odd Byte of the Word.
D15-D00 PC Card I/O Mode			This signal is the same as the PC Card Memory Mode signal.
D15-D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
-IOWR (PC Card Memory Mode except UDMA protocol active) STOP (All Modes – UDMA protocol active)	I	35	This signal is not used in this mode. In all modes, while UDMA mode protocol is active, the assertion of this signal causes the termination of the UDMA data burst.
-IOWR (PC Card I/O Mode except UDMA protocol active) STOP (All Modes – UDMA protocol active)			The I/O Write strobe pulse is used to clock I/O data onto the data bus and into the controller registers. The clocking occurs on the negative to positive edge of the signal (trailing edge). Same as STOP above.
-IOWR (True IDE Mode except UDMA protocol active) STOP (All Modes – UDMA protocol active)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode. Same as STOP above.
-IORD (PC Card Memory Mode except UDMA protocol active)	I	34	This signal is not used in this mode.

Signal Name	Type	Pin Number	Description
–HDMARDY (All Modes – UDMA protocol DMA Read) HSTROBE (All Modes – UDMA protocol DMA Writer)			In all modes when UDMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive UDMA data-in bursts. The host may negate -HDMARDY to pause an UDMA transfer In all modes when UDMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an UDMA data-out burst.
-IORD (PC Card I/O Mode except UDMA protocol active) -HDMARDY (All Modes – UDMA protocol DMA Read –IORD HSTROBE (All Modes – UDMA protocol DMA Writer			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CF Card. Same as –HDMARDY above. Same as HSTROBE above.
-IORD (True IDE Mode except UDMA protocol active) -HDMARDY (All Modes – UDMA protocol DMA Read –IORD HSTROBE (All Modes – UDMA protocol DMA Writer)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode. Same as –HDMARDY above. Same as HSTROBE above.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data into the registers. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode, this input signal is not used and should be connected to VCC.
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CF Card in PC Card Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATASEL (True IDE Mode)			To enable True IDE Mode, this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CF Card is ready to accept a new data transfer operation and held low when the CF Card is busy. The host must provide a pull-up resistor. At power up and at reset, the RDY/-BSY signal is held low (busy) until the CF Card completes its power up or reset function. No access of any type should be made to the CF Card during this time. The RDY/-BSY signal is held high (disabled from being busy) when the CF Card is powered up with RESET continuously disconnected or asserted high.
-IREQ (PC Card I/O Mode)			After card has been configured for I/O operation, signal is used as active low interrupt request. Strobe low to generate pulse mode interrupt or hold low for level mode interrupt.

Signal Name	Type	Pin Number	Description
INTRQ (True IDE Mode)			In True IDE Mode, this signal is the active high interrupt request to the host.
A10-A0 (PC Card Memory Mode)	I	8, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20	These address lines along with the -REG signal are used to select the following: the I/O port address registers within the CF Card, the memory mapped port address registers within the CF Card, a byte in the CIS and the Configuration Control and Status Registers.
A10-A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2-A0 (True IDE Mode)		18, 19, 20	In True IDE Mode only, A2:A0 are used to select the one of eight registers in the Task File. The remaining address lines should be grounded.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7, 32	These input signals are used both to select the CF Card and to indicate to the CF Card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8-bit hosts to access all data on D0-D7.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip enable for the task file registers while -CS1 is used to select the Alternate Status Register and the CF Card Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure the card as a Master or Slave. When the pin is grounded, the card is configured as a Master. When the pin is open, the card is configured as a Slave.
-REG (PC Card Memory Mode except UDMA protocol active) Attribute Memory Select -DMACK (PC Card Memory Mode when UDMA protocol is active)	I	44	This signal distinguishes between accesses to Common Memory (high) and Register Attribute Memory (low). In PC Card Memory Mode, when UDMA protocol is supported by host and host has enable UDMA on the card, the host shall keep the –REG signal negated during the execution of any DMA Command by the device. This is a DMA Acknowledge signal that is asserted by the host in response to (-)DMARQ to initiate DMA transfers. In True IDE Mode, while DMA operations are not active, the card shall ignore the (-)DMARQ signal, including a floating condition. If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host. A host that does not support DMA and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation all modes
-REG (PC Card I/O Mode except UDMA protocol active) DMACK			The signal must also be active (low) during I/O Cycles when the I/O address is on the bus. In PC Card I/O Mode, when UDMA protocol is support by host and host has enable UDMA on card, the host shall keep the –REG signal asserted during the execution of any DMA Command by the device. Same as (-)DMACK above.

Signal Name	Type	Pin Number	Description
(PC Card I/O Mode when UDMA protocol is active)			
-DMACK (True IDE Mode)			Same as (-)DMACK above.
WP (PC Card Memory Mode) Write Protect	O	24	The CF Card does not have a write protect switch; therefore, this signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			A low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOCS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.
-INPACK (PC Card Memory Mode except UDMA protocol active) -DMARQ (PC Card Memory Mode – UDMA protocol active)	O	43	This signal is not used in this mode. This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with (-)DMACK, i.e., the device shall wait until the host asserts (-)DMACK before negating (-)DMARQ, and re-asserting (-)DMARQ if there is more data to transfer. In PCMCIA I/O Mode, the -DMARQ shall be ignored by the host while the host is performing an I/O Read cycle to the device. The host shall not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE Mode, DMARQ shall not be driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1)and -CS1 (-CE2) shall be held negated and the width of the transfers shall be 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode operation. A host that does not support DMA mode and implements both PC Card and True IDE modes of operation need not alter the PC Card mode connections while in True IDE mode as long as this does not prevent proper operation in any mode.
-INPACK (PC Card I/O Mode except UDMA protocol active) Input Acknowledge -DMARQ (PC Card I/O Mode – UDMA protocol active)			The Input Acknowledge signal is asserted by the CF Card when it is selected and responding to an I/O read cycle at the address that is on the bus. The host uses this signal to control the enable of any input data buffers between the CF Card and the host's CPU. Same as (-)DMARQ above.
DMARQ (True IDE Mode)			Same as (-)DMARQ above.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as since a battery is not used with this product.

Signal Name	Type	Pin Number	Description
-STSCHG (PC Card I/O Mode) Status Changed			Asserted low to alert host to changes in RDY/-BSY, Write Protect states. Use is controlled by Configuration and Status Register.
-PDIAG (True IDE Mode)			In True IDE Mode, this input/output signal is the Pass Diagnostic signal in the Master/Slave handshake protocol.
-WAIT (PC Card Memory Mode except UDMA protocol active) -DDMARDY (All Modes – UDMA Write protocol active) DSTROBE (All Modes – UDMA Read protocol active)	O	42	This signal is not used by the CF Card, and is pulled up to VCC through a 4.7K ohm resistor. In all modes, when Ultra DMA mode DMA Write is active, this signal is asserted by the device during a data burst to indicate that the device is ready to receive Ultra DMA data out bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer. In all modes, when Ultra DMA mode DMA Read is active, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst
-WAIT (PC Card I/O Mode except UDMA protocol active) -DDMARDY (All Modes – UDMA Write protocol active) DSTROBE (All Modes – UDMA Read protocol active)			This signal is not used by the CF Card, and is pulled up to VCC through a 4.7K ohm resistor. Same as –DDMARDY above. Same as DSTROBE above.
IORDY (True IDE Mode except UDMA protocol active) -DDMARDY (All Modes – UDMA Write protocol active) DSTROBE (All Modes – UDMA Read protocol active)			This signal is not used by the CF Card, and is pulled up to VCC through a 4.7K ohm resistor. Same as –DDMARDY above. Same as DSTROBE above.
GND (PC Card Memory Mode)	GND	1, 50	Ground
GND (PC Card I/O Mode)			Ground
GND (True IDE Mode)			Ground
VCC (PC Card Memory Mode)	VCC	13, 38	+5 V or 3.3V power
VCC (PC Card I/O Mode)			+5 V or 3.3V power
VCC (True IDE Mode)			+5 V or 3.3V power
RESET (PC Card Memory Mode)	I	41	When RESET is high, this signal resets the CF Card. The CF Card is reset only at power up if this signal is left high or open from power-up. The CF Card can also be reset when the soft reset bit in the Configuration Option Register is set.

Signal Name	Type	Pin Number	Description
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
-VS1 -VS2 (PC Card Memory Mode)	O	33, 40	-VS1 is grounded, so that the card CIS can be read 3.3 volts. -VS2 is reserved for a secondary voltage and is not connected.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is not used in IDE Mode.

1.5 Performance

Table 4: CF Card Read/Write Performance

Parameter	Value
Data transfer rate to/from host	100 MBytes/s (burst)
Sustained read	up to 35 MBytes/s
Sustained write	up to 25 MBytes/s

Note: Performance may vary under extreme temperatures.

1.6 CHS Parameters

Table 5: CHS Parameters per capacity

Capacity	Cylinder (C) (standard)	Head (H)	Sectors/Track (S)
1GB	1,926	16	63
2GB	3,852	16	63
4GB	7,704	16	63
8GB	15,408	16	63

2.0 Environmental Specifications

2.1 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Commercial Operating Temperature	Ta1	0	25	70	°C
VCC voltage (5V)	VCC5.0	4.5	5.0	5.5	V
VCC voltage (3.3V)	VCC3.3	2.97	3.3	3.63	V

2.2 Reliability

Table 7: CF Card Endurance & Data Reliability

Parameter	Value
Endurance	Up to 2,000,000 Write/Erase Cycles (varies by flash type used)
Data reliability	1 in 10^{14} bits, read
Data retention	10 years

2.3 Shock, Vibration, and Humidity

Table 8: CF Card Shock, Vibration & Humidity

Parameter	Value
Shock	1.5K G peak, 0.5ms pulse duration, five (5) pulses per each of six (6) directions (per JEDEC JESD22 standard, method B110)
Vibration	20 G peak, 20Hz-2000Hz, 4 cycles per direction (per JEDEC JESD22 standard, method B103)
Humidity	85°C 85% RH, 500 hrs

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 9: CF Card Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage	Vin, Vout	-0.5 to VCC +0.5	V
Storage temperature range	Tstg	-65 to +150	°C

3.2 DC Characteristics

Measurements at Recommended Operating Conditions unless otherwise specified.

Table 10: CF Card DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
VIL (5V)	Input LOW Voltage	-0.3	+0.8	V	VCC= 5.0V
VIL (3.3V)	Input LOW Voltage	-0.3	+0.6	V	VCC= 3.3V
VIH (5V)	Input HIGH Voltage	4.0	VCC +0.3	V	VCC= 5.0V
VIH (3.3V)	Input HIGH Voltage	2.4	VCC +0.3	V	VCC= 3.3V
VOL	Output LOW Voltage		0.8		VCC=5.0V or 3.3V
VOH	Output HIGH Voltage	VCC-0.8		V	VCC=5.0V or 3.3V
ICCSB	Standby Mode	0.50	2	mA	ICC at VCC=5.0V or 3.3V
ICC	Operating Current	10	90	mA	ICC at VCC=5.0V or 3.3V
RPU	Pull-Up Resistance	40		K ohms	
RPD	Pull-Down Resistance	40		K ohms	

3.3 AC Characteristics

Measurements at Recommended Operating Conditions, unless otherwise specified.

3.3.1 PC Card Memory Mode Attribute Memory Read

Table 11: PC Card Memory Mode Attribute Memory Read AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from -CE	tdis(CE)	tEHQZ		100
Output Disable Time from -OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Output Enable Time from -CE	ten(CE)	tELQNZ	5	
Output Enable Time from -OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Hold Time	th(A)	—	20	
-CE Setup Time	tsu(CE)	—	0	
-CE Hold Time	th(CE)	—	20	

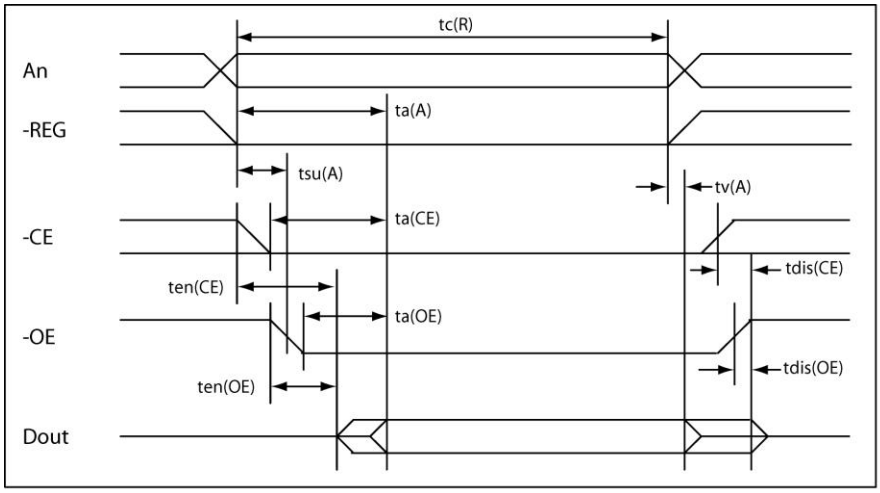


Figure 3: PC Card Memory Mode Attribute Memory Read Timing Diagram

3.3.2 PC Card Memory Mode Attribute Memory Write

Table 12: PC Card Memory Mode Attribute Memory Write AC Characteristics

Parameter	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Address Setup Time (-WE)	tsu(A-WEH)	—	180	
-CE Setup Time (-WE)	tsu(CE-WEH)	—	180	
Data Setup Time (-WE)	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Output Disable Time (-WE)	tdis(WE)	—		100
Output Disable Time (-OE)	tdis(OE)	—		100
Output Enable Time (-WE)	ten(WE)	—		125
Output Enable Time (-OE)	ten(OE)	—		125
Output Enable Setup Time (-WE)	tsu(OE-WE)	—	5	
Output Enable Hold Time (-WE)	th(OE-WE)	—	10	
-CE Setup Time	tsu(CE)	—	5	
-CE Hold Time	th(CE)	—	20	

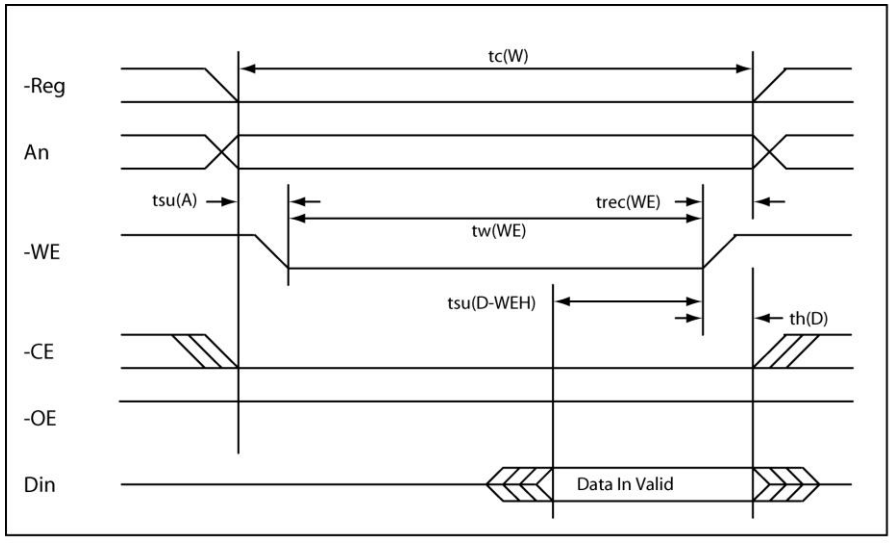


Figure 4: PC Card Memory Mode Attribute Memory Write Timing Diagram

3.3.3 PC Card Memory Mode Common Memory Read

Table 13: PC Card Memory Mode Common Memory Read AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Output Enable Access Time (max)	ta(OE)	tGLQV	125	60	50	45
Output Disable Time from OE (max)	tdis(OE)	tGHQZ	100	60	50	45
Address Setup Time (min)	tsu(A)	tAVGL	30	15	10	10
Address Hold Time (min)	th(A)	tGHAX	20	15	15	10
CE Setup before OE (min)	tsu(CE)	tELGL	0	0	0	0
CE Hold following OE (min)	th(CE)	tGHEH	20	15	15	10
Wait Delay Falling from OE (max)	tv(WT-OE)	tGLWTV	35	35	35	N/A
Data Setup for Wait Release (max)	tv(WT)	tQVWTH	0	0	0	N/A
Wait Width Time (max)	tw(WT)	tWTLWTH	350	350	350	N/A

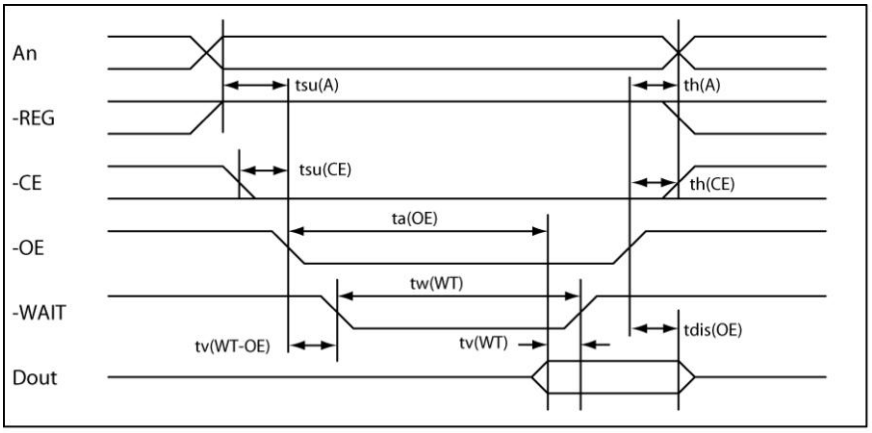


Figure 5: PC Card Memory Mode Common Memory Read Timing Diagram

3.3.4 PC Card Memory Mode Common Memory Write

Table 14: PC Card Memory Mode Common Memory Write AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Data Setup before WE(min)	tsu(D-WEH)	tDVWH	80	50	40	30
Data Hold following WE (min)	th(D)	tWMDX	30	15	10	10
WE Pulse Width (min)	tw(WE)	tWLWH	150	70	60	55
Address Setup Time (min)	tsu(A)	tAVWL	30	15	10	10
CE Setup before WE (min)	tsu(CE)	tELWL	0	0	0	0
Write Recovery Time (min)	trec(WE)	tWMAX	30	15	15	15
Address Hold Time (min)	th(A)	tGHAX	20	15	15	15
CE Hold following WE (min)	th(CE)	tGHEH	20	15	15	10
Wait Delay Falling from WE (max)	tv(WT-WE)	tWLWTV	35	35	35	N/A
WE High from Wait Release (min)	tv(WT)	tWTHWH	0	0	0	N/A
Wait Width Time (max)	tw(WT)	tWTLWTH	350	350	350	N/A

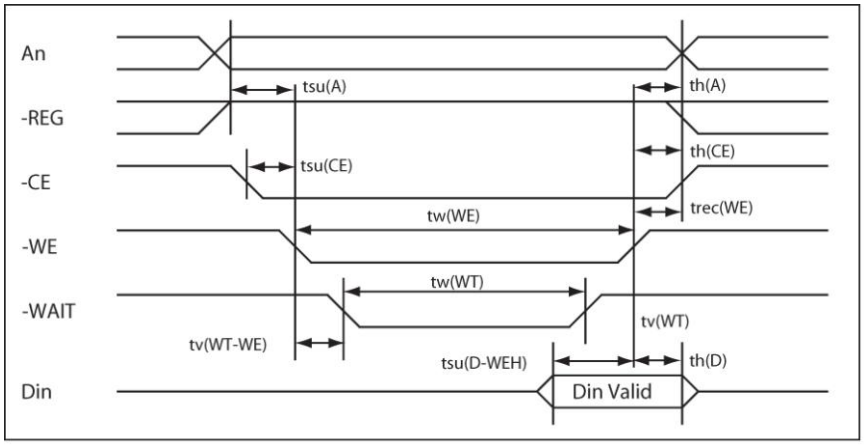


Figure 6: PC Card Memory Mode Common Memory Write Timing Diagram

3.3.5 PC Card I/O Mode Read AC Characteristics

Table 15: PC Card I/O Mode Read AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Data Delay after -IORD (max)	td(IORD)	tIGLQV	100	50	50	45
Data Hold following -IORD (min)	th(IORD)	tIGHQX	0	5	5	5
-IORD Width Time (min)	tw(IORD)	tIGLIGH	165	70	65	55
Address Setup before -IORD (min)	tsuA(IORD)	tAVIGL	70	25	25	15
Address Hold following -IORD (min)	thA(IORD)	tIGHAX	20	10	10	10
-CE Setup before -IORD (min)	tsuCE(IORD)	tELIGL	5	5	5	5
-CE Hold following -IORD (min)	thCE(IORD)	tIGHEH	20	10	10	10
-REG Setup before -IORD (min)	tsuREG(IORD)	tRGLIGL	5	5	5	5
-REG Hold following -IORD (min)	thREG(IORD)	tIGHRGH	0	0	0	0

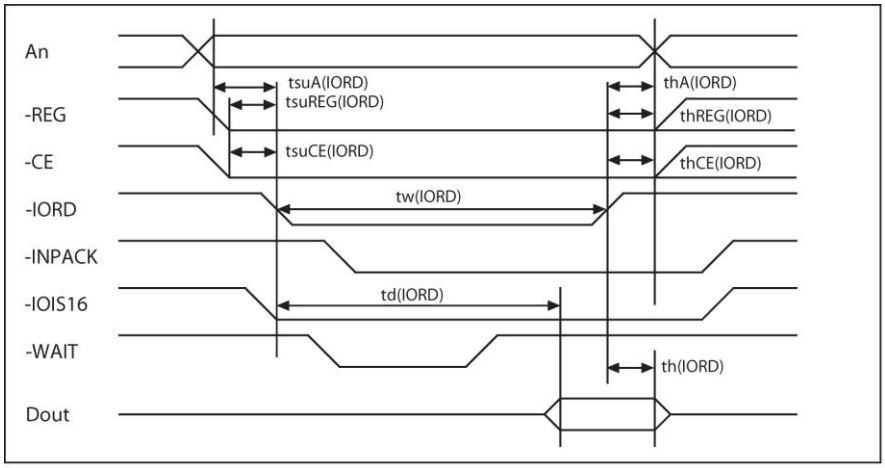


Figure 7: PC Card I/O Mode Read Timing Diagram

3.3.6 PC Card I/O Mode Write AC Characteristics

Table 16: PC Card I/O Mode Write AC Characteristics

Parameter	Symbol	IEEE Symbol	250 ns Cycle Time Mode	120 ns Cycle Time Mode	100 ns Cycle Time Mode	80 ns Cycle Time Mode
Data Setup before -IOWR (min)	tsu(IOWR)	tDVIWH	60	20	20	15
Data Hold following -IOWR (min)	th(IOWR)	tIWHDX	30	10	5	5
-IOWR Width Time (min)	tw(IOWR)	tIWLIWH	165	70	65	55
Address Setup before -IOWR (min)	tsuA(IOWR)	tAVIWL	70	25	25	15
Address Hold following -IOWR (min)	thA(IOWR)	tIWHAX	20	20	10	10
-CE Setup before -IOWR (min)	tsuCE(IOWR)	tELIWL	5	5	5	5
-CE Hold following -IOWR (min)	thCE(IOWR)	tIWHEH	20	20	10	10
-REG Setup before -IOWR (min)	tsuREG(IOWR)	tRGLIWL	5	5	5	5
-REG Hold following -IOWR (min)	thREG(IOWR)	tIWHRGH	0	0	0	0

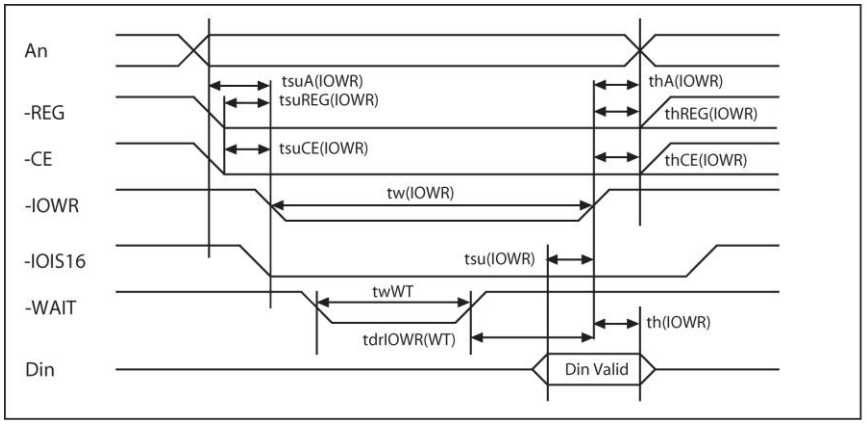


Figure 8: PC Card I/O Mode Read Timing Diagram

3.3.7 True IDE Mode Register Access

Table 17: True IDE Mode Register Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release (max)	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

3.3.8 True IDE Mode PIO Access

Table 18: True IDE Mode PIO Access AC Characteristics

Parameter	Symbol	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Cycle time (min)	t0	600	383	330	180	120	100	80	ns
Address valid to -IORD/-IOWR (min) setup	t1	70	50	30	30	25	15	10	ns
-IORD/-IOWR pulse width 8bit (min)	t2	290	290	290	80	70	65	55	ns
-IORD/-IOWR recovery time (min)	t2i	—	—	—	70	25	25	20	ns
-IOWR data setup (min)	t3	60	45	30	30	20	20	15	ns
-IOWR data hold (min)	t4	30	20	15	10	10	5	5	ns
-IORD data setup (min)	t5	50	35	20	20	20	15	10	ns
-IORD data hold (min)	t6	5	5	5	5	5	5	5	ns
-IORD data tristate (max)	t6z	30	30	30	30	30	20	20	ns
Addresses valid to -IOCS16 assert. (max)	t7	90	50	40	N/A	N/A	N/A	N/A	ns
Address valid to -IOCS16 release	t8	60	45	30	N/A	N/A	N/A	N/A	ns
-IORD/-IOWR to address valid hold	t9	20	15	10	10	10	10	10	ns

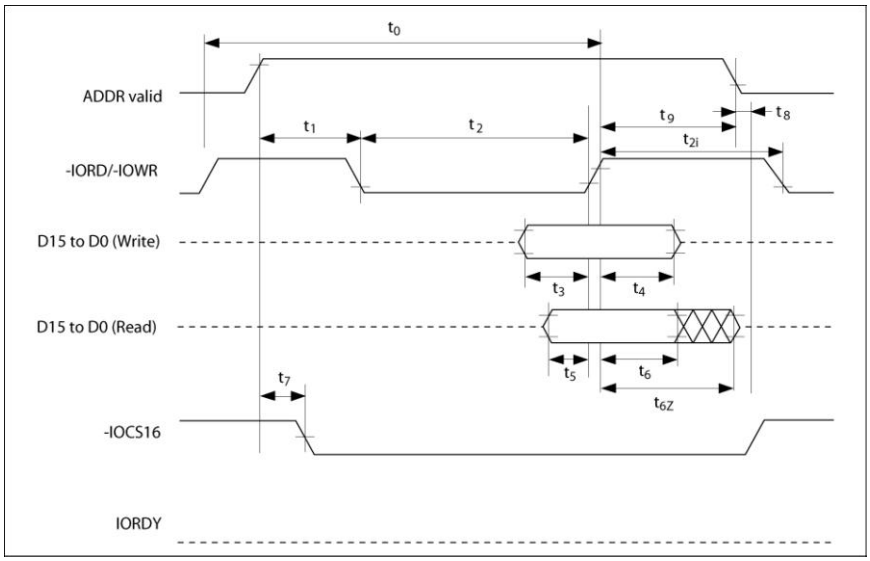


Figure 9: True IDE Mode PIO Access Timing Diagram

3.3.9 True IDE Mode Multiword DMA

Table 19: True IDE Mode Multiword DMA AC Characteristics

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min)	t_0	480	150	120	100	80	ns
-IORD/-IOWR Asserted Pulse (min)	t_D	215	80	70	65	55	ns
-IORD data access (max)	t_E	150	60	50	50	45	ns
-IORD data hold (min)	t_F	5	5	5	5	5	ns
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10	ns
-IOWR data hold (min)	t_H	20	15	10	5	5	ns
DMACK to -IORD/-IOWR setup (min)	t_I	0	0	0	0	0	ns
-IORD/-IOWR to DMACK hold (min)	t_J	20	5	5	5	5	ns
-IORD negated pulse width (max)	t_{KR}	50	50	25	25	20	ns
-IOWR negated pulse width (min)	t_{KW}	215	50	25	25	20	ns
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35	ns
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35	ns

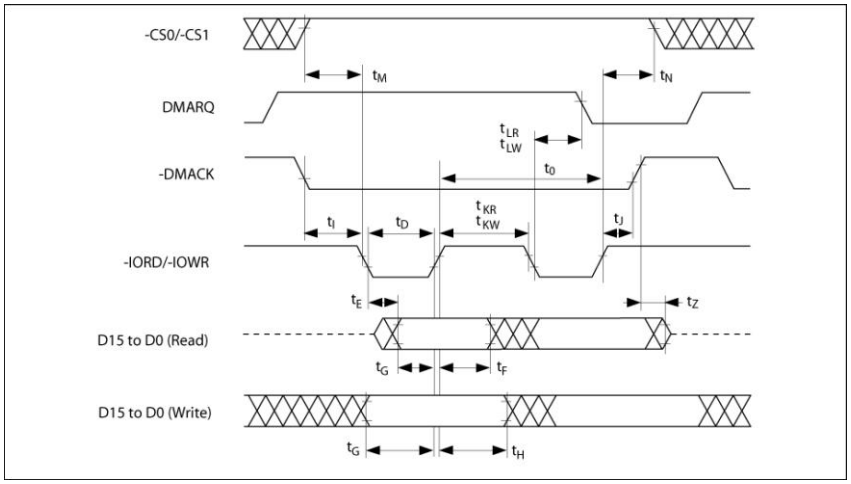


Figure 10: True IDE Mode Multiword DMA Timing Diagram

3.3.10 Ultra DMA AC Characteristics

Table 20: UDMA Burst Timing Requirements

Symbol	UDMA0 (ns)	UDMA1 (ns)	UDMA2 (ns)	UDMA3 (ns)	UDMA4 (ns)	UDMA5 (ns)	Measure location (see Note2)
t2CYCTYP (min)	240	160	120	90	60	40	Sender
tCYC (min)	112	73	54	39	25	16.8	Note3
t2CYC (min)	230	153	115	86	57	38	Sender
tDS (min)	15.0	10.0	7.0	7.0	5.0	4.0	Recip'nt
tDH (min)	5.0	5.0	5.0	5.0	5.0	4.6	Recip'nt
tDVS (min)	70.0	48.0	31.0	20.0	6.7	4.8	Sender
tDVH (min)	6.2	6.2	6.2	6.2	6.2	4.8	Sender
tCS (min)	15.0	10.0	7.0	7.0	5.0	5.0	Device
tCH (min)	5.0	5.0	5.0	5.0	5.0	5.0	Device
tCVS (min)	70.0	48.0	31.0	20.0	6.7	10.0	Host
tCVH (min)	6.2	6.2	6.2	6.2	6.2	10.0	Host
tZFS (min)	0	0	0	0	0	35	Device
tDZFS (min)	70.0	48.0	31.0	20.0	6.7	25	Sender
tFS (max)	230	200	170	130	120	90	Device
tLI (min)	0	0	0	0	0	0	Note4
tLI (max)	150	150	150	100	100	75	Note4
tMLI (min)	20	20	20	20	20	20	Host
tUI (min)	0	0	0	0	0	0	Host
tAZ (max)	10	10	10	10	10	10	Note5
tZAH (min)	20	20	20	20	20	20	Host
tZAD (min)	0	0	0	0	0	0	Device
tENV (min)	20	20	20	20	20	20	Host
tENV (max)	70	70	70	55	55	50	Host
tRFS (max)	75	70	60	60	60	50	Sender
tRP (min)	160	125	100	100	100	85	Recip'nt
tIORDYZ (max)	20	20	20	20	20	20	Device
tZIORDY (min)	0	0	0	0	0	0	Device
tACK (min)	20	20	20	20	20	20	Host
tSS (min)	50	50	50	50	50	50	Sender

Notes:

1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and –DMARDY transitions are measured at the sender connector.
3. The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4. The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
5. The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

Table 21: UDMA Timing Parameter Descriptions

Symbol	Parameter
t2CYCTYP	Typical sustained average two cycle time
tCYC	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)
t2CYC	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
tDS	Data setup time at recipient (from data valid until STROBE edge)
tDH	Data hold time at recipient (from STROBE edge until data may become invalid)
tDVS	Data valid setup time at sender (from data valid until STROBE edge)
tDVH	Data valid hold time at sender (from STROBE edge until data may become invalid)
tCS	CRC word setup time at device
tCH	CRC word hold time device
tCVS	CRC word valid setup time at host (from CRC valid until -DMACK negation)
tCVH	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)
tZFS	Time from STROBE output released-to-driving until the first transition of critical timing.
tDZFS	Time from data output released-to-driving until the first transition of critical timing.
tFS	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)
tLI	Limited interlock time
tMLI	Interlock time with minimum
tUI	Unlimited interlock time
tAZ	Maximum time allowed for output drivers to release (from asserted or negated)
tZAH	Minimum delay time required for output
tZAD	Drivers to assert or negate (from released)
tENV	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)
tRFS	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)
tRP	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)
tIORDYZ	Maximum time before releasing IORDY
tZIORDY	Minimum time before driving IORDY
tACK	Setup and hold times for -DMACK (before assertion or negation)
tSS	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)

Table 22: Ultra DMA Sender and Recipient IC Timing Requirements

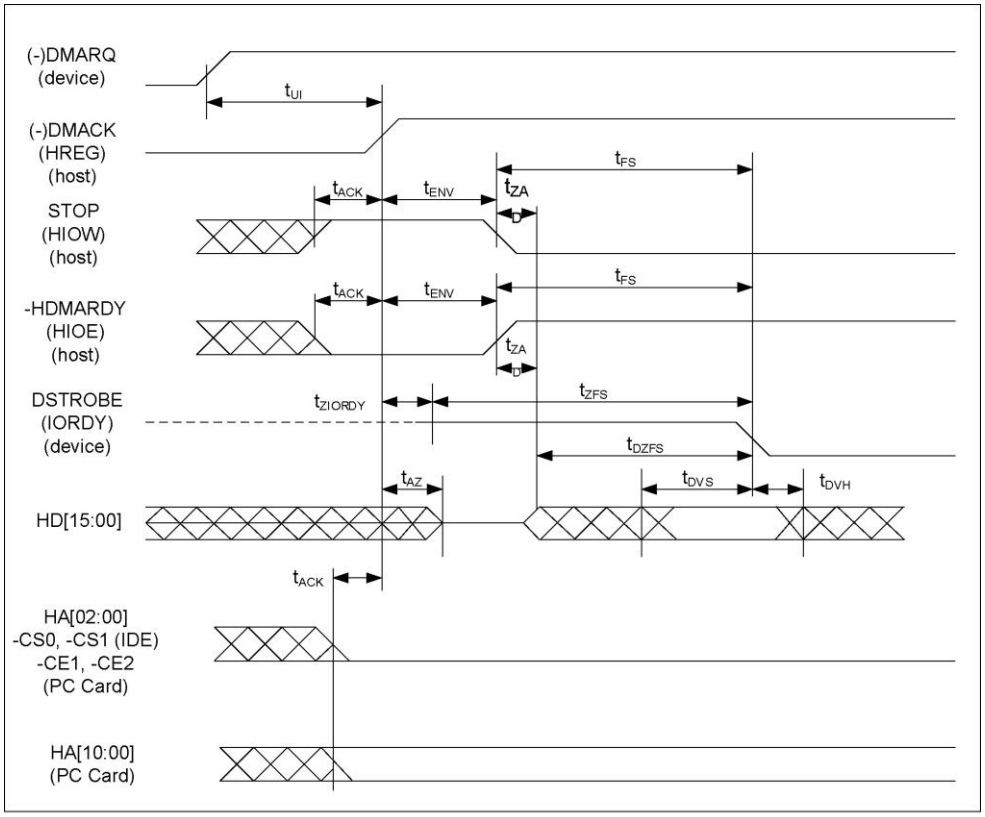
Symbol	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	Unit
tDSIC (min)	14.7	9.7	6.8	6.8	4.8	2.3	ns
tDHIC (min)	4.8	4.8	4.8	4.8	4.8	2.8	ns
tDVSIC (min)	72.9	50.9	33.9	22.6	9.5	6.0	ns
tDVHIC (min)	9.0	9.0	9.0	9.0	9.0	6.0	ns

Table 23: Ultra DMA Sender and Recipient IC Timing Parameter Descriptions

Symbol	Parameter
tDSIC	Recipient IC data setup time (from data valid until STROBE edge)
tDHIC	Recipient IC data hold time (from STROBE edge until data may become invalid)
tDVSIC	Sender IC data valid setup time (from data valid until STROBE edge)
tDVHIC	Sender IC data valid hold time (from STROBE edge until data may become invalid

Table 24: Ultra DMA AC Signal Requirements

Symbol	Parameter	Max (V/ns)
SRISE	Rising Edge Slew Rate for any signal	1.25
SFALL	Falling Edge Slew Rate for any signal	1.25



Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 11: UDMA Data-In Burst Initiation Timing

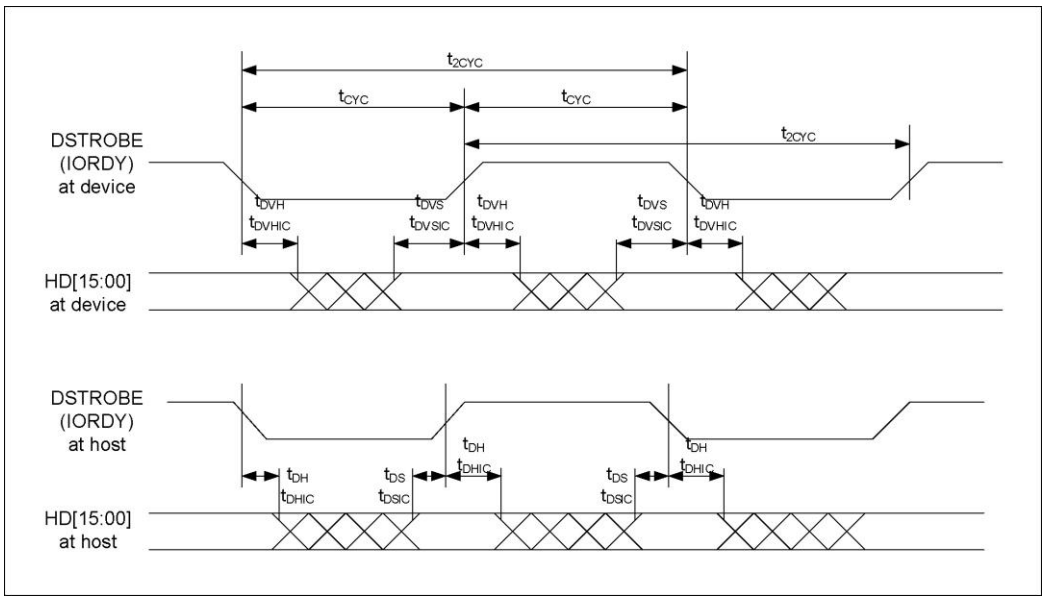
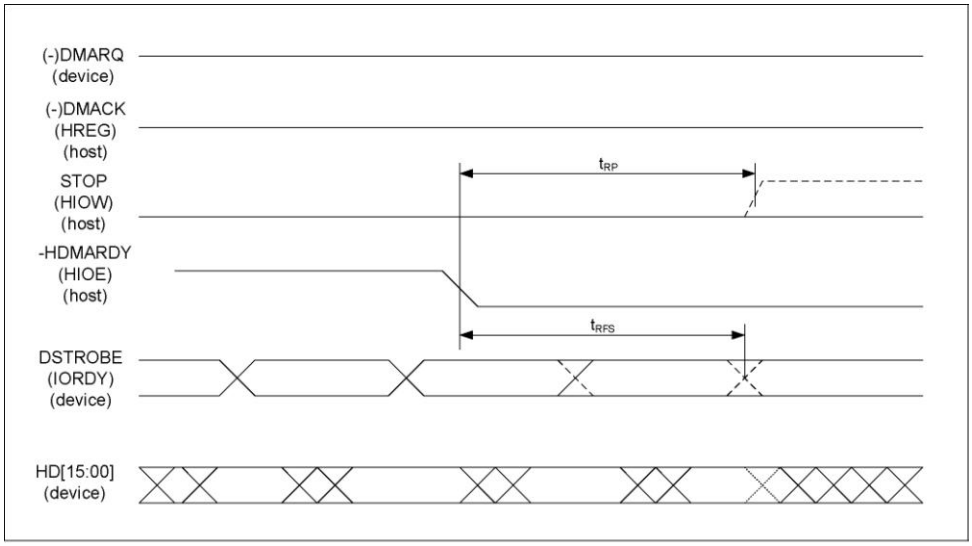
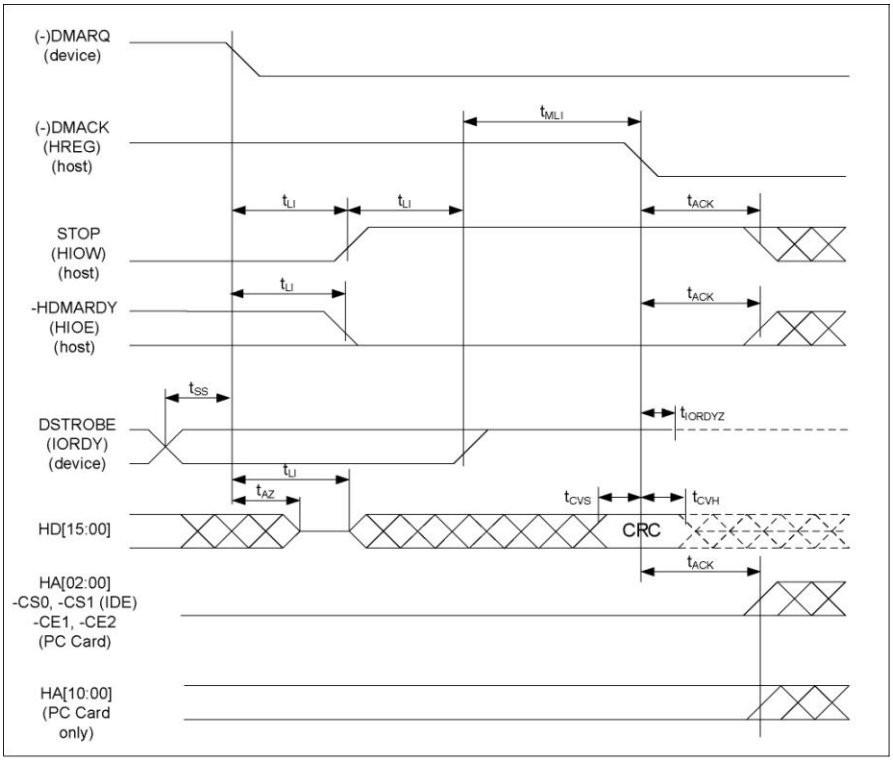


Figure 12: Sustained UDMA Data-In Burst Timing



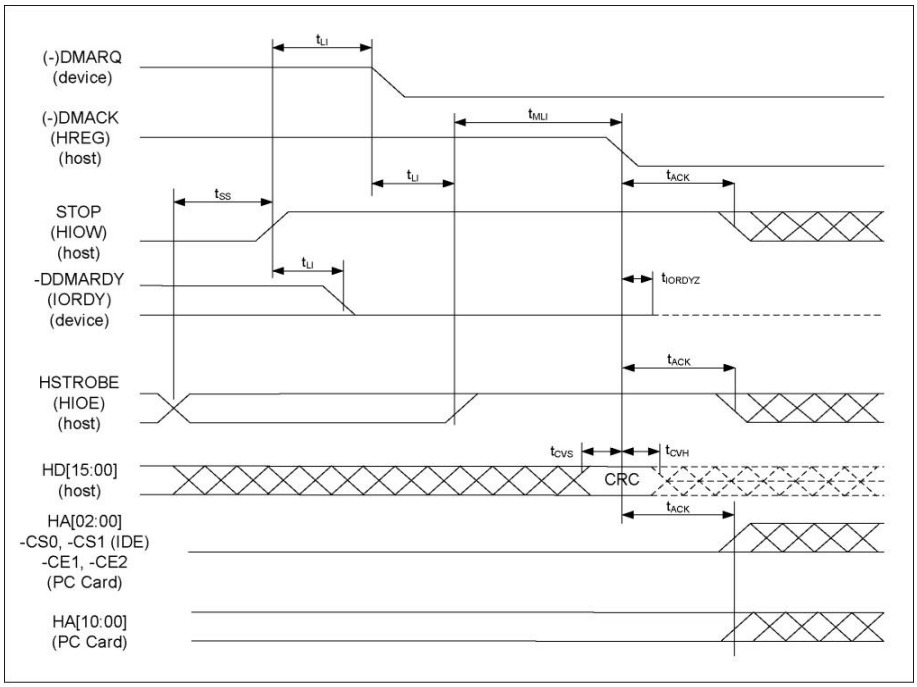
Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 13: UDMA Data-In Burst Host Pause Timing



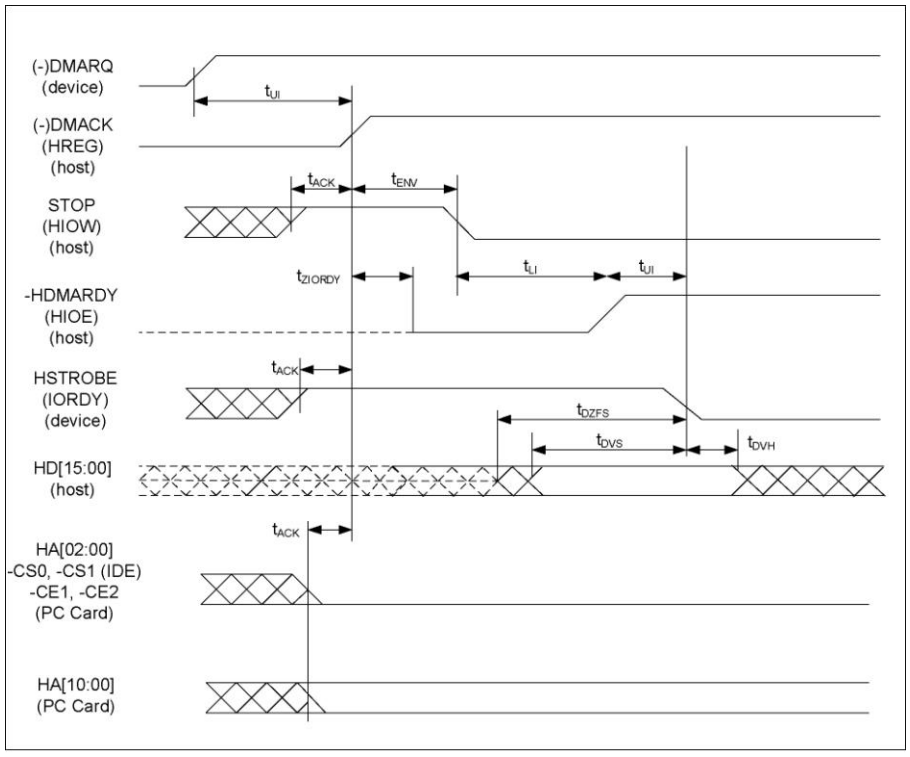
Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 14: UDMA Data-In Burst Device Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 15: UDMA Data-In Burst Host Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 16: UDMA Data-Out Burst Initiation Timing

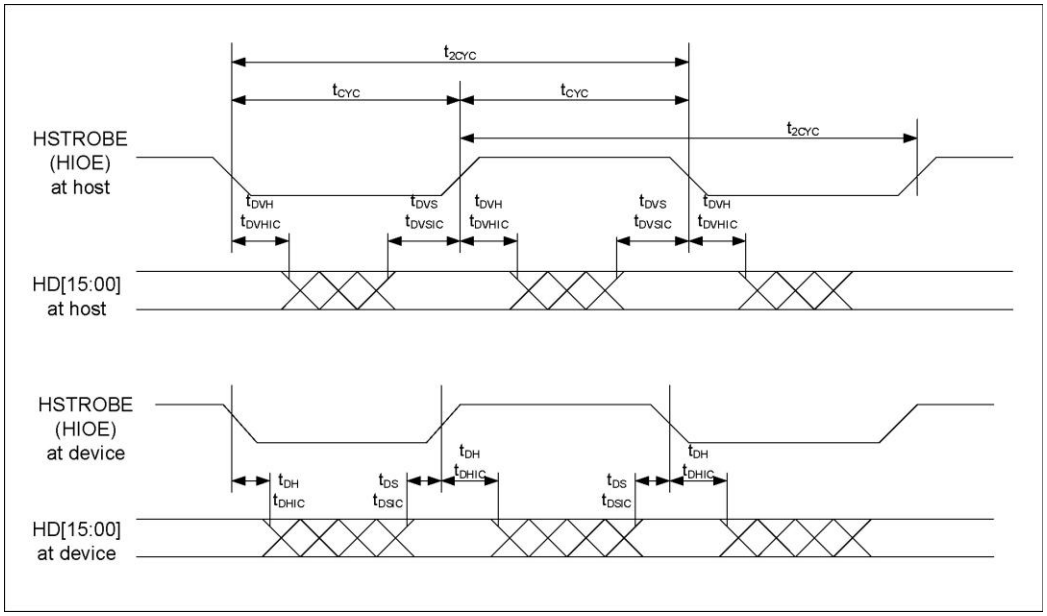
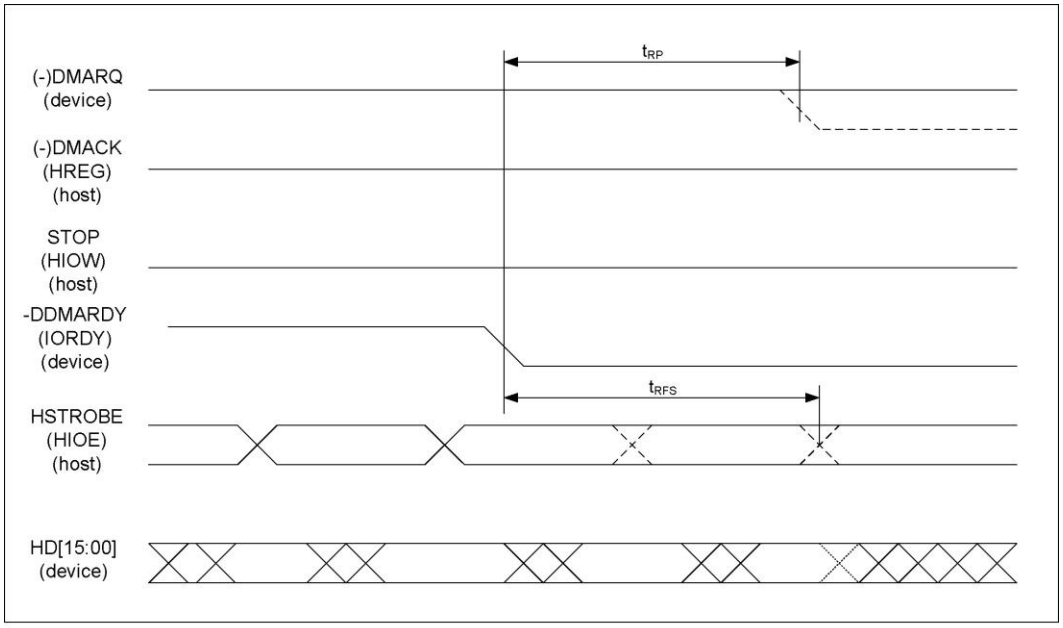
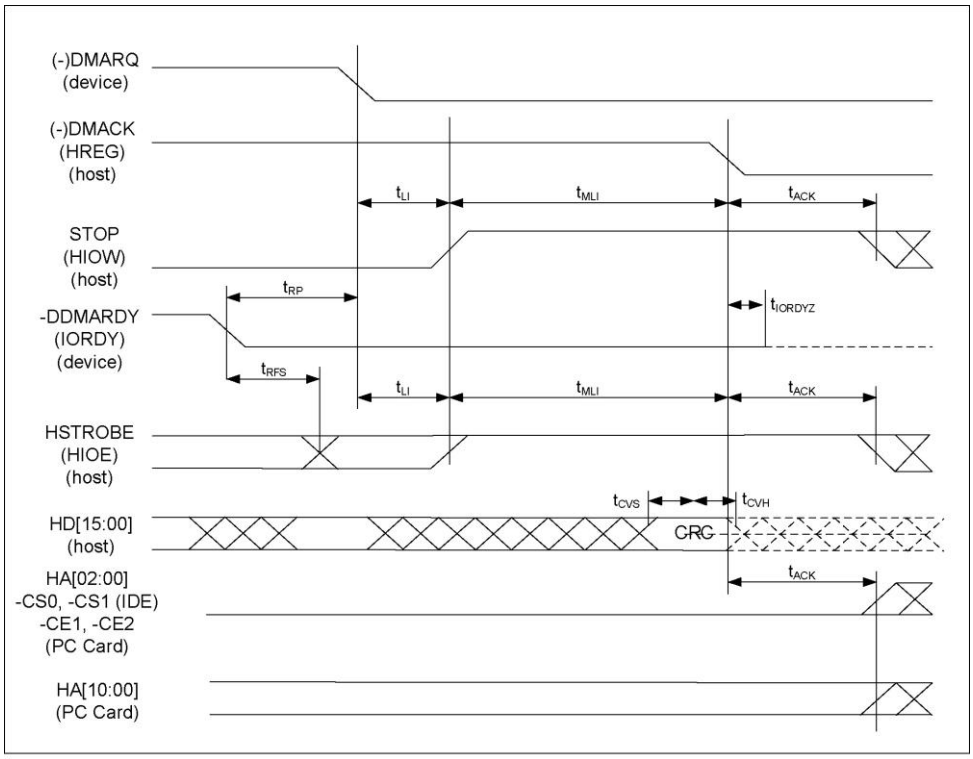


Figure 17: Sustained UDMA Data-Out Burst Timing



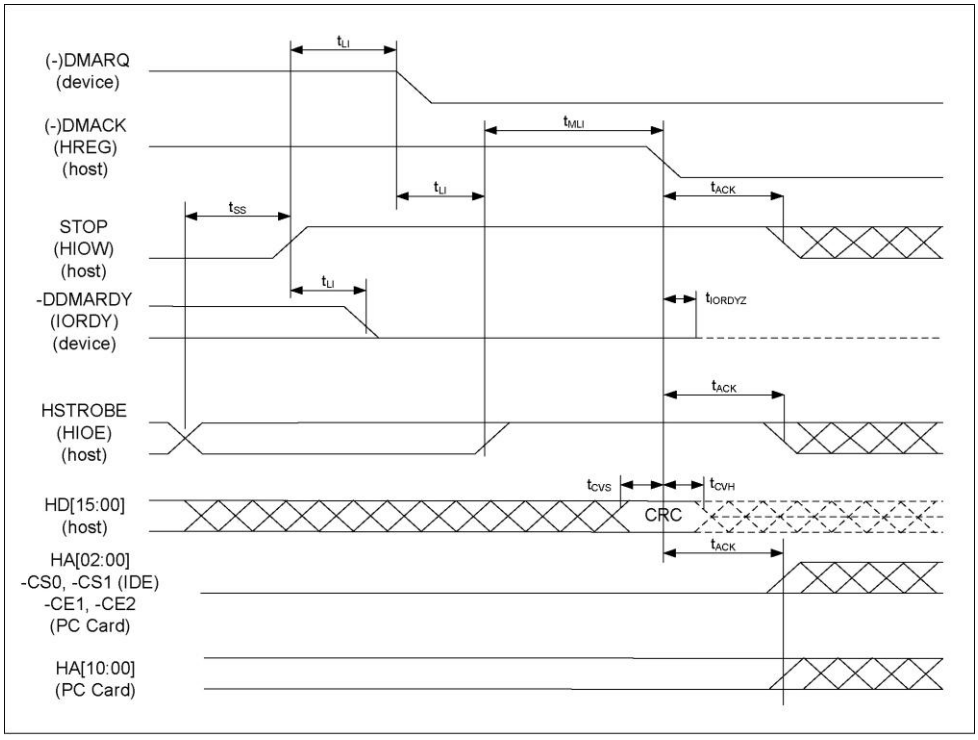
Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 18: UDMA Data-Out Burst Device Pause Timing



Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 19: UDMA Data-Out Burst Device Termination Timing



Note: All waveforms in this diagram are shown with the asserted state high.
Negative true signals appear inverted on the bus relative to the diagram.

Figure 20: UDMA Data-Out Burst Host Termination Timing

4.0 Host Access Specification

4.1 Task File Register and Byte/Word/Odd-Byte Mode Mappings

Please refer to the CompactFlash standard for complete details on the following items:

- Task File Register mapping for the interface modes
- Byte/Word/Odd-byte mode mapping within each of the interface modes

4.2 Host Access Interface Modes

The host can access the CF Card by using the following interface modes with the Task Registers:

- *PC Card Memory Mode, Attribute Memory*
  The Card Information Structure (CIS) in Attribute Memory can be accessed by Byte/Word/Odd-byte modes in PC Card Memory Mode. The -REG signal must be asserted when accessing Attribute Memory. The CF Card is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register. An example of a CIS is listed in *4.3, Card Information Structure (CIS).*
- *PC Card Memory Mode, Common Memory*
  Common Memory can be accessed in the Byte/Word/Odd Byte modes in PC Card Memory Mode. The -REG signal must be de-asserted when accessing the Common Memory. The CF Card is mapped to PC Card Memory Mode by the Index bits in the Configuration Option Register
- *PC Card I/O Mode*
  The CF Card can be accessed by Byte/Word/Odd Byte modes in PC Card I/O Mode. The CF Card is mapped to PC Card I/O Mode by the Index bits in the Configuration Option Register. The Index bits also select Contiguous I/O, Primary I/O, or Secondary I/O mapping when using the PC Card I/O Mode.
- *True-IDE mode*
  The CF Card is configured in a True IDE Mode of operation when the -ATASEL input signal is asserted GND by the host at power up. In the True IDE Mode, Attribute Registers are not accessible from the host. The Data Register is accessed in word (16-bit) mode at power up. The CF Card permits 8-bit accesses if the host issues a Set Feature Command to put the CF Card in 8-bit mode. Parameter information that the CF Card uses in True IDE mode is returned when the Identify Drive command (ECh) is invoked. Refer to *4.4 Identify Drive Parameter* for an example.

4.3 Card Information Structure (CIS)

The card uses a Card Information Structure (CIS) as summarized below:

1. 0000: Code 01, link 04
   D79 01 FF
   Tuple CISTPL_DEVICE (01), length 4 (04) at offset 0
   - Device type is FUNCSPEC
   - Device speed is 80ns
   - Write protect switch is not in control
   - Device size is 2K bytes
2. 0006: Code 1C, link 05
   02 DF 79 01 FF
   Tuple CISTPL_DEVICE_OC (1C), length 5 (05) at offset 6
   - Device conditions: minimum cycle with WAIT at Vcc = 3.3V
   - Device type is FUNCSPEC
   - Device speed is 80ns
   - Write protect switch is not in control
   - Device size is 2K bytes
3. 000D: Code 18, link 02
   DF 01
   Tuple CISTPL_JEDEC_C (18), length 2 (02) at offset B
   - Device 0 JEDEC id: Manufacturer DF, ID 01
4. 0011: Code 20, link 04
   4F 00 00 00
   Tuple CISTPL_MANFID (20), length 4 (04) at offset 11
   - Manufacturer # 0x004F hardware rev 0.00
5. 0017: Code 15, link 14
   04 01 53 54 45 43 20 4D 32 00 53 54 45 43 20 4D 32 00 00 FF
   Tuple CISTPL_VERS_1 (15), length 20 (14) at offset 17
   - Major version 4, minor version 1
   - Product Information: "STEC M2" (Manufacuturer) "STEC M2" (Product Name)
6. 002D: Code 21, link 02
   04 /xx 01
   Tuple CISTPL_FUNCID (21), length 2 (02) at offset 2D

   Function code 04 (Fixed), or xx (Removable), system init 01
7. 0031: Code 22, link 02
   01 01
   Tuple CISTPL_FUNCE (22), length 2 (02) at offset 31
   - This is an PC Card ATA Disk

8. 0035: Code 22, link 03
   02 0C 0F
   Tuple CISTPL_FUNCE (22), length 3 (03) at offset 35
   - Vpp is not required
   - This is a silicon device
   - Identify Drive Model/Serial Number is guaranteed unique
   - Low-Power Modes supported: Sleep Standby Idle
   - Drive automatically minimizes power
   - All modes include 3F7 or 377
   - Index bit is not supported
   - -IOIS16 is unspecified in Twin configurations
9. 003A: Code 1A, link 05
   01 03 00 02 0F
   Tuple CISTPL_CONFIG (1A), length 5 (05) at offset 3A
   - Last valid configuration index is 3
   - Configuration Register Base Address is 200
   - Configuration Registers Present:
     - Configuration Option Register at 200
     - Card Configuration and Status Register at 202
     - Pin Replacement Register at 204
     - Socket and Copy Register at 206
10. 0041: Code 1B, link 08
    C0 C0 A1 01 55 08 00 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 8 (08) at offset 41
    - Configuration Table Index is 00 (default)
    - Interface type is Memory
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support required
    - Vcc Power Description: Nom V = 5.0 V
    - Map 2048 bytes of memory to CF Card address 0
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
11. 004B: Code 1B, link 06
    00 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 4B
    - Configuration Table Index is 00
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

12. 0053: Code 1B, link 0A
    C1 41 99 01 55 64 F0 FF FF 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 10 (0A) at offset 53
    - Configuration Table Index is 01 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 4 I/O lines, bus size 8 or 16
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Interrupts in mask FFFF are supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
13. 005F: Code 1B, link 06
    01 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 5F
    - Configuration Table Index is 01
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA
14. 0067: Code 1B, link 0F
    C2 41 99 01 55 EA 61 F0 01 07 F6 03 01 EE 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 67
    - Configuration Table Index is 02 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 10 I/O lines, bus size 8 or 16
    - I/O block at 01F0, length 8
    - I/O block at 03F6, length 2
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Only IRQ14 is supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
15. 0078: Code 1B, link 06
    02 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 78
    - Configuration Table Index is 02
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

16. 0080: Code 1B, link 0F
    C3 41 99 01 55 EA 61 70 01 07 76 03 01 EE 20
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F) at offset 80
    - Configuration Table Index is 03 (default)
    - Interface type is I/O
    - BVDs not active, WP not active, RdyBsy active
    - Wait signal support not required
    - Vcc Power Description: Nom V = 5.0 V
    - Decode 10 I/O lines, bus size 8 or 16
    - I/O block at 0170, length 8
    - I/O block at 0376, length 2
    - IRQ may be shared, pulse and level mode interrupts are supported
    - Only IRQ14 is supported
    - Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown
17. 0091: Code 1B, link 06
    03 01 21 B5 1E 4D
    Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06) at offset 91
    - Configuration Table Index is 03
    - Vcc Power Description: Nom V = 3.30 V, Peak I = 45.0 mA
18. 0099: Code 14, link 00
    Tuple CISTPL_NO_LINK (14), length 0 (00) at offset 99
19. 009B: Code FF
    Tuple CISTPL_END (FF) at offset 9B

4.4 Identify Drive Parameter

An example of the parameter information received from the CF Card when invoking the Identify Drive command (ECh) is listed in Table 25.

Table 25: Identify Drive Parameter Information

Word Address	Data	Total Bytes	Description
0	XXXXH	2	*848AH:* Removable media device when used as CF card; *044AH:* Fixed media device when used as IDE device
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per track
5	XXXXH	2	Do not use this word. Before retirement, was number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 - 8	XXXXH	4	Number of sectors per CF Card (word 7 = MSW, word 8 = LSW)
9	0000H	2	Reserved
10 - 19	Unique per card	20	Serial Number in ASCII (20 characters): STEC proprietary
20	XXXXH	2	Do not use this word. Before retirement, was buffer type
21	XXXXH	2	Do not use this word. Before retirement, was buffer size in 512 byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long commands
23 - 26	See description	8	Firmware revision in ASCII (8 characters): 20070918 32 30 30 37 30 39 31 38 hex
27 - 46	See description	40	Model Number in ASCII (40 characters): STEC M2 <left justified> 53 54 45 43 20 4D 32 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 20 hex
47	8001H	2	Maximum of 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0B00H	2	Standby Timer defined; IORDY supported; IORDY may not be disabled; DMA supported; LBA supported;
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single word DMA data transfer cycle timing mode (not supported)
53	0007H	2	Words 54 – 58, 64 – 70, and 88 are valid
54	XXXXH	2	Number of Current Cylinders
55	XXXXH	2	Number of Current Heads
56	XXXXH	2	Number of Current Sectors Per Track
57	XXXXH	2	LSW of the Current Capacity in Sectors
58	XXXXH	2	MSW of the Current Capacity in Sectors
59	010XH	2	Current Setting for Block Count=1 for R/W Multiple commands
60 - 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single word DMA transfer not supported
63	0007H	2	Multiword DMA modes 0-2 supported

Word Address	Data	Total Bytes	Description
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum multiword DMA transfer cycle time per word (120ns)
66	0078H	2	Recommended multiword DMA transfer cycle time per word (120ns)
67	0078H	2	Minimum PIO transfer without flow control (120ns)
68	0078H	2	Minimum PIO transfer with IORDY flow control (120ns)
69 - 79	0000H	22	Reserved
80	0070H	2	Major revision number; ATA/ATAPI-4 and ATA/ATAPI-5 supported
81-87	XXXXH	2	Reserved
88	003FH	2	Ultra DMA modes 0-5 supported
89-255	334	334	Reserved
XXXXH = These values depend on the specific CF Card.			

5.0 Registers

This chapter lists the registers of the CF Card. Refer to CompactFlash standards for further details.

5.1 Configuration Registers

In PC Card Mode, four configuration registers, as listed in Table 26, are used.

Note: In True IDE Mode, these registers cannot be used.

Table 26: Configuration Registers

Configuration Register	Description
Configuration Option Register	This register is used to configure and observe the status of the CF Card, and to issue soft resets to it. Also, the Index bits of this register are used to select the PC Card mapping mode that the CF Card uses: 1) PC Card Memory, 2) PC Card Contiguous I/O, 3).PC Card Primary I/O, and 4) PC Card Secondary I/O
Configuration and Status Register	This register is used for observing the CF Card state.
Pin Replacement Register	This register is used for providing the signal state of -IREQ when the CF Card is configured in the PC Card I/O Mode.
Socket and Copy Register.	This read/write register is used to identify the CF Card from other devices. This register should be set by the host before this Configuration Option register is set.

5.2 Task File Registers

Table 27: CF Card Task File Registers

Task File Register	Description
Data Register	The Data Register is a 16-bit read/write register used for transferring data between the CF Card and the host. This register can be accessed in word mode and byte mode.
Error Register	The Error Register is a read-only register that is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to “0” (Ready). Diagnostic Codes are returned in the Error Register after a Execute Drive Diagnostic command (code 90h). Extended Error Codes returned in the Error Register after an Request Sense command (code 03h).
Sector Count Register	This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CF Card. If the value in the register is 0, a count of 256 sectors is indicated.
Sector Number Register	When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.
Cylinder Low Register	In CHS mode (LBA=0), this register contains the low-order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.
Cylinder High Register	In CHS mode (LBA=0), this register contains the high-order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.
Drive/Head Register	This register selects the CF Card address translation (CHS or LBA) and provides head address (CHS) or high-order address bits 27:24 for LBA.
Status Register	This read-only register indicates status of a command execution. When the BSY bit is “0”, the other bits are valid; when the BSY bit is “1”, the other bits are not valid. When the register is read, the interrupt pin, is cleared.
Alternate Status Register	This register is the same as the Status register, except that is not negated when the register is read.
Device Control Register	This write-only register is used for controlling the interrupt request and issuing an ATA soft reset to the CF Card.
Drive Address Register	This read-only register is used for confirming the CF Card’s status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host’s I/O space because of potential conflicts on bit 7.
Command Register	This write-only register is used for writing the command that executes the CF Card’s operation. The command code is written in the command register after its parameters are written in the Task File during the CF Card ready state.

6.0 Supported ATA Commands

The ATA commands used by the CF Card are listed in Table 28. Refer to CompactFlash standards for details.

Table 28: CF Card Supported ATA Commands

Command Set	Code	Description
Check Power Mode	E5h or 98h	This command checks the power mode.
Execute Drive Diagnostic	90h	Command performs internal diagnostic tests implemented by the CF Card. Diagnostic Code is returned in Error Register.
Erase Sector(s)	C0h	Cmd is used to pre-erase/condition data sectors in advance.
Format Track	50h	This command writes the desired head and cylinder of the selected drive with a vender unique data pattern (typically 00h or FFh). Card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.
Identify Drive	ECh	This command lets the host receive parameter information from the CF Card in the same protocol as Read Sector(s) command.
Idle	E3h or 97h	This command causes the CF Card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.
Idle Immediate	E1h or 95h	This command causes the CF Card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt.
Initialize Drive Parameters	91h	This command enables the host to set the number of sectors per track and the number of heads per cylinder.
NOP	00h	No Operation.
Read Buffer	E4h	This command enables the host to read the current contents of the CF Card's sector buffer.
Read DMA	C8h	If UDMA is enabled, this command is the sector read command used for UDMA transfer. If UDMA is not enabled, this command is the sector read command used for MWDMA transfer
Read Multiple	C4h	This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Read Long Sector	22h or 23h	Command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.
Read Sector(s)	20h (w/ retry) 21h (w/o retry)	Command reads from 1 to 256 sectors as specified in Sector Count register. A sector count of 0 requests 256 sectors. Transfer begins at sector specified in Sector Number register.
Read Verify Sector(s)	40h (w/ retry) 41h (w/o retry	This command verifies one or more sectors on the CF Card by transferring data from the flash media to the data buffer in the CF Card and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.
Recalibrate	1Xh	The CF Card performs only the interface timing and register operations. When this command is issued, the CF Card sets BSY and waits for an appropriate length of time, after which it clears BSY and issues an interrupt. When this command ends normally, the CF Card is initialized.
Request Sense (Extended Error)	03h	Command requests extended error code after command ends with error. Extended error code is returned in Error Register.

Command Set	Code	Description
Seek	7Xh	This command is effectively a NOP command to the CF Card although it does perform a range check.
Set Features	EFh	This command is used by the host to establish or select certain features.
Set Multiple Mode	C6h	Command enables card to perform multiple read and write operations and establishes block count for these commands.
Set Sleep Mode	E6h or 99h	This is the only command that allows the host to set the CF Card into Sleep mode. When the CF Card is set to sleep mode, the CF Card clears the BSY line and issues an interrupt. The CF Card enters sleep mode and the only method to make the CF Card active again (back to normal operation) is by performing a hardware reset or a software reset.
Stand By	E2h or 96h	This command sets the CF Card in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the CF Card returns to the idle mode, the timer starts a countdown. Time is set in Sector Count Register.
Stand By Immediate	E0h or 94h	This command causes the CF Card to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.
Translate Sector	87h	This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.
Wear Level	F5h	This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.
Write Buffer	E8h	This command enables the host to overwrite the contents of the CF Card's sector buffer with any data pattern desired.
Write DMA	CAh	If UDMA is enabled, this command is the sector write command used for UDMA transfer. If UDMA is not enabled, this command is the sector write command used for MWDMA transfer.
Write Long Sector	32h or 33h	This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.
Write Multiple	C5h	This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.
Write Multiple w/o Erase	CDh	This command is similar to the Write Multiple command, except that an implied erase before the write operation is not performed. **Note:** Before using this command, it is required to erase the respective sectors using the Erase Sectors command
Write Sector(s)	30h (w/ retry) 31h (w/o retry)	This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.
Write Sector(s) w/o Erase	38h	This command is similar to the Write Sector(s) command, except that an implied erase before the write operation is not performed. **Note:** Before using this command, it is required to erase the respective sectors using the Erase Sectors command.
Write Verify	3Ch	This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

7.0 Appendix: CompactFlash Adapter

In addition to the CF Card form factor, a passive CompactFlash Adapter allows the card to be used in a PC Card Type II slot. This appendix provides information on the CompactFlash Adapter available from STEC.

7.1 CF Adapter Ordering Information

Refer to Table 29 for the CF Adapter part number.

Table 29: CF Adapter Ordering Information

Part Number	CF Form Factor	PC Card Form Factor
SLCFAD(I)U	Type I	Type II

Legend:

- **SLCFAD =** STEC standard CompactFlash Adapter part number prefix.
- **Part numbers without (I) =** Commercial temperature range (0ºC to 70ºC).
- **I =** Industrial temperature range (-40ºC to +85 ºC)
- **U =** RoHS-6 compliant lead-free.

7.2 CF Adapter Specifications

Table 30: CF Adapter Specifications

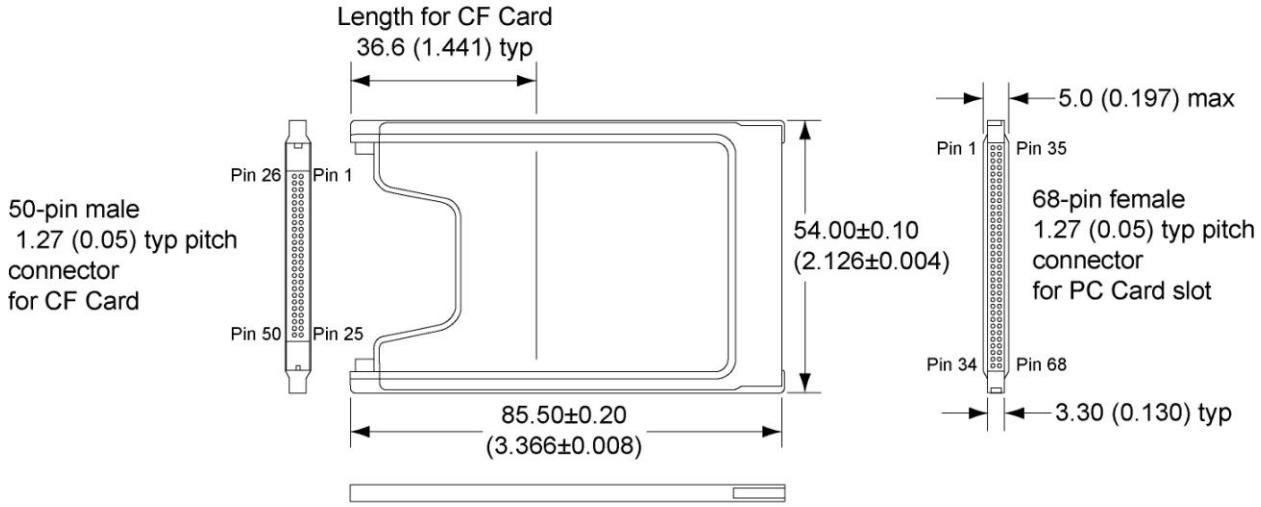
Parameter	Value
Mating/unmating life	10,000 cycles
Operating voltage	240 VAC max
Current rating	1A max
Contact resistance	3 ohms max
Insulation resistance	200M ohms min (300V DC)
Commercial Operating Temperature	0ºC to 70ºC
Industrial Operating Temperature	-40ºC to +85 ºC
Lead content	RoHS-6 compliant, lead-free

7.3 CF Adapter Package Dimensions and Pin Locations

Table 31 and Figure 21 show the mechanical dimensions of the CF Adapter Type I.

Table 31: Mechanical dimensions CF Adapter Type I

Parameter	Value
Length	85.50 ± 0.20 mm (3.366 ±. 0.008 in)
Width	54.40 ± 0.10 mm (2.126 ± 0.004 in)
Height (including label area)	5.00 mm (0.197 in) max



50-pin male connector pin lengths for CF Card:		
detect	Pins 25, 26	3.50±0.10 (0.138±0.004)
general	other pins	4.25±0.10 (0.167±0.004)
power	Pins 1, 13, 38, 50	5.00±0.10 (0.197±0.004)

Figure 21: Mechanical dimensions CF Adapters Type I

7.4 CF Adapter Pin Assignment

Table 32: CF Adapter Pin Assignment

Pin Number	PC Card	CF Card	Pin Number	PC Card	CF Card
1	GND	GND	35	GND	-IOWR
2	D03	D03	36	-CD1	-WE
3	D04	D04	37	D11	-RDY/-BSY, -IREQ, INTRQ
4	D05	D05	38	D12	VCC
5	D06	D06	39	D13	-CSEL
6	D07	D07	40	D14	-VS2
7	-CE1, -CS0	-CE1, -CS0	41	D15	RESET, -RESET
8	A10	A10	42	-CE2, -CS1	-WAIT, IORDY
9	-OE, -ATASEL	-OE, -ATASEL	43	-VS1	-INPACK, DMARQ
10		A09	44	-IORD	-REG, -DMACK
11	A09	A08	45	-IOWR	BVD2, -SPKR, -DASP
12	A08	A07	46		BVD1, -STSCHG, -PDIAG
13		VCC	47		D08
14		A06	48		D09
15	-WE	A05	49		D10
16	-RDY/-BSY, -IREQ, INTRQ	A04	50		GND
17	VCC	A03	51	VCC	
18		A02	52		
19		A01	53		
20		A00	54		
21		D00	55		
22	A07	D01	56		
23	A06	D02	57	-VS2	
24	A05	WP, -IOIS16	58	RESET, -RESET	
25	A04	-CD2	59	-WAIT, IORDY	
26	A03	-CD1	60	-INPACK, DMARQ	
27	A02	D11	61	-REG, -DMACK	
28	A01	D12	62	BVD2, -SPKR -DASP	
29	A00	D13	63	BVD1, -STSCHG, -PDIAG	
30	D00	D14	64	D08	
31	D01	D15	65	D09	
32	D02	-CE2, -CS1	66	D10	
33	WP, -IOIS16	-VS1	67	-CD2	
34	GND	-IORD	68	GND	

Legend: “-“ = Low active

8.0 Revision History

Revision	*Date*	*Description*
-101	7/16/07	Initial release.
-102	8/06/07	Warranty bullet removed from features column on page 1.
-103	10/09/07	CIS and ID Parameter tables updated. Power up table removed. UDMA timings and pinout added.
-104	10/17/07	Operating current updated.
-105	11/7/07	Layout updated for consistency and easier editing. Disclaimer notice reformatted with headings.
-106	1/2/08	16GB capacity, Type II package, and Industrial Temperature removed. CHS parameters corrected. General Description text updated.
-107	2/28/08	Power down data protection bullet removed from General Description.
-108	3/7/08	Contact information on last page updated.
-109	4/2/08	STEC China address on last page updated.

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