Am29LV010B

SPANSION®

Data Sheet *(Retired Product)*

The following document contains information on Spansion memory products.

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary.

For More Information

Please contact your local sales office for additional information about Spansion memory solutions.

This page left intentionally blank.

AMD

Am29LV010B

1 Megabit (128 K x 8-Bit)
CMOS 3.0 Volt-only Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

❥ **Single power supply operation**
— Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
— Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors

❥ **Manufactured on 0.32 µm process technology**

❥ **High performance**
— Full voltage range: access times as fast as 55 ns

❥ **Ultra low power consumption (typical values at 5 MHz)**
— 200 nA Automatic Sleep mode current
— 200 nA standby mode current
— 7 mA read current
— 15 mA program/erase current

❥ **Flexible sector architecture**
— Eight 16 Kbyte
— Supports full chip erase
— Sector Protection features:
   Hardware method of locking a sector to prevent any program or erase operations within that sector
   Sectors can be locked in-system or via programming equipment
   Temporary Sector Unprotect feature allows code changes in previously locked sectors

❥ **Unlock Bypass Mode Program Command**
— Reduces overall programming time when issuing multiple program command sequences

❥ **Embedded Algorithms**
— Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
— Embedded Program algorithm automatically writes and verifies data at specified addresses

❥ **Minimum 1,000,000 write cycle guarantee per sector**

❥ **20 Year data retention at 125°C**
— Reliable operation for the life of the system

❥ **Package option**
— 32-pin TSOP
— 32-pin PLCC

❥ **Compatibility with JEDEC standards**
— Pinout and software compatible with single-power supply Flash
— Superior inadvertent write protection

❥ **Data# Polling and toggle bits**
— Provides a software method of detecting program or erase operation completion

❥ **Erase Suspend/Erase Resume**
— Supports reading data from or programming data to a sector that is not being erased

GENERAL DESCRIPTION

The Am29LV010B is a 1 Mbit, 3.0 Volt-only Flash memory device organized as 131,072 bytes. The Am29LV010B has a uniform sector architecture.

The device is offered in 32-pin PLCC and 32-pin TSOP packages. The byte-wide (x8) data appears on DQ7-DQ0. All read, erase, and program operations are accomplished using only a single power supply. The device can also be programmed in standard EPROM programmers.

The standard Am29LV010B offers access times of 55, 70, and 90 ns (100 ns part is also available), allowing high speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a single power supply (2.7V-3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.
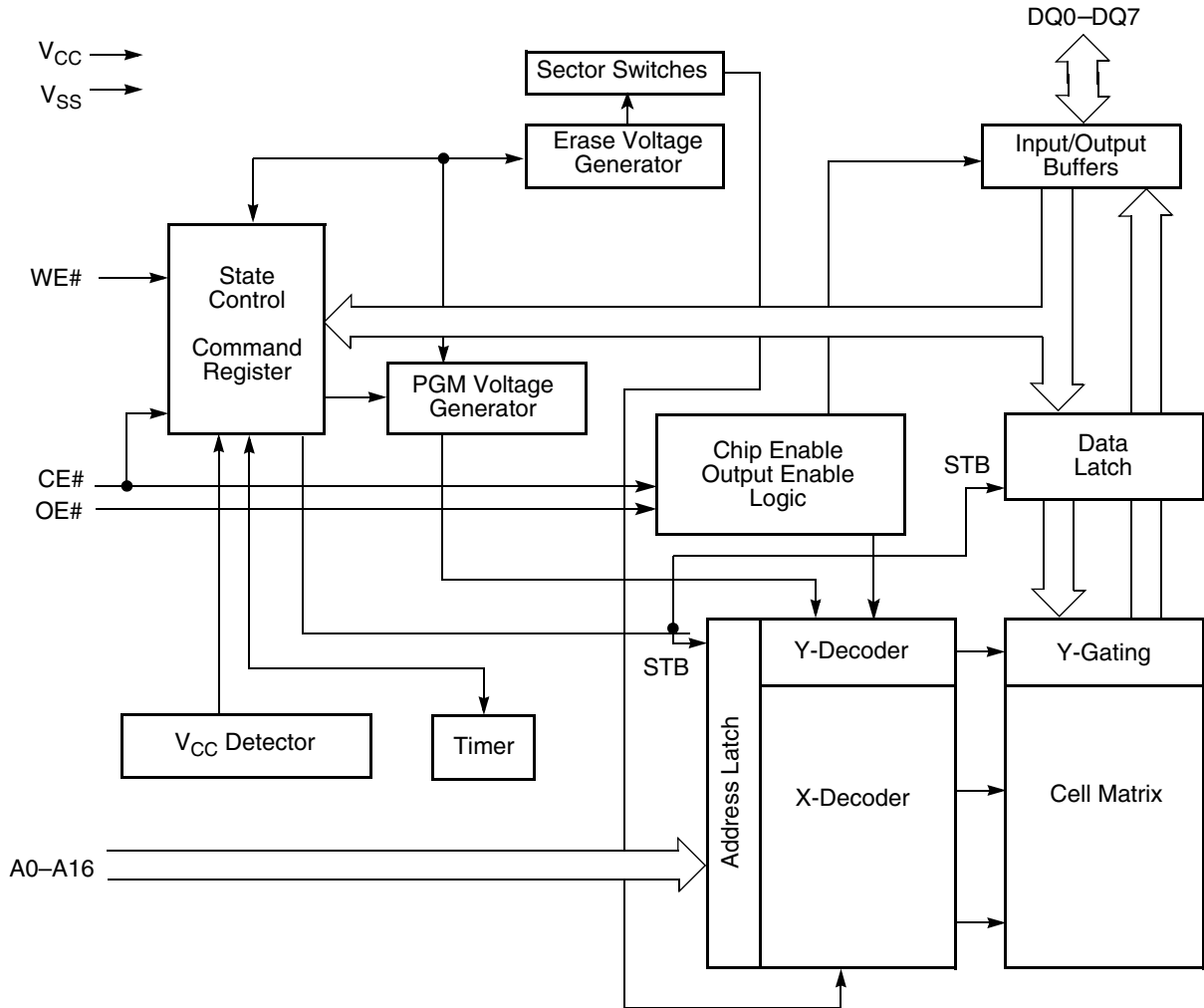
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Family Part Number		Am29LV010B		
Speed Options	Full Voltage Range: V_{CC} = 2.7–3.6 V	**-55**	**-70**	**-90**
Max access time, ns (t_{ACC})		55	70	90
Max CE# access time, ns (t_{CE})		55	70	90
Max OE# access time, ns (t_{OE})		30	30	35

Note: See "AC Characteristics" for full specifications.

BLOCK DIAGRAM

CONNECTION DIAGRAMS

32-Pin Standard TSOP

Pin	Signal		Pin	Signal
1	A11		32	OE#
2	A9		31	A10
3	A8		30	CE#
4	A13		29	DQ7
5	A14		28	DQ6
6	NC		27	DQ5
7	WE#		26	DQ4
8	V_{CC}		25	DQ3
9	NC		24	V_{SS}
10	A16		23	DQ2
11	A15		22	DQ1
12	A12		21	DQ0
13	A7		20	A0
14	A6		19	A1
15	A5		18	A2
16	A4		17	A3

PLCC

Top pins (left to right): 4 A12, 3 A15, 2 A16, 1 NC, 32 V_{CC}, 31 WE#, 30 NC

Left		Right	
5	A7	29	A14
6	A6	28	A13
7	A5	27	A8
8	A4	26	A9
9	A3	25	A11
10	A2	24	OE#
11	A1	23	A10
12	A0	22	CE#
13	DQ0	21	DQ7

Bottom pins (left to right): 14 DQ1, 15 DQ2, 16 V_{SS}, 17 DQ3, 18 DQ4, 19 DQ5, 20 DQ6

PIN CONFIGURATION

A0–A16=17 addresses

DQ0–DQ7=8 data inputs/outputs

CE# = Chip enable

OE# = Output enable

WE# = Write enable

V_{CC} = 3.0 volt-only single power supply
(see Product Selector Guide for speed
options and voltage supply tolerances)

V_{SS} = Device ground

NC   = Pin not connected internally

LOGIC SYMBOL
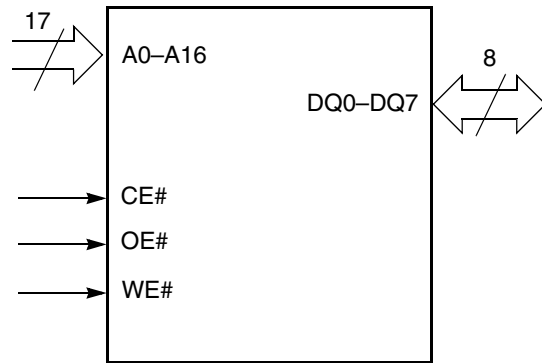
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29LV010B　　**-55**　**E**　**C**

TEMPERATURE RANGE

C= Commercial (0°C to +70°C)

D= Commercial (0°C to +70°C) with Pb-free package

I = Industrial (–40°C to +85°C)

F = Industrial (–40°C to +85°C) with Pb-free package

E = Extended (–55°C to +125°C)

K= Extended (–55°C to +125°C) with Pb-free package

PACKAGE TYPE

E= 32-Pin Thin Small Outline Package (TSOP)
Standard Pinout (TS 032)

J = 32-Pin Rectangular Plastic Leaded Chip
Carrier (PL 032)

SPEED OPTION

See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION

Am29LV010B
1 Megabit (128 K x 8-Bit) CMOS Flash Memory
3.0 Volt-only Read, Program and Erase

Valid Combinations	
AM29LV010B-55	EC, ED, EI, EF, EE, EK JC, JD, JI, JF, JE, JK
AM29LV010B-70	
AM29LV010B-90	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1.   Am29LV010B Device Bus Operations

Operation	CE#	OE#	WE#	Addresses (Note 1)	DQ0–DQ7
Read	L	L	H	A_{IN}	D_{OUT}
Write	L	H	L	A_{IN}	D_{IN}
Standby	$V_{CC} \pm 0.3$ V	X	X	X	High-Z
Output Disable	L	H	H	X	High-Z
Reset	X	X	X	X	High-Z
Sector Protect (Note 2)	L	H	L	Sector Address, A6 = L, A1 = H, A0 = L	D_{IN}, D_{OUT}
Sector Unprotect (Note 2)	L	H	L	Sector Address, A6 = H, A1 = H, A0 = L	D_{IN}, D_{OUT}
Temporary Sector Unprotect	X	X	X	A_{IN}	D_{IN}

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 $\pm$ 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. Addresses are A16–A0.

2. Sector protection/unprotection can be implemented by using programming equipment. See the "Sector Protection/Unprotection" section.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to Figure 11 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a byte, instead of four. The "Byte Program Command Sequence" section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 2 indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Command Definitions" section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The

system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to "AC Characteristics" for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# pin is held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# is held at V_{IH},

but not within $V_{CC} \pm 0.3$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC} + 30$ ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC4} in the DC Characteristics table represents the automatic sleep mode current specification.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 2.   Am29LV010B Uniform Sector Address Table

Sector	A16	A15	A14	Address Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 3. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 2). When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 4. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 3. Am29LV010B Autoselect Codes

Description	CE#	OE#	WE#	A16 to A14	A13 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29LV010B	L	L	H	X	X	V_{ID}	X	L	X	L	H	6Eh
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected)
												00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

The method intended only for programming equipment requires V_{ID} on address pin A9, and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only AMD flash devices. Publication number 22134 contains further details; contact an AMD representative to request a copy.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See "Autoselect Mode" for details.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 4 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 4 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters, and Figure 11 shows the timing diagram.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 4 shows the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table 2 for the valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Byte Program Command Sequence

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally

generated program pulses and verify the programmed cell margin. Table 4 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a "0" back to a "1".** Attempting to do so may halt the operation and set DQ5 to "1," or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 4 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares for both cycles. The device then returns to reading array data.

Figure 1 illustrates the algorithm for the program operation. See the Erase/Program Operations table in "AC Characteristics" for parameters, and to Figure 12 for timing diagrams.
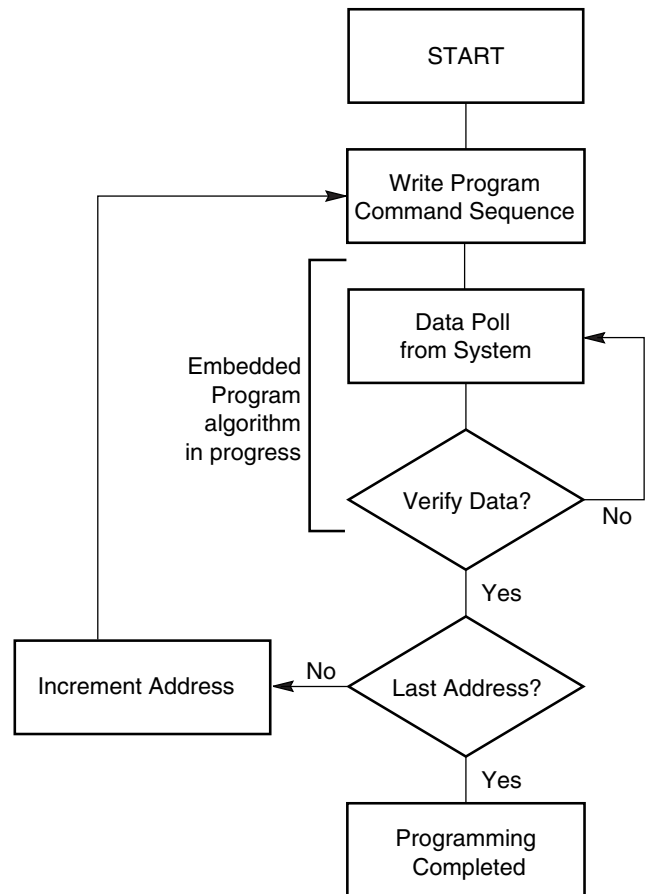
Note:See Table 4 for program command sequence.

Figure 1.   Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 4 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See "Write Operation Status" for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 2 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 13 for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table 4 shows the address and data requirements for the sector erase command sequence.

The device does *not* require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data.** The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. (Refer to "Write Operation Status" for information on these status bits.)

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to Figure 13 for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the

device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.
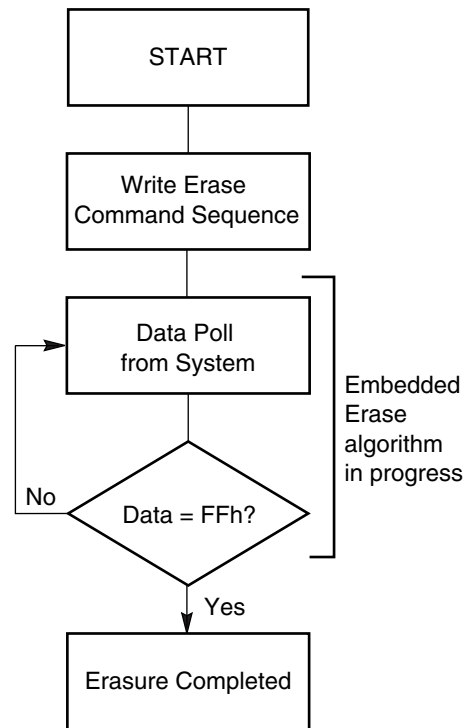
Notes:

1. *See Table 4 for erase command sequence.*

2. *See "DQ3: Sector Erase Timer" for more information.*

Figure 2.   Erase Operation

Command Definitions

Table 4. Am29LV010B Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Am29LV010B	4	555	AA	2AA	55	555	90	X01	6E				
	Sector Protect Verify (Note 8)	4	555	AA	2AA	55	555	90	SA X02	00 01				
Byte Program		4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 9)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 10)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 11)		1	XXX	B0										
Erase Resume (Note 12)		1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the WE# or CE# pulse.

PD = Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.

SA = Address of the sector to be erased or verified. Address bits A16–A14 uniquely select any sector.

Notes:

1. *See Table 1 for descriptions of bus operations.*

2. *All values are in hexadecimal.*

3. *Except when reading array or autoselect data, all bus cycles are write operations.*

4. *Address bits A16–A11 are don't care for unlock and command cycles, unless SA or PA required.*

5. *No unlock or command cycles required when device is in read mode.*

6. *The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.*

7. *The fourth cycle of the autoselect command sequence is a read cycle.*

8. *The data is 00h for an unprotected sector and 01h for a protected sector. The complete bus address in the fourth cycle is composed of the sector address (A16–A14), A1 = 1, and A0 = 0.*

9. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*

10. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.*

11. *The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*

12. *The Erase Resume command is valid only during the Erase Suspend mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 5 and the following subsections describe the functions of these bits. DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the *following* read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Figure 14, Data# Polling Timings (During Embedded Algorithms), in the "AC Characteristics" section illustrates this.

Table 5 shows the outputs for Data# Polling on DQ7. Figure 3 shows the Data# Polling algorithm.
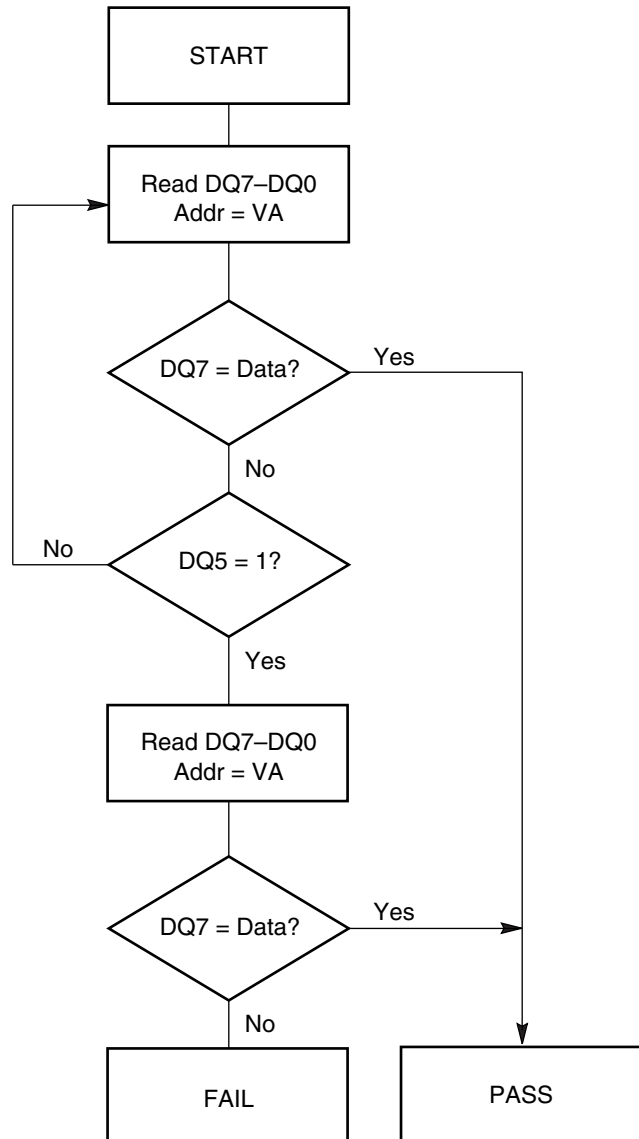
Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*

2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 3.   Data# Polling Algorithm

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on DQ6. Figure 4 shows the toggle bit algorithm in flowchart form, and the section "Reading Toggle Bits DQ6/DQ2" explains the algorithm. Figure 15 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 16 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for era-

sure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 5 to compare outputs for DQ2 and DQ6.

Figure 4 shows the toggle bit algorithm in flowchart form, and the section "Reading Toggle Bits DQ6/DQ2" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 15 shows the toggle bit timing diagram. Figure 16 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 4).

Table 5 shows the outputs for Toggle Bit I on DQ6. Figure 4 shows the toggle bit algorithm. Figure 15 in the "AC Characteristics" section shows the toggle bit timing diagrams. Figure 16 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

Figure 4.   Toggle Bit Algorithm
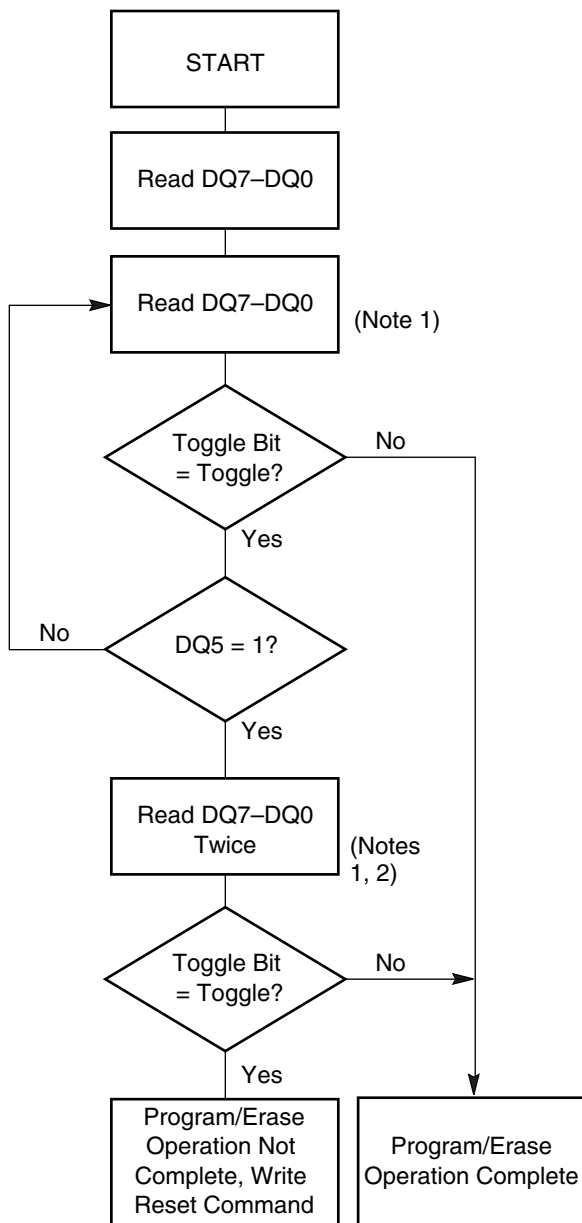
Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*

2. *Recheck toggle bit because it may stop toggling as DQ5 changes to "1". See text.*

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1." This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a "1" to a location that is previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1."

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 5 shows the outputs for DQ3.

Table 5.   Write Operation Status

|	Operation	DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.*

2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground
All pins except A9 and OE#
(Note 1) . . . . –0.5 V to V_{CC}+0.5 V

V_{CC} (Note 1). . . . . –0.5 V to +4.0 V

A9 **and** OE# (Note 2) . . . . –0.5 V to +12.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 5. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 6.*

2. *Minimum DC input voltage on pins A9 and OE# is –0.5 V. During voltage transitions, A9 and OE# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 5. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*
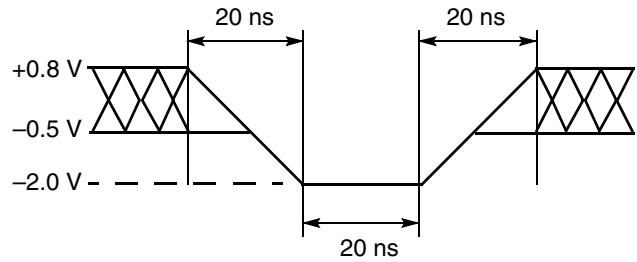
**Figure 5.   Maximum Negative
Overshoot Waveform**
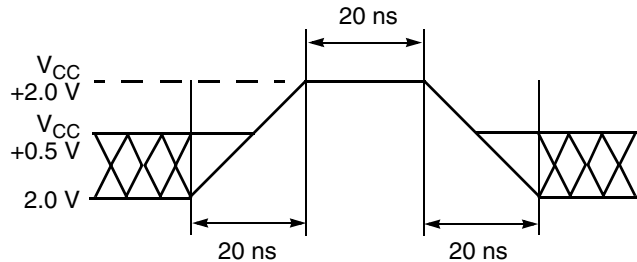
**Figure 6.   Maximum Positive
Overshoot Waveform**

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range. . . . . . +3.0 V to 3.6 V

V_{CC} for full voltage range . . . . +2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Notes 1, 2)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		7	12	mA
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2, 3, 5)	CE# = V_{IL}, OE# = V_{IH}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE# = $V_{CC} \pm 0.3$ V			0.2	5	µA
I_{CC4}	Automatic Sleep Mode Current (Notes 2, 4)	$V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V			0.2	5	µA
V_{IL}	Input Low Voltage			−0.5		0.8	V
V_{IH}	Input High Voltage			$0.7 \times V_{CC}$		$V_{CC} + 0.3$	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	$V_{CC} = 3.3$ V		11.5		12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 4.0$ mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.0$ mA, $V_{CC} = V_{CC\ min}$		$0.85\ V_{CC}$			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC\ min}$		$V_{CC} - 0.4$			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:

1.　The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.

2.　Maximum I_{CC} currents listed are tested with $V_{CC}=V_{CC}$max.

3.　I_{CC} active while Embedded Erase or Embedded Program is in progress.

4.　Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.
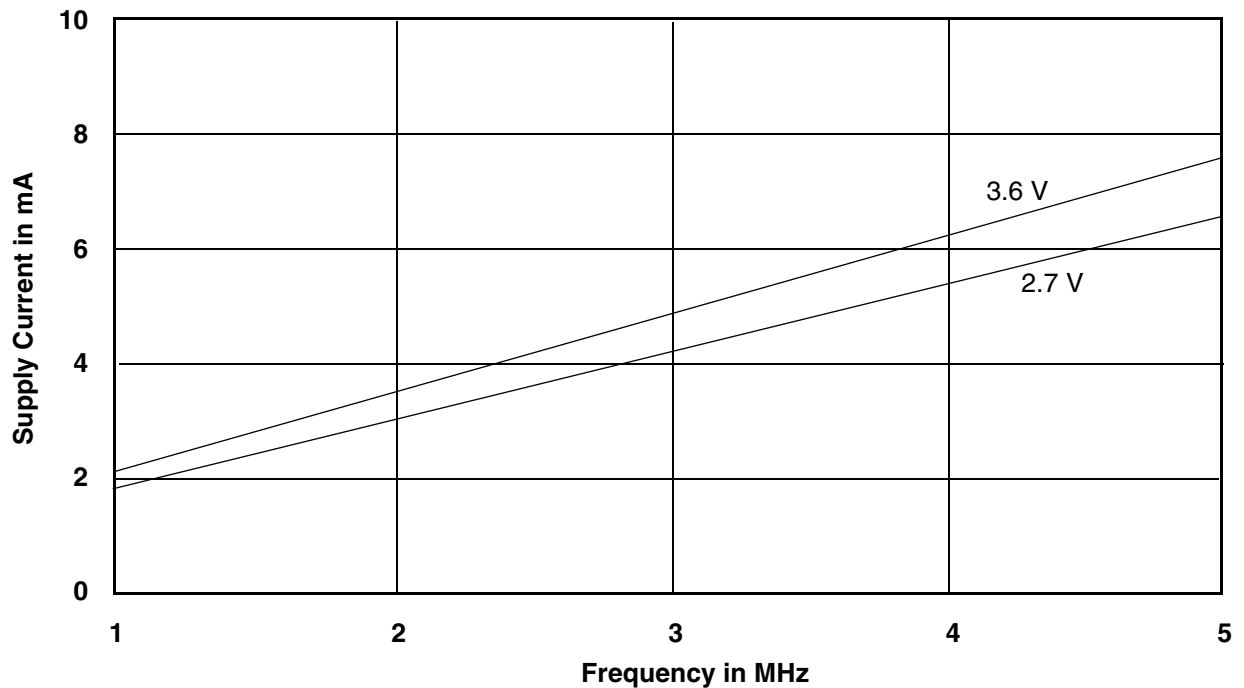
5.　Not 100% tested.

DC CHARACTERISTICS (continued)

Zero Power Flash
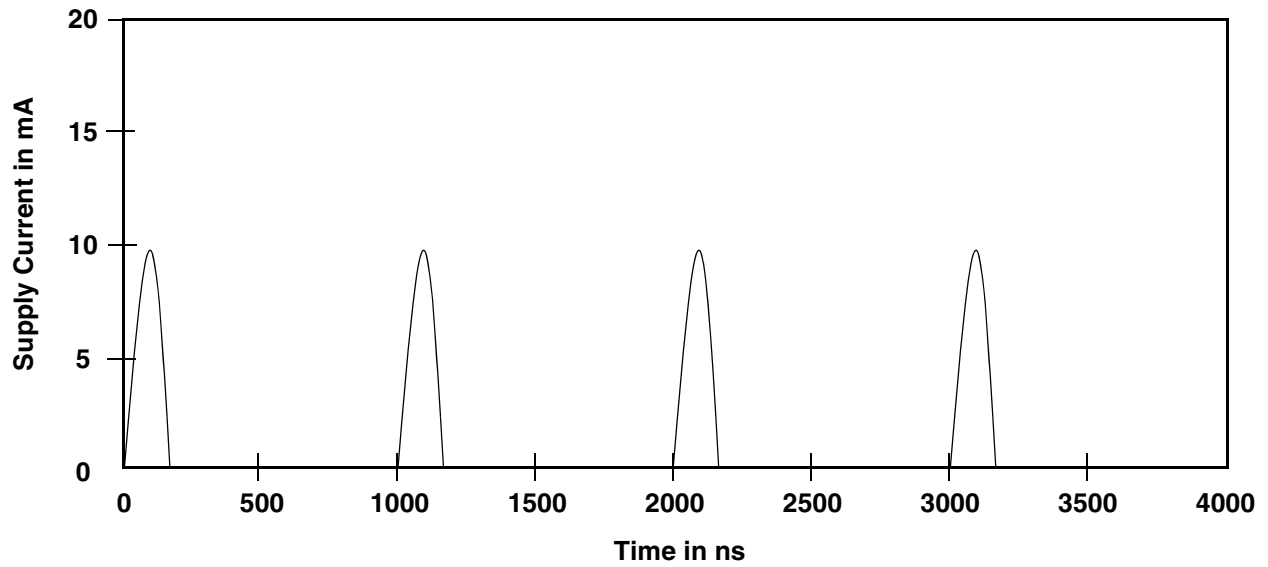
Note: *Addresses are switching at 1 MHz*

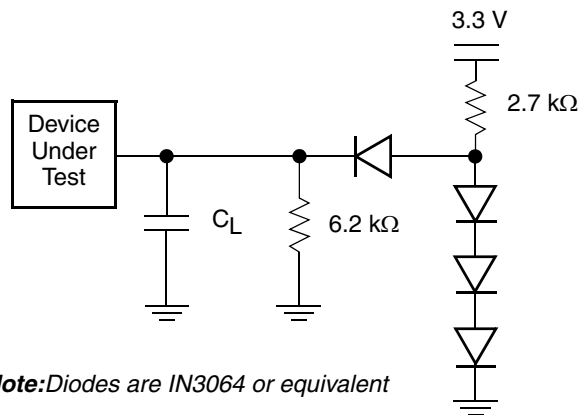**Figure 7.** I_{CC1} **Current vs. Time (Showing Active and Automatic Sleep Currents)**

Note: *T = 25 °C*

Figure 8. I_{CC1} **vs. Frequency**

TEST CONDITIONS

Note:Diodes are IN3064 or equivalent

Figure 9.   Test Setup

Table 6.   Test Specifications

Test Condition	-55	-70, -90	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

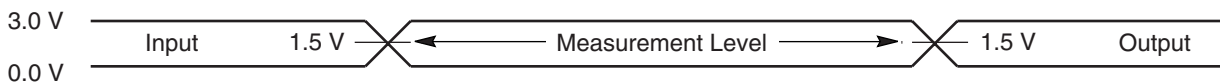| WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Figure 10.   Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Read Operations

Parameter			Test Setup			Speed Options			Unit
JEDEC	Std	Description				-55	-70	-90	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)		Min		55	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	CE# = V_{IL} OE# = V_{IL}	Max		55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max		55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max		30	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)		Max		15	25	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)		Max		15	25	30	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read	Min		0			ns
			Toggle and Data# Polling	Min		10			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)		Min		0			ns

Notes:

1. Not 100% tested.
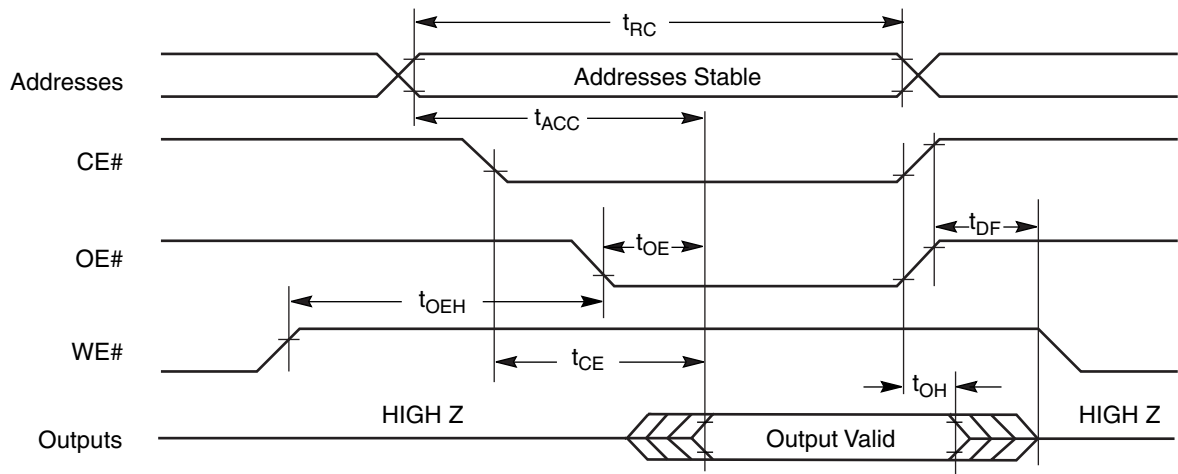
2. See Figure 9 and Table 6 for test specifications.

Figure 11.   Read Operations Timings
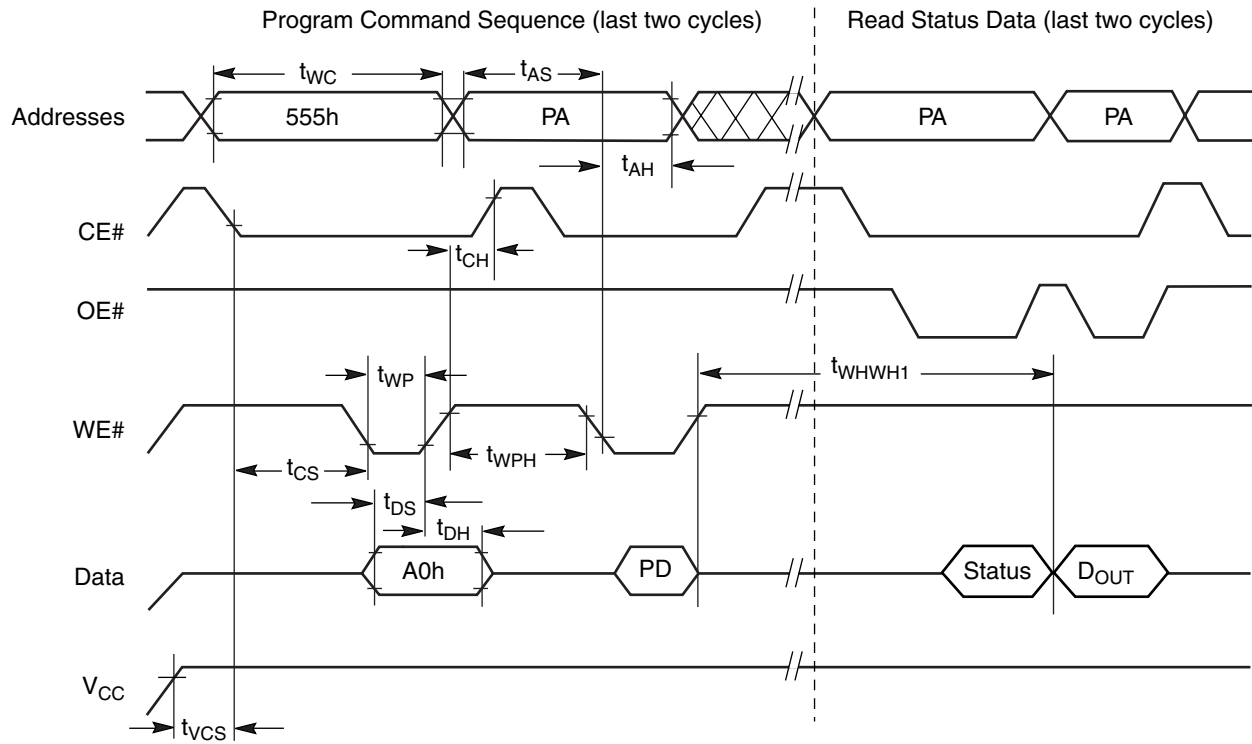
AC CHARACTERISTICS

Erase/Program Operations

Parameter				Speed Options			
JEDEC	Std	Description		-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	55	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min		0		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	20	35	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min		0		ns
	t_{OES}	Output Enable Setup Time (Note 1)	Min		0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min		0		ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min		0		ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min		0		ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	30	35	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ		9		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ		0.7		sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min		50		µs

Notes:

1. Not 100% tested.

2. See the "Erase and Programming Performance" Section for more information.
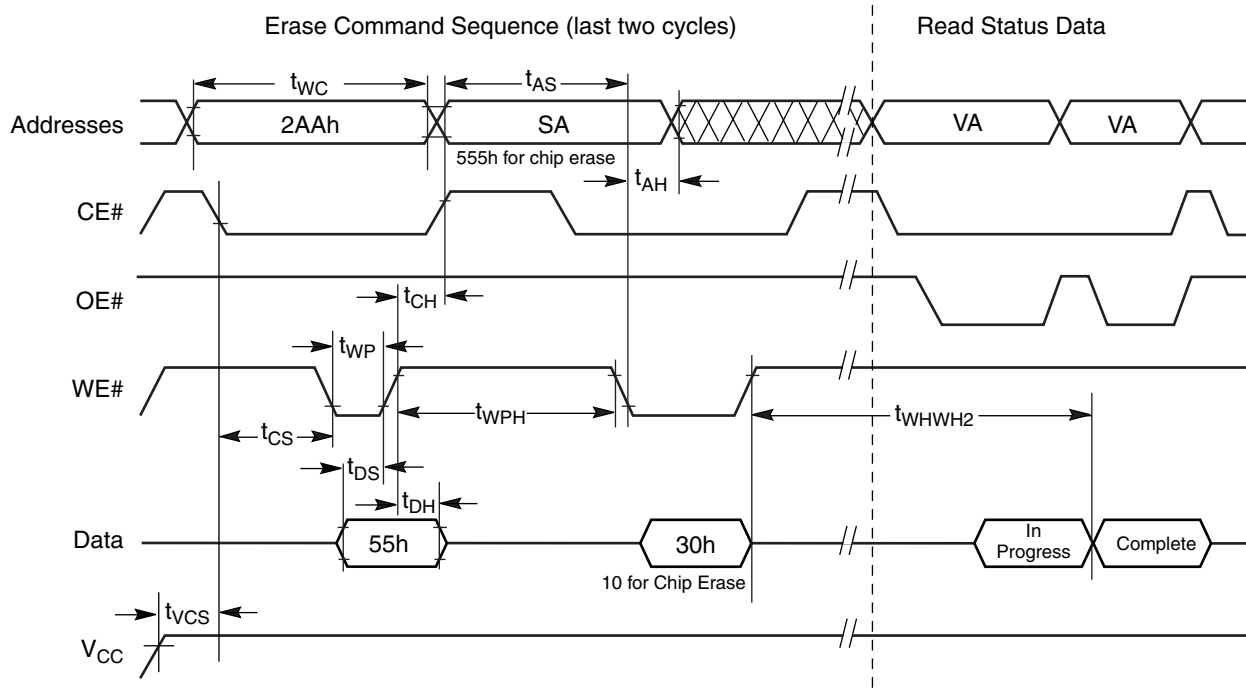
AC CHARACTERISTICS

Note:
PA = program address, PD = program data, D_{OUT} is the true data at the program address.

Figure 12.   Program Operation Timings
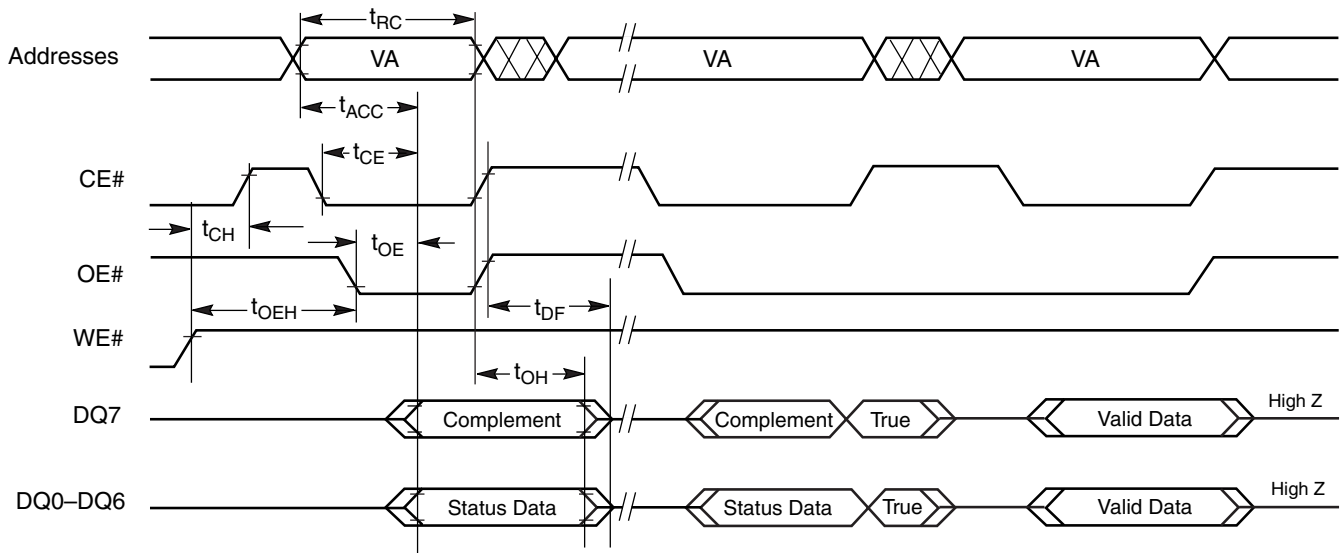
AC CHARACTERISTICS

Note:
SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").

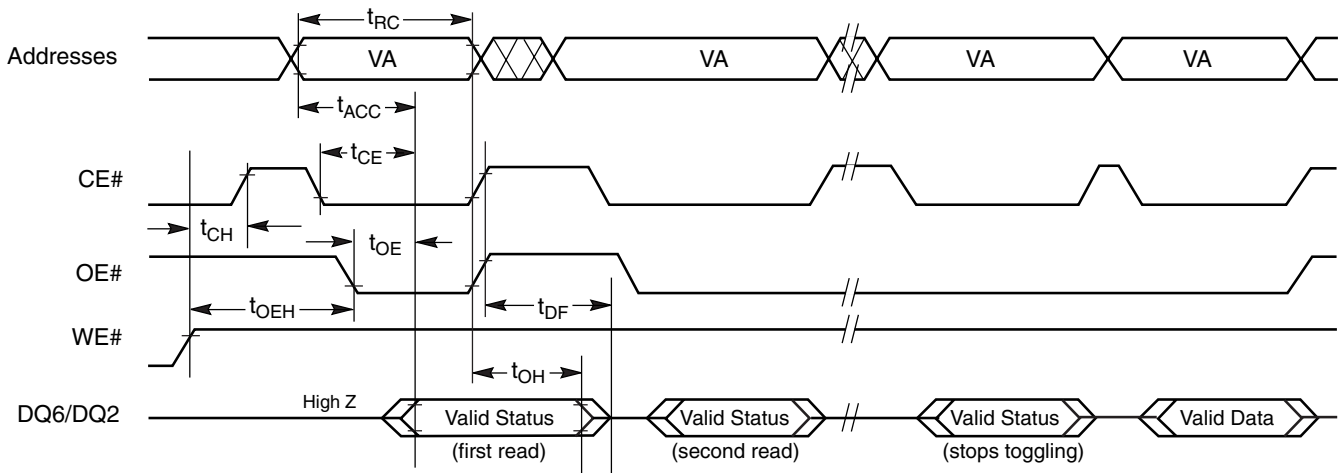**Figure 13.   Chip/Sector Erase Operation Timings**

AC CHARACTERISTICS

Note:

VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

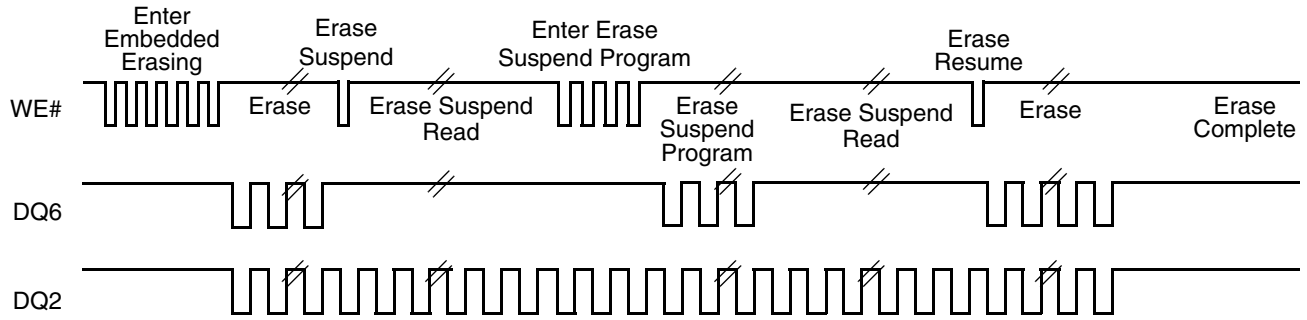**Figure 14.   Data# Polling Timings (During Embedded Algorithms)**

Note:

VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 15.   Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS

Note:

The system can use OE# or CE# to toggle DQ2/DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.

**Figure 16.   DQ2 vs. DQ6**

AC CHARACTERISTICS

Alternate CE# Controlled Erase/Program Operations

Parameter					Speed Options			
JEDEC	**Std**	**Description**			**-55**	**-70**	**-90**	**Unit**
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min		55	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min			0		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min		45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min		20	35	45	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min			0		ns
	t_{OES}	Output Enable Setup Time (Note 1)	Min			0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min			0		ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min			0		ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min			0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min		30	35	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min			30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ			9		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ			0.7		sec

Notes:

1. Not 100% tested.

2. See the "Erase and Programming Performance" Section for more information.

AC CHARACTERISTICS

Figure 17.   Alternate CE# Controlled Write Operation Timings
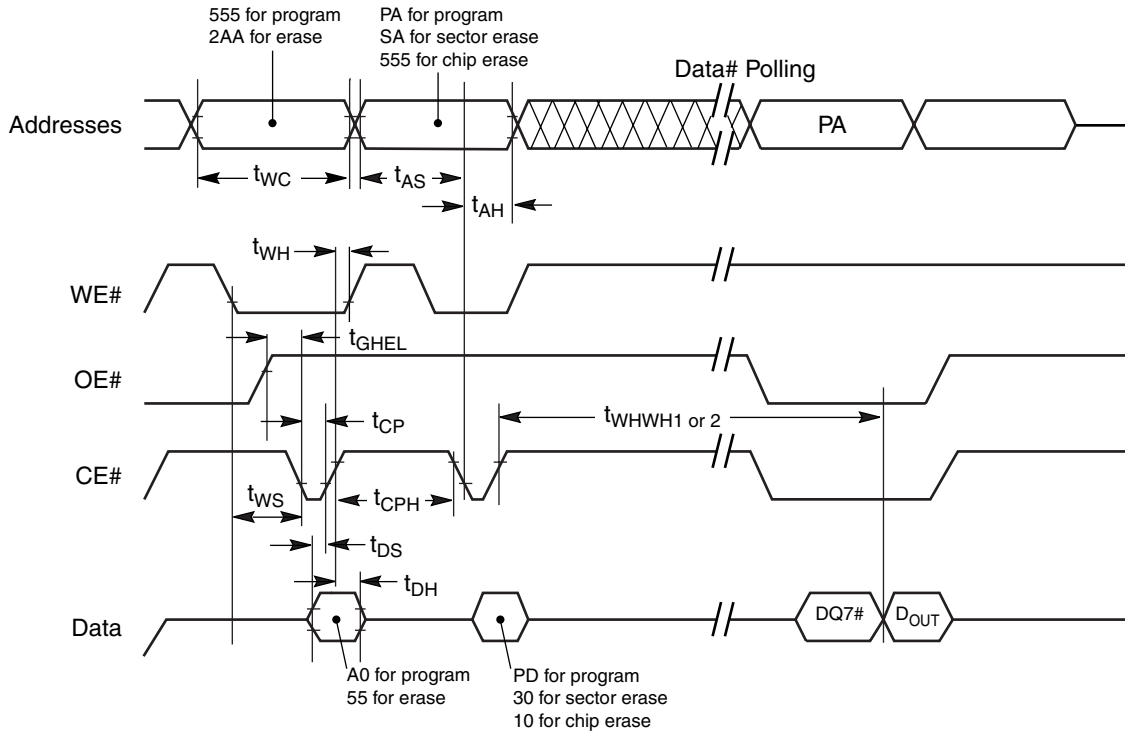
Notes:

1. *PA is the address of the memory location to be programmed.*

2. *PD is the data to be programmed at address PA.*

3. *DQ7 is the complement of the data written to the device.*

4. *D_{OUT} is the data written to the device.*

5. *Figure indicates the last two bus cycles of the command sequence.*

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 3)	Unit	Comments
Sector Erase Time	0.7	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time (Note 2)	6		s	
Byte Programming Time	9	300	µs	Excludes system level overhead (Note 5)
Chip Programming Time (Note 2)	1.1	3.3	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*

2. *Under worst case conditions of 90°C, $V_{CC} = 2.7$ V, 1,000,000 cycles.*

3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*

4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*

5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 4 for further information on command definitions.*

6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9 and OE#)	−1.0 V	13.0 V
Input voltage with respect to V_{SS} on all I/O pins	−1.0 V	V_{CC} + 1.0 V
V_{CC} Current	−100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP PIN PACKAGE CAPACITANCE

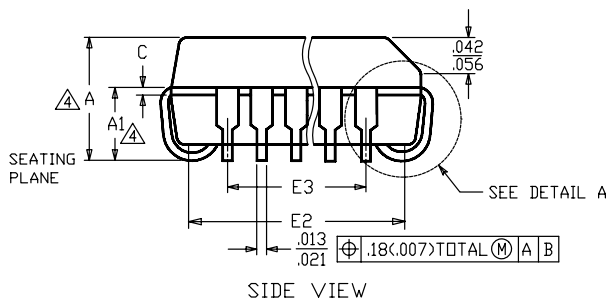| Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	12	pF
C_{IN2}	Control Pin Capacitance	V_{PP} = 0	8	12	pF

Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

PL 032—32-Pin Plastic Leaded Chip Carrier

TOP VIEW

DETAIL A

SEE NOTE 6

SEE NOTE 7

.013
.018

.015 MIN

SEATING PLANE

45°

10°

10°

.025
.045 R

.026
.032

.066
.072

.023
.029

.026
.032

.050 REF

PIN 1 ID

BOTTOM VIEW

LEAD POCKET

.042
.048

.005 REF MIN

.0085 TYP

-A-

-B-

FRONT VIEW

SIDE VIEW

SEATING PLANE

C

A

A1

D3

D2

.013
.021

.042
.056

SEE DETAIL A

.18(.007)TOTAL Ⓜ A B

SEATING PLANE

C

A

A1

E3

E2

.013
.021

.042
.056

SEE DETAIL A

.18(.007)TOTAL Ⓜ A B
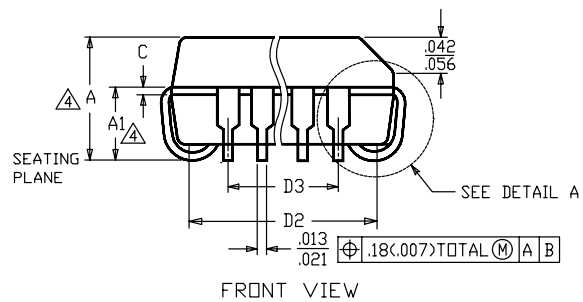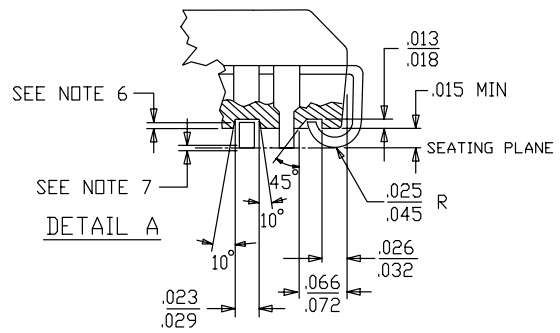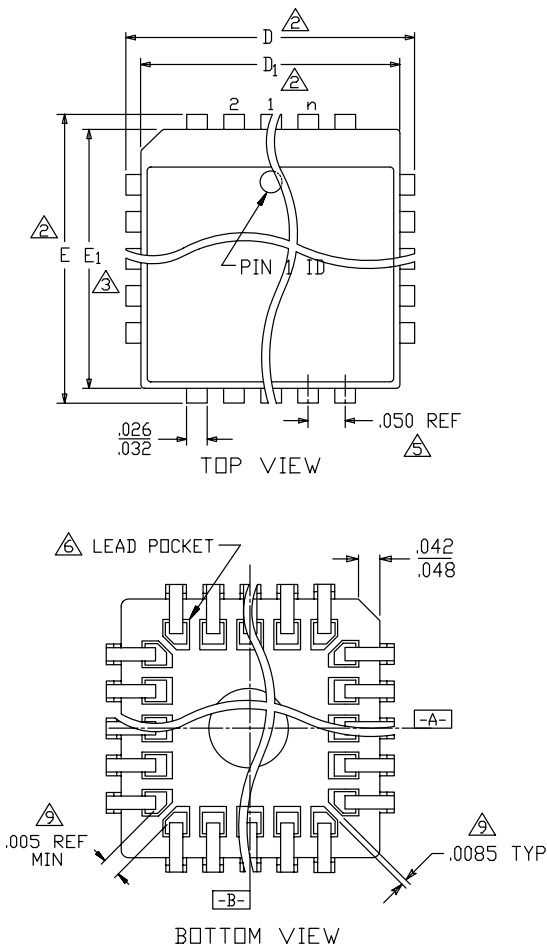
| PACKAGE	PL32	
JEDEC	MO-052(A)AE	
SYMBOL	MIN	MAX
A	.125	.140
A1	.080	.095
D	.485	.495
D1	.447	.453
D2	.390	.430
D3	.300	REF
E	.585	.595
E1	.547	.553
E2	.490	.530
E3	.400	REF
C	.009	.015

Dwg rev AH; 10/99

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.

2. DIMENSIONS "D" AND "E" ARE MEASURED FROM OUTERMOST POINT.

3. DIMENSIONS D1 AND E1 DO NOT INCLUDE CORNER MOLD FLASH. ALLOWABLE CORNER MOLD FLASH IS .010"

4. DIMENSIONS "A", "A1", "D2" AND "E2" ARE MEASURED AT THE POINTS OF CONTACT TO BASE PLANE

5. LEAD SPACING AS MEASURED FROM CENTERLINE TO CENTERLINE SHALL BE WITHIN ±.005".

6. J-LEAD TIPS SHOULD BE LOCATED INSIDE THE "POCKET.

7. LEAD COPLANARITY SHALL BE WITHIN .004" AS MEASURED FROM SEATING PLANE. COPLANARITY IS MEASURED PER AMD 06-500.

8. LEAD TWEEZE SHALL BE WITHIN .0045" ON EACH SIDE AS MEASURED FROM A VERTICAL FLAT PLANE. TWEEZE IS MEASURED PER AMD 06-500.

9. LEAD POCKET MAY BE RECTANGULAR (AS SHOWN) OR OVAL. IF CORNER LEAD POCKETS ARE CONNECTED THEN 5 MILS MINIMUM CORNER LEAD SPACING IS REQUIRED.

PHYSICAL DIMENSIONS*

TS 032—32-Pin Standard Thin Small Outline Package

STANDARD PIN OUT (TOP VIEW)

SEE DETAIL B

SEE DETAIL A

DETAIL A

DETAIL B

SECTION B-B

Dwg rev AA; 10/99
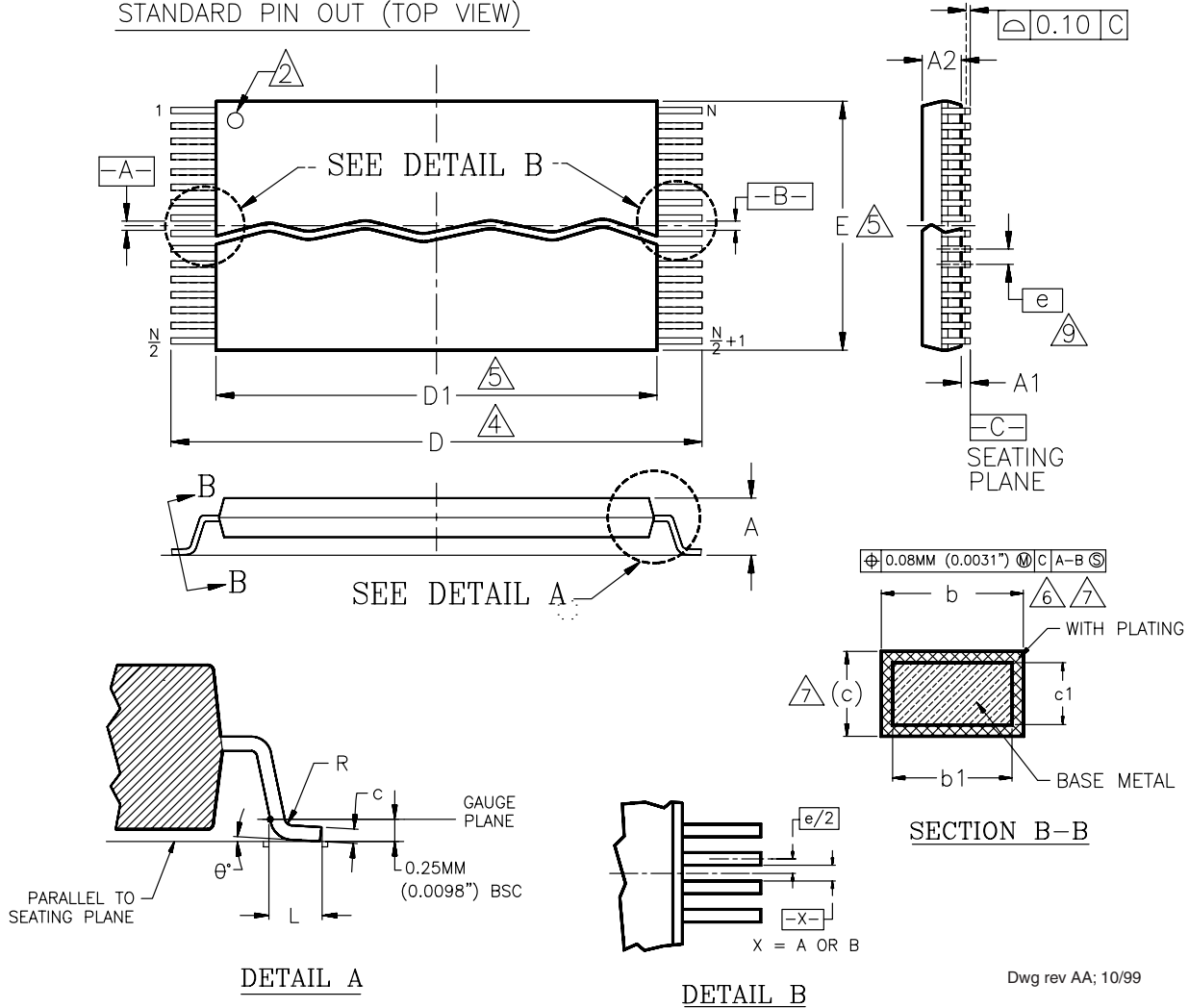
Package	TS 32		
Jedec	MO-142 (B) BD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.90	8.00	8.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	32		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm).
   (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)

2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).

3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN); INK OR LASER MARK.

4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.

5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15mm (.0059") PER SIDE.

6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").

7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.

8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.

9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

For reference only. BSC is an ANSI standard for Basic Space Centering

REVISION SUMMARY

Revision A (April 1998)

Split the Am29LV001B/Am29LV010B data sheet into separate documents. The Am29LV001B data sheet retains publication number 21557B and later; the Am29LV010B data sheet has been reassigned publication number 22140.

Valid Combinations

Changes since publication number 21557A was released: deleted the "R" designation from the 55 ns option. Corrected the part numbers.

Revision B (September 1998)

Expanded data sheet from Advanced Information to Preliminary version.

Distinctive Characteristics

Changed "Manufactured on 0.35 μm process technology" to "Manufactured on 0.32 μm process technology".

Revision C (January 1999)

Data Retention

Added new table.

Revision C+1 (March 22, 1999)

Product Selector Guide

The parameter t_{CE} should be 25 ns for the -45R device and 30 ns for the -70 device.

Revision Summary

Deleted draft revision items.

Revision C+2 (October 5, 1999)

DC Characteristics

CMOS Compatible table: Deleted I_{CC4}, V_{CC} Reset Current. This device does not have the RESET# pin. Changed I_{CC5}, Automatic Sleep Mode Current, to I_{CC4}, amd corresponding reference in Automatic Sleep Mode section.

Requirements for Reading Array Data

Deleted reference to hardware reset. This device does not have the RESET# pin.

Revision D (December 2, 1999)

AC Characteristics—Figure 12. Program Operations Timing and Figure 13. Chip/Sector Erase Operations

Deleted t_{GHWL} and changed OE# waveform to start at high.

Physical Dimensions

Replaced figures with more detailed illustrations.

Revision D+1 (November 13, 2000)

Added table of contents. Deleted burn-in option from Ordering Information section.

Revision D+2 (June 11, 2004)

Ordering Information

Added Pb-free OPNs.

Revision D+3 (June 16, 2005)

Removed -45 ns Speed Option

Added Colophon and update Trademark

Revision D+4 (August 19, 2005)

Added Pb-free for PDIP or PLCC package

Revision D+5 (January 4, 2006)

Removed 32-pin Reverse Pinout TSOP option.

Revision D6 (October 11, 2006)

Global

Added notice on product availability to cover page and first page of data sheet.

Revision D7 (February 24, 2009)

Global

Added obsolescence information.

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Spansion will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks