REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 – 06. Add U packages. Changes to Table I and Figures 1, 3, and 4. Editorial changes throughout.	93-02-19	M. A. Frye
B	Changes in accordance with NOR 5962-R239-93	93-10-01	M. A. Frye
C	Boilerplate update, part of 5 year review. ksr	07-02-15	Joseph Rodenbeck

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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REV																			
SHEET																			

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
91-03-29

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 32K X 8-BIT UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89817**

SHEET 1 OF 12

DSCC FORM 2233
APR 97

5962-E206-07

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89817	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		32K x 8 UVEPROM	55 ns
02		32K x 8 UVEPROM	45 ns
03		32K x 8 UVEPROM	35 ns
04		32K x 8 UVEPROM	55 ns
05		32K x 8 UVEPROM	45 ns
06		32K x 8 UVEPROM	35 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP4-T28 or CDIP3-T28	28	Dual-in-line 2/
Y	GDFP2-F28	28	Flat pack 2/
Z	CQCC1-N32	32	Rectangular leadless chip carrier 2/
U	GDIP1-T28 or CDIP2-T28	28	Dual-in-line 2/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
DC program voltage	13.0 V dc
Maximum power dissipation (P_D)	1 .0 W 3/
Lead temperature (soldering, 10 seconds maximum)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Endurance	10 cycles/byte minimum
Data Retention	10 years/minimum

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Ground voltage (GND)	0.0 V DC
Input high voltage (V_{IH})	2.0 V dc minimum
Input Low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.
3/ Must withstand the added P_D due to short circuit test; (e.g., I_{OS}).

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 6.0 mA, $V_{IN} = V_{IH}, V_{IL}$				0.4	
Input high voltage 1/	V_{IH}				2.0		
Input low voltage 1/	V_{IL}					0.8	
Input leakage current	I_{LI}	$GND \le V_{IN} \le V_{CC}$			-10	+10	µA
Output leakage current	I_{OZ}	$GND \le V_{OUT} \le V_{CC}$ V_{CC} = 5.5 V			-40	+40	
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.0 V			-20	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V, $f = f_{MAX}$ 4/ 5/				130	
Standby supply current	I_{SB}	V_{CC} = 5.5 V, $\overline{CS}_1 \ge V_{IH}$, I_{OUT} = 0 mA, V_{IN} = 2.0 V				40	
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.3.1c)	4			10	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.3.1c)	4			10	
Functional testing		See 4.3.1e	7,8				
Address to output valid	t_{AA}	See figures 3 and 4 and note 6/	9,10,11	01,04		55	ns
				02,05		45	
				03,06		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Chip select inactive to high Z ($\overline{CS}_1$ and CS_2 only) 3/ 7/	t_{HZCS}	See figures 3 and 4 and note 6/	9,10,11	01,02		30	ns
				03		25	
Output enable inactive to high Z 3/ 7/	t_{HZOE}			04		30	
				05,06		25	
Chip select active to output valid ($\overline{CS}_1$ and CS_2 only)	t_{ACS}			01,02		30	
				03		25	
Output enable active to output valid	t_{OE}			04		30	
				05,06		25	
Chip enable inactive to high Z ($\overline{CE}$ only) 3/ 7/	t_{HZCE}			01,04		60	
				02,05		50	
				03,06		40	
Chip enable active to output valid ($\overline{CE}$ only)	t_{ACE}			01,04		60	
				02,05		50	
				03,06		40	
Chip enable active to power up 3/	t_{PU}			ALL	0		
Chip enable inactive to power down 3/	t_{PD}			01,04		60	
				02,05		50	
				03,06		40	
Output hold from address change 3/	t_{OH}			ALL	0		

1/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed thirty seconds.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ At $f = f_{MAX}$, the inputs are switching at $1/t_{AA}$.
5/ Devices 01-03 $\overline{CE}$ = 0.0 V, $\overline{CS}_1$ = 3.0 V, CS_2 = 0.0 V; devices 04-06 $\overline{CE}$ = 0.0 V, $\overline{OE}$ = 3.0 V.
6/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 3, circuit A.
7/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input with the output load on figure 3, circuit B.

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Device Types	01 - 03		04 - 06	
Case Outlines	X, Y	Z	U	Z
Terminal Number	Terminal Symbol		Terminal Symbol	
1	A_9	NC	V_{PP}	NC
2	A_8	A_9	A_{12}	V_{PP}
3	A_7	A_8	A_7	A_{12}
4	A_6	A_7	A_6	A_7
5	A_5	A_6	A_5	A_6
6	A_4	A_5	A_4	A_5
7	A_3	A_4	A_3	A_4
8	A_2	A_3	A_2	A_3
9	A_1	A_2	A_1	A_2
10	A_0	A_1	A_0	A_1
11	O_0	A_0	O_0	A_0
12	O_1	NC	O_1	NC
13	O_2	O_0	O_2	O_0
14	GND	O_1	GND	O_1
15	O_3	O_2	O_3	O_2
16	O_4	GND	O_4	GND
17	O_5	NC	O_5	NC
18	O_6	O_3	O_6	O_3
19	O_7	O_4	O_7	O_4
20	$\overline{CE}$	O_5	$\overline{CE}$	O_5
21	CS_2	O_6	A_{10}	O_6
22	$\overline{CS}_1$	O_7	$\overline{OE}$	O_7
23	A_{14}	$\overline{CE}$	A_{11}	$\overline{CE}$
24	A_{13}	CS_2	A_9	A_{10}
25	A_{12}	$\overline{CS}_1$	A_8	$\overline{OE}$
26	A_{11}	NC	A_{13}	NC
27	A_{10}	A_{14}	A_{14}	A_{11}
28	V_{CC}	A_{13}	V_{CC}	A_9
29	---	A_{12}	---	A_8
30	---	A_{11}	---	A_{13}
31	---	A_{10}	---	A_{14}
32	---	V_{CC}	---	V_{CC}

FIGURE 1. Terminal connections.

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Devices 01 - 03

State	Mode	CS_2	$\overline{CS}_1$	$\overline{CE}$	A_{14} - A_0	Power	Outputs
Programmed	Read	V_{IH}	V_{IL}	V_{IL}	X	I_{CC}	Data out
	Standby	X	X	V_{IH}	X	I_{SB}	High Z
	Output disable	X	V_{IH}	X	X	I_{CC}	High Z
	Output disable	V_{IL}	X	X	X	I_{CC}	High Z
Unprogrammed	Blank check ones	V_{IHP}	V_{PP}	V_{ILP}	X	I_{CC}	Zeros
	Blank check zeros	V_{ILP}	V_{PP}	V_{ILP}	X	I_{CC}	Ones

Devices 04 - 06

State	Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	A_{14} - A_0	Power	Outputs
Programmed	Read	V_{IL}	V_{IL}	X	X	I_{CC}	Data out
	Standby	V_{IH}	X	X	X	I_{SB}	High Z
	Output disable	X	V_{IH}	X	X	I_{CC}	High Z
Unprogrammed	Blank check ones	V_{IHP}	V_{ILP}	V_{PP}	X	I_{CC}	Zeros
	Blank check zeros	V_{ILP}	V_{ILP}	V_{PP}	X	I_{CC}	Ones

NOTES:
1. X = Don't care
2. High Z = High-impedance state

FIGURE 2. Truth table.

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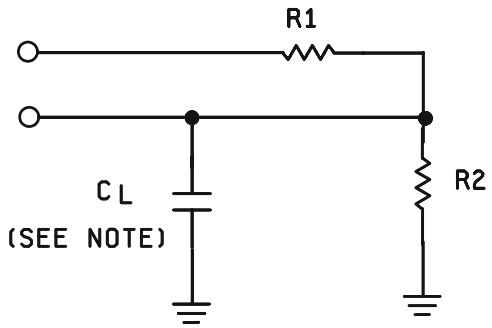
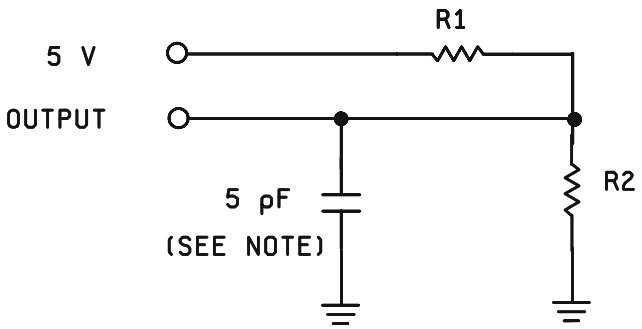


Circuit A
Output load



Circuit B
Output load for t_{HZCS}, t_{HZOE}, and t_{HZCE}

NOTE: Including scope and jig (minimum values).

Load	Circuit A	Circuit B
R1	658	658
R2	403	403
C_L	30	5

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuits and test conditions.

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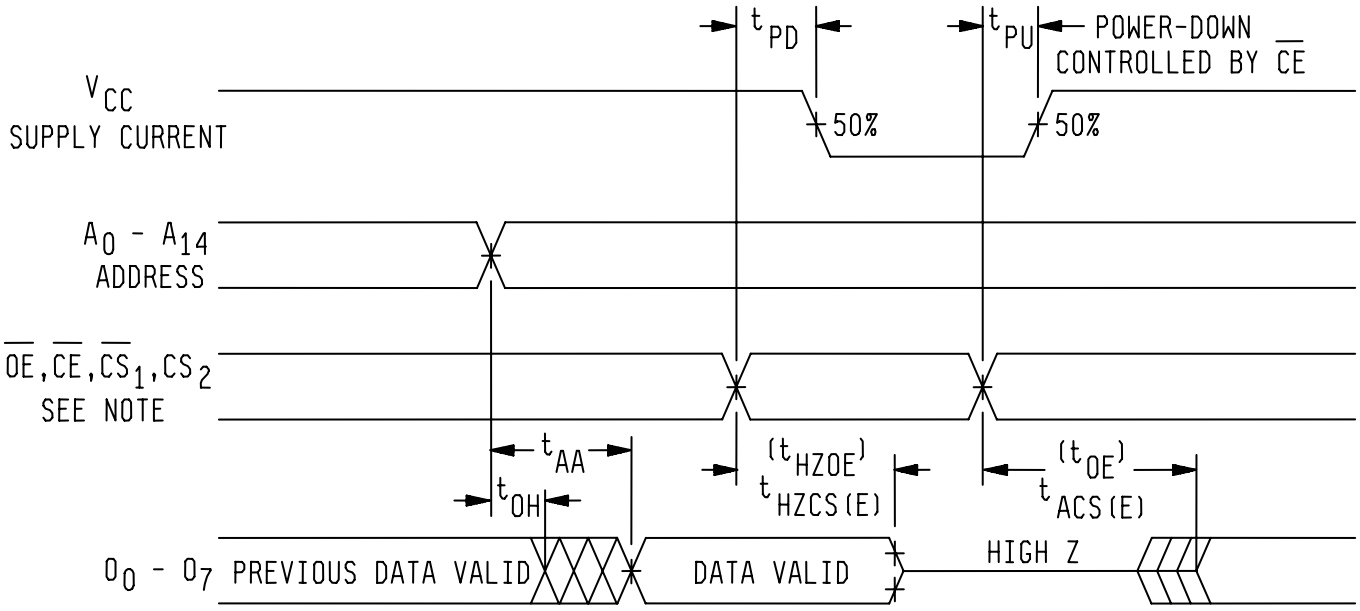

NOTES:

1. $\overline{CS_1}$ and CS_2 are valid for device types 01-03 only. $\overline{OE}$ is valid for device types 04-06 only.
2. t_{HZOE} and t_{OE} are valid for device types 04-06 only.

FIGURE 4. Switching waveforms.

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3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPROMs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure of programmability of EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all cells are in the proper state. Any cell that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed 200°C for packaged devices or 300°C for unassembled devices.)

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Margin test method.

(1) Program a minimum of 50 percent of the total number of bits (see 3.10.2).
(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours a +200°C or for 2 hours at +300°C for unassembled devices only.
(3) Test at +25°C (minimum) (see 3.10.3), including a margin test using verify mode at V_M = +4.5 V and loose timing (i.e., t_{AA} = 1 μs).
(4) Erase (see 3.10.1).
(5) Program at +25°C with a 50 percent pattern (checkerboard or equivalent).
(6) Perform dynamic burn-in (see 4.2a).
(7) Perform electrical tests at T_C = +25°C, including a margin test using read mode at V_M = +5.7 V and loose timing (i.e., t_{AA} = 1 μs).
(8) Perform electrical tests at T_C = -55°C, including a margin test using read mode at V_M = +5.7 V and loose timing (i.e., t_{AA} = 1 μs).
(9) Perform electrical tests at T_C = +125°C, including a margin test using read mode at V_M = +5.7 V and loose timing (i.e., t_{AA} = 1 μs).
(10) Erase (see 3.10.1). Devices may be submitted for groups A, B, C, and D testing prior to erasure provided the devices have been 100 percent seal tested in accordance with method 5004 of MIL-STD-883.
(11) Verify erasure (see 3.10.3).

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent.

e. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose time (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of devices to high intensity UV light for long periods may cause permanent damage.

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4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1,2,3,4**,7,8A,8B, 9, 10,11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ ** see 4.3.1c.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-02-15

Approved sources of supply for SMD 5962-89817 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8981701XA	3/ 0C7V7	CY7C271-55WMB QP7C271-55WMB
5962-8981701YA	3/ 0C7V7	CY7C271-55TMB QP7C271-55TMB
5962-8981701ZA	3/ 0C7V7	CY7C271-55QMB QP7C271-55QMB
5962-8981702XA	65786 0C7V7	CY7C271-45WMB QP7C271-45WMB
5962-8981702YA	3/ 0C7V7	CY7C271-45TMB QP7C271-45TMB
5962-8981702ZA	3/ 0C7V7	CY7C271-45QMB QP7C271-45QMB
5962-8981703XA	3/ 0C7V7	CY7C271-35WMB QP7C271-35WMB
5962-8981703YA	3/ 0C7V7	CY7C271-35TMB QP7C271-35TMB
5962-8981703ZA	3/ 0C7V7	CY7C271-35QMB QP7C271-35QMB
5962-8981704UA	3/	CY7C274-55WMB
5962-8981704ZA	3/	CY7C274-55QMB
5962-8981705UA	3/	CY7C274-45WMB
5962-8981705ZA	3/	CY7C274-45QMB
5962-8981706UA	3/	CY7C274-35WMB
5962-8981706ZA	65786	CY7C274-35QMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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