REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Updated boilerplate. Added device types 13-16. glg	95 – 12 – 15	Michael Frye
E	Revision in accordance with NOR 5962-R069-99. glg	99 – 08 – 04	Raymond Monnin
F	Add devices 17 – 20. This revision addresses programming interchangeability issue as a result of revision E, NOR 5962-R069-99. Figure 2, Truth table; will be modified to add a second truth table for devices 17 – 20. This change indicates devices which require V_{PP} to be tied to V_{CC}, from those devices which may be tied to either V_{IL} or V_{IH} as was previously the requirement prior to revision E. ksr	03 – 02 – 05	Raymond Monnin

REV																				
SHEET																				
REV	F	F	F	F	F															
SHEET	15	16	17	18	19															

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
James E. Jamison

CHECKED BY
Raymond Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
95 – 12 – 15

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
FOR USE BY ALL DEPARTMENTS
AND AGENCIES OF THE
DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 128K X 8-BIT UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89614**

SHEET
1 OF 19

DSCC FORM 2233
APR 97

5962-E142-03

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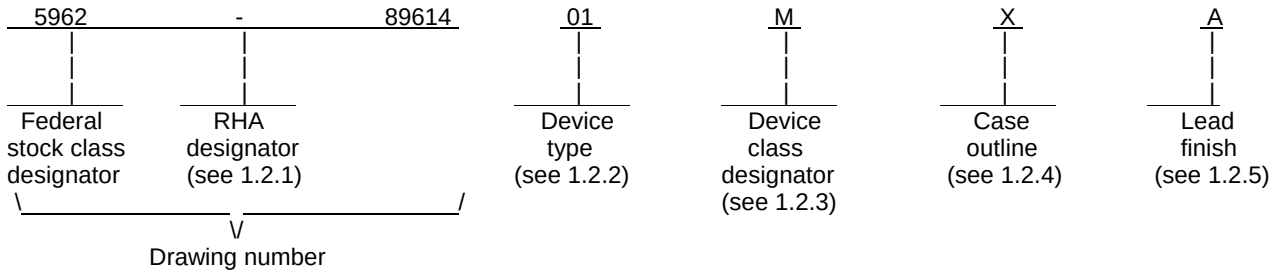
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		(128K x 8) UVEPROM	300 ns
02		(128K x 8) UVEPROM	250 ns
03,17		(128K x 8) UVEPROM	200 ns
04,18		(128K x 8) UVEPROM	170 ns
05,10,19		(128K x 8) UVEPROM	150 ns
06,11,20		(128K x 8) UVEPROM	120 ns
07,12		(128K x 8) UVEPROM	90 ns
08,13		(128K x 8) UVEPROM	70 ns
09,14		(128K x 8) UVEPROM	55 ns
15		(128K x 8) UVEPROM	45 ns
16		(128K x 8) UVEPROM	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style 2/
X	GDIP1-T32 or CDIP2-T32	32	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CQCC2-N32	32	Rectangular leadless chip carrier

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103 (see 6.6 herein)..
2/ Lid shall be transparent to permit ultraviolet light erasure.

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1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 3/

Storage temperature	-65°C to +150°C
All input or output voltage with respect to ground	-0.6 V dc to V_{CC} +0.5 V dc
Voltage on A9 with respect to ground	-0.6 V dc to +13.0 V dc
V_{PP} supply voltage with respect to ground	
during programming (device types 01-12,17-20)	-0.6 V dc to +13.5 V dc
(device types 13-16)	-0.5 V dc to +13.0 V dc
V_{CC} supply voltage with respect to ground (device types 01-12,17-20)	-0.6 V dc to +7.0 V dc
(device types 13-16)	-0.5 V dc to +7.0 V dc
Power dissipation (P_D)	330 mW 4/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X, Y and Z	See MIL-STD-1835
Junction temperature (T_J)	+150°C 5/
Endurance	50 cycles/byte, minimum
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

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2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Processing EPROM's. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.5.1 Erasure of EPROM's. When specified, devices shall be erased in accordance with the procedure and characteristics specified in 4.5 herein.

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3.5.2 Programmability of EPROM's. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6 herein.

3.5.3 Verification of erasure of programmability of EPROM's. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

3.10 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.12 Substitution. Substitution data shall be as indicated in appendix A herein.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.14 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein, over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request by the preparing or acquiring activity, along with the test data.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V\ dc \le V_{CC} \le 5.5\ V\ dc$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input load current	I_{LI}	V_{IN} = 0 V to 5.5 V	1,2,3	All	-5	+5	µA
Output leakage current	I_{LO}	V_{OUT} = 0 V to 5.5 V	1,2,3	All	-10	+10	µA
V_{PP} load current read	I_{PP1}	V_{PP} = 5.5 V	1,2,3	All		100	µA
V_{CC} active current	I_{CC1}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA V_{CC} = V_{PP} = 5.5 V f = $1/t_{AVQV}$	1,2,3	01-09, 17-20		60	mA
				10-12		30	
		same as above except f = 10 MHz		13-16		60	mA
V_{CC} standby current (TTL)	I_{CC2}	$\overline{CE}$ = V_{IH} V_{CC} = 5.5 V f = 0 Hz 1/	1,2,3	01-06, 10-12, 17-20		1	mA
		$\overline{OE}$ = ADDR = STATIC		07-09, 13-16		35	
V_{CC} super standby current (CMOS)	I_{CC3}	$\overline{CE}$ = $\overline{OE}$ = V_{CC} + 0.3 V V_{CC} = 5.5 V f = 0 Hz 1/	1,2,3	01-06, 10-12, 17-20		100	µA
				07-09		1	
		$\overline{OE}$ = ADDR = STATIC		13-16		25 2/	mA
Input low voltage	V_{IL}		1,2,3	All	-0.1 2/	0.8	V
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC} +0.5 V 2/	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA; V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	01-06, 10-12, 17-20		0.45	V
		I_{OL} = 10 mA		07-09, 13-16			
Output high voltage	V_{OH}	I_{OH} = -400 µA; V_{IL} = 0.8 V, V_{IH} = 2.0 V	1,2,3	01-06, 10-12, 17-20	2.4		V
		I_{OH} = -4 mA		07-09, 13-16			
Input capacitance 3/ 4/	C_{IN}	T_A = +25°C, f = 1 MHz, V_{IN} = 0 V, see 4.4.1e	4	All		12	pF

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance 3/ 4/	C_{OUT}	T_A = +25°C, f = 1 MHz, V_{OUT} = 0 V, see 4.4.1e	4	All		15	pF
Functional tests		See 4.4.1c	7,8A, 8B	All			
Address to output delay 5/	t_{AVQV}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} See figures 3 and 4 as applicable	9,10,11	01		300	ns
				02		250	
				03,17		200	
				04,18		170	
				05,10,19		150	
				06,11,20		120	
				07,12		90	
				08,13		70	
				09,14		55	
				15		45	
				16		35	
$\overline{CE}$ to output delay 5/	t_{ELQV}	$\overline{OE}$ = V_{IL} See figures 3 and 4 as applicable	9,10,11	01		300	ns
				02		250	
				03,17		200	
				04,18		170	
				05,10,19		150	
				06,11,20		120	
				07,12		90	
				08,13		70	
				09,14		55	
				15		45	
				16		35	
$\overline{OE}$ to output delay 5/	t_{OLQV}	$\overline{CE}$ = V_{IL} See figures 3 and 4 as applicable	9,10,11	01,02		100	ns
				03,17		75	
				04,18		65	
				05-07,10, 19,20		40	
				08,11,12		35	
				09,13,14		25	
				15,16		20	
$\overline{CE}$ or $\overline{OE}$ high to output float 2/	t_{EHQZ} t_{OHQZ}	$\overline{OE}$ or $\overline{CE}$ = V_{IL} See figures 3 and 4 as applicable	9,10,11	01-03,17		60	ns
				04,18		50	
				05-07,10 19,20		40	
				08,11,12		35	
				09,13,14		25	
				15,16		20	
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first 2/	t_{AXQX}	See figures 3 and 4 as applicable	9,10,11	All	0		ns

1/ The amount of current drawn in standby mode depends on the frequency and the number of address pins switching.
2/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table IA.
3/ All pins not being tested shall be grounded.
4/ Input rise and fall times $\le$ 20 ns for devices 01 through 06, 10 through 12 and 17 through 20. Input rise and fall times $\le$ 5 ns for devices 07 through 09 and 13 through 16.
5/ May not be tested, but shall be guaranteed to the limits specified in table IA.

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Device types	All
Case outlines	All
Terminal number	Terminal symbol
1	V_{PP}
2	A_{16}
3	A_{15}
4	A_{12}
5	A_7
6	A_6
7	A_5
8	A_4
9	A_3
10	A_2
11	A_1
12	A_0
13	I/O
14	I/O
15	I/O
16	GND
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	$\overline{CE}$
23	A_{10}
24	$\overline{OE}$
25	A_{11}
26	A_9
27	A_8
28	A_{13}
29	A_{14}
30	NC
31	$\overline{PGM}$
32	V_{CC}

FIGURE 1. Terminal connections.

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For devices 01 through 16

Mode		Pins (notes 1 and 2) $\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		V_{CC} ±0.3 V	X	X	X	X	X	High Z
Output disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto select (notes 3 and 4)	Manufacturer code (note 5)	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	
	Device code (note 6)	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	

NOTES:

1. V_H = High voltage +12.0 ±0.5 V.
2. X = Either V_{IH} or V_{IL}.
3. A_1 - A_8 = A_{10} - A_{16} = V_{IL}.
4. V_{PP} (see 4.6).
5. The output for DQ_0 - DQ_7 shall be as follows:

DQ_0 - DQ_7

DATA = 1E or 01 or 89 or 23 or 34. (SEE SOURCE BULLETIN AT END OF SMD)

6. The output for DQ_0 - DQ_7 shall be as follows:

DQ_0 - DQ_7

DATA = O5 or OE or 05 or C1 or 1D. (SEE SOURCE BULLETIN AT END OF SMD)

FIGURE 2. Truth table. (for devices 01 through 16)

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For devices 17 through 20

Mode		Pins (notes 1 and 2) $\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_0	A_9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	V_{CC}	D_{OUT}
Standby (TTL)		V_{IH}	X	X	X	X	V_{CC}	High Z
Standby (CMOS)		V_{CC} ±0.3 V	X	X	X	X	V_{CC}	High Z
Output disable		V_{IL}	V_{IH}	X	X	X	V_{CC}	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto select (notes 3 and 4)	Manufacturer code (note 5)	V_{IL}	V_{IL}	X	V_{IL}	V_H	V_{CC}	
	Device code (note 6)	V_{IL}	V_{IL}	X	V_{IH}	V_H	V_{CC}	

NOTES:

1. V_H = High voltage +12.0 ±0.5 V.
2. X = Either V_{IH} or V_{IL}.
3. A_1 - A_8 = A_{10} - A_{16} = V_{IL}.
4. V_{PP} (see 4.6).
5. The output for DQ_0 - DQ_7 shall be as follows:

   DQ_0 - DQ_7

   DATA = 97

6. The output for DQ_0 - DQ_7 shall be as follows:

   DQ_0 - DQ_7

   DATA = D6

FIGURE 2. Truth table Continued. (for devices 17 through 20)

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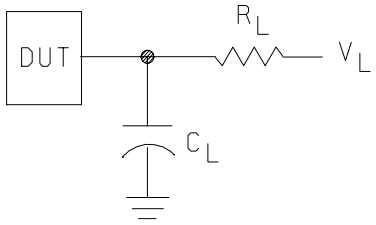
Devices 07 - 09, 13-16

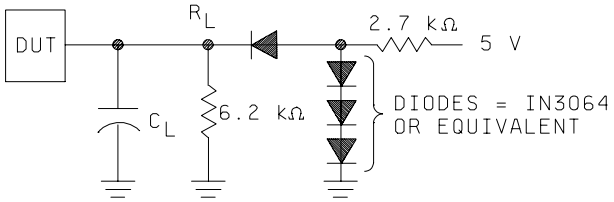


SEE NOTES 1,2,3, AND 4

CIRCUIT A

NOTES:
1. R_L = 121Ω.
2. V_L = 1.9 V.
3. C_{L1} = 30 pF. For all tests except t_{EHQZ} and t_{OHQZ}.
4. C_{L2} = 5 pF. Use for t_{EHQZ} and t_{OHQZ} tests only.

Devices 01 - 06, 10 – 12, 17 - 20



CIRCUIT B

NOTE: C_L = 100 pF including jig capacitance.

FIGURE 3. Switching time test circuit (or equivalent)

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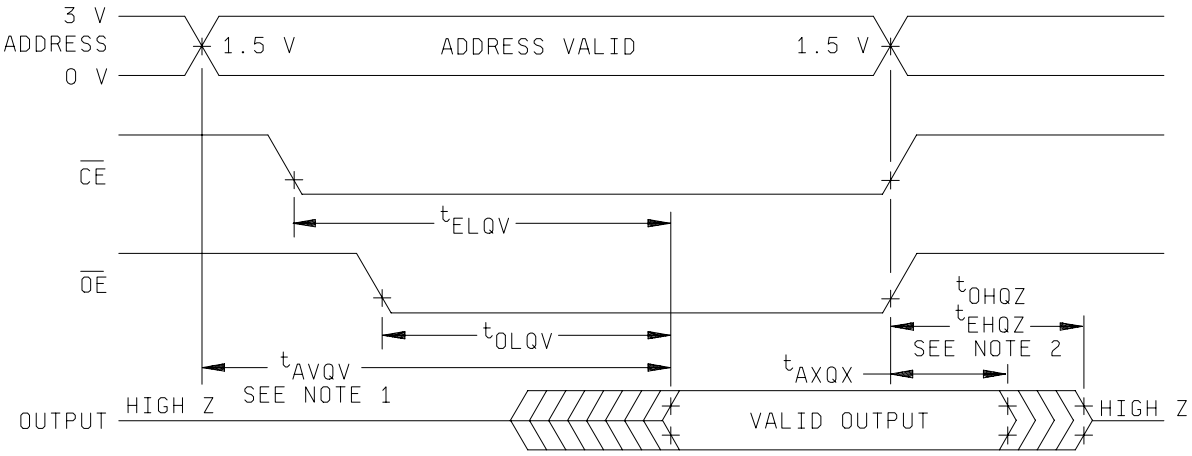
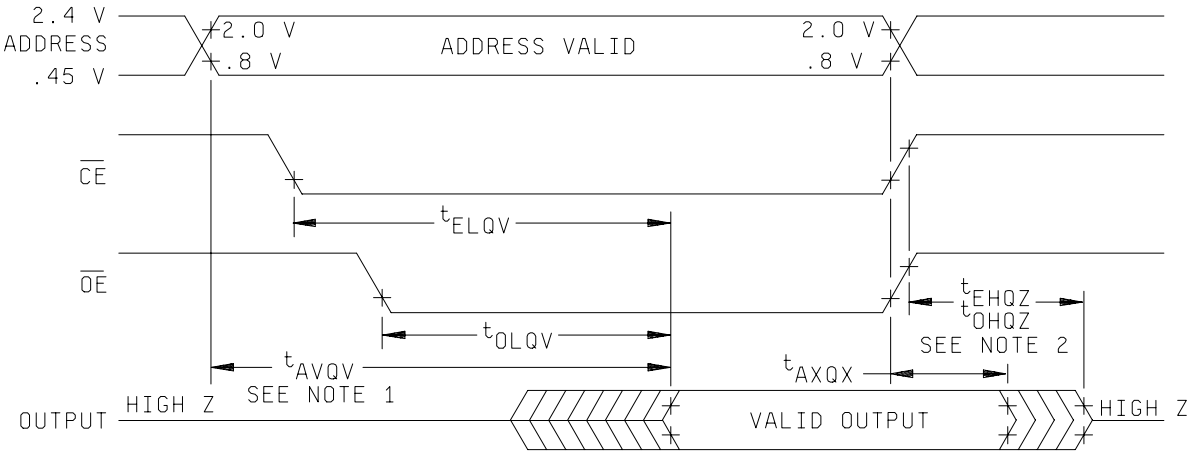
Device types 07, 08, 09, 13-16



Device types 01 - 06, 10 - 12, 17-20



NOTES:

1. $\overline{OE}$ may be delayed up to t_{AVQV} - t_{OLQV} after the falling edge of $\overline{CE}$ without impact on t_{AVQV}.
2. t_{EHQZ} or t_{OHQZ} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

FIGURE 4. Read cycle waveforms.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit referenced (see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B and as detailed in table IIB herein.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of Table IA of method 5005 of MIL-STD-883 shall be omitted.

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c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Not required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.6 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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4.5 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., ultraviolet intensity times exposure time) for erasure should be minimum of 15 ws/cm^2 for device types 01-12, 17-20, and 25 ws/cm^2 for device types 13-16. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 uW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 ws/cm^2 (1 week at 12,000 uW/cm^2). Exposure of the device to high intensity ultraviolet light for long periods may cause permanent damage.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.7 Delta measurements for device classes V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

TABLE IIB. Delta limits at +25°C.

	Device types
Test 1/	All
I_{CC3} standby	±10% of specified value in table IA
I_{LI}	±10% of specified value in table IA
I_{LO}	±10% of specified value in table IA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

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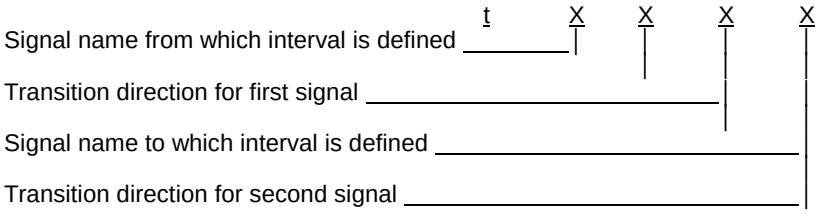
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows.

C_{IN}, C_{OUT} ----------	Input and bidirectional output, terminal-to-GND capacitance.
GND ----------	Ground zero voltage potential.
I_{CC} ----------	Supply current.
I_{LI} ----------	Input load current
T_C ----------	Case temperature.
V_{CC} ----------	Positive supply voltage.
O/V ----------	Latchup over-voltage

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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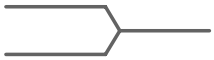
6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.7 herein) to DESC-EC and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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APPENDIX A

SUBSTITUTION DATA

10. SCOPE

10.1 Scope. This appendix contains the PIN substitution information to support the one part - one part number system. For new designs after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing designs prior to the date of this document the NEW PIN can be used in lieu of the OLD PIN. This appendix is a mandatory part of the drawing. The information contained herein is intended for compliance. The PIN substitution data shall be as follows:

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. SUBSTITUTION DATA

NEW PIN	OLD PIN
5962-8961401MXX	5962-8961401XX
5962-8961401MYX	5962-8961401YX
5962-8961402MXX	5962-8961402XX
5962-8961402MYX	5962-8961402YX
5962-8961403MXX	5962-8961403XX
5962-8961403MYX	5962-8961403YX
5962-8961404MXX	5962-8961404XX
5962-8961404MYX	5962-8961404YX
5962-8961405MXX	5962-8961405XX
5962-8961405MYX	5962-8961405YX
5962-8961406MXX	5962-8961406XX
5962-8961406MYX	5962-8961406YX

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: **03-02-05**

Approved sources of supply for SMD 5962-89614 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 3/
5962-8961401MXA	2/ 2/ 0C7V7	AT27C010-30DM/883 AM27C010-300/BXA WS27C010L-30DMB
5962-8961401MYA	2/ 2/ 0C7V7	AT27C010-30LM/883 AM27C010-300/BUA WS27C010L-30CMB
5962-8961401MYC	0C7V7	WS27C010L-30CMB
5962-8961401MZA	2/	AT27CT010-30LM/883
5962-8961402MXA	2/ 2/ 2/ 0C7V7	AT27C010-25DM/883 AM27C010-250/BXA MD27C010-25/B WS27C010L-25DMB
5962-8961402MYA	2/ 2/ 0C7V7	AT27C010-25LM/883 AM27C010-250/BUA WS27C010L-25CMB
5962-8961402MYC	0C7V7	WS27C010L-25CMB
5962-8961402MZA	2/	AT27CT010-25LM/883
5962-8961403MXA	2/ 2/ 2/ 0C7V7	AT27C010-20DM/883 AM27C010-200/BXA MD27C010-20/B WS27C010L-20DMB
5962-8961403QXA	2/	SMJ27C010A-20JM
5962-8961403MYA	2/ 2/ 0C7V7	AT27C010-20LM/883 AM27C010-200/BUA WS27C010L-20CMB
5962-8961403MYC	0C7V7	WS27C010L-20CMB
5962-8961403QYA	2/	AS27C010A-20ECAM
5962-8961403MZA	2/	AT27CT010-20LM/883

See footnotes at end of table.

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Standard microcircuit drawing PIN	Vendor CAGE number	Vendor Similar PIN
5962-8961404MXA	2/ 2/ 2/ 0C7V7	AT27C010-17DM/883 AM27C010-170/BXA MD27C010-17/B WS27C010L-17DMB
5962-8961404MYA	2/ 2/ 2/ 0C7V7	AT27C010-17LM/883 AM27C010-170/BUA SMJ27C010A-17ECAM WS27C010L-17CMB
5962-8961404QYA	2/	AS27C010A-17ECAM
5962-8961404MYC	0C7V7	WS27C010L-17CMB
5962-8961404MZA	2/	AT27CT010-17LM/883
5962-8961405MXA	2/ 0C7V7 2/ 2/	AM27C010-150/BXA WS27C010L-15DMB MD27C010-15/B AT27C010-15DM/883
5962-8961405QXA	2/	SMJ27C010A-15JM
5962-8961405MYA	2/ 0C7V7 2/	AM27C010-150/BUA WS27C010L-15CMB AT27C010-15LM/883
5962-8961405MYC	0C7V7	WS27C010L-15CMB
5962-8961405QYA	2/	AS27C010A-15ECAM
5962-8961406MXA	2/ 0C7V7	AM27C010-120/BXA WS27C010L-12DMB
5962-8961406MYC	0C7V7	WS27C010L-12CMB
5962-8961406QXA	2/	SMJ27C010A-12JM
5962-8961406MYA	2/ 0C7V7	AM27C010-120/BUA WS27C010L-12CMB
5962-8961406QYA	2/	AS27C010A-12ECAM
5962-8961407MXA	2/ 0C7V7	AM27H010-90/BXA WS57C010F-90DMB
5962-8961407MYA	2/ 0C7V7	AM27H010-90/BUA WS57C010F-90CMB
5962-8961407MYC	0C7V7	WS57C010F-90CMB
5962-8961408MXA	2/ 0C7V7	AM27H010-70/BXA WS57C010F-70DMB
5962-8961408MYA	2/ 0C7V7	AM27H010-70/BUA WS57C010F-70CMB
5962-8961408MYC	0C7V7	WS57C010F-70CMB

See footnotes at end of table.

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Standard microcircuit drawing PIN	Vendor CAGE number	Vendor Similar PIN
5962-8961409MXA	2/ 0C7V7	AM27H010-55/BXA WS57C010F-55DMB
5962-8961409MYA	2/ 0C7V7	AM27H010-55/BUA WS57C010F-55CMB
5962-8961409MYC	0C7V7	WS57C010F-55CMB
5962-8961410MXA	2/	AT27C010L-15DM/883
5962-8961410MYA	2/	AT27C010L-15LM/883
5962-8961411MXA	2/	AT27C010L-12DM/883
5962-8961411MYA	2/	AT27C010L-12LM/883
5962-8961412MXA	2/	AT27C010L-90DM/883
5962-8961412MYA	2/	AT27C010L-90LM/883
5962-8961413MXA	0C7V7	WS57C010F-70DMB
5962-8961413MYA	0C7V7	WS57C010F-70CMB
5962-8961413MYC	0C7V7	WS57C010F-70CMB
5962-8961413QXA	2/	CY27H010-70WMB
5962-8961413QYA	2/	CY27H010-70QMB
5962-8961414MXA	0C7V7	WS57C010F-55DMB
5962-8961414MYA	0C7V7	WS57C010F-55CMB
5962-8961414MYC	0C7V7	WS57C010F-55CMB
5962-8961414QXA	2/	CY27H010-55WMB
5962-8961414QYA	2/	CY27H010-55QMB
5962-8961415MXA	0C7V7	WS57C010F-45DMB
5962-8961415MYA	0C7V7	WS57C010F-45CMB
5962-8961415MYC	0C7V7	WS57C010F-45CMB
5962-8961415QXA	2/	CY27H010-45WMB
5962-8961415QYA	2/	CY27H010-45QMB
5962-8961416MXA	0C7V7	WS57C010F-35DMB
5962-8961416MYA	0C7V7	WS57C010F-35CMB
5962-8961416MYC	0C7V7	WS57C010F-35CMB
5962-8961416QXA	2/	CY27H010-35WMB
5962-8961416QYA	2/	CY27H010-35QMB
5962-8961417QXA 4/	0EU86	SMJ27C010A-20JM
5962-8961417QYA 4/	0EU86	AS27C010A-20ECAM
5962-8961418QYA 4/	0EU86	AS27C010A-17ECAM

See footnotes at end of table.

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Standard microcircuit drawing PIN	Vendor CAGE number	Vendor Similar PIN
5962-8961419QXA 4/	0EU86	SMJ27C010A-15JM
5962-8961419QYA 4/	0EU86	AS27C010A-15ECAM
5962-8961420QXA 4/	0EU86	SMJ27C010A-12JM
5962-8961420QYA 4/	0EU86	AS27C010A-12ECAM

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ No longer available from an approved source.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

4/ Devices 17-20 were previously supplied by CAGE 0EU86 as devices 03-06 respectively however due to programming issues these parts are not necessarily interchangeable.

Vendor CAGE number	Vendor name and address	Manufacturer code	Device code
0C7V7	Qualified Parts Laboratory, Inc. 3605 Kifer Road Santa Clara, CA 95051	23 23	C1 (for devices 01-06) F8 (for devices 7,8,9, & 13 –16)
0EU86	Austin Semiconductor 8701 Cross Park Drive Austin, TX 78754	97	D6

NOTE: The following information is provided for customer service when reviewing figure 2 of former revisions of this SMD. The following vendors no longer directly supply to this SMD.

Vendor CAGE number	Vendor name and address	Manufacturer code	Device code
1FN41	Atmel Corporation	1E	05
34335	Advanced Micro Devices	01	0E
34649	Intel Corporation	89	05
66579	Waferscale Integration, Inc.	23	C1
65786	Cypress Semiconductor	34	1D

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