32K x 8 Power Switched and Reprogrammable PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 25 ns (Commercial)**
- **Low power**
  - **— 275 mW (Commercial)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100%programmable**
- **Slim 300-mil package**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >4001V static discharge**

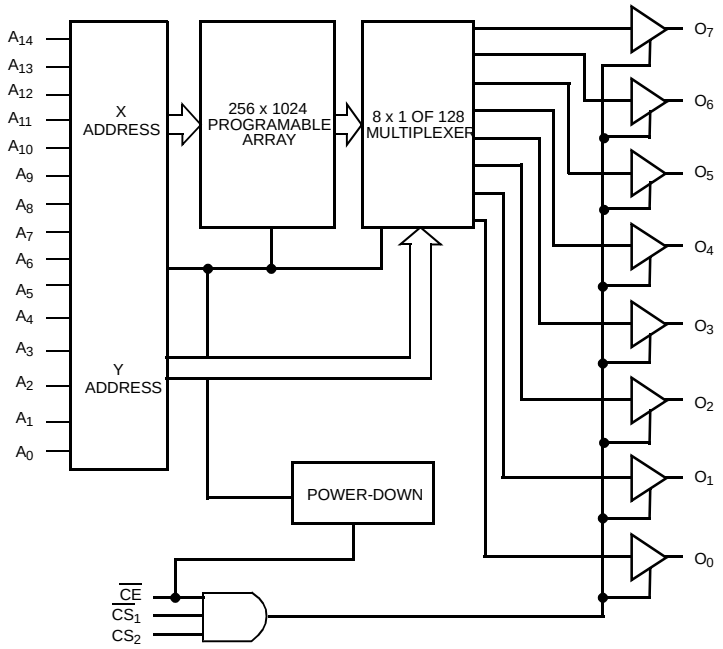
Functional Description

The CY7C271A is a high-performance 32,768-word by 8-bit CMOS PROM. When disabled ($\overline{CE}$ HIGH), the 7C271A automatically powers down into a low-power stand-by mode. The CY7C271A is packaged in the 300-mil slim package and is available in a cerDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271A offers the advantages of lower power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the super voltage, and low current requirements allow for gang programming. The EPROM cells allow each memory location to be tested 100% because each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

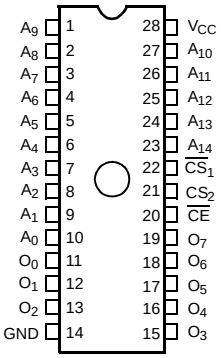
Reading the 7C271A is accomplished by placing active LOW signals on $\overline{CS_1}$ and $\overline{CE}$, and an active HIGH on CS_2. The contents of the memory location addressed by the address lines (A_0–A_{14}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

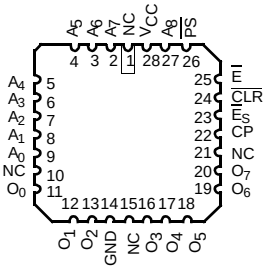


Pin Configurations

DIP/Flatpack



PLCC
Top View



Selection Guide

		7C271A-25	7C271A-30	7C271A-35	7C271A-45	Unit
Maximum Access Time		25	30	35	45	ns
Maximum Operating Current	Com'l	75	75	50	50	mA
Standby Current	Com'l	15	15	15	15	mA

Maximum Ratings[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage..... –3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage..... >4001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +700°C	5V ±10%

Electrical Characteristics Over the Operating Range[2, 3]

Parameter	Description	Test Conditions		7C271A-25 7C271A-30		7C271A-35		7C271A-45		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		–10	+10	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND		–20	–90	–20	–90	–20	–90	mA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT} = 0 mA, f = 10 MHz	Com'l		75		50		50	mA
I_{SB}	Stand-By Current	$\overline{V_{CC}}$=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA

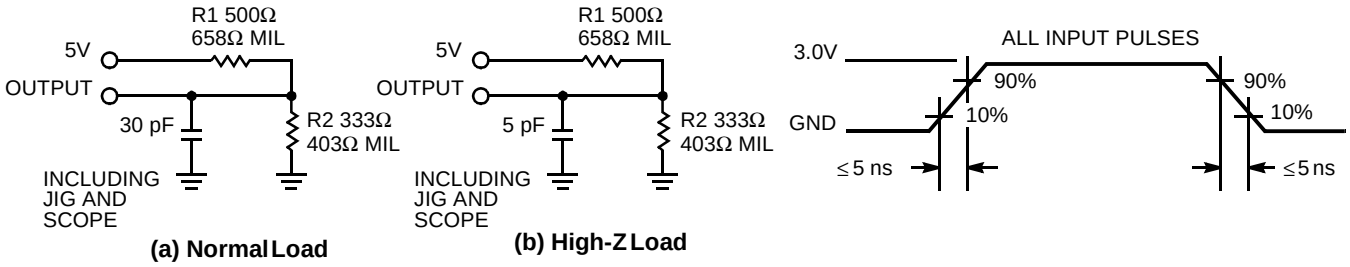
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

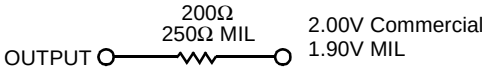
Notes:

1. The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. See the last page of this specification for Group A subgroup testing information.
3. See Introduction to CMOS PROMs in this Data Book for general information on testing.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms



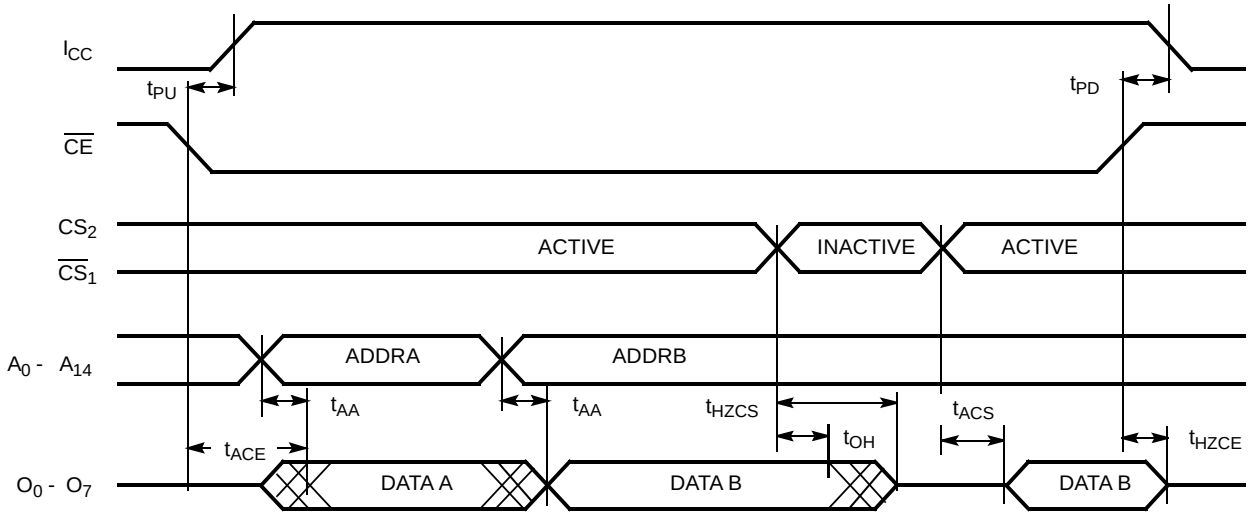
Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3]

Parameter	Description	7C271A-25		7C271A-30		7C271A-35		7C271A-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45	ns
t_{ACS}	$\overline{CS_1}/CS_2$ Active to Output Valid		12		18		18		18	ns
t_{ACE}	$\overline{CE}$ Active to Output Valid		30		35		35		45	ns
t_{HZCS}	$\overline{CS_1}/CS_2$ Inactive to High Z		12		18		18		18	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		18		18		18	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		40	ns
t_{OH}	Output Data Hold	0		0		0		0		ns

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C271A in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C271A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	–0.5	0.4	V
V_{CCP}	Programming V_{CC}	6.0	6.5	V

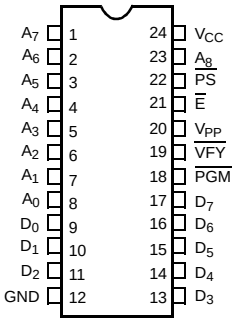
Table 2. Mode Selection

Mode	Pin Function[5]					
	$\overline{CS_1}/V_{PP}$	$CS_2/\overline{PGM}$	$\overline{CE}/\overline{VFY}$	A_0	A_9	Data
Read	V_{IL}	V_{IH}	V_{IL}	A_0	A_9	O_7–O_0
Output Disable	V_{IH}	V_{IH}	V_{IL}	A_0	A_9	High Z
Output Disable	V_{IL}	V_{IL}	V_{IL}	A_0	A_9	High Z
Stand-by	X	X	V_{IH}	A_0	A_9	High Z
Program	V_{PP}	V_{ILP}	V_{IHP}	A_0	A_9	D_7–D_0
Program Verify	V_{PP}	V_{IHP}	V_{ILP}	A_0	A_9	O_7–O_0
Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	X	X	X
Signature (MFG)	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{HV}[6]	34H
Signature (DEV)	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{HV}[6]	20H

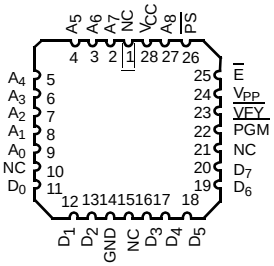
Note:
5. X can be V_{IL} or V_{IH}.
6. V_{HV}=12±0.5V

Programming Pinouts

DIP
Top View

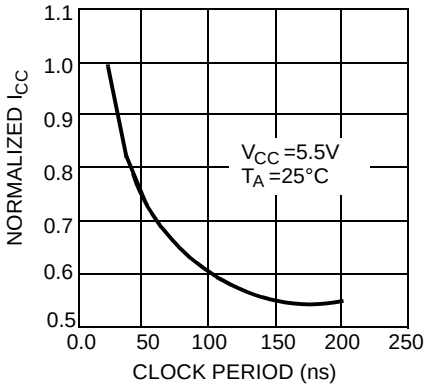


PLCC
Top View

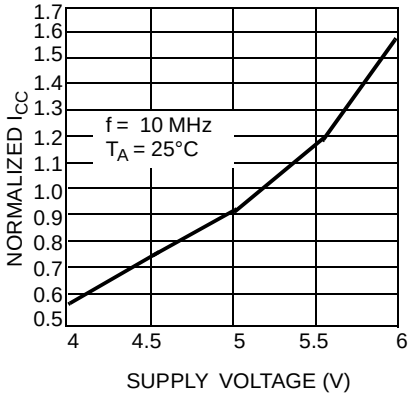


Typical DC and AC Characteristics

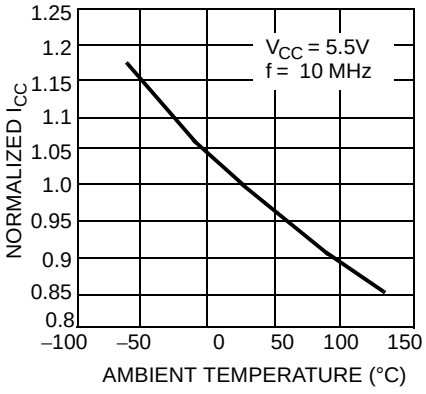
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



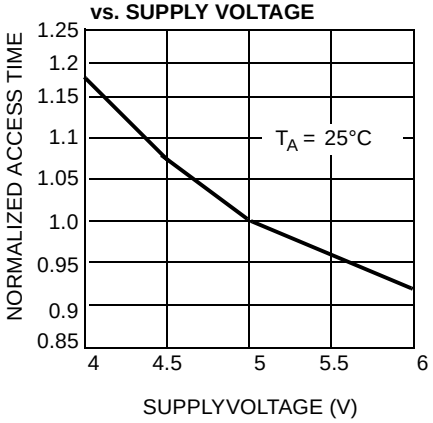
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



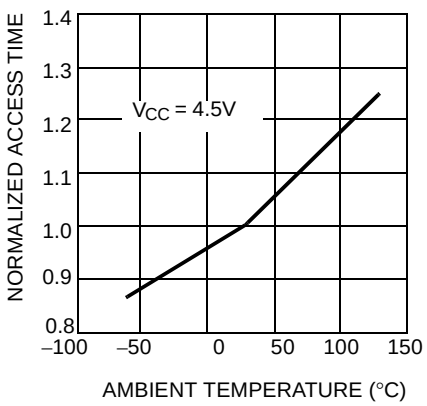
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



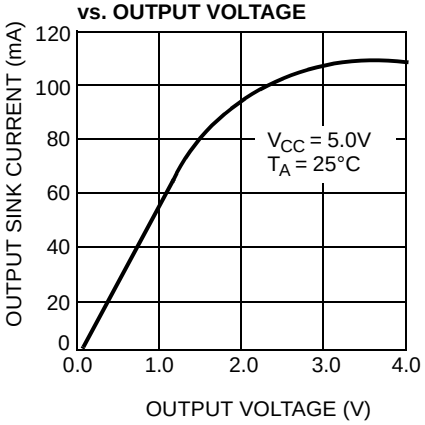
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



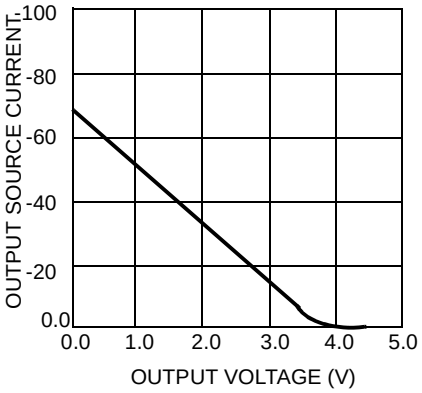
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



C271A-9

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C271A-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
30	CY7C271A-30PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
35	CY7C271A-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C271A-35WC	W22	28-Lead (300-Mil) Windowed CerDIP	
45	CY7C271A-45WC	W22	28-Lead (300-Mil) Windowed CerDIP	Commercial

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

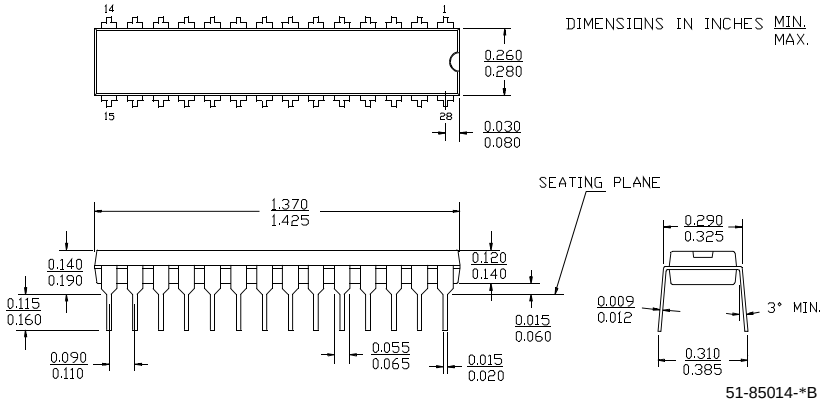
Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

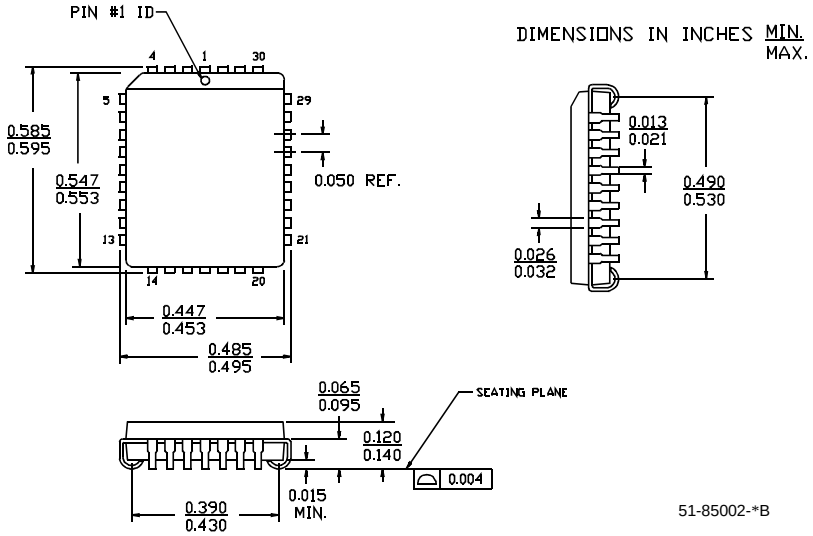
Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11

Package Diagrams

28-Lead (300-Mil) Molded DIP P21

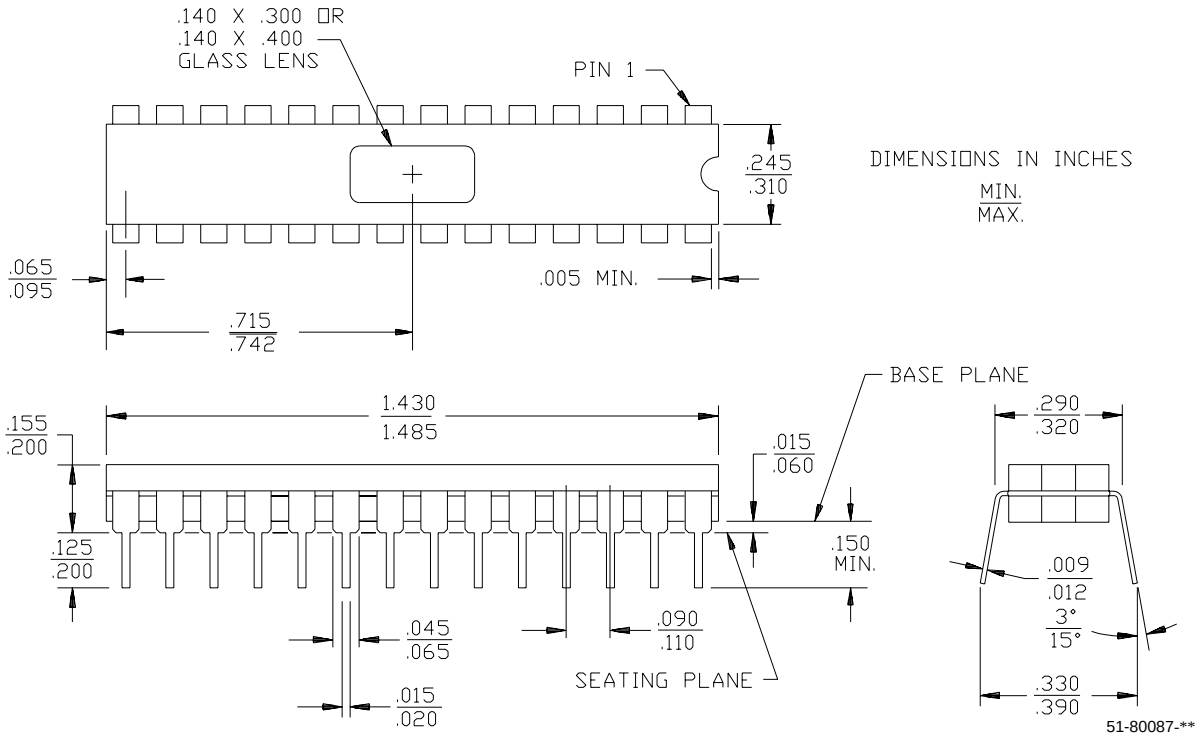


32-Lead Plastic Leaded Chip Carrier J65



Package Diagrams (continued)

28-Lead (300-Mil) Windowed CerDIP W22
MIL-STD-1835 D-15 Config. A



Document History Page

Document Title: CY7C271A 32K x 8 Power Switched and Reprogrammable PROM Document Number: 38-04013				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	114409	3/26/02	DSG	Change from Spec number: 38-00424 to 38-04013
*A	118899	9/13/02	GBI	Update Ordering Information
*B	122254	12/26/02	RBI	Add power up requirements to maximum ratings information