Mobile LPDDR (only)

152-Ball Package-on-Package (PoP) TI-OMAP™

MT46HxxxMxxLxCG

MT46HxxxMxxLxKZ

Features

- V_{DD}/V_{DDQ} = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; 2 data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths (BLs): 2, 4, 8, or 16[1]
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- STATUS REGISTER READ (SRR) supported[2]
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh

Options	Marking
• V_{DD}/V_{DDQ}	
– 1.8V/1.8V	H
• Configuration	
– 128 Meg x 32 (16 Meg x 16 x 4 banks x 4)	128M32
– 64 Meg x 32 (8 Meg x 32 x 4 banks x 2)	64M32
– 32 Meg x 32 (8 Meg x 32 x 4 banks)	32M32
– 16 Meg x 32 (4 Meg x 32 x 4 banks)	16M32
• Device version	
– Single die, standard addressing	LF
– 2-die stack, standard addressing	L2
– 4-die stack, standard addressing	L4
• Plastic “green” package	
– 152-ball VFBGA (14 x 14 x 1.0mm)	CG
– 152-ball VFBGA (14 x 14 x 1.2mm)	KZ
• Timing – cycle time	
– 5ns @ CL = 3	-5
– 5.4ns @ CL = 3	-54
– 6ns @ CL = 3	-6
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT

Notes: 1. BL 16: contact factory for availability.
2. Contact factory for remapped SRR output.

Table 1: Configuration Addressing

Architecture	128 Meg x 32[1]	64 Meg x 32	32 Meg x 32	16 Meg x 32
Configuration	16 Meg x 16 x 4 banks x 4 die	8 Meg x 32 x 4 banks x 2 die	8 Meg x 32 x 4 banks	4 Meg x 32 x 4 banks
Refresh count	8K	8K	8K	8K
Row addressing	16K (A[13:0])	8K (A[12:0])	8K (A[12:0])	8K (A[12:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])	512 (A[8:0])

Notes: 1. Quad die stack. Each CS configured with two x16 die connected in parallel to make up a 32-bit-wide bus.

Part Numbering Information – 152-Ball PoP

Micron® 152-ball packaged LPDDR devices are available in several configurations.

Figure 1: Marketing Part Number Example

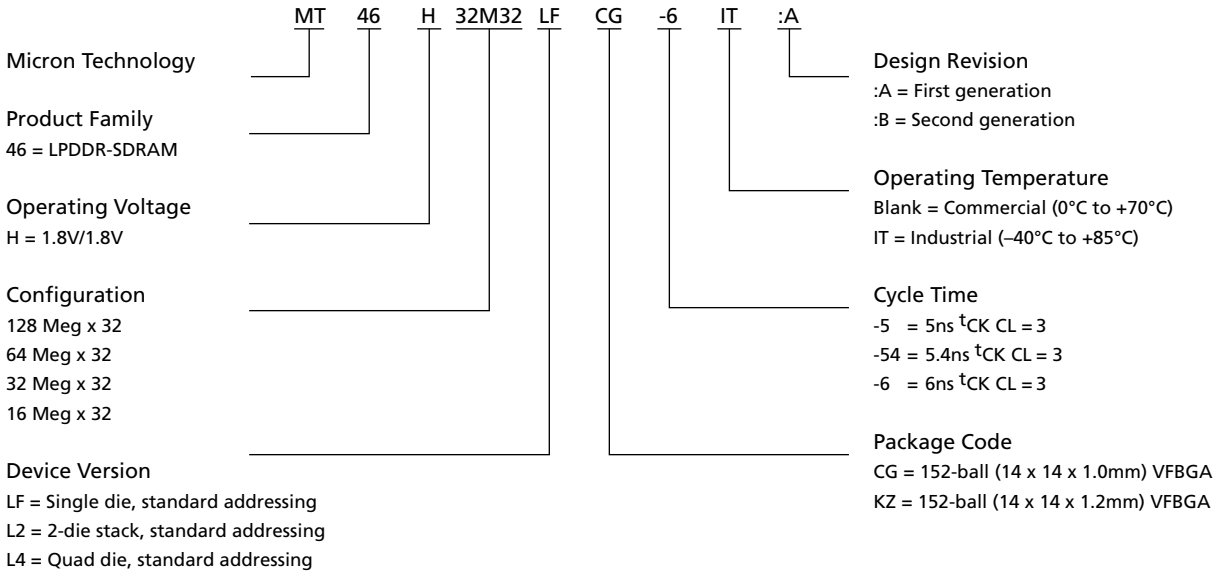


Table 2: 152-Ball Production Marketing Part Numbers

Part Numbers	LPDDR Product	Physical Part Marking
MT46H16M32LFCG-5:B	512Mb DDR, x32, 200 MHz	D9KTK
MT46H16M32LFCG-5 IT:B	512Mb DDR, x32, 200 MHz	D9KTL
MT46H16M32LFCG-54:B	512Mb DDR, x32, 185 MHz	D9KTM
MT46H16M32LFCG-54 IT:B	512Mb DDR, x32, 185 MHz	D9KTN
MT46H16M32LFCG-6:B	512Mb DDR, x32, 166 MHz	D9KGX
MT46H16M32LFCG-6 IT:B	512Mb DDR, x32, 166 MHz	D9KGZ
MT46H32M32LFCG-5:A	1Gb DDR, x32, 200 MHz	D9KTP
MT46H32M32LFCG-5 IT:A	1Gb DDR, x32, 200 MHz	D9KLD
MT46H32M32LFCG-54:A	1Gb DDR, x32, 185 MHz	D9KTQ
MT46H32M32LFCG-54 IT:A	1Gb DDR, x32, 185 MHz	D9KTR
MT46H32M32LFCG-6:A	1Gb DDR, x32, 166 MHz	D9KHL
MT46H32M32LFCG-6 IT:A	1Gb DDR, x32, 166 MHz	D9JZJ
MT46H64M32L2CG-5:A	2 x 1Gb DDR, x32, 200 MHz	D9KTS
MT46H64M32L2CG-5 IT:A	2 x 1Gb DDR, x32, 200 MHz	D9KLF
MT46H64M32L2CG-54:A	2 x 1Gb DDR, x32, 185 MHz	D9KTV
MT46H64M32L2CG-54 IT:A	2 x 1Gb DDR, x32, 185 MHz	D9KTW
MT46H64M32L2CG-6:A	2 x 1Gb DDR, x32, 166 MHz	D9KJV
MT46H64M32L2CG-6 IT:A	2 x 1Gb DDR, x32, 166 MHz	D9KFJ
MT46H128M32L4KZ-6 IT ES:A	4 × 1Gb DDR, x32, 166 MHz	Z9KZL

Device Marking

Due to the size of the package, the Micron-standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a 5-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at the FBGA Part Marking Decoder site: www.micron.com/decoder. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, “Product Mark/Label,” at www.micron.com/csn.

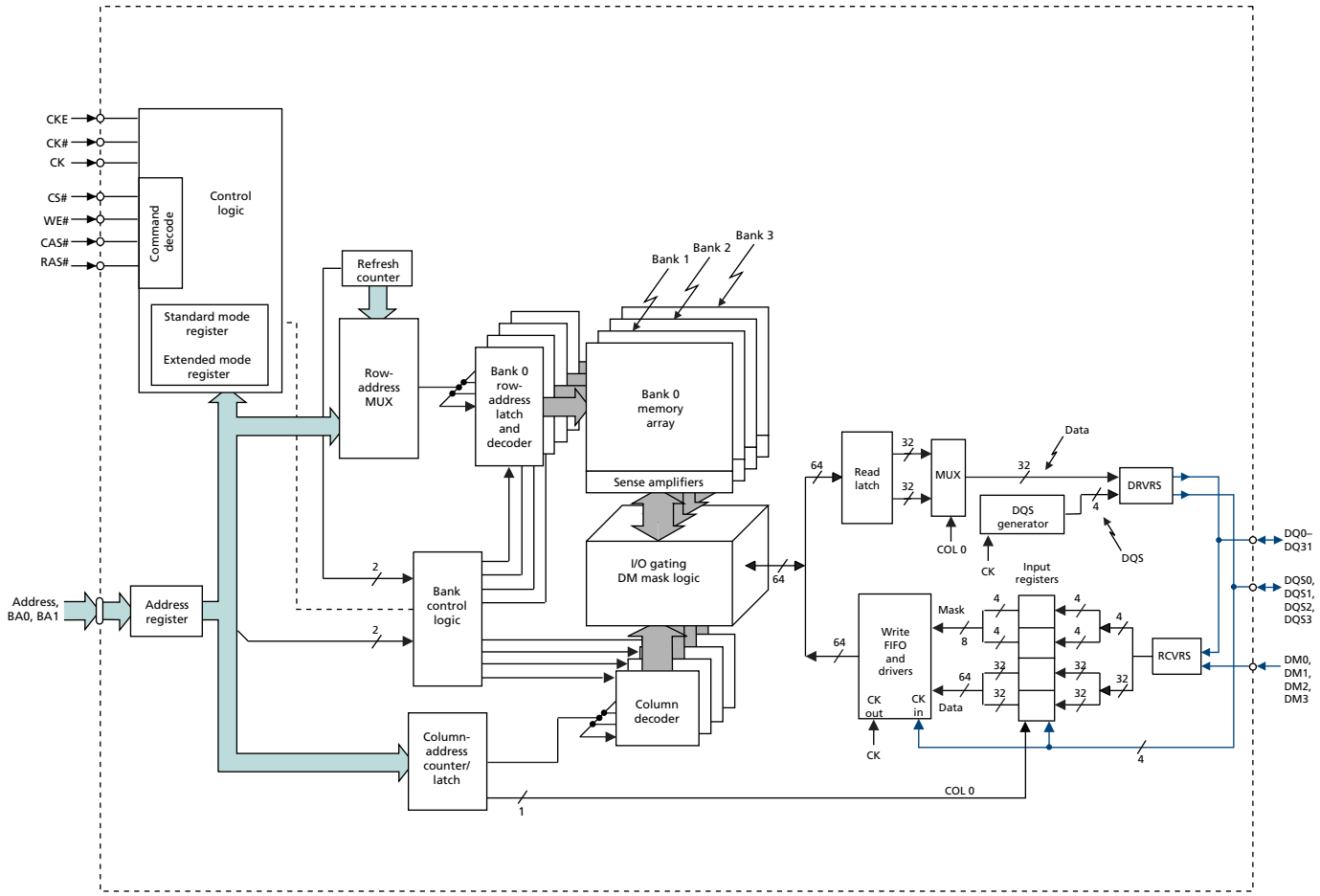
General Description

Micron 152-ball packaged Mobile Low-Power DDR SDRAM (LPDDR) devices contain either 1Gb LPDDR or 512Mb LPDDR die.

The 1Gb LPDDR die is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824 bits. It is internally configured as a quad-bank DRAM. Each of the x32's 268,435,456-bit banks is organized as 8192 rows by 1024 columns by 32 bits.

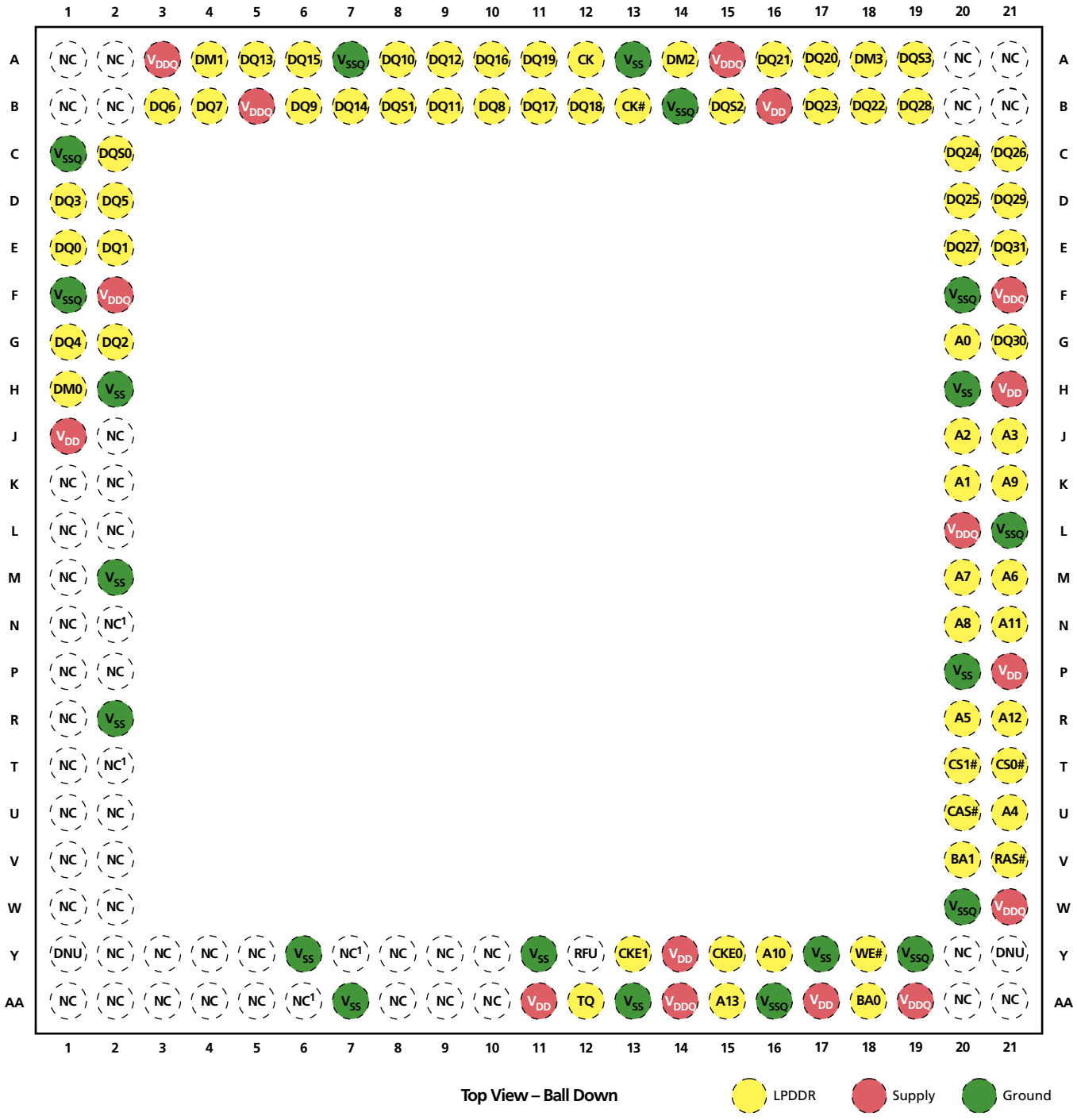
The 512Mb LPDDR die is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits.

Figure 2: Functional Block Diagram



Ball Assignments and Descriptions

Figure 3: 152-Ball VFBGA Ball Assignments



Notes: 1. Although not bonded to the die, these pins may be connected on the package substrate.

Table 3: Ball Assignments

Symbol	Type	Description
A[13:0]	Input	Address inputs: Specify the row or column address. Also used to load the mode registers. The maximum address is determined by density and configuration. Consult the LPDDR product data sheet for the maximum address for a given density and configuration. Unused address pins become RFU.[1]
BA0, BA1	Input	Bank address inputs: Specify one of the 4 banks.
CAS#	Input	Column select: Specifies the command to execute.
CK, CK#		CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
CKE0, CKE1	Input	Clock enable. CKE0 is used for a single LPDDR product. CKE1 is used for dual LPDDR products, and is considered RFU for single products.
CS0#, CS1#	Input	Chip select: CS0# is used for a single LPDDR product. CS1# is used for dual LPDDR products, and is considered RFU for single products.
DM[3:0]	Input	Data mask: Determines which bytes are written during WRITE operations.
RAS#	Input	Row select: Specifies the command to execute.
WE#	Input	Write enable: Specifies the command to execute.
DQ[31:0]	Input/ output	Data bus: Data inputs/outputs.
DQS[3:0]	Input/ output	Data strobe: Coordinates read/write transfers of data; one DQS per DQ byte.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR T_J exceeds 85°C.
V_{DD}	Supply	V_{DD}: LPDDR power supply.
V_{DDQ}	Supply	V_{DDQ}: LPDDR I/O power supply.
V_{SSQ}	Supply	V_{SSQ}: LPDDR I/O ground.
RFU[1]	–	Reserved for future use.

Notes: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

Table 4: Non-Device-Specific Ball Assignments

Symbol	Type	Description
V_{SS}	Supply	V_{SS}: Shared ground.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.

Electrical Specifications

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Absolute Maximum Ratings

Note 1 applies to all parameters in this table.

Parameters/Conditions	Symbol	Min	Max	Unit
V_{DD}, V_{DDQ} supply voltage relative to V_{SS}	V_{DD}, V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature range		–55	+150	°C

Notes: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Table 6: Recommended Operating Conditions

Parameters		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{DD}	1.70	1.80	1.95	V
I/O supply voltage		V_{DDQ}	1.70	1.80	1.95	V
Operating temperature range	Commercial		0	–	+70	°C
	Industrial		-40	–	+85	°C

Device Diagrams

Figure 4: 152-Ball VFBGA Functional Block Diagram (non-Quad Die)

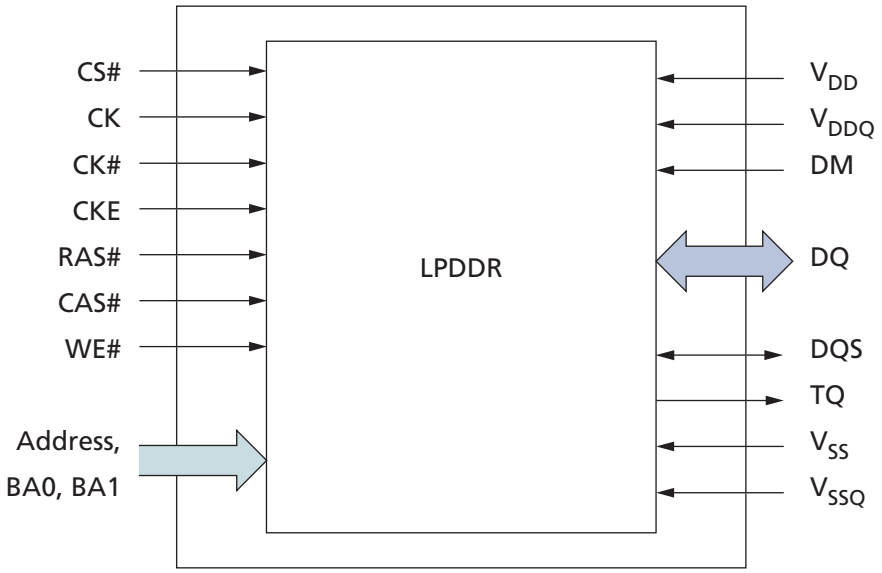
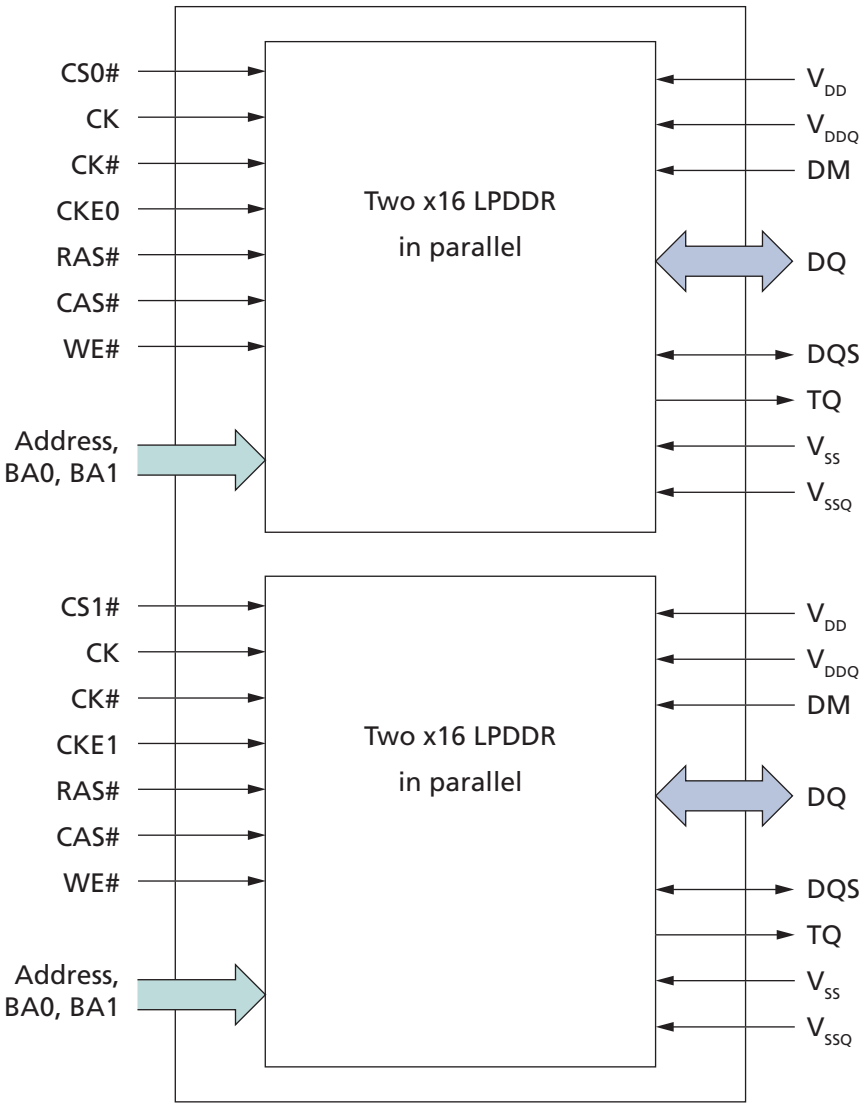
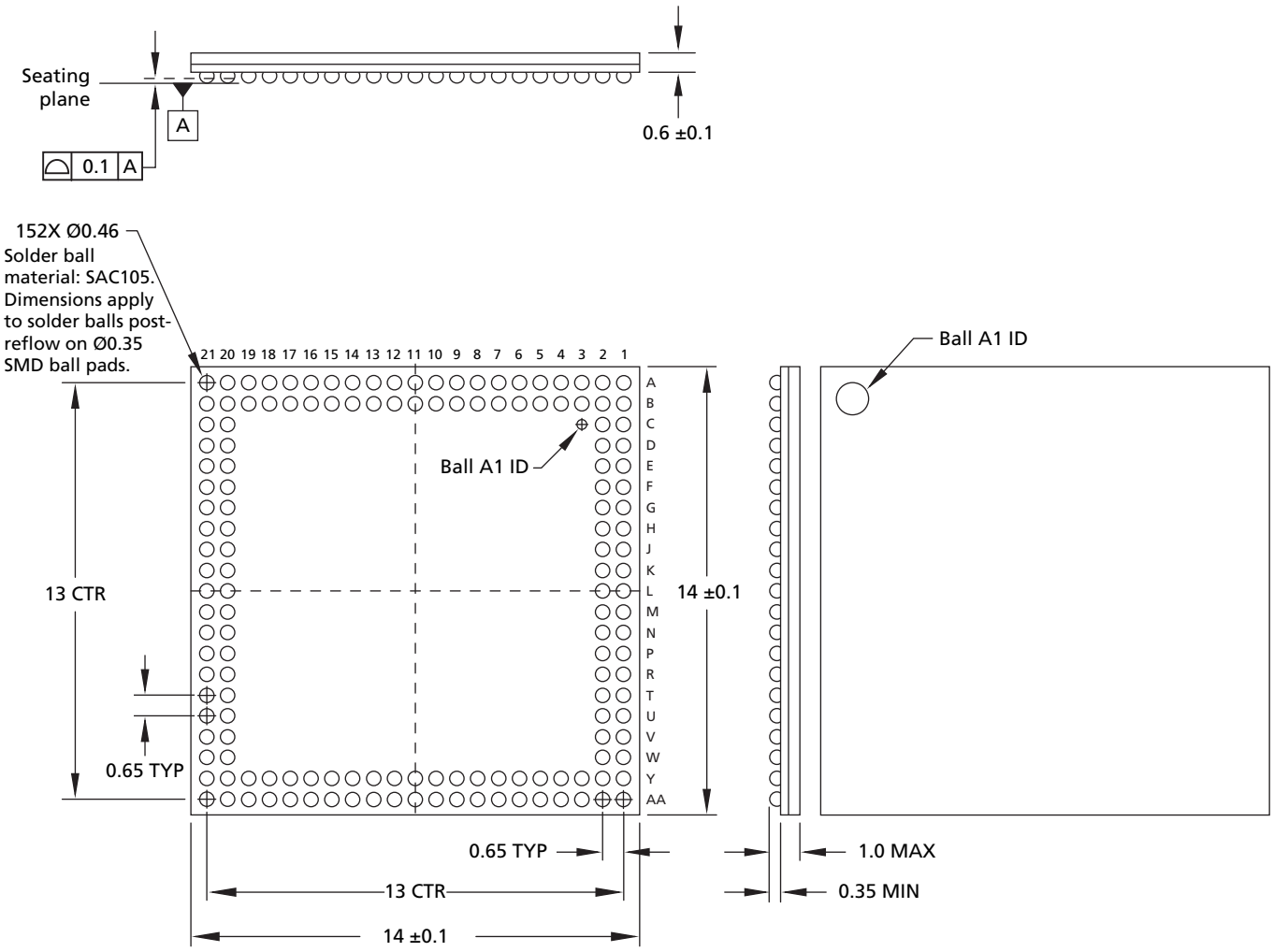


Figure 5: 152-Ball VFBGA Functional Block Diagram, Quad Die



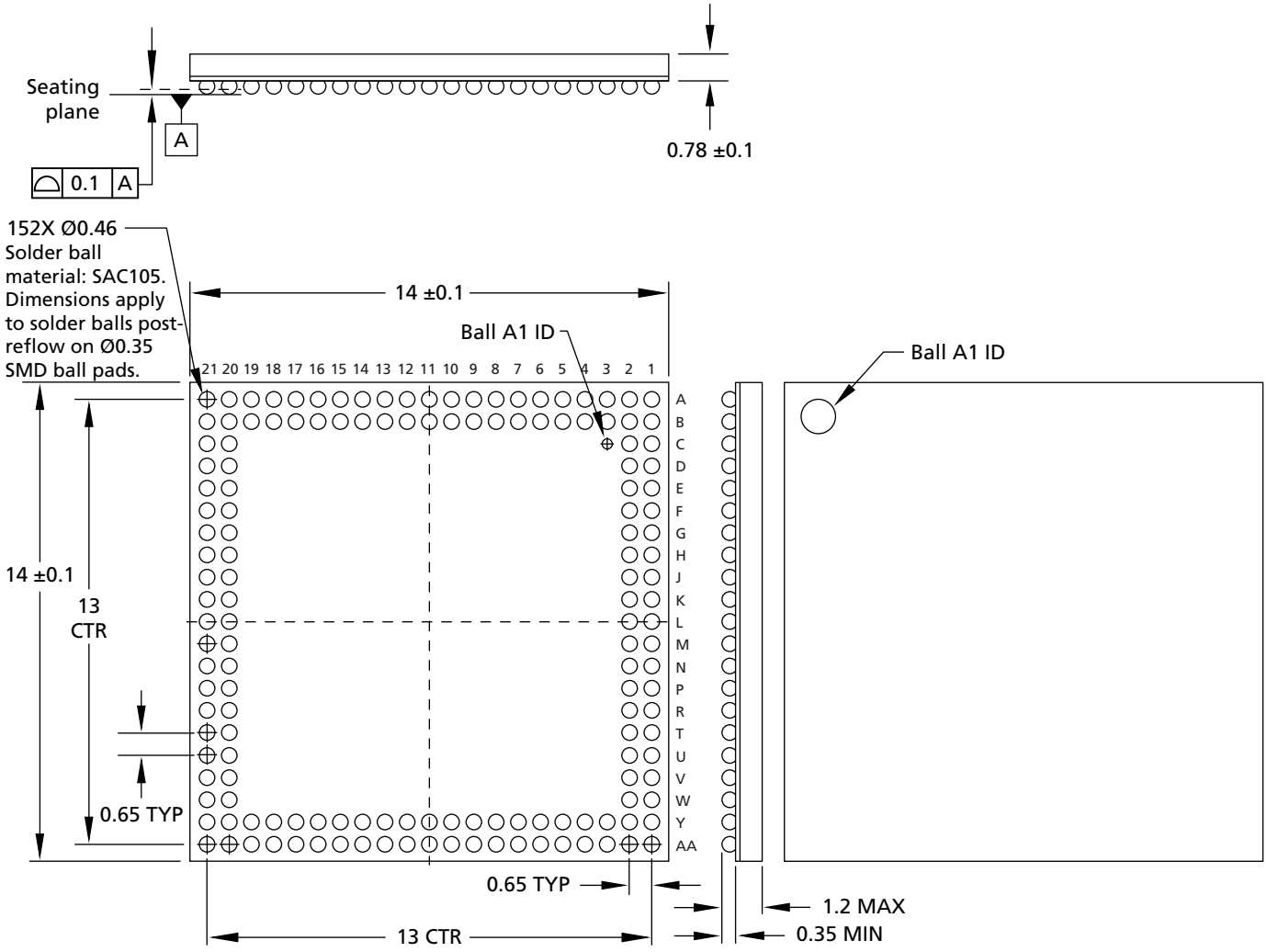
Package Dimensions

Figure 6: 152-Ball VFBGA Package, 1.0mm (Package Code: CG)



Notes: 1. All dimensions are in millimeters.

Figure 7: 152-Ball VFBGA Package, 1.2mm (Package Code: KZ)



Notes: 1. All dimensions are in millimeters.

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Revision History

Rev. E, Production 6/09

- Table 3, “Ball Assignments,” on page 6: Deleted ball numbers.
- Table 4, “Non-Device-Specific Ball Assignments,” on page 6: Deleted ball numbers.
- Table 5, “Absolute Maximum Ratings,” on page 7: Added note.
- Table 6, “Recommended Operating Conditions,” on page 7: Updated symbol for I/O supply voltage.

Rev. D, Preliminary 1/09

- Added 4Gb option and updated these items to reflect the addition:
  - “MT46HxxxMxxLxKZ” on page 1
  - “Options” on page 1
  - Table 1, “Configuration Addressing,” on page 1, including note 1
  - Table 2, “152-Ball Production Marketing Part Numbers,” on page 3, part number
  - Figure 1: “Marketing Part Number Example,” on page 2
  - Figure 3: “152-Ball VFBGA Ball Assignments,” on page 5
  - Table 4, “Non-Device-Specific Ball Assignments,” on page 6
  - Added Figure 5: “152-Ball VFBGA Functional Block Diagram, Quad Die,” on page 9
  - Added Figure 7: “152-Ball VFBGA Package, 1.2mm (Package Code: KZ),” on page 11.
- Removed references to reduced-page-size devices.
- Figure 4: “152-Ball VFBGA Functional Block Diagram (non-Quad Die),” on page 8: Added parenthetic comment to title.
- Figure 6: “152-Ball VFBGA Package, 1.0mm (Package Code: CG),” on page 10 and Figure 7: “152-Ball VFBGA Package, 1.2mm (Package Code: KZ),” on page 11: Added package codes to figure titles.

Rev. C, Preliminary 11/08

- Updated template and standards.
- Added Table 2, “152-Ball Production Marketing Part Numbers,” on page 3.

Rev. B, Preliminary 5/08

- Added reduced page-size options (LA and LG) to Table 1, “Configuration Addressing,” on page 1; Figure 1: “Marketing Part Number Example,” on page 2; “General Description” on page 4.

Rev. A, Preliminary 4/08

- Initial release.