Features

- 64-Mbit Flash and 16-Mbit PSRAM
- Single 66-ball (8 mm x 10 mm x 1.2 mm) CBGA Package
- 2.7V to 3.1V Operating Voltage

Flash

- Single Voltage Read/Write Operation: 2.65V to 3.6V
- Access Time – 70 ns
- Sector Erase Architecture
  - One Hundred Twenty-seven 32K Word Sectors with Individual Write Lockout
  - Eight 4K Word Sectors with Individual Write Lockout
- Fast Word Program Time – 10 µs
- Typical Sector Erase Time: 32K Word Sectors – 700 ms; 4K Word Sectors – 100 ms
- Suspend/Resume Feature for Erase and Program
  - Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector
  - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
  - 10 mA Active
  - 15 µA Standby
- VPP Pin for Write Protection and Accelerated Program Operation
- $\overline{WP}$ Pin for Sector Protection
- $\overline{RESET}$ Input for Device Initialization
- Flexibel Sector Protection
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)

PSRAM

- 16-megabit (1M x 16)
- 2.7V to 3.1V V_{CC}
- 70 ns Access Time

Device Number	Flash Boot Location	Flash Plane Configuration	PSRAM Configuration
AT52BC6402D	Bottom	64M (4M x 16)	16M (1M x 16)
AT52BC6402DT	Top	64M (4M x 16)	16M (1M x 16)

Flash & PSRAM Datasheets

Datasheets	PDF File
64M Flash Memory: AT49BV640D(T)	Acrobat Document
16M PSRAM: 2FHY64UD16161B	Acrobat Document

64-megabit Flash + 16-megabit PSRAM Stack Memory

AT52BC6402D
AT52BC6402DT

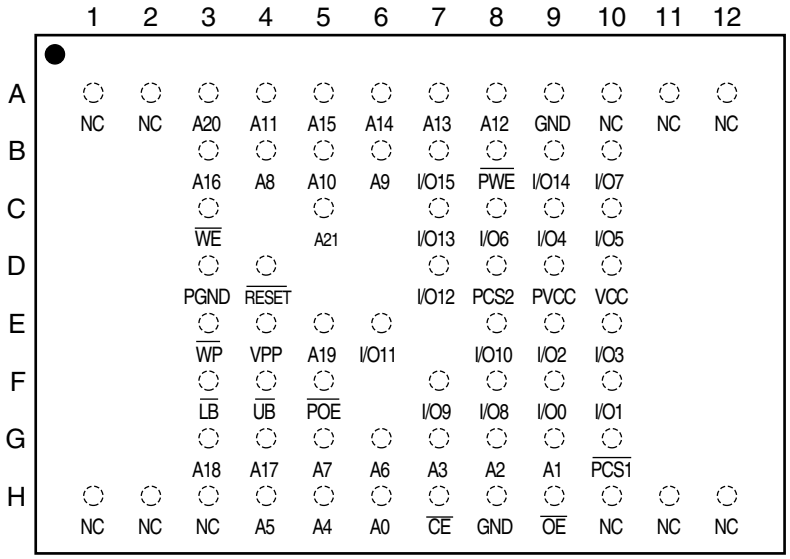
Preliminary

3619A–STKD–7/06

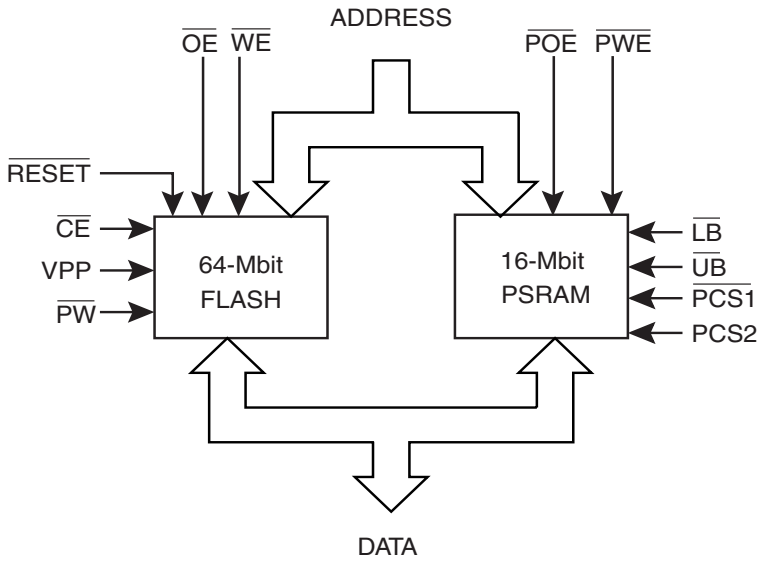
1. Pin Configuration

Pin Name	Function
A0 - A19, A21	Common Address Input for 16M PSRAM/Flash, Flash Address Input
$\overline{CE}$	Flash Chip Enable
$\overline{OE}$	Flash Output Enable
$\overline{WE}$	Flash Write Enable
$\overline{RESET}$	Flash Reset
$\overline{PW}$	Flash Write Protect
VPP	Flash Power Supply for Accelerated Program Operation
VCC	Flash Power
GND	Flash Ground
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect
$\overline{LB}$	PSRAM Lower Byte
$\overline{UB}$	PSRAM Upper Byte
PVCC	PSRAM Power
PGND	PSRAM Ground
$\overline{PCS1}$	PSRAM Chip Select 1
PCS2	Low Power Modes
$\overline{PWE}$	PSRAM Write Enable
$\overline{POE}$	PSRAM Output Enable

2. AT52BC6402D(T) (Top View)



3. Block Diagram



4. Description

The AT52BC6402D(T) combines a 64-megabit Flash (4M x 16) and an 16-megabit PSRAM (organized as 1M x 16) in a stacked 66-ball CBGA package. The stacked modules operate at 2.7V to 3.1V in the extended temperature range.

5. Absolute Maximum Ratings

Temperature under Bias	-55° C to +85° C
Storage Temperature	-55° C to +150° C
All Input Voltages except V_{PP} (including NC Pins) with Respect to Ground	-0.2V to V_{CC} +0.3V
Voltage on V_{PP} with Respect to Ground	-0.2V to + 10.0V
All Output Voltages with Respect to Ground	-0.2V to V_{CC} +0.3V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6. DC and AC Operating Range

	AT52BC6402D(T)-70CU
Operating Temperature (Case)	-30° C - 85° C
V_{CC} Power Supply	2.7V to 3.1V

7. Flash Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	V_{PP}[2]	Ai	I/O	PSRAM Operation
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Ai	D_{OUT}	PSRAM Must Be High-Z
Program/Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IHPP}[3]	Ai	D_{IN}	
Program Inhibit	V_{IL}	X	V_{IH}	V_{IH}	X			
	V_{IL}	X	X	X	V_{ILPP}[4]			
Software Product Identification	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	A0 = V_{IL}, A1 - A19 = V_{IL}	Manufacturer Code	
						A0 = V_{IH}, A1 - A19 = V_{IL}	Device Code	
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	X	High Z	Any PSRAM Operation is Allowed
Output Disable	X	V_{IH}	X	V_{IH}	X		High Z	
Reset	X	X	X	V_{IL}	X	X	High Z	

Notes: 1. X can be V_{IL} or V_{IH}
2. The VPP pin can be tied to V_{CC}. For faster program operations, V_{PP} can be set to 9.5V ± 0.5V.
3. V_{IHPP} (min) = 1.65V
4. V_{ILPP} (max) = 0.4V

8. Functional Description

$\overline{PCS1}$	PCS2	$\overline{POE}$	$\overline{PWE}$	$\overline{LB}$	$\overline{UB}$	I/O0 - 7	I/O8 - 15	Mode	Power	Flash Operation
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby	Any Flash Operation Allowed
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Low-power Modes	
L[1]	H	X[1]	X[1]	H	H	High-Z	High-Z	Output Disabled	Active	Flash Must Be High Z
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active	
	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active	
L	H	L	H	L	H	D_{OUT}	High-Z	Lower Byte Read	Active	
				H	L	High-Z	D_{OUT}	Upper Byte Read	Active	
				L	L	D_{OUT}	D_{OUT}	Word Read	Active	
		X[1]	L	L	H	D_{IN}	High-Z	Lower Byte Write	Active	
				H	L	High-Z	D_{IN}	Upper Byte Write	Active	
				L	L	D_{IN}	D_{IN}	Word Write	Active	

Note: 1. X means don't care (must be low or high state).

9. Ordering Information

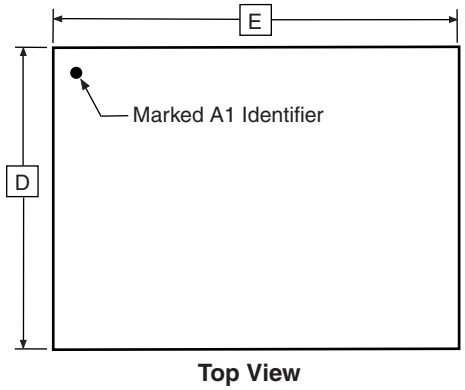
9.1 Green Package (Pb/Halide-free)

t_{ACC} (ns)	Ordering Code	Flash Boot Block	Flash Plane Architecture	PSRAM	Package	Operation Range
70	AT52BC6402D-70CU	Bottom	64M – Single Bank	1M x 16	66C7	Extended (-30° to 85° C)
	AT52BC6402DT-70CU	Top	64M – Single Bank			

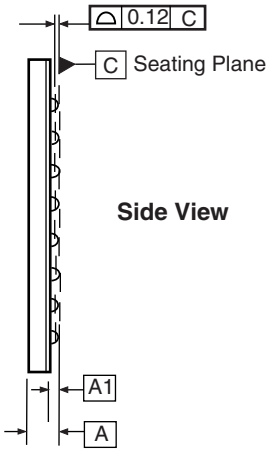
Package Type	
66C7	66-ball, Plastic Chip-size Ball Grid Array Package (CBGA)

10. Packaging Information

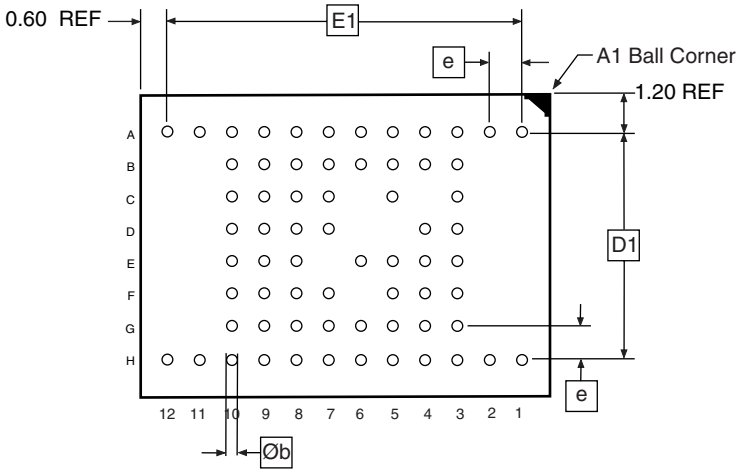
10.1 66C7 – CBGA



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
E	9.90	10.00	10.10	
E1	8.75	8.80	8.85	
D	7.90	8.00	8.10	
D1	5.55	5.60	5.65	
A	–	–	1.20	
A1	0.25	–	–	
e	0.80 TYP			
Øb	–	0.40	–	

5/01/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**66C7**, 66-ball (12 x 8 Array), 10 x 8 x 1.2 mm Body, 0.8 mm Ball Pitch Chip-scale Ball Grid Array Package (CBGA)	66C7	A

11. Revision History

Revision No.	History
Revision A – July 2006	• Initial Release

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