S71WS-N

Stacked Multi-Chip Product (MCP)

1.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with CellularRAM

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71WS-N_00 **Revision** A **Amendment** 7 **Issue Date** April 4, 2008

Notice On Data Sheet Designations

Spansion Inc. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion Inc. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion Inc. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion Inc. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion Inc. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

S71WS-N

Stacked Multi-Chip Product (MCP)

1.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with CellularRAM

Data Sheet

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed: 54 MHz, 66 MHz, 80 MHz**
- **Package**
  - 8 x 11.6 mm, 9 x 12 mm
- **Operating Temperature**
  - Wireless, –25° C to +85° C

General Description

The S71WS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more flash memory die (for the S71WS512N, two S29WS256N devices are used)
- CellularRAM Type 2 pSRAM

The products covered by this document are listed in the table below. For details about their specifications, please refer to the individual constituent datasheet for further details.

Flash Density	pSRAM		
	32 Mb	64 Mb	128 Mb
S29WS128N	S71WS128NB0	S71WS128NC0	
S29WS256N		S71WS256NC0	S71WS256ND0
S29WS512N		S71WS512NC0	S71WS512ND0

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS-N	S29WS-N_00
32 M CellularRAM Type 2	CellularRAM_08
64 M CellularRAM Type 2	Cellram_07
128 M CellularRAM Type 2	Cellram_07

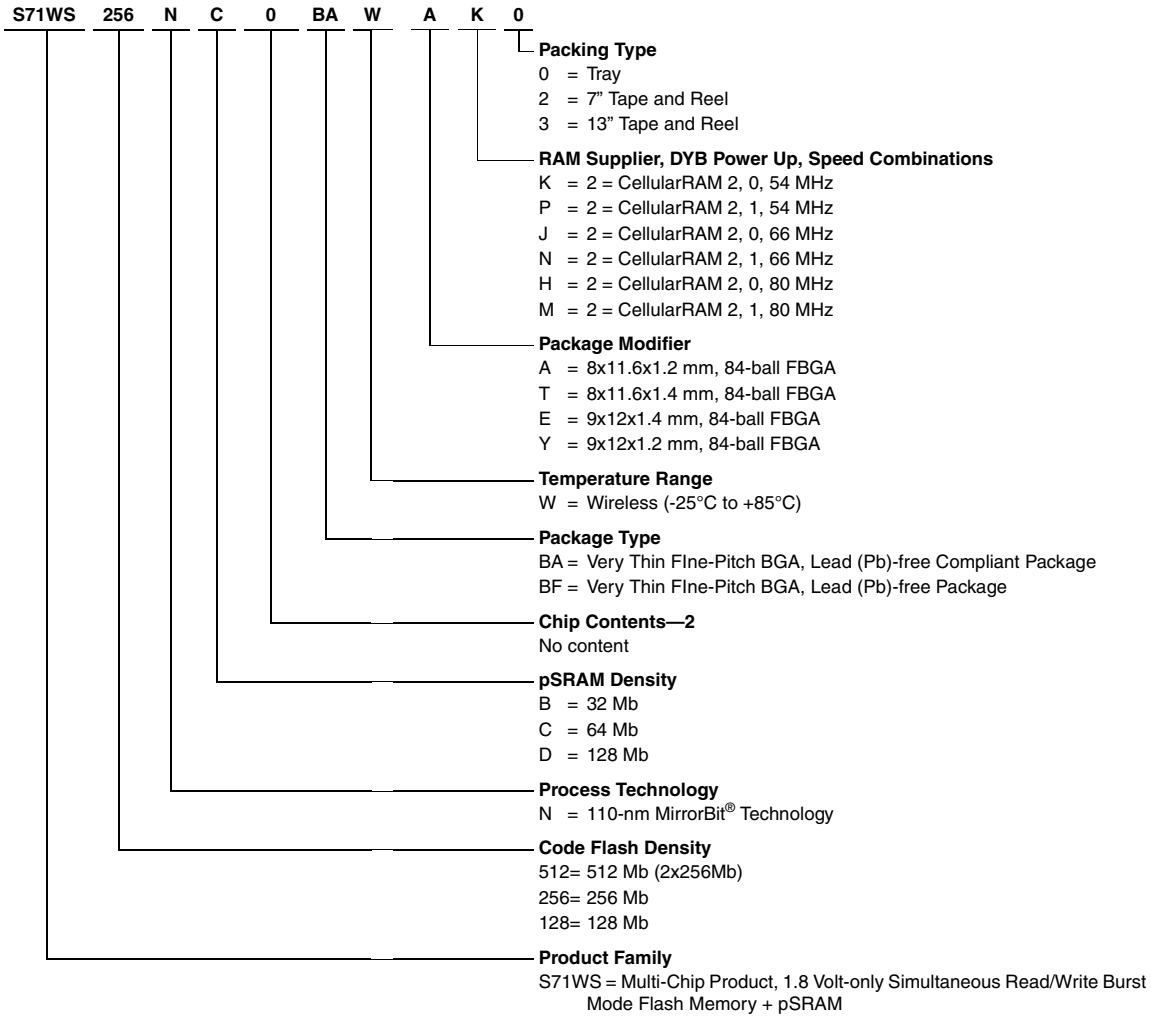
1. Product Selector Guide

Device	Model Numbers	Flash	pSRAM Density (Mb)	Flash Speed (MHz)	pSRAM Speed (MHz)	DYB Power-Up State (See Note)	pSRAM (Cellular RAM) Supplier	Package (mm)
S71WS128NB0	AK	WS128N	32	54	54	0	2	8.0X11.6X1.2
	AP					1		
	AJ			66	66	0		
	AN					1		
	AH			80	80	0		
	AM					1		
S71WS128NC0	AK	WS128N	64	54	54	0	2	8.0X11.6X1.2
	AP					1		
	AJ			66	66	0		
	AN					1		
	AH			80	80	0		
	AM					1		
S71WS256NC0	AK	WS256N	64	54	54	0	2	11.6x8.0x1.2
	AP					1		
	AJ			66	66	0	2	
	AN					1		
	AH			80	80	0	2	
	AM					1		
S71WS256ND0	YK		128	54	54	0	2	9x12x1.2
	YP					1		
	YJ			66	66	0		
	YN					1		
	YH			80	80	0		
	YM					1		
S71WS512NC0	AK	WS512N	64	54	54	0	2	11.6x8.0x1.2
	AP					1		
	TJ			66	66	0	2	11.6x8.0x1.4
	TN					1		
	TH			80	80	0	2	
	TM					1		
S71WS512ND0	EK		128	54	54	0	2	9x12x1.4
	EP					1		
	EJ			66	66	0		
	EN					1		
	EH			80	80	0		
	EM					1		

Note:
0 (Protected), 1 (Unprotected [Default State])

2. Ordering Information

The order number is formed by a valid combinations of the following:



2.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2.1 MCP Configurations and Valid Combinations

Valid Combinations					
S71WS128N	B	0	BAW, BFW	A	K, P, J, N, H, M
	C			A	K, P, J, N, H, M
S71WS256N	C			A	K, P, J, N, H, M
	D			Y	K, P, J, N, H, M
S71WS512N	C			A	K, P, H, M
				T	J, N, H, M
	D			E	K, P, J, N, H, M

Package Marking Note:
The package marking omits the leading S *from the ordering part number.*

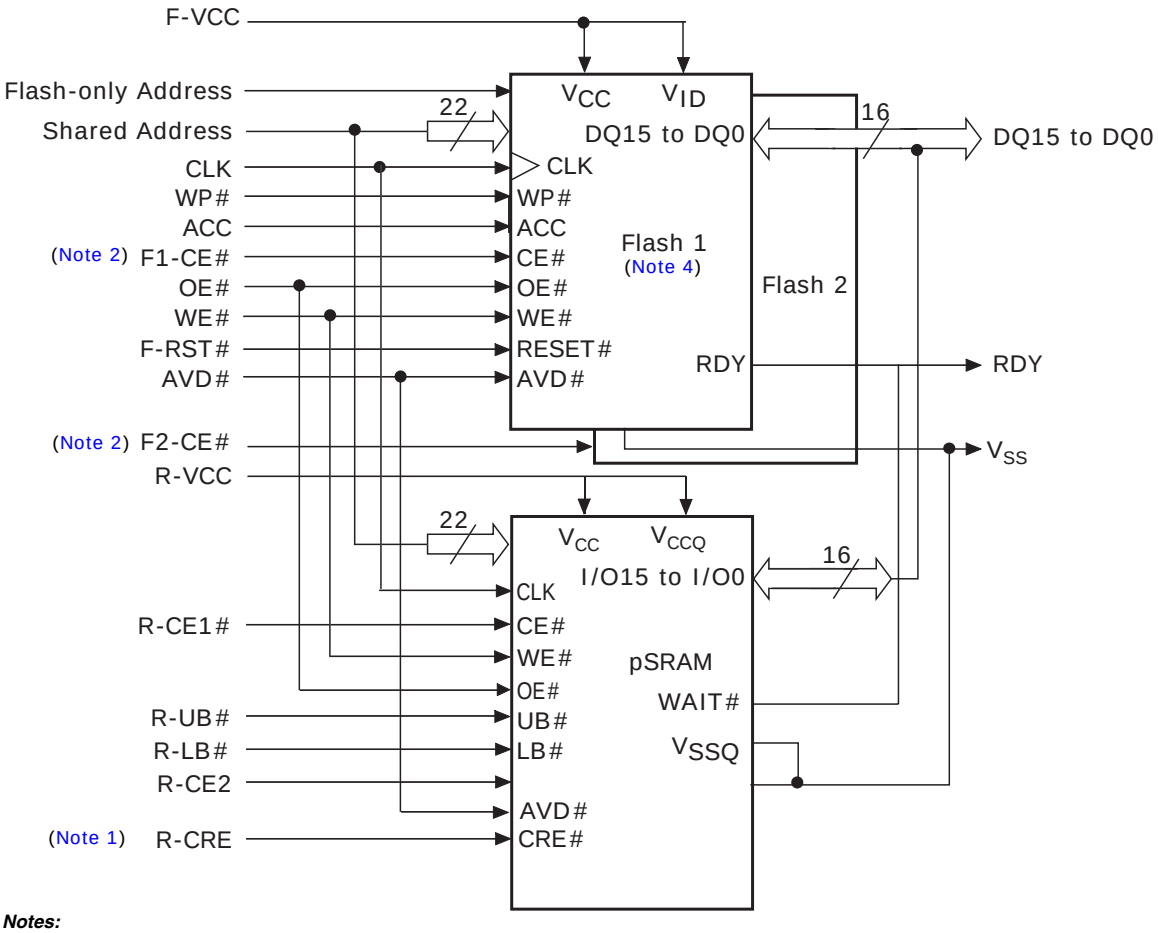
3. Input/Output Descriptions

Table 3.1 identifies the input and output package connections provided on the device.

Table 3.1 Input/Output Descriptions

Symbol	Description
A23-A0	Address inputs
DQ15-DQ0	Data input/output
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.
WE#	Write Enable input.
V_{SS}	Ground
NC	No Connect; not connected internally
RDY	Ready output. Indicates the status of the Burst read. The WAIT# pin of the pSRAM is tied to RDY.
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs
F-RST#	Hardware reset input. Low = device resets and returns to reading array data
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.
F-ACC	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.
R-CE1#	Chip-enable input for pSRAM.
F1-CE#	Chip-enable input for Flash 1. Asynchronous relative to CLK for Burst Mode.
F2-CE#	Chip-enable input for Flash 2. Asynchronous relative to CLK for Burst Mode. This applies to the 512Mb MCP only.
R-CRE	Control Register Enable (pSRAM). For CellularRAM only.
F-VCC	Flash 1.8 Volt-only single power supply.
R-VCC	pSRAM Power Supply.
R-UB#	Upper Byte Control (pSRAM).
R-LB#	Lower Byte Control (pSRAM)
DNU	Do Not Use

4. MCP Block Diagram



Notes:

1. *R-CRE is only present in CellularRAM-compatible pSRAM.*
2. *For 1 Flash + pSRAM, F1-CE# = CE#. For 2 Flash + pSRAM, CE# = F1-CE# and F2-CE# is the chip-enable pin for the second Flash.*
3. *Only needed for S71WS512N.*
4. *For the 128M pSRAM devices, there are 23 shared addresses.*

5. Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S71WS-N.

5.1 Special Handling Instructions for FBGA Packages

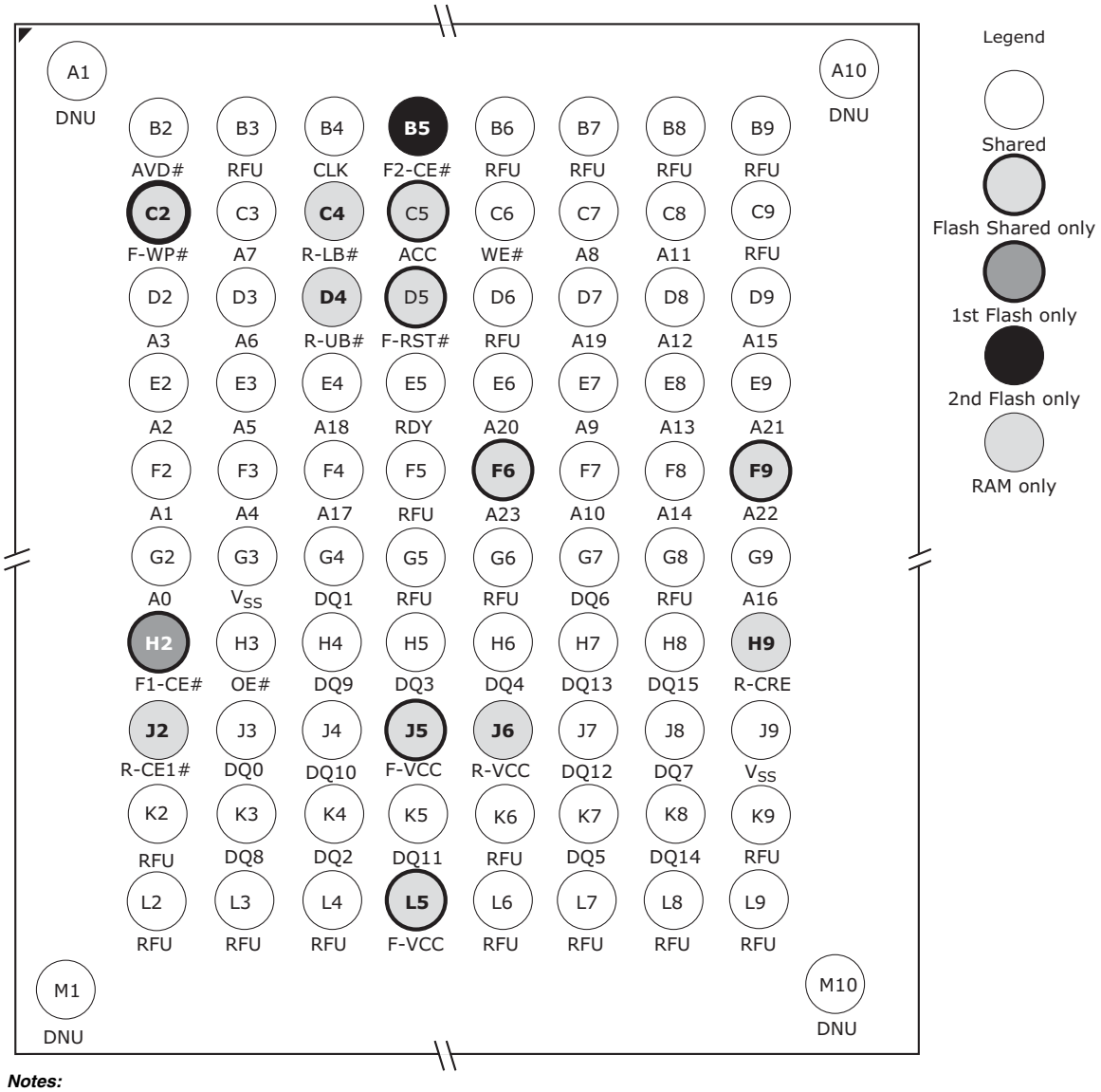
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.2 Connection Diagrams

5.2.1 CellularRAM Based Pinout

84-ball Fine-Pitch Ball Grid Array
CellularRAM-based Pinout (Top View, Balls Facing Down)



Notes:

1. *In MCPs based on a single S29WS256N (S71WS256N), ball B5 is RFU. In MCP's based on two S29WS256N (S71WS512), ball B5 is F2-CE#.*
2. *Addresses are shared between Flash and RAM depending on the density of the pSRAM.*

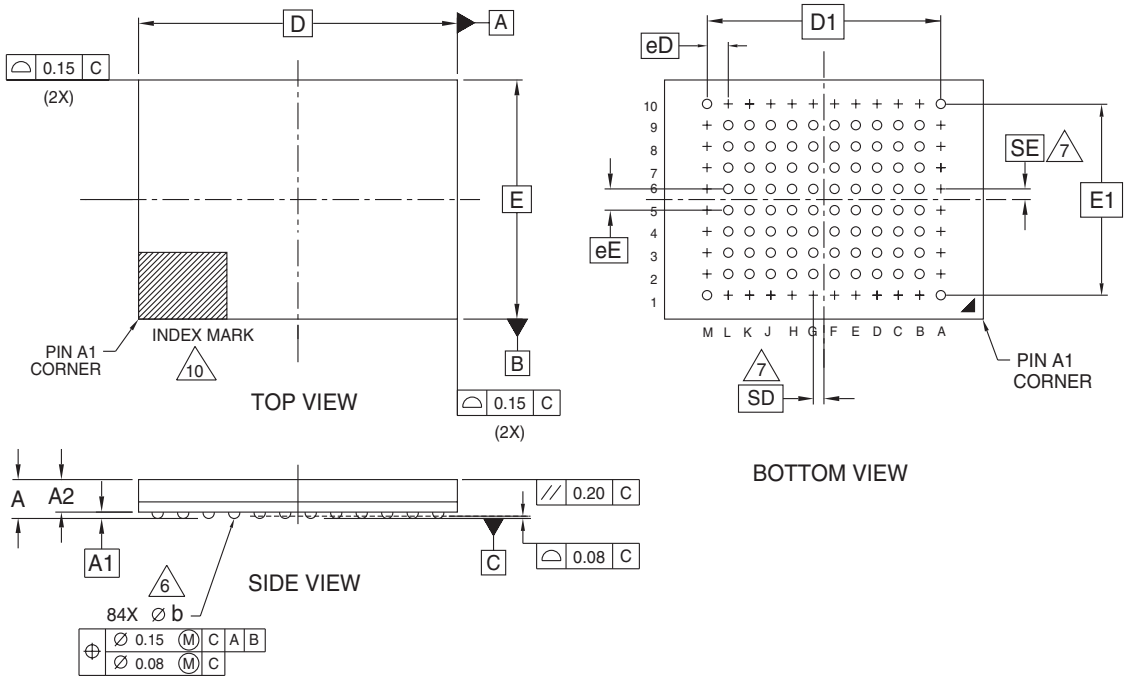
MCP	Flash-only Addresses	Shared Addresses
S71WS128NB0	A22-A21	A20-A0
S71WS128NC0	A22	A21-A0
S71WS256NC0	A23 – A22	A21 – A0
S71WS256ND0	A23	A22 – A0
S71WS512NC0	A23 – A22	A21-A0
S71WS512ND0	A23	A22-A0

5.2.2 Look-Ahead Pinout for Future Designs

Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design_Scalable_Wireless_A0_E). Contact your local Spansion sales representative for more details.

5.3 Physical Dimensions

5.3.1 TLA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 11.6 x 8.0 x 1.2 mm



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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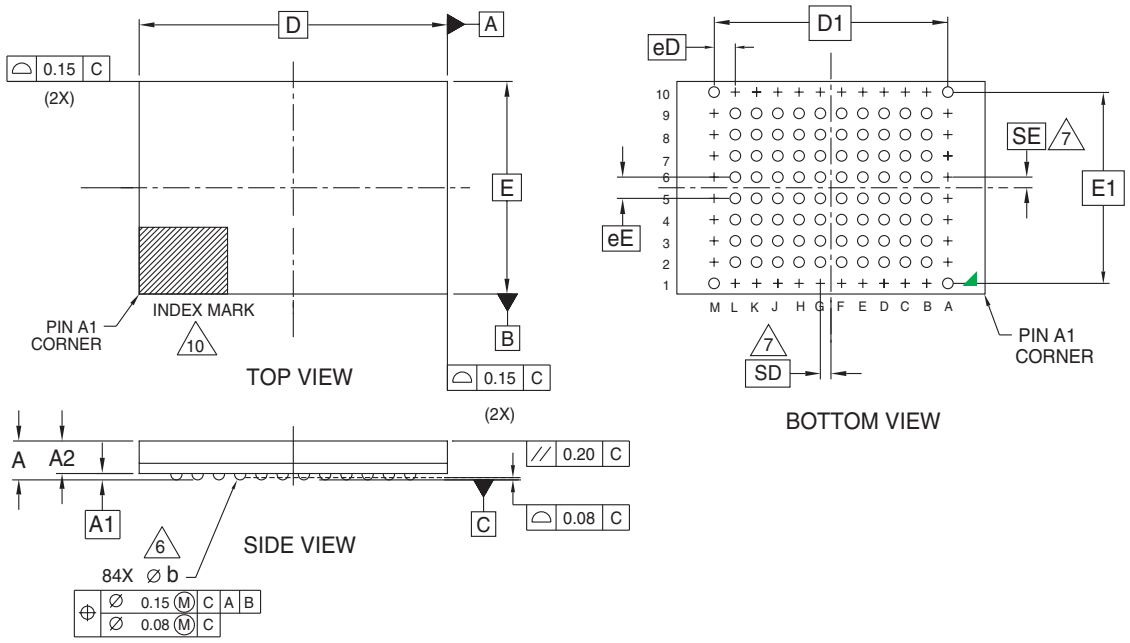
5.3.2 FTA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 11.6 x 8.0 x 1.4 mm



PACKAGE	FTA 084			NOTE
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	1.02	---	1.17	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10,E1,E10 F1,F10,G1,G10,H1,H10 J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

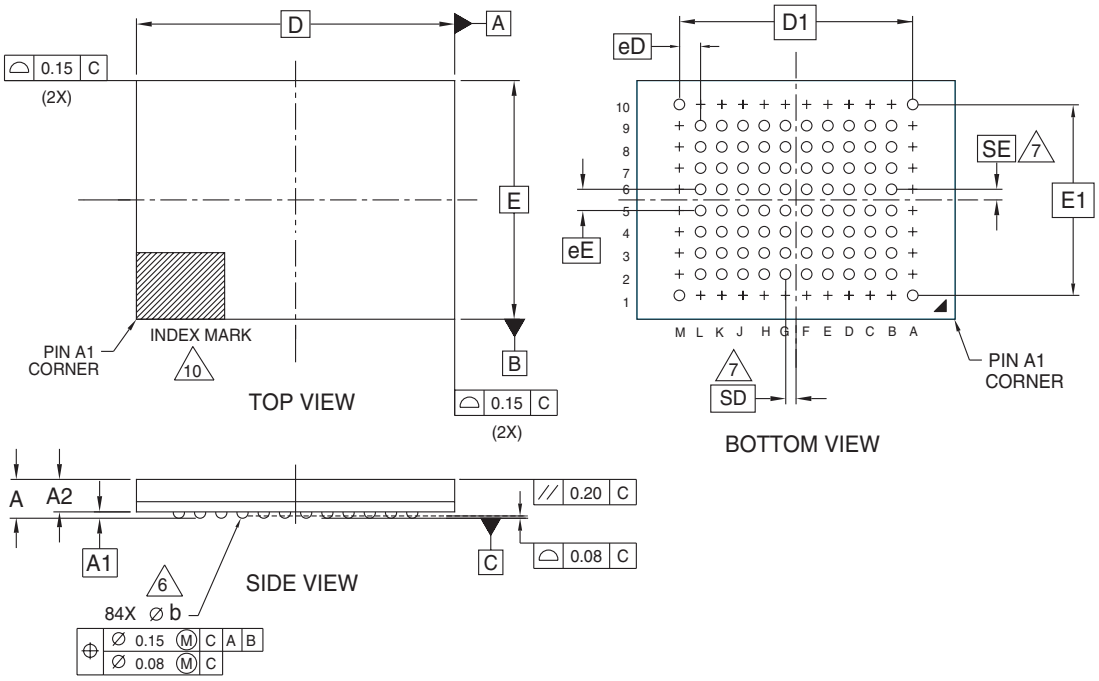
   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3388 \ 16-038.21a

5.3.3 TSD084—84-ball Fine-Pitch Ball Grid Array (FBGA) 12.0 x 9.0 x 1.2 mm



PACKAGE	TSD 084			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.94	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,7,A8,A9 B1,B10,C1,C10,D1,D10 E1,E10,F1,F10,G1,G10 H1,H10,J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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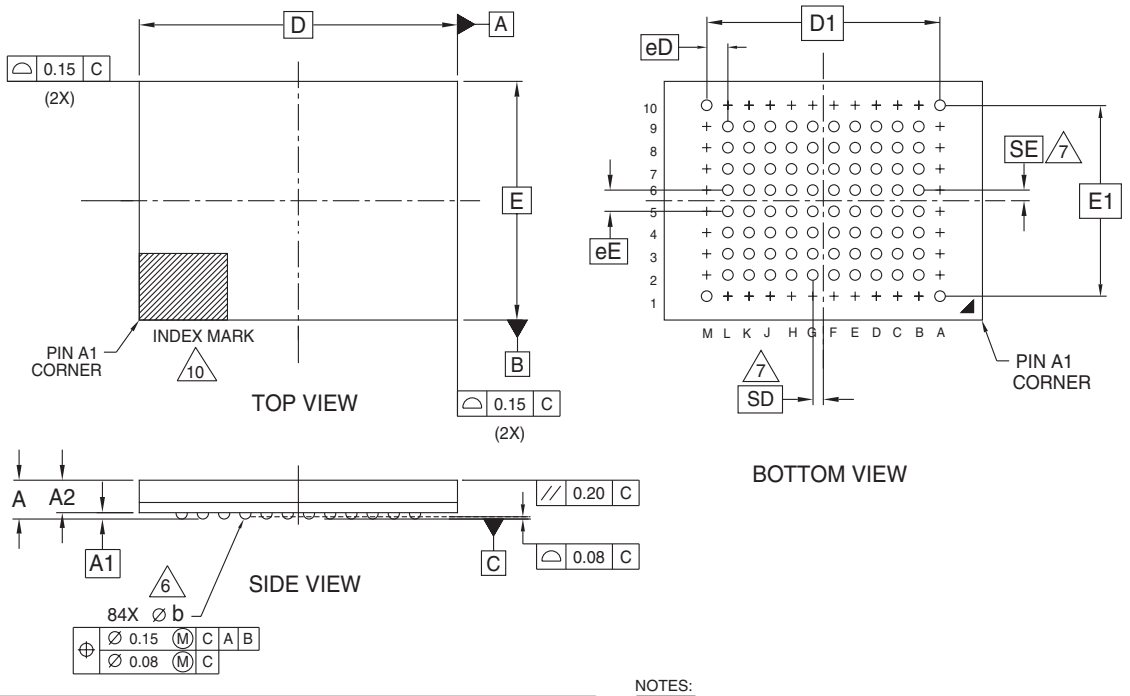
5.3.4 FEA084—84-ball Fine-Pitch Ball Grid Array (FBGA) 12.0 x 9.0 x 1.4 mm



PACKAGE	FEA 084			NOTE
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.10	---	---	BALL HEIGHT
A2	1.11	---	1.26	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10 E1,E10,F1,F10,G1,G10 H1,H10,J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

Note:
BSC is an ANSI standard for Basic Space Centering.

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3423 \ 16-038.21a

6. Revision History

Section	Description
Revision A (February 1, 2004)	
	Initial release.
Revision A1 (February 9, 2005)	
Global	Updated document to include Burst Speed of 66 MHz Updated Publication Number
Revision A2 (March 31, 2005)	
Global	Updated Product Selector Guide and Ordering Information tables
Revision A3 (May 2, 2005)	
Global	Added 80 MHz speed options to: Product Selector Guide Ordering Information table Valid Combination table
Revision A4 (August 25, 2005)	
Global	Replaced module cellRAM_00_A0 with cellRAM_03 and cellRAM_04
Revision A5 (February 7, 2006)	
Global	Updated Product Selector Guide with new options Updated the Ordering Part Number table Updated the Valid Combinations table Removed the Look-ahead Diagram
Revision A6 (July 19, 2006)	
Global	Reformatted document to new template Added reference to 32 Mb CellRAM module
Revision A7 (April 4, 2008)	
Global	Removed "Advanced Information" status
General Description	Updated pSRAM Publication Identification Numbers