S71PL-N MirrorBit® MCPs

S71PL256N, S71PL127N, S71PL129N

256/128/128 Megabit (16/8/8 M x 16-Bit)
CMOS 3.0 Volt-only Simultaneous Read/Write,
Page Mode Flash Memory

Data Sheet

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71PL-N_00 **Revision** A **Amendment** 11 **Issue Date** June 9, 2010

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Questions regarding these document designations may be directed to your local sales office.

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Page Mode Flash Memory

Data Sheet

Features

- **Speed**
  - Flash: 70 ns
  - pSRAM: 70 ns
- **8.0 x 11.6 x 1.2 mm Packages**
  - 84-Ball Fine-Pitch Ball Grid Array (FBGA)
    S71PL256NC0
    S71PL256ND0
  - 64 Ball Fine-Pitch Ball Grid Array (FBGA)
    S71PL129NB0
    S71PL129NC0
    S71PL127NB0
    S71PL127NC0
- **Speed**
  - Flash: 70 ns
  - pSRAM: 70 ns
- **Operating Temperature Range**
  - Temperature Range of –25°C to +85°C

General Description

This document contains information for the S71PL-N MirrorBit MCP product. For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number (PID)
S29PL-N	S29PL-N_00
32M pSRAM Type 8 (90 nm)	comspec_02
32M pSRAM Type 8 (130 nm)	pSRAM_31
32M pSRAM Type 7	pSRAM_29
32M pSRAM Type 2	pSRAM_19
64M pSRAM Type 2	pSRAM_20
64M pSRAM Type 8 (90 nm)	SPH064D970R1R
64M pSRAM Type 8 (130 nm)	pSRAM_32
128M pSRAM Type 2	pSRAM_15

Publication Number S71PL-N_00 **Revision** A **Amendment** 11 **Issue Date** June 9, 2010

1. Flash/RAM Combinations Table

		pSRAM Density		
		32 Mb	64 Mb	128 Mb
Flash Density	PL127N	S71PL127NB0	S71PL127NC0	
	PL129N	S71PL129NB0	S71PL129NC0	
	PL256N		S71PL256NC0	S71PL256ND0

2. Product Selector Guide

Device	pSRAM Density	pSRAM Type
S71PL127NB0	32 Mb	pSRAM Type 2
S71PL127NB0	32 Mb	pSRAM Type 7
S71PL127NB0	32 Mb	pSRAM Type 8 (90 & 130 nm)
S71PL127NC0	64 Mb	pSRAM Type 2
S71PL127NC0	64 Mb	pSRAM Type 8 (90 & 130 nm)
S71PL129NB0	32 Mb	pSRAM Type 2
S71PL129NB0	32 Mb	pSRAM Type 7
S71PL129NB0	32 Mb	pSRAM Type 8 (130 nm)
S71PL129NC0	64 Mb	pSRAM Type 2
S71PL129NC0	64 Mb	pSRAM Type 8 (90 & 130 nm)
S71PL256NC0	64 Mb	pSRAM Type 2
S71PL256NC0	64 Mb	pSRAM Type 8 (90 & 130 nm)
S71PL256ND0	128 Mb	pSRAM Type 2

3. Ordering Information

The order number is formed by a valid combinations of the following:

S71PL 256 N C0 HF W 5B 0

Packing Type
0 = Tray
2 = 7” Tape and Reel
3 = 13” Tape and Reel

Model Number (V_{IO} Range, Package Type)
Refer to the Valid Combinations table below

Temperature Range
W = Wireless (–25°C to +85°C)

Package Type & Material Set
HA = MCP BGA, 1.2 mm height, 0.8 mm pitch, Lead (Pb)-free Compliant package
HF = MCP BGA, 1.2 mm height, 0.8 mm pitch, Lead (Pb)-free package
HH = MCP BGA, 1.2 mm height, 0.8 mm pitch, Low-Halogen, Lead (Pb)-free package

pSRAM Density
B0 = 32 Mb pSRAM
C0 = 64 Mb pSRAM
D0 = 128 Mb pSRAM

Process Technology
N = 110 nm MirrorBit® Technology

Flash Density
256= 256 Mb
129= 128 Mb (Dual CE#)
127= 128 Mb (Single CE#)

Product Family
S71PL =3.0 Volt-only Simultaneous Read/Write, Page Mode Flash Memory

3.1 Valid Combinations

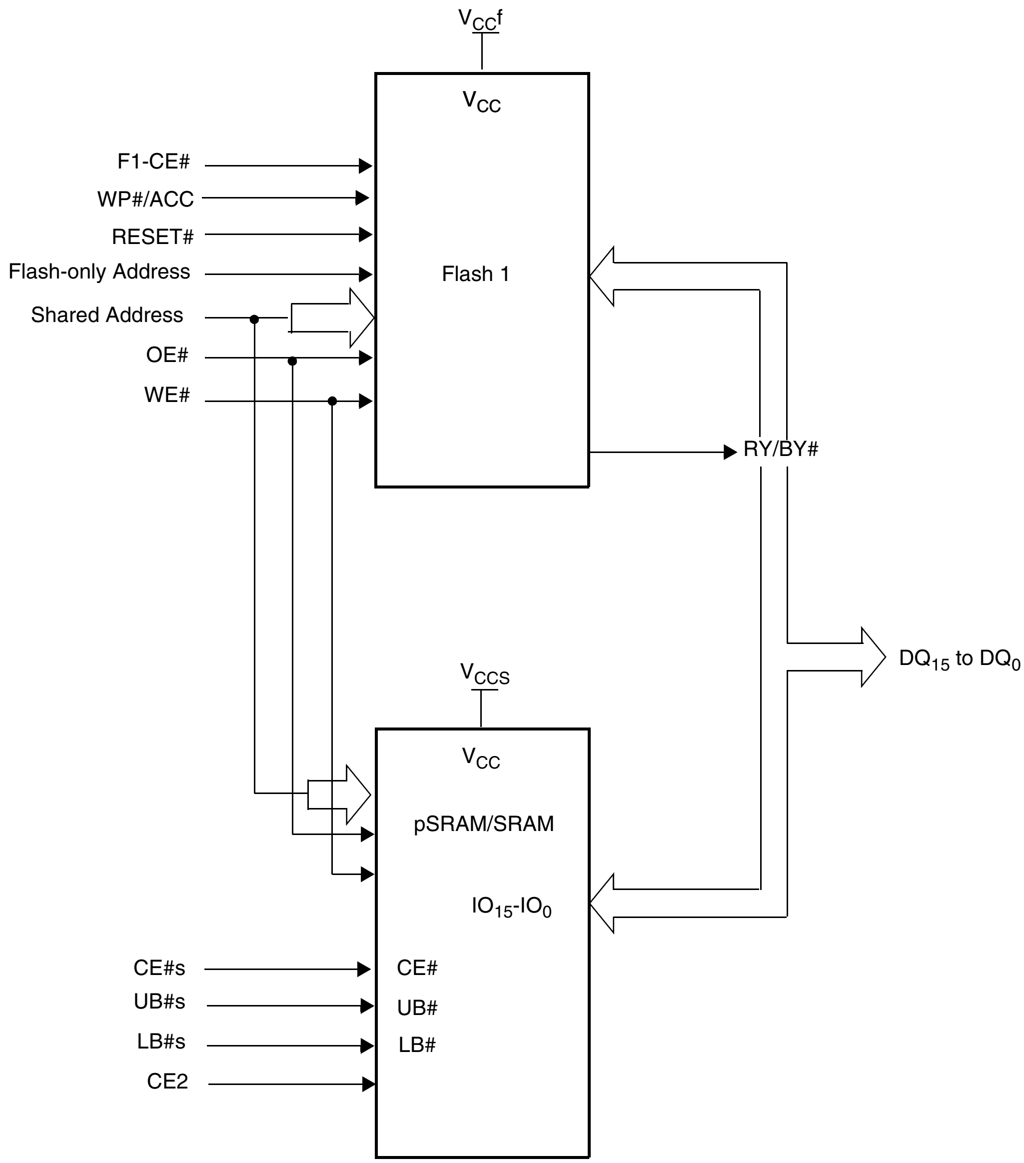
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 3.1 Valid Combinations

Base Ordering Part Number (2)	Package & Temperature	Model Number	Packing Type	pSRAM Type	Flash Speed Option	pSRAM Speed Options	Package Name
S71PL127NB0	HAW, HFW	4B (4)	0, 2, 3 (1), (2)	Type 2	70 ns	70 ns	TLA064 - 8 x 11.6 x 1.2 mm, 64-ball
		4U		Type 8			
		4Z (4)		Type 7			
	HHW	4U		Type 8			
S71PL127NC0	HAW, HFW	4B (4)		Type 2			
		4U		Type 8 (5)			
S71PL129NB0		4B (4)		Type 2			
		4U (4)		Type 8			
		4Z (4)		Type 7			
S71PL129NC0		4B (4)		Type 2			
		4U (4)		Type 8 (5)			
S71PL256NC0		5B (4)		Type 2			TLA084- 8 x 11.6 x 1.2 mm, 84-ball
		5U (4)		Type 8 (5)			
S71PL256ND0		5B (4)		Type 2			TSB084 - 8 x 11.6 x 1.2, 84-ball

Notes:
1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Contact factory for availability for any of the OPNs listed since RAM type availability may vary over time.*
4. *Part not recommended for new designs.*
5. *MCP with 90 nm Type 8 pSRAM has package material character F for Pb-free but also satisfies low-Halogen requirement.*

4. Block Diagram



Notes:

1. RY/BY# is an open drain output.

2. A_{MAX} = A23 (PL256N), A22 (PL127N), A21 (PL129N).

5. Physical Dimensions/Connection Diagrams

This section shows the I/O designations and package specifications for the S71PL-N.

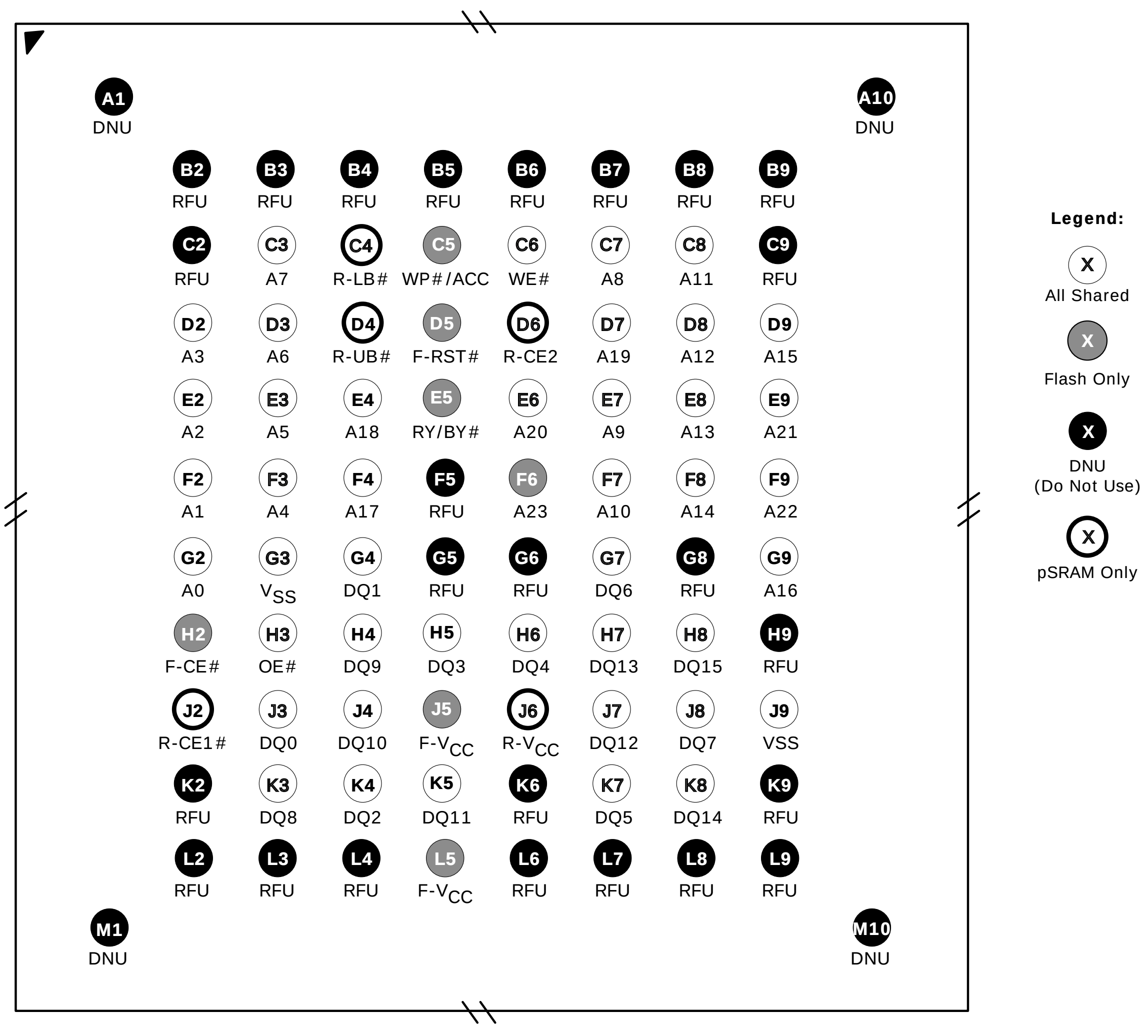
5.1 Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.2 S71PL256N TLA084/TSB084

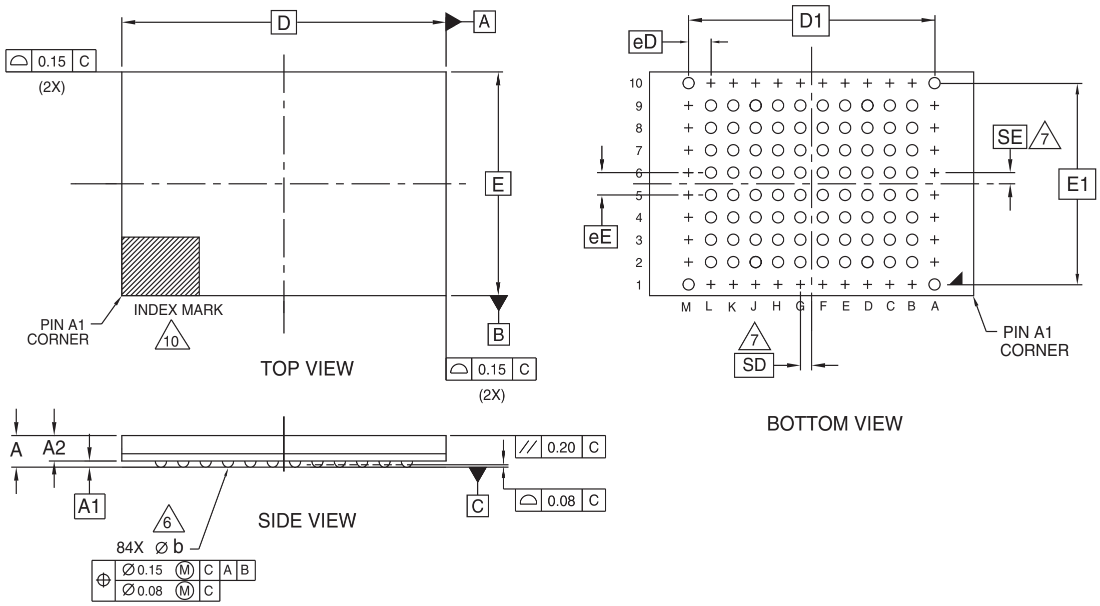
Figure 5.1 84-ball Fine-Pitch Ball Grid Array (S71PL256N)



Note:
Top view—balls facing down.
The addresses that are shared vary by MCP combination as shown in the table below:

	Flash-only Addresses	Shared Addresses
S71PL256NC0	A23-A22	A21:A0
S71PL256ND0	A23	A22:A0

Figure 5.2 TSB084 Physical Dimensions



PACKAGE	TSB 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	11.60 BSC.			BODY SIZE
E	8.00 BSC.			BODY SIZE
D1	8.80 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	84			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10 E1,E10,F1,F10,G1,G10 H1,H10,J1,J10,K1,K10,L1,L10 M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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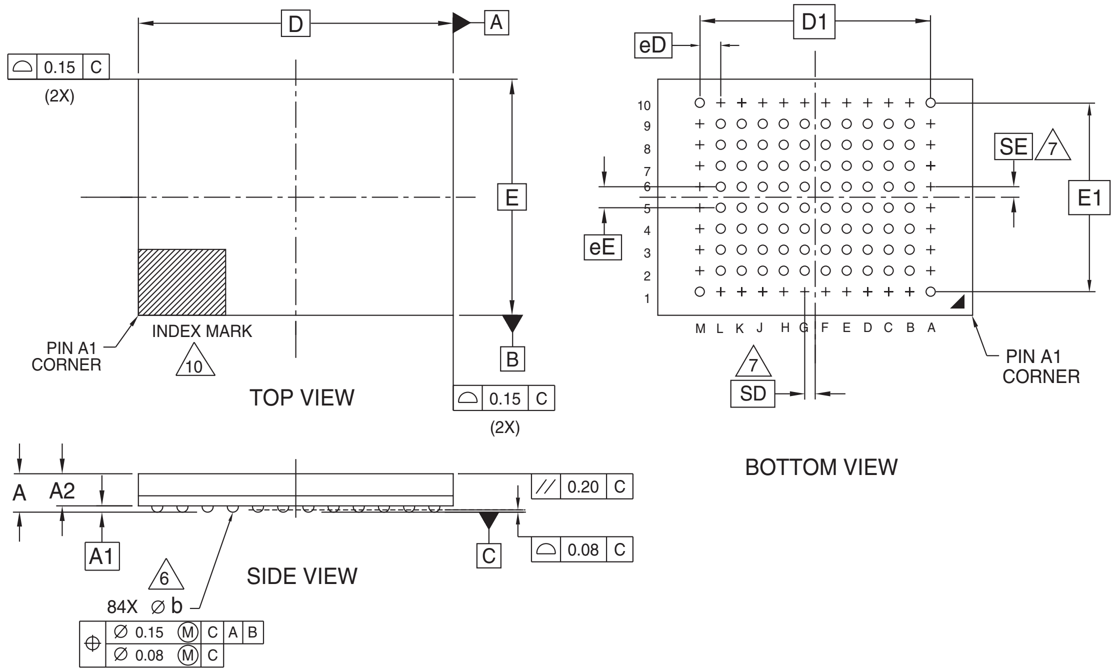
Figure 5.3 TLA084 Physical Dimensions



PACKAGE	TLA 084			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		84		BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B10,C1,C10,D1,D10, E1,E10,F1,F10,G1,G10, H1,H10,J1,J10,K1,K10,L1,L10, M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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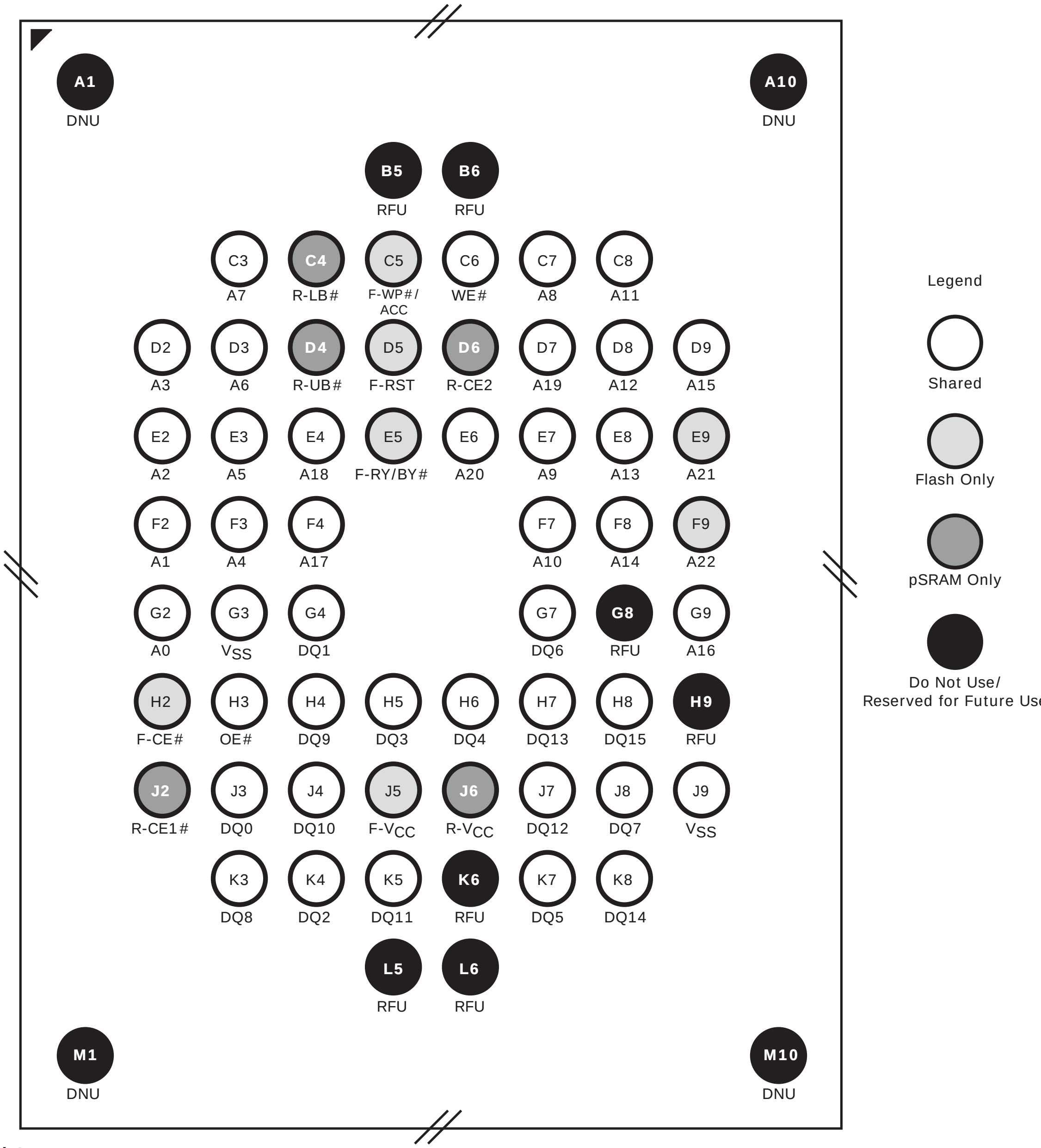
5.3 S71PL127N—TLA064

Figure 5.4 64-ball Fine-Pitch Ball Grid Array (S71PL127N)

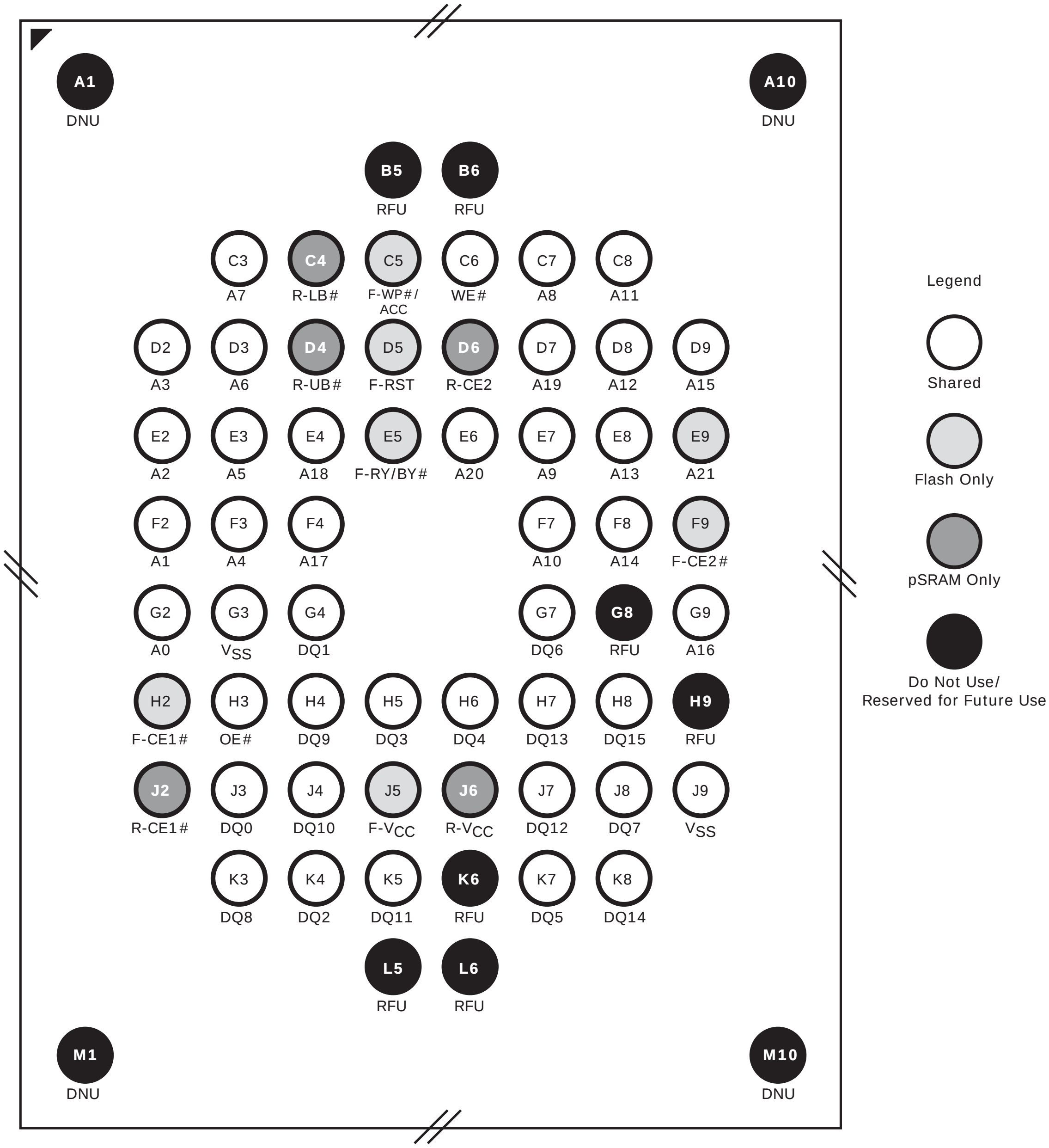


Note:
Top view—balls facing down.
The addresses that are shared vary by MCP combination as shown in the table below:

	Flash-only Addresses	Shared Addresses
S71PL127NB0	A22-A21	A20:A0
S71PL127NC0	A22	A21:A0

5.4 S71PL129N—TLA064

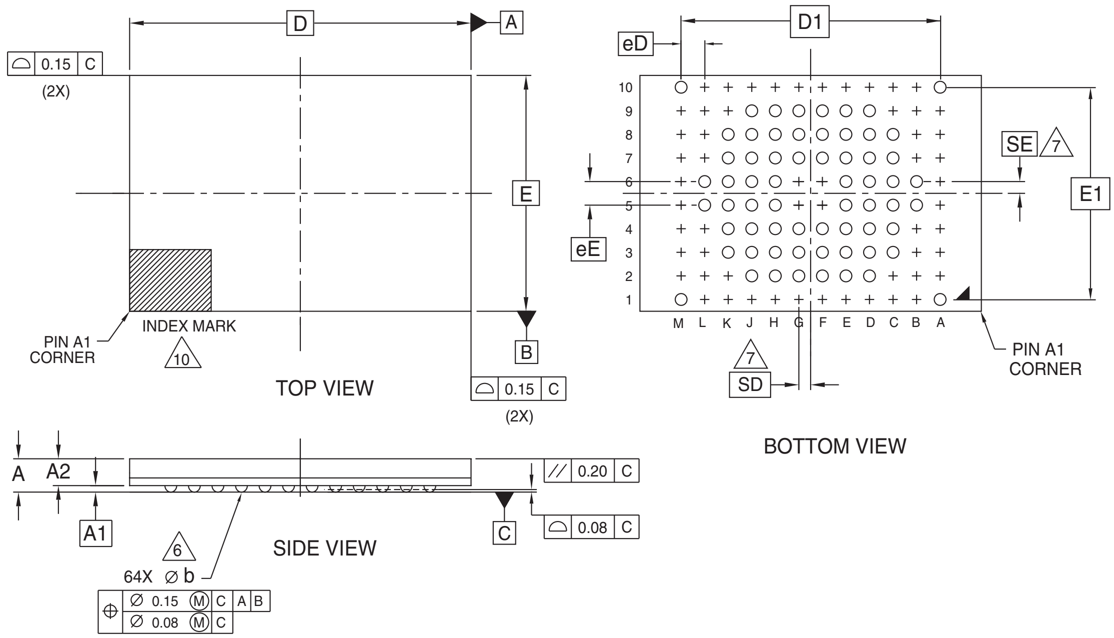
Figure 5.5 64-ball Fine-Pitch Ball Grid Array (S71PL129N)



Note:
Top view—balls facing down.
The addresses that are shared vary by MCP combination as shown in the table below:

	Flash-only Addresses	Shared Addresses
S71PL129NB0	A21	A20:A0
S71PL129NC0	—	A21:A0

Figure 5.6 TLA064 Physical Dimensions



PACKAGE	TLA 064			
JEDEC	N/A			
D x E	11.60 mm x 8.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		11.60 BSC.		BODY SIZE
E		8.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		64		BALL COUNT
φb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A2,A3,A4,A5,A6,A7,A8,A9 B1,B2,B3,B4,B7,B8,B9,B10 C1,C2,C9,C10,D1,D10,E1,E10, F1,F5,F6,F10,G1,G5,G6,G10 H1,H10,J1,J10,K1,K2,K9,K10 L1,L2,L3,L4,L7,L8,L9,L10 M2,M3,M4,M5,M6,M7,M8,M9		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Revision History

Section	Description
Revision A (March 11, 2005)	
	Initial release
Revision A1 (April 27, 2005)	
Performance Characteristics pSRAM Density table	Added 128 Mb pSRAM device
Ordering Information and Valid Combination tables	Updated options to include 128 Mb pSRAM device
Block Diagram	Changed chip enable pin from CE#f1 to F1-CE#
Physcial Dimensions/Connection Diagrams	Replaced VBH084 with TLA084 and VSA084 Replaced VBU056 with TLC056
V_{CC} Power Up	Changed t_{VCS} speed from 30 µs to 50 µs
DC Characteristics	Changed I_{CC4} Max. to 50 µA
Revision A2 (August 18, 2005)	
Global	Removed all references to 56-ball package
Performance Characteristis	Updated the product selector tables
Ordering Information	Updated model number
Valid Combinations table	Added new ordering options
Connection Diagram	Updated the PL127N connection diagram Updated the PL12xN connection diagram
Revision A3 (October 21, 2005)	
Performance Characteristics	Updated the Typical Sector Erase times
Revision A4 (November 29, 2005)	
Global	Added the 1.2 mm option to S71PL256ND0 Updated the S29PL-N Flash data sheet
Revision A5 (January 3, 2006)	
Global	Changed the name of in F3 from A14 to A4 in pinout figure of section 3.2 Removed all references to Type 6 pSRAMs from the Product Selector Guide Added a document reference table Modified the Package Type and Material options Removed the VSA084 package option Removed the datasheet from the MCP wrapper
Revision A6 (April 12, 2006)	
Global	Added pSRAM Type 7 as an option to S71PL127NB0 and S71PL129NB0
Revision A7 (September 6, 2006)	
Global	Updated document to new template.
Revision A8 (October 6, 2006)	
Global	Added 32 Mb pSRAM Type 8 to the valid combinations
Revision A9 (December 8, 2006)	
Global	Added 64 Mb pSRAM Type 8 to the valid combinations.
Revision A10 (June 27, 2008)	
Global	Added OPN S71PL127NB0HHW4U
General Description	Added 32M pSRAM Type 8 (90 nm)
Ordering Information	Added Package Type & Material Set ordering option HH
Valid Combinations	Added Note 4 for parts with pSRAM Type 2 or 7

Section	Description
Revision A11 (June 9, 2010)	
General Description	Corrected 32 Mb pSRAM Type 8 (90 nm) PID to comspec_02 Clarified that PID pSRAM_32 is for 64 Mb pSRAM Type 8 (130 nm) Added PID SPH064D970R1R for 64 Mb pSRAM Type 8 (90 nm)
Product Selector Guide	Clarified that pSRAM Type 8 may be of either 90 nm or 130 nm node for both 32 and 64 Mb
Valid Combinations	Added Note 5 for MCPs with pSRAM Type 8 (90 nm) Added Note 4 to all PL129N and PL256N MCP combinations

Colophon

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