FLASH AND CellularRAM™ COMBO MEMORY

MT28C64416W18/W30A (ADVANCE‡‡)
MT28C64432W18/W30A
MT28C64464W18/W30A

Low Voltage, Wireless Temperature

Features

Stacked die Combo package
- Includes one 64Mb Flash device
- Choice of either 16Mb, 32Mb, or 64Mb Cellular-RAM™ device

Basic configuration

Flash
- Flexible multibank architecture
- 4 Meg x 16 Async/Page/Burst interface
- Support for true concurrent operations with no latency

CellularRAM
- Low-power, high-density design
- 1 Meg x 16, 2 Meg x 16, or 4 Meg x 16 configurations
- Async/Page

F_VCC, VCCQ, F_VPP, C_VCC voltages
- 1.70V (MIN)/1.95V (MAX) F_VCC, C_VCC
- 1.70V (MIN)/2.24V (MAX) VCCQ (W18)
- 2.20V (MIN)/3.30V(MAX) VCCQ (W30)
- 1.80V (TYP) F_VPP (in-system PROGRAM/ERASE)
- 12V ±5% (HV) F_VPP tolerant (factory programming compatibility)

Fast programming Algorithm (FPA)

Enhanced suspend options
- ERASE-SUSPEND-to-READ within same bank
- PROGRAM-SUSPEND-to-READ within same bank
- ERASE-SUSPEND-to-PROGRAM within same bank

Flash device contains two 64-bit chip protection registers for security purposes

100,000 ERASE cycles per block

Cross-compatible command set support
- Extended command set
- Common Flash interface (CFI) compliant

Manufacturer's Identification Code (ManID)
- Micron®
- Intel®

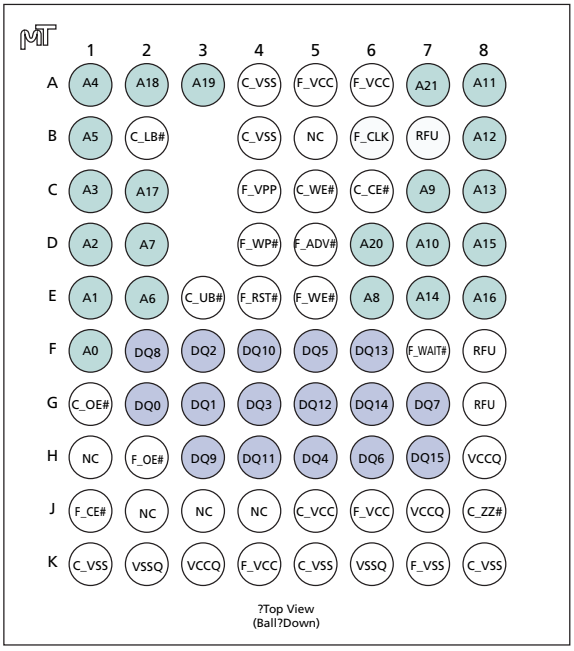
††MT28C64416W18/W30A is advance status.

Options

Flash Timing
- 60ns[1] (W18)
- 70ns (W18/W30)

Flash Burst Frequency
- 66 MHz[1] (W18)
- 54 MHz (W18/W30)

Figure 1: 77-Ball FBGA



NOTE:

Balls B6, D5, and F7 are only used for Flash burst operation.

Flash Boot Block Configuration

Top

Bottom

CellularRAM Timing
- 70ns
- 85ns

I/O Voltage Range
- VccQ 1.70V–2.24V (W18)
- VccQ 2.20V–3.30V (W30)

Manufacturer's Identification Code (ManID)
- Micron (0x2Ch)
- Intel (0x89h)

Operating Temperature Range
- Wireless Temperature (-25°C to +85°C)

Package
- 77-ball (Standard) FBGA 8 x 10 grid
- 77-ball (Lead-free) FBGA 8 x 10 grid[2]

NOTE: 1. Contact factory for availability.
2. Contact factory for details.

Table of Contents

List of Figures

List of Tables

Device General Description

The MT28C64416W18/W30A, MT28C64432W18/W30A, and MT28C64464W18/W30A combination Flash and CellularRAM are high-performance, high-density, memory solutions that can significantly improve system performance. This memory solution is comprised of one 64Mb Flash device and one 16Mb, 32Mb, or 64Mb CellularRAM device.

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets.

For all asyncronous/page Flash devices, the burst mode specifications in the referenced Flash discrete data sheet should be ignored, as they do not pertain to asyncronous/page mode operation.

Flash General Description

The Flash architecture features a multipartition configuration that supports READ-while-PROGRAM/ERASE operations with no latency. A 4Mb partition size enables optimal design flexibility.

The Flash device enables soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, one user-programmable 64-bit chip protection register is provided for the Flash device.

The embedded WORD PROGRAM and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip device status register can be used to monitor the WSM status and determine the progress of the PROGRAM/ERASE tasks.

The Flash device has a read configuration register (RCR) that defines how the Flash interacts with the memory bus. For device specifications and additional documentation concerning Flash features, please refer to the MT28F644W18/W30 data sheet at www.micron.com/flash.

Flash Configurations

The Flash memory implements a multibank architecture (16 banks of 4Mb each) to allow concurrent operations. Any address within a block address range selects that block for the required READ, PROGRAM, or ERASE operation.

The Flash memory features eight 4K-word sectors (8 x 65,536 bits), designated as parameter blocks, and the remaining part is organized in main blocks of 32K words each (524,288 bits). The parameter blocks are addressed either by the low order addresses (bottom boot) or by the higher order addresses (top boot).

CellularRAM General Description

The CellularRAM architecture features high-speed CMOS, dynamic random-access memories developed for low-power portable applications The CellularRAM device is available in either 16Mb, 32Mb, or 64Mb densities.

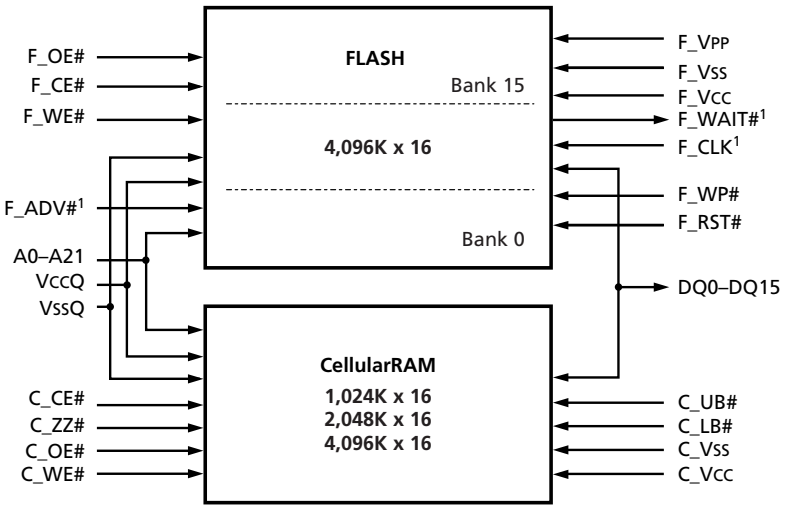
To operate seamlessly on a burst Flash bus, CellularRAM products have incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

The configuration register (CR) is used to control how refresh is performed on the CellularRAM array. These registers are automatically loaded with default settings during power-up and can be updated any time during normal operation. Special attention has been focused on standby current consumption during self-refresh.

CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial array refresh (PAR) limits refresh to the portion of the memory array being used. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the ambient temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Deep power down (DPD) halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are adjusted through the configuration register (CR) .

For device specifications and additional documentation concerning CellularRAM, please refer to the MT45W1MW16PAFA, MT45W2MW16PFA, MT45W1ML16PAFA, MT45W2ML16PFA, MT45W4MW16PFA, and MT45W4ML16PFA CellularRAM data sheets at www.micron.com/cellularram.

Figure 2: Block Diagram

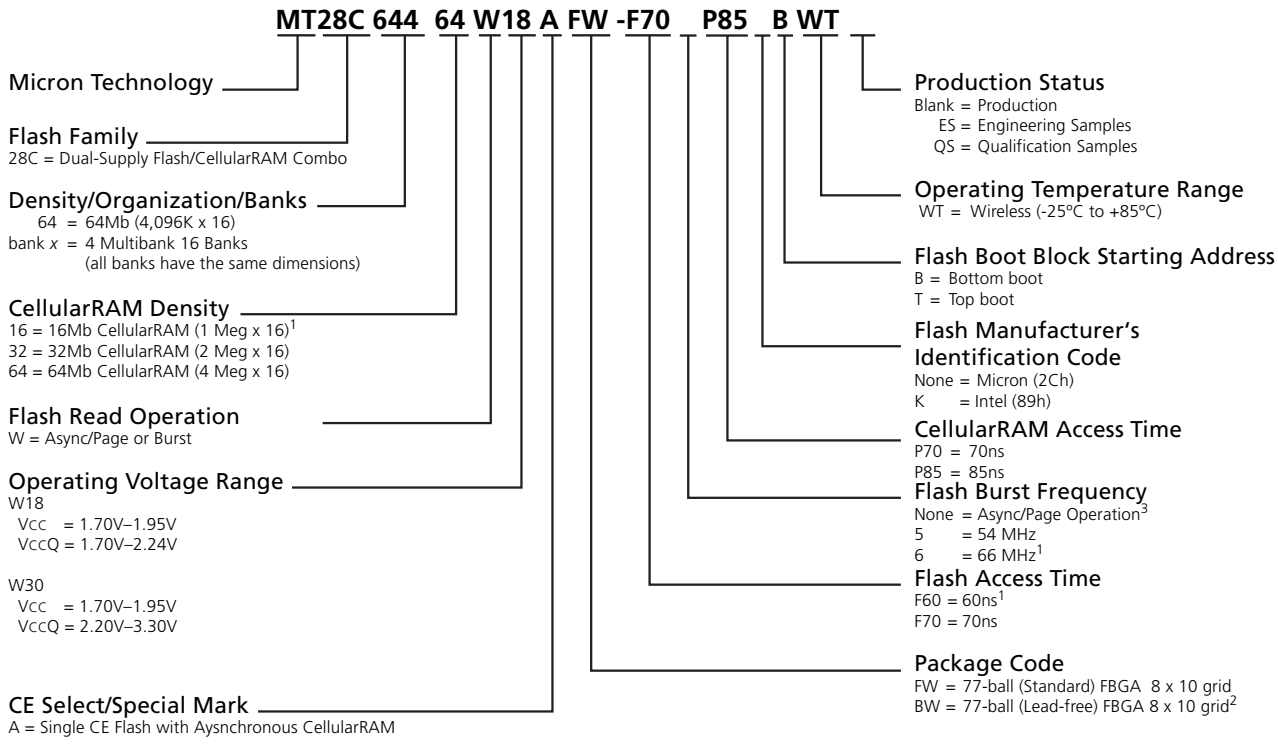


NOTE:
1. For Flash burst operation only.

Part Numbering Information

Micron's combination memory devices are available with several different combinations of features (see Figure 3).

Figure 3: Part Number Chart



NOTE:
1. Contact factory for availabilty.
2. Contact factory for details.
3. Burst mode specifications in the referenced Flash discrete data sheet are not guaranteed.

Valid Part Number Combinations

After building the part number from the part number chart above, please go to Micron's Part Marking Decoder Web site at www.micron.com/decoder to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/decoder. To view the location of the abbreviated mark on the device, please refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

Table 1: Ball Descriptions

77-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTIONS
F1, E1, D1, C1, A1, B1, E2, D2, E6, C7, D7, A8, B8, C8, E7, D8, E8, C2, A2, A3, D6, A7	A0–A21	Input	Addresses: Flash: A0–A21. CellularRAM: A0–A19 (16Mb). CellularRAM: A0–A20 (32Mb). CellularRAM: A0–A21 (64Mb).
J1	F_CE#	Input	Flash Chip Enable.
H2	F_OE#	Input	Flash Output Enable.
E5	F_WE#	Input	Flash Write Enable.
D4	F_WP#	Input	Flash Write Protect.
D5	F_ADV#	Input	Flash Address Valid (burst operation only)[1].
B6	F_CLK	Input	Flash Clock (burst operation only)[2].
E4	F_RST#	Input	Flash Reset.
B2	C_LB#	Input	CellularRAM Lower Byte Control.
E3	C_UB#	Input	CellularRAM Upper Byte Control.
C5	C_WE#	Input	CellularRAM Write Enable.
G1	C_OE#	Input	CellularRAM Output Enable.
C6	C_CE#	Input	CellularRAM Chip Enable.
J8	C_ZZ#	Input	CellularRAM Deep Sleep Mode and Configuration Mode.
G2, G3, F3, G4, H5, F5, H6, G7, F2, H3, F4, H4, G5, F6, G6, H7	DQ0–DQ15	I/O	Flash/CellularRAM Data Input/Output.
F7	F_WAIT#	Output	Flash WAIT# (burst operation only)[3]. See "WAIT Ball Operation" on page 9.
K7	F_VSS	Supply	Flash Core Ground.
C4	F_VPP	Supply	Flash VPP.
A5, A6, J6, K4	F_VCC	Supply	Flash Core Power Supply.
A4, B4, K1, K5, K8	C_VSS	Supply	CellularRAM Core Ground.
J5	C_VCC	Supply	CellularRAM Core Power Supply.
H8, J7, K3	VCCQ	Supply	Flash/CellularRAM I/O Supply.
K2, K6	VSSQ	Supply	Flash/CellularRAM I/O Ground.
B5, H1, J2, J3, J4	NC	–	No Connect. Not internally connected to the die.
B3, C3, D3	RFU	–	Ball not Mounted. Reserved for Future Use (A23, A24, A25).
B7	RFU	–	Reserved for Future Use (A22).
F8	RFU	–	Reserved for Future Use (F_CE2#).
G8	RFU	–	Reserved for Future Use (F_OE2#).

NOTE:
1. Tie this ball to VSS for Flash asynchronous/page non-latched operation. For latched operation, please refer to the Flash discrete data sheet.
2. Tie this ball to VSS or VCC for Flash asynchronous/page operation.
3. Do not use (DNU) for Flash asynchronous/page operation.

MultiChip Packaging Considerations

Multichip packaging presents unique challenges when controlling complex memory devices.

The MT28C64416W18/W30A, MT28C64432W18/W30A, and MT28C644644W18/W30A devices combine one Micron Flash device with a single CellularRAM device.

Unique IDs, State Machines, and Registers

The Flash device has a command state machine (CSM) and status register (SR) and read configuration register (RCR). The Flash device has its own OTP, CFI, and device code. Depending on the boot configuration of the device, the OTP, CFI, and device code information may differ.

The CellularRAM device has a configuration register (CR) that defines how the device performs self refresh.

WAIT Ball Operation

The WAIT ball polarity for the Flash device is configured by programming bit 10 in the read configuration register (RCR). The default setting for the WAIT ball is active LOW.

Power Consumption

Multiple chip packaging requires that power calculations consider the active operation of the Flash as well as that of the CellularRAM. Total power consumed will be the sum of the currents associated with the state of each device.

Table 2: Truth Table

		FLASH SIGNALS						CellularRAM SIGNALS					MEMORY OUTPUT	
	MODES	F_CE#	F_OE#	F_WE#	F_RST#	F_ADV#[2]	F_WAIT#[3]	C_CE#	C_ZZ#	C_OE#	C_UB/LB#	C_WE#	MEMORY BUS CONTROL	DQ0–DQ15
FLASH	Read	L	L	H	H	L	Active[1]	CellularRAM memory must be in High-Z					Flash	DOUT
	Write	L	H	L	H	X	Asserted						Flash	DIN
	Standby	H	X	X	H	X	High-Z	CellularRAM memory any mode allowable					Other	High-Z
	Output Disable	L	H	H	H	X	Active[1]						Other	High-Z
	Reset	X	X	X	L	X	High-Z						None	High-Z
CellularRAM MEMORY	Read	Flash must be in High-Z						L	H	L	L	H	Cellular RAM	DOUT
	Write							L	H	H	L	L	Cellular RAM	DIN
	Standby	Flash any mode allowable						H	H	X	X	X	Other	High-Z
	Output Disable							L	H	H	X	H	Other	High-Z
	Deep Sleep Mode							H	L	X	X	X	Other	High-Z

NOTE:

1. WAIT status is only valid for burst mode operation. WAIT should be ignored for all other operating modes.
2. Not used in asynchronous/page non-latched operation. For latched operation, please refer to the Flash discrete data sheet.
3. Not used in asynchronous/page operation.

Electrical Specifications

Table 3: Absolute Maximum Ratings

Note 1

PARAMETERS/CONDITIONS	MIN	MAX	UNITS	NOTES
Operating Temperature Range	-25	+85	°C	
Storage Temperature Range	-55	+125	°C	
Soldering Cycle		+260	°C	2

NOTE:

1. Stresses greater than those listed in Table 3 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See technical note TN-00-15, "Recommended Soldering Techniques," for more information.

Table 4: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VCC Supply Voltage (F_VCC and C_VCC)	VCC	1.70	–	1.95	V
I/O Supply Voltage	VccQ (W18)	1.70	–	2.24	V
	VccQ (W30)	2.20		3.30	

Table 5: Capacitance

T_A = +25°C; f = 1 MHz

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS
Input Capacitance	CIN	13	17	pF
Output Capacitance	COUT	18	20	pF
Clock Capacitance	CCLK	22	23	pF

Table 6: DC Characteristics

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets. All currents are in RMS unless otherwise noted.

PARAMETER	SYMBOL	W18/W30		UNITS	NOTES
		TYP	MAX		
V_{CC} Standby Current with 16Mb CellularRAM with 32Mb CellularRAM with 64Mb CellularRAM	I_{CCS}		 115 135 145	µA	4
V_{CC} Standby Current with CellularRAM Device in deep power-down mode with 16Mb CellularRAM with 32Mb CellularRAM with 64Mb CellularRAM	I_{SBZZ}	 35 35 35		µA	1, 4
V_{CC} Program Suspend Current with 16Mb CellularRAM with 32Mb CellularRAM with 64Mb CellularRAM	I_{CCWS}		 115 135 145	µA	2, 4
V_{CC} Erase Suspend Current with 16Mb CellularRAM with 32Mb CellularRAM with 64Mb CellularRAM	I_{CCES}		 115 135 145	µA	2, 4
V_{CC} Automatic Power Save Current with 16Mb CellularRAM with 32Mb CellularRAM with 64Mb CellularRAM	I_{CCAPS}		 115 135 145	µA	3, 4

NOTE:

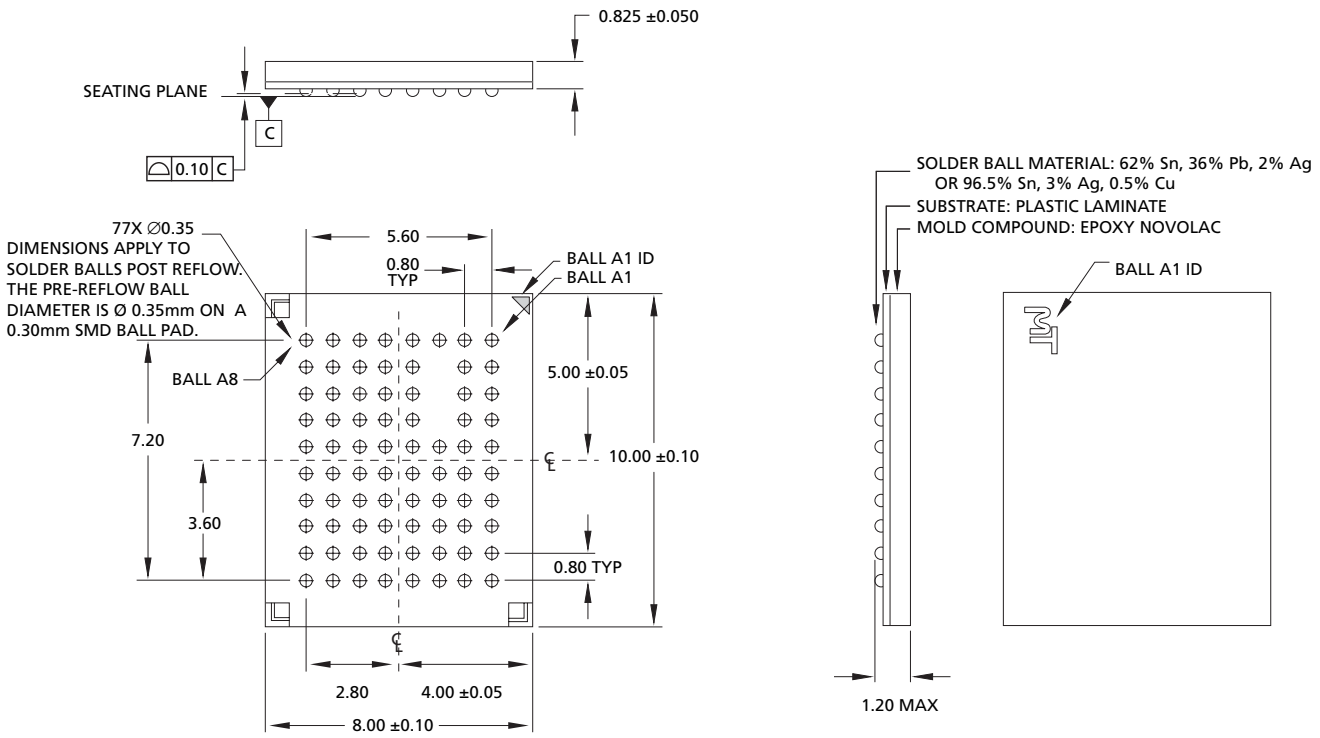
1. C_ZZ# ball LOW, CR4 bit in the CellularRAM configuration register set to zero. Measured at 25°C, this standby current is the sum of the Flash standby current and the CellularRAM deep-power down mode current.
2. I_{CCES} and I_{CCWS} values are valid when the device is deselected. Any READ operation performed while in suspend mode will have an additional current draw of suspend current.
3. Automatic power save (APS) mode reduces I_{CC} to approximately I_{CCS} levels.
4. Currents are measured using CellularRAM full array self-refresh. Currents may be further reduced by using the TCR or PAR features.

Table 7: CFI

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets.

OFFSET	DATA	DESCRIPTION
78	16Mb: 0010	CellularRAM Density
	32Mb: 0020	
	64Mb: 0040	

Figure 4: 77-Ball FBGA



NOTE:

1. All dimensions in millimeters.

Data Sheet Designation

Production: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur. Production designation applies to MT28C64432W18/W30A and MT28C644W18/W30A only.

Advance: This data sheet contains initial descriptions of products still under development. Advance designation applies to MT28C64416W18/W30A only.

For additional documentation concerning Flash and CellularRAM features, functional descriptions, programming, and timing, please refer to the table below.

Table 8: References

DEVICE	PART NUMBER	LINK
Flash	MT28F644W18/W30	www.micron.com/flash
CellularRAM	MT45W1MW16PAFA, MT45W2MW16PFA, MT45W1ML16PAFA, MT45W2ML16PFA, MT45W4MW16PFA, and MT45W4ML16PFA	www.micron.com/cellularram

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

Revision History

Rev F, Production 2/04

Rev E, Preliminary 1/04
- Updated notes on F_CLK and F_ADV balls
- Updated standby current specifications in the DC Characteristics Table

Rev D, Preliminary 11/03
- Modified the Part Numbering Chart to allow for Async/Page Flash devices

Rev C, Preliminary 11/03

Rev. B., Preview 9/03
Updated with addition of 16Mb CellularRAM

Original document, Rev. A 7/03