S71GL032A Based MCPs

Stacked Multi-Chip Product (MCP)
Flash Memory and RAM
32 Megabit (2 M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory and 16/8/4 Megabit (1M/512K/256K x 16-bit) pSRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71GL032A_00 **Revision** A **Amendment** 3 **Issue Date** August 3, 2006

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Combination

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion Inc. applies the following conditions to documents in this category:

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 2.7 V to 3.1 V**
- **High performance**
  - 100 ns (100 ns Flash, 70 ns pSRAM/SRAM)
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71GL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- **One S29GL032A Flash memory die**
- **pSRAM or SRAM**

The products covered by this document are listed in the table below:

		Flash Memory Density
		32Mb
(p)SRAM Density	4 Mb	S71GL032A40
	8 Mb	S71GL032A80/S71GL032A08
	16 Mb	S71GL032AA0

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number (PID)
S29GL-A MirrorBit™ Flash Family Data Sheet	S29GL-A_00
4 Mb pSRAM Type 4	pSRAM_18
4/8 Mb SRAM Type 1	SRAM_02
pSRAM Type 1	pSRAM_12
16 Mb pSRAM Type 7	pSRAM_13

Note:
8M pSRAM Type 4 is identical to pSRAM Type 1, which is the publication pSRAM_12.

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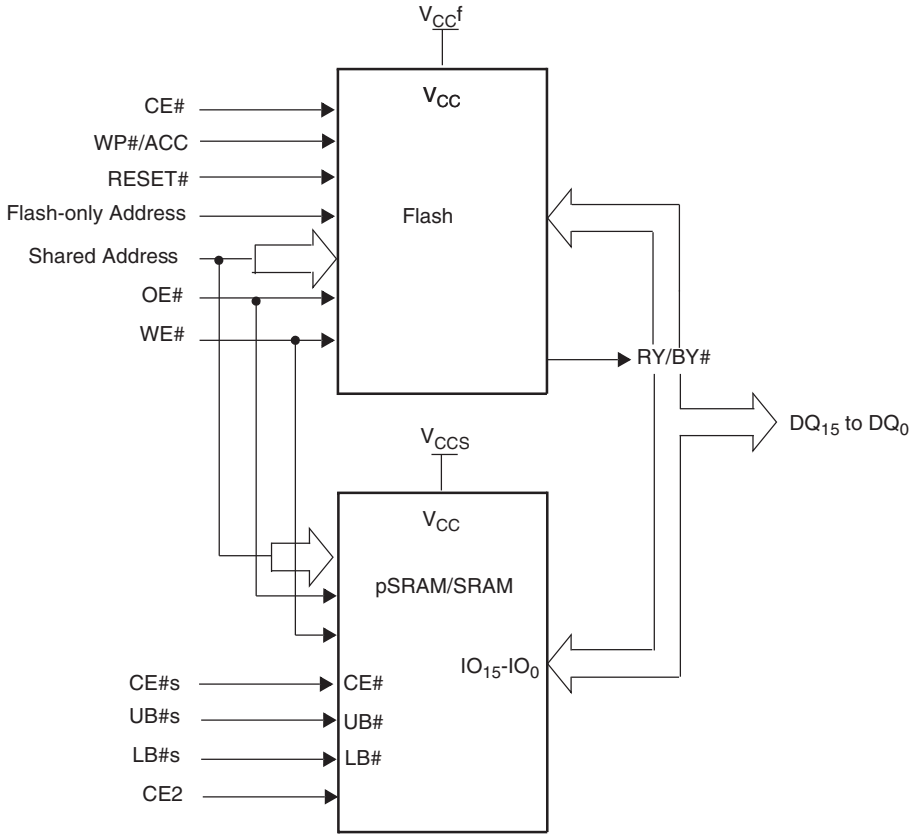
1. Product Selector Guide

1.1 32 Mb Flash Memory

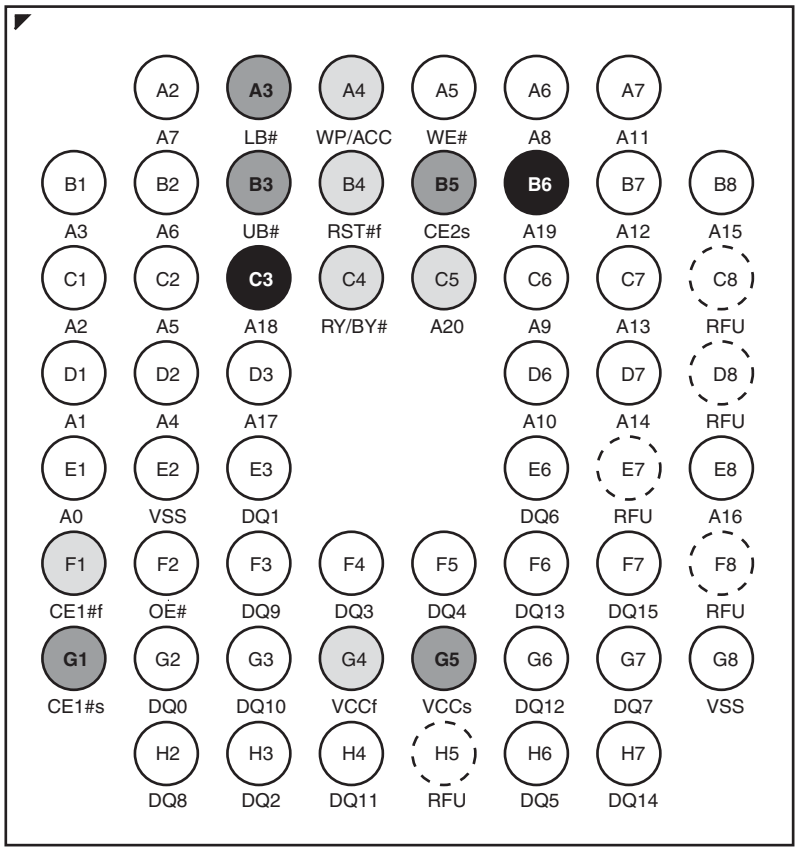
Device-Model#	(p)SRAM density	Boot Option (Discrete Model#)	pSRAM type	Package
S71GL032A40-0B	4 M pSRAM	Bottom (W4)	pSRAM4	TLC056
S71GL032A40-0F		Top (W3)		
S71GL032A08-0B	8 M SRAM	Bottom (W4)	SRAM1	
S71GL032A08-0F		Top (W3)		
S71GL032A80-0K	8 M pSRAM	Bottom (W4)	pSRAM4	
S71GL032A80-0P		Top (W3)		
S71GL032AA0-0U	16 M pSRAM	Bottom (W4)	pSRAM7	
S71GL032AA0-0Z		Top (W3)		

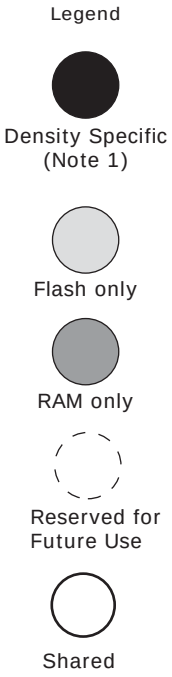
2. MCP Block Diagram



3. Connection Diagram (S71GL032A)

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)





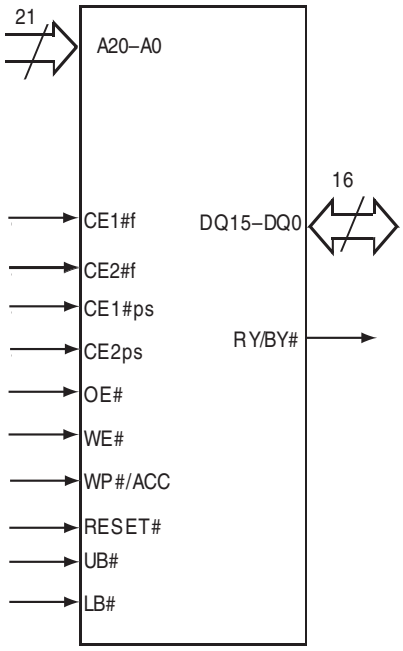
Note:
May be shared depending on density.

MCP	Flash-only Addresses	Shared Addresses
S71GL032AA0	A20	A19-A0
S71GL032A80	A20-A19	A18-A0
S71GL032A08	A20-A19	A18-A0
S71GL032A40	A20-A18	A17-A0

4. Pin Description

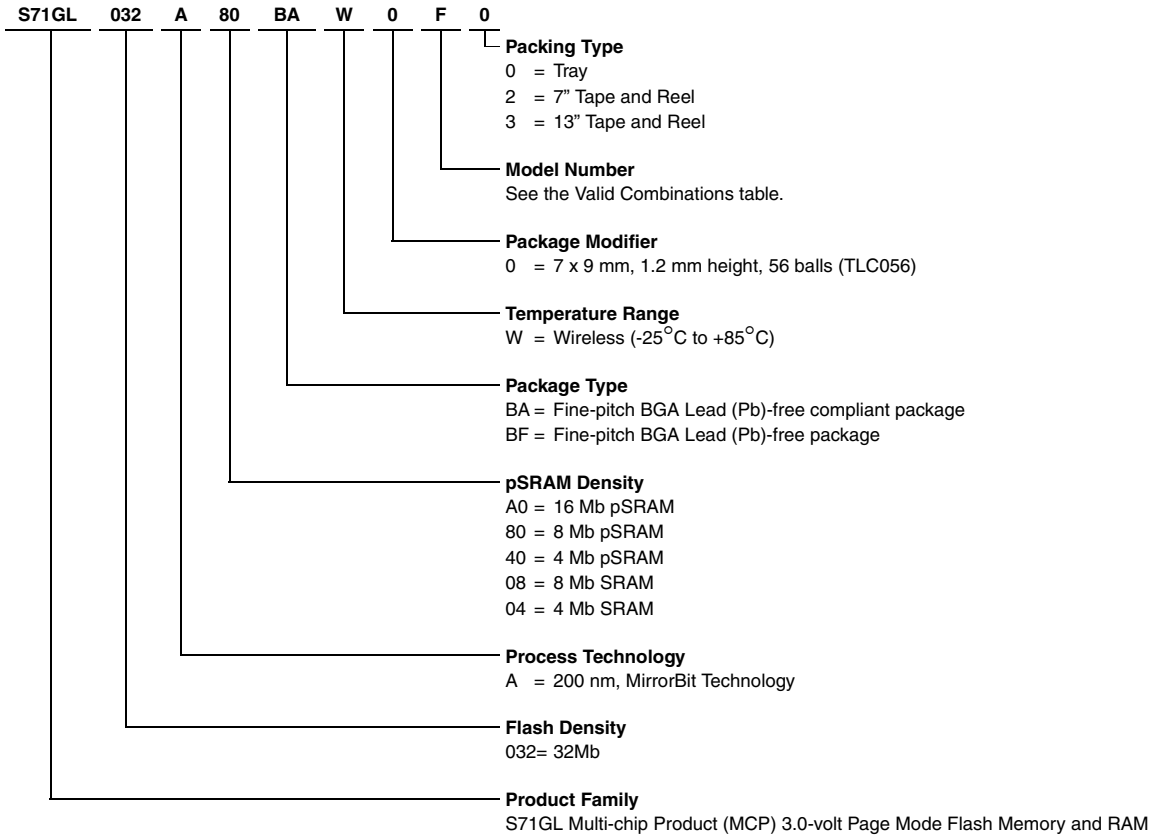
A20–A0	=	21 Address Inputs (Common and Flash only)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE#f	=	Chip Enable (Flash)
CE#ps	=	Chip Enable 1 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash 1)
UB#	=	Upper Byte Control (pSRAM/SRAM)
LB#	=	Lower Byte Control (pSRAM/SRAM)
RESET#	=	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	=	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}ps$	=	pSRAM/SRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

5. Logic Symbol



6. Ordering Information

The order number is formed by a valid combinations of the following:



6.1 Valid Combinations

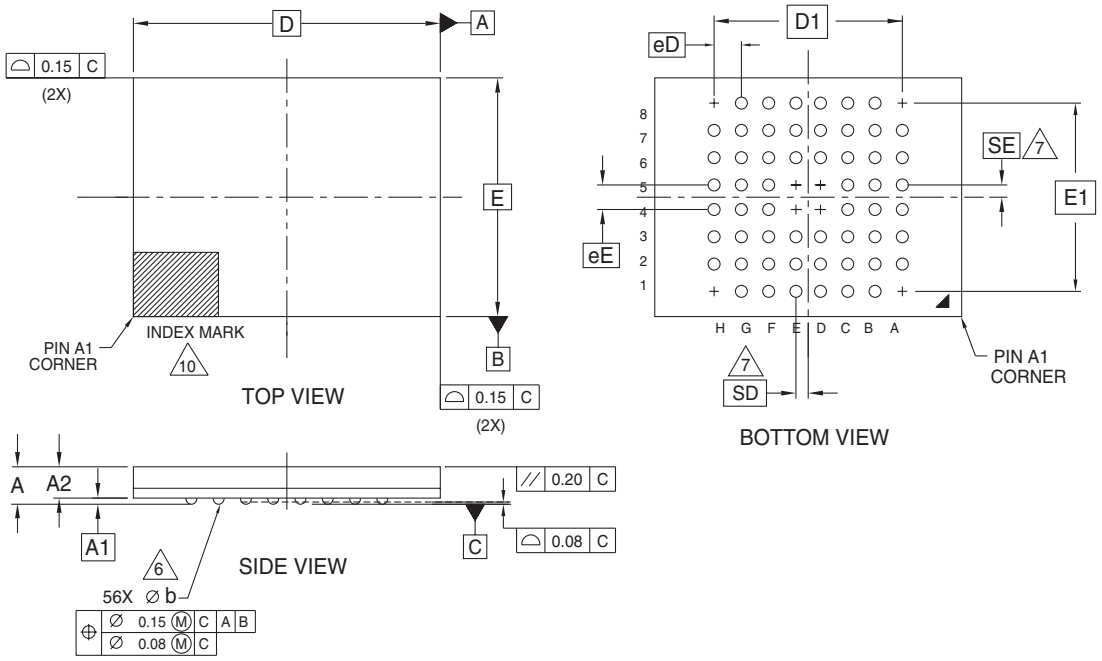
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S71GL032A Valid Combinations				Speed Options (ns)/Boot Sector Option	(p)SRAM Type/Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type			
S71GL032A40	BAW	0B	0, 2, 3 (Note)	100 / Bottom Boot Sector	pSRAM4/ 70	TLC056
S71GL032A40		0F		100 / Top Boot Sector		
S71GL032A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL032A08		0F		100 / Top Boot Sector		
S71GL032A40	BFW	0B		100 / Bottom Boot Sector	pSRAM4/ 70	
S71GL032A40		0F		100 / Top Boot Sector		
S71GL032A08		0B		100 / Bottom Boot Sector	SRAM1 / 70	
S71GL032A08		0F		100 / Top Boot Sector		
S71GL032A80	BAW	0K		100 / Bottom Boot Sector	pSRAM4/ 70	
S71GL032A80		0P		100 / Top Boot Sector		
S71GL032AA0		0U		100 / Bottom Boot Sector	pSRAM7/ 70	
S71GL032AA0		0Z		100 / Top Boot Sector		
S71GL032A80	BFW	0K		100 / Bottom Boot Sector	pSRAM4/ 70	
S71GL032A80		0P		100 / Top Boot Sector		
S71GL032AA0		0U		100 / Bottom Boot Sector	pSRAM7/ 70	
S71GL032AA0		0Z		100 / Top Boot Sector		

Note:
Type 0 is standard. Specify other options as required.

7. Physical Dimensions

Figure 7.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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8. Revision History

Section	Description
Revision A (August 5, 2005)	
	Initial release
Revision A1 (September 30, 2005)	
Global	Changed PL to GL in one line of the data sheet. Updated the flash module.
Revision A2 (March 21, 2006)	
Global	Added following MCPs: S71GL032J80-0K/0P and S71GL032JA0-0U/0Z Included references to discrete model# W3 & W4 to explicitly map the MCP boot types and voltage ranges to the exact specifications Removed Industrial temperature from the part# offerings Modularized MCP and added cross-reference table to relevant documents
Revision A3 (August 3, 2006)	
Valid Combinations Table	OPNs of pSRAM type 7 corrected to 0U/0Z

Colophon

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