4 MEG x 16 ASYNCHRONOUS/PAGE FLASH
512K x 16 SRAM COMBO MEMORY

FLASH AND SRAM COMBO MEMORY

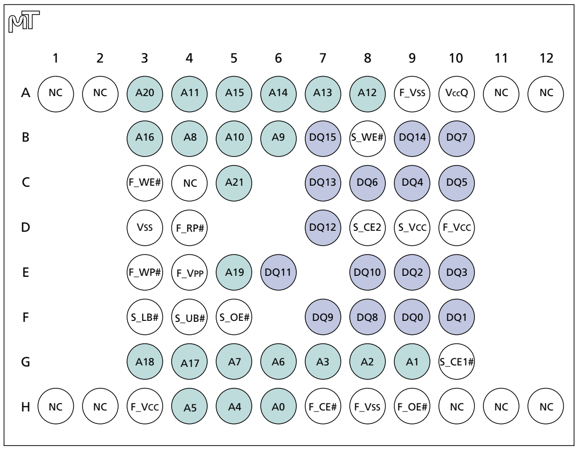
MT28C6428P20
MT28C6428P18

Low Voltage, Extended Temperature
0.18µm Process Technology

FEATURES

- Flexible dual-bank architecture
- Support for true concurrent operations with no latency:
  Read bank *b* during program bank *a* and vice versa
  Read bank *b* during erase bank *a* and vice versa
- Organization: 4,096K x 16 (Flash)
  512K x 16 (SRAM)
- Basic configuration:
  Flash
  Bank *a* (16Mb Flash for data storage)
  – Eight 4K-word parameter blocks
  – Thirty-one 32K-word blocks
  Bank *b* (48Mb Flash for program storage)
  – Ninety-six 32K-word main blocks
  SRAM
  8Mb SRAM for data storage
  – 512K-words
- F_Vcc, VccQ, F_Vpp, S_Vcc voltages
  MT28C6428P20
  1.80V (MIN)/2.20V (MAX) F_Vcc read voltage
  1.80V (MIN)/2.20V (MAX) S_Vcc read voltage
  1.80V (MIN)/2.20V (MAX) VccQ
  MT28C6428P18
  1.70V (MIN)/1.90V (MAX) F_Vcc read voltage
  1.70V (MIN)/1.90V (MAX) S_Vcc read voltage
  1.70V (MIN)/1.90V (MAX) VccQ
  MT28C6428P20/P18
  1.80V (TYP) F_Vpp (in-system PROGRAM/ERASE)
  1.0V (MIN) S_Vcc (SRAM data retention)
  12V ±5% (HV) F_Vpp (in-house programming and accelerated programming algorithm [APA] activation)
- Asynchronous access time
  Flash access time: 80ns @ 1.80V F_Vcc
  SRAM access time: 80ns @ 1.80V S_Vcc
- Page Mode read access
  Interpage read access: 80ns @ 1.80V F_Vcc
  Intrapage read access: 30ns @ 1.80V F_Vcc
- Low power consumption
- Enhanced suspend options
  ERASE-SUSPEND-to-READ within same bank
  PROGRAM-SUSPEND-to-READ within same bank
  ERASE-SUSPEND-to-PROGRAM within same bank
- Read/Write SRAM during program/erase of Flash

BALL ASSIGNMENT
67-Ball FBGA (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	A20	A11	A15	A14	A13	A12	F_Vss	VccQ	NC	NC
B			A16	A8	A10	A9	DQ15	S_WE#	DQ14	DQ7		
C			F_WE#	NC	A21		DQ13	DQ6	DQ4	DQ5		
D			Vss	F_RP#			DQ12	S_CE2	S_Vcc	F_Vcc		
E			F_WP#	F_Vpp	A19	DQ11		DQ10	DQ2	DQ3		
F			S_LB#	S_UB#	S_OE#		DQ9	DQ8	DQ0	DQ1		
G			A18	A17	A7	A6	A3	A2	A1	S_CE1#		
H	NC	NC	F_Vcc	A5	A4	A0	F_CE#	F_Vss	F_OE#	NC	NC	NC

Top View
(Ball Down)

- Dual 64-bit chip protection registers for security purposes
- PROGRAM/ERASE cycles
  100,000 WRITE/ERASE cycles per block
- Cross-compatible command set support
  Extended command set
  Common flash interface (CFI) compliant

OPTIONS	MARKING
• Timing	
80ns	-80
85ns	-85
• Boot Block Configuration	
Top	T
Bottom	B
• Operating Voltage Range	
F_Vcc = 1.70V–1.90V	18
F_Vcc = 1.80V–2.20V	20
• Operating Temperature Range	
Commercial (0ºC to +70ºC)	None
Extended (-40ºC to +85ºC)	ET
• Package	
67-ball FBGA (8 x 8 grid)	FM

Part Number Example:

MT28C6428P20FM-80 BET

GENERAL DESCRIPTION

The MT28C6428P20 and MT28C6428P18 combination Flash and SRAM memory devices provide a compact, low-power solution for systems where PCB real estate is at a premium. The dual-bank Flash devices are high-performance, high-density, nonvolatile memory with a revolutionary architecture that can significantly improve system performance.

This new architecture features:

- A two-memory-bank configuration supporting dual-bank operation;
- A high-performance bus interface providing a fast page data transfer; and
- A conventional asynchronous bus interface.

The devices also provide soft protection for blocks by configuring soft protection registers with dedicated command sequences. For security purposes, dual 64-bit chip protection registers are provided.

The embedded WORD WRITE and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). The WSM simplifies these operations and relieves the system processor of secondary tasks. An on-chip status register, one for each bank, can be used to monitor the WSM status to determine the progress of a PROGRAM/ERASE command.

The erase/program suspend functionality allows compatibility with existing EEPROM emulation software packages.

The devices take advantage of a dedicated power source for the Flash memory (F_VCC) and a dedicated power source for the SRAM (S_VCC), both at 1.70V–2.20V for optimized power consumption and improved noise immunity. A dedicated I/O power supply (VCCQ) is provided with an extended range (1.70V–2.20V), to allow a direct interface to most common logic controllers and to ensure improved noise immunity. The separate S_VCC pin for the SRAM provides data retention capability when required. The data retention S_VCC is specified as low as 1.0V. The MT28C6428P20 and MT28C6428P18 devices support two F_VPP voltage ranges, an in-circuit voltage of 0.9V–2.2V and a production compatibility voltage of 12V ±5%. The 12V ±5% F_VPP2 is supported for a maximum of 100 cycles and 10 cumulative hours.

The MT28C6428P20 and MT28C6428P18 contain an asynchronous 8Mb SRAM organized as 512K-words by 16 bits. The devices are fabricated using an advanced CMOS process and high-speed/ultra-low-power circuit technology, and then are packaged in a 67-ball FBGA package with 0.80mm pitch.

ARCHITECTURE AND MEMORY ORGANIZATION

The Flash devices contain two separate banks of memory (bank *a* and bank *b*) for simultaneous READ and WRITE operations, which are available in the following bank segmentation configuration:

- Bank *a* comprises one-fourth of the memory and contains 8 x 4K-word parameter blocks, while the remainder of bank *a* is split into 31 x 32K-word blocks.
- Bank *b* represents three-fourths of the memory, is equally sectored, and contains 96 x 32K-word blocks.

Figures 2 and 3 show the bottom and top memory organizations.

DEVICE MARKING

Due to the size of the package, Micron's standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross referenced to Micron part numbers in Table 1.

Table 1
Cross Reference for Abbreviated Device Marks

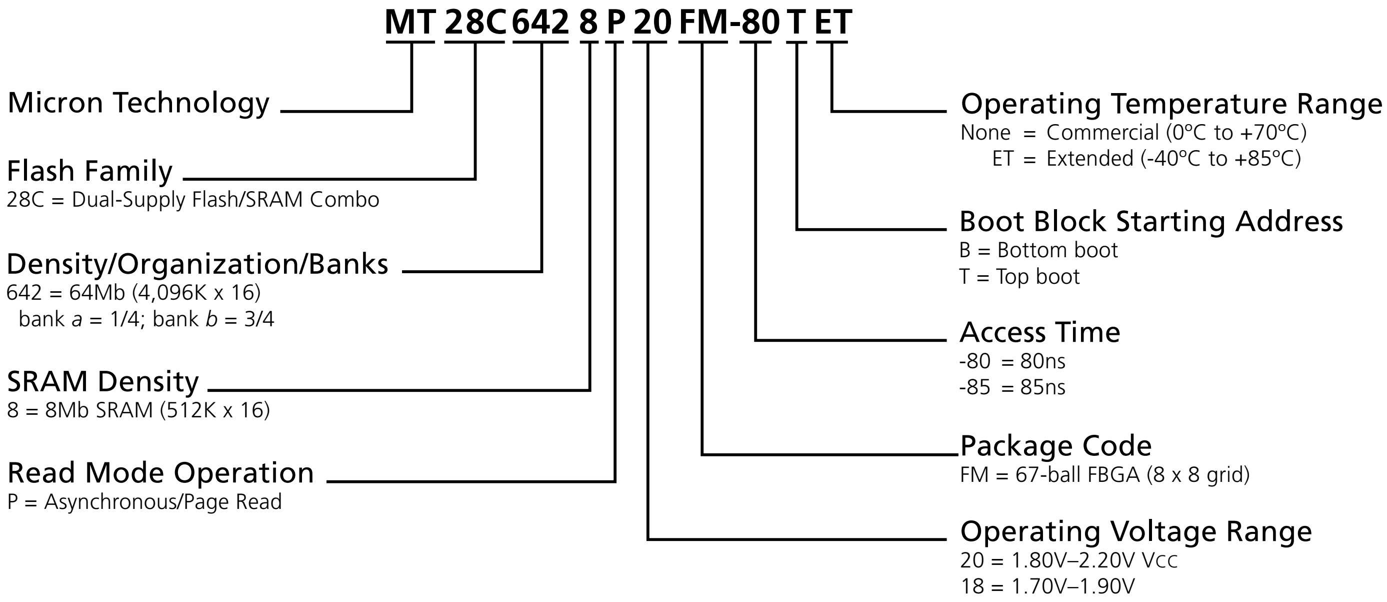
PART NUMBER	PRODUCT MARKING	SAMPLE MARKING	MECHANICAL SAMPLE MARKING
MT28C6428P20FM-80 BET	FW454	FX454	FY454
MT28C6428P20FM-80 TET	FW453	FX453	FY453
MT28C6428P18FM-85 BET	FW455	FX455	FY455
MT28C6428P18FM-85 TET	FW452	FX452	FY452

PART NUMBERING INFORMATION

Micron's low-power devices are available with several different combinations of features (see Figure 1).

Valid combinations of features and their corresponding part numbers are listed in Table 2.

Figure 1
Part Number Chart



MT 28C 642 8 P 20 FM-80 T ET

Micron Technology

Flash Family
28C = Dual-Supply Flash/SRAM Combo

Density/Organization/Banks
642 = 64Mb (4,096K x 16)
bank *a* = 1/4; bank *b* = 3/4

SRAM Density
8 = 8Mb SRAM (512K x 16)

Read Mode Operation
P = Asynchronous/Page Read

Operating Temperature Range
None = Commercial (0°C to +70°C)
ET = Extended (-40°C to +85°C)

Boot Block Starting Address
B = Bottom boot
T = Top boot

Access Time
-80 = 80ns
-85 = 85ns

Package Code
FM = 67-ball FBGA (8 x 8 grid)

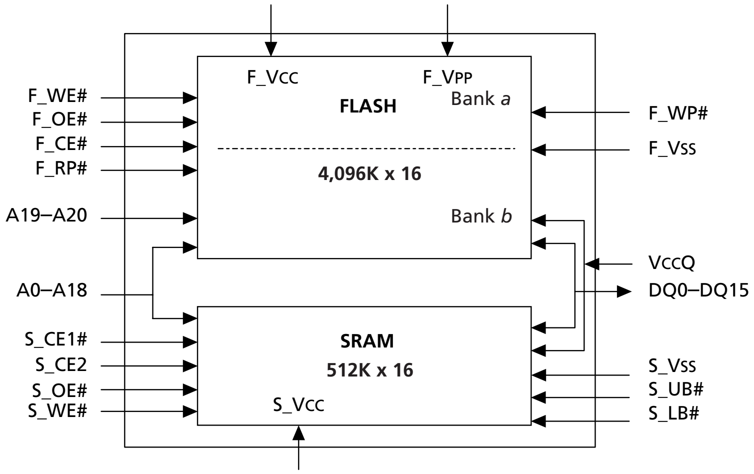
Operating Voltage Range
20 = 1.80V–2.20V Vcc
18 = 1.70V–1.90V

Table 2
Valid Part Number Combinations[1]

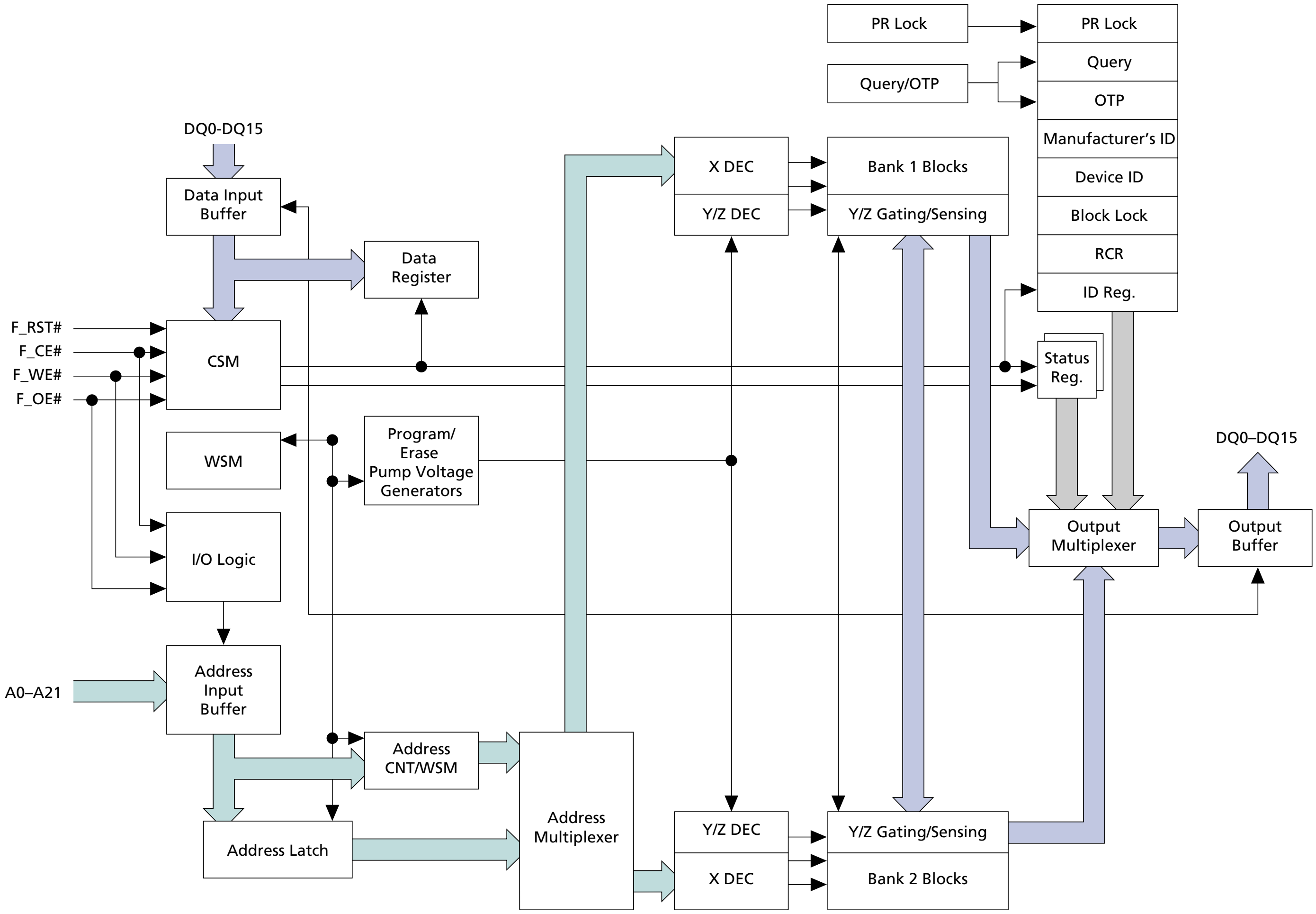
PART NUMBER	ACCESS TIME (ns)	BOOT BLOCK STARTING ADDRESS	OPERATING TEMPERATURE RANGE
MT28C6428P20FM-80 BET	80	Bottom	-40°C to +85°C
MT28C6428P20FM-80 TET	80	Top	-40°C to +85°C
MT28C6428P18FM-85 BET	85	Bottom	-40°C to +85°C
MT28C6428P18FM-85 TET	85	Top	-40°C to +85°C

NOTE: 1. For part number combinations not listed in this table, please contact your Micron representative.

BLOCK DIAGRAM



FLASH FUNCTIONAL BLOCK DIAGRAM



BALL DESCRIPTIONS

67-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
H6, G9, G8, G7, H5, H4, G6, G5, B4, B6, B5, A4, A8, A7, A6, A5, B3, G4, G3, E5, A3, C5	A0–A21	Input	Address Inputs: Inputs for the addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. Flash: A0–A21; SRAM: A0–A18.
H7	F_CE#	Input	Flash Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
H9	F_OE#	Input	Flash Output Enable: Enables Flash output buffers when LOW. When F_OE# is HIGH, the output buffers are disabled.
C3	F_WE#	Input	Flash Write Enable: Determines if a given cycle is a Flash WRITE cycle. F_WE# is active LOW.
D4	F_RP#	Input	Reset. When F_RP# is a logic LOW, the device is in reset, which drives the outputs to High-Z and resets the WSM. When F_RP# is a logic HIGH, the device is in standard operation. When F_RP# transitions from logic LOW to logic HIGH, the device resets all blocks to locked and defaults to the read array mode.
E3	F_WP#	Input	Flash Write Protect. Controls the lock down function of the flexible locking feature.
G10	S_CE1#	Input	SRAM Chip Enable1: Activates the SRAM when it is LOW. HIGH level deselects the SRAM and reduces the power consumption to standby levels.
D8	S_CE2	Input	SRAM Chip Enable2: Activates the SRAM when it is HIGH. LOW level deselects the SRAM and reduces the power consumption to standby levels.
F5	S_OE#	Input	SRAM Output Enable: Enables SRAM output buffers when LOW. When S_OE# is HIGH, the output buffers are disabled.
B8	S_WE#	Input	SRAM Write Enable: Determines if a given cycle is an SRAM WRITE cycle. S_WE# is active LOW.
F3	S_LB#	Input	SRAM Lower Byte: When LOW, it selects the SRAM address lower byte (DQ0–DQ7).
F4	S_UB#	Input	SRAM Upper Byte: When LOW, it selects the SRAM address upper byte (DQ8–DQ15).
F9, F10, E9, E10, C9, C10, C8, B10, F8, F7, E8, E6, D7, C7, B9, B7	DQ0–DQ15	Input/ Output	Data Inputs/Outputs: Input array data on the second CE# and WE# cycle during PROGRAM command. Input commands to the command user interface when CE# and WE# are active. Output data when CE# and OE# are active.

(continued on next page)

BALL DESCRIPTIONS (continued)

67-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
E4	F_VPP	Input/ Supply	Flash Program/Erase Power Supply: [0.9V–2.2V or 11.4V–12.6V]. Operates as input at logic levels to control complete device protection. Provides backward compatibility for factory programming when driven to 11.4V–12.6V. A lower F_VPP voltage range (0.0V–2.2V) is available. Contact factory for more information.
D10, H3	F_VCC	Supply	Flash Power Supply: [1.70V–1.90V or 1.80V–2.20V]. Supplies power for device operation.
A9, H8	F_VSS	Supply	Flash Specific Ground: Do not float any ground ball.
D9	S_VCC	Supply	SRAM Power Supply: [1.70V–1.90V or 1.80V–2.20V]. Supplies power for device operation.
D3	S_VSS	Supply	SRAM Specific Ground: Do not float any ground ball.
A10	VCCQ	Supply	I/O Power Supply: [1.70–1.90V or 1.80V–2.20V].
A1, A2, A11, A12, C4, H1, H2, H10, H11, H12	NC	–	No Connect: Lead is not internally connected; it may be driven or floated.
C6, D5, D6, E7, F6	–	–	Contact balls not mounted; corresponding position on PCB can be used to reduce routing complexity.

TRUTH TABLE – FLASH

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read	H	L	L	H	SRAM must be High-Z						Flash	DOUT	1, 2, 3
Write	H	L	H	L							Flash	DIN	1
Standby	H	H	X	X	SRAM any mode allowable						Other	High-Z	4
Output Disable	H	L	H	H							Other	High-Z	4, 5
Reset	L	X	X	X							Other	High-Z	4, 6

TRUTH TABLE – SRAM

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read	Flash must be High-Z												
DQ0–DQ15					L	H	L	H	L	L	SRAM	DOUT	1, 3
DQ0–DQ7					L	H	L	H	H	L	SRAM	DOUT LB	7
DQ8–DQ15					L	H	L	H	L	H	SRAM	DOUT UB	8
Write													
DQ0–DQ15					L	H	H	L	L	L	SRAM	DIN	1, 3
DQ0–DQ7					L	H	H	L	H	L	SRAM	DIN LB	9
DQ8–DQ15					L	H	H	L	L	H	SRAM	DIN UB	10
Standby	Flash any mode allowable				H	X	X	X	X	X	Other	High-Z	4
					X	L	X	X	X	X	Other	High-Z	4
Output Disable					L	H	X	X	X	X	Other	High-Z	4

NOTE:
1. Two devices may not drive the memory bus at the same time.
2. Allowable Flash read modes include read array, read query, read configuration, and read status.
3. Outputs are dependent on a separate device controlling bus outputs.
4. Modes of the Flash and SRAM can be interleaved so that while one is disabled, the other controls outputs.
5. SRAM is enabled and/or disabled with the logical function: S_CE1# or S_CE2.
6. Simultaneous operations can exist, as long as the operations are interleaved such that only one device attempts to control the bus outputs at a time.
7. Data output on lower byte only; upper byte High-Z.
8. Data output on upper byte only; lower byte High-Z.
9. Data input on lower byte only.
10. Data input on upper byte only.

Figure 2
Bottom Boot Block Device

Bank *b* = 48Mb		
Block	Block Size (K-bytes/ K-words)	Address Range (x16)
134	64/32	3F8000h–3FFFFFh
133	64/32	3F0000h–3F7FFFh
132	64/32	3E8000h–3EFFFFh
131	64/32	3E0000h–3E7FFFh
130	64/32	3D8000h–3DFFFFh
129	64/32	3D0000h–3D7FFFh
128	64/32	3C8000h–3CFFFFh
127	64/32	3C0000h–3C7FFFh
126	64/32	3B8000h–3BFFFFh
125	64/32	3B0000h–3B7FFFh
124	64/32	3A8000h–3AFFFFh
123	64/32	3A0000h–3A7FFFh
122	64/32	398000h–39FFFFh
121	64/32	390000h–397FFFh
120	64/32	388000h–38FFFFh
119	64/32	380000h–387FFFh
118	64/32	378000h–37FFFFh
117	64/32	370000h–377FFFh
116	64/32	368000h–36FFFFh
115	64/32	360000h–367FFFh
114	64/32	358000h–35FFFFh
113	64/32	350000h–357FFFh
112	64/32	348000h–34FFFFh
111	64/32	340000h–347FFFh
110	64/32	338000h–33FFFFh
109	64/32	330000h–337FFFh
108	64/32	328000h–32FFFFh
107	64/32	320000h–327FFFh
106	64/32	318000h–31FFFFh
105	64/32	310000h–317FFFh
104	64/32	308000h–30FFFFh
103	64/32	300000h–307FFFh
102	64/32	2F8000h–2FFFFFh
101	64/32	2F0000h–2F7FFFh
100	64/32	2E8000h–2EFFFFh
99	64/32	2E0000h–2E7FFFh
98	64/32	2D8000h–2DFFFFh
97	64/32	2D0000h–2D7FFFh
96	64/32	2C8000h–2CFFFFh
95	64/32	2C0000h–2C7FFFh
94	64/32	2B8000h–2BFFFFh
93	64/32	2B0000h–2B7FFFh
92	64/32	2A8000h–2AFFFFh
91	64/32	2A0000h–2A7FFFh
90	64/32	298000h–29FFFFh
89	64/32	290000h–297FFFh
88	64/32	288000h–28FFFFh
87	64/32	280000h–287FFFh

Bank *b* = 48Mb		
Block	Block Size (K-bytes/ K-words)	Address Range (x16)
86	64/32	278000H–27FFFFh
85	64/32	270000h–277FFFh
84	64/32	268000h–26FFFFh
83	64/32	260000h–267FFFh
82	64/32	258000h–25FFFFh
81	64/32	250000h–257FFFh
80	64/32	248000h–24FFFFh
79	64/32	240000h–247FFFh
78	64/32	238000h–23FFFFh
77	64/32	230000h–237FFFh
76	64/32	228000h–22FFFFh
75	64/32	220000h–227FFFh
74	64/32	218000h–21FFFFh
73	64/32	210000h–217FFFh
72	64/32	208000h–20FFFFh
71	64/32	200000h–207FFFh
70	64/32	1F8000h–1FFFFFh
69	64/32	1F0000h–1F7FFFh
68	64/32	1E8000h–1EFFFFh
67	64/32	1E0000h–1E7FFFh
66	64/32	1D8000h–1DFFFFh
65	64/32	1D0000h–1D7FFFh
64	64/32	1C8000h–1CFFFFh
63	64/32	1C0000h–1C7FFFh
62	64/32	1B8000h–1BFFFFh
61	64/32	1B0000h–1B7FFFh
60	64/32	1A8000h–1AFFFFh
59	64/32	1A0000h–1A7FFFh
58	64/32	198000h–19FFFFh
57	64/32	190000h–197FFFh
56	64/32	188000h–18FFFFh
55	64/32	180000h–187FFFh
54	64/32	178000h–17FFFFh
53	64/32	170000h–177FFFh
52	64/32	168000h–16FFFFh
51	64/32	160000h–167FFFh
50	64/32	158000h–15FFFFh
49	64/32	150000h–157FFFh
48	64/32	148000h–14FFFFh
47	64/32	140000h–147FFFh
46	64/32	138000h–13FFFFh
45	64/32	130000h–137FFFh
44	64/32	128000h–12FFFFh
43	64/32	120000h–127FFFh
42	64/32	118000h–11FFFFh
41	64/32	110000h–117FFFh
40	64/32	108000h–10FFFFh
39	64/32	100000h–107FFFh

Bank *a* = 16Mb		
Block	Block Size (K-bytes/ K-words)	Address Range (x16)
38	64/32	0F8000h–0FFFFFh
37	64/32	0F0000h–0F7FFFh
36	64/32	0E8000h–0EFFFFh
35	64/32	0E0000h–0E7FFFh
34	64/32	0D8000h–0DFFFFh
33	64/32	0D0000h–0D7FFFh
32	64/32	0C8000h–0CFFFFh
31	64/32	0C0000h–0C7FFFh
30	64/32	0B8000h–0BFFFFh
29	64/32	0B0000h–0B7FFFh
28	64/32	0A8000h–0AFFFFh
27	64/32	0A0000h–0A7FFFh
26	64/32	098000h–097FFFh
25	64/32	090000h–097FFFh
24	64/32	088000h–087FFFh
23	64/32	080000h–087FFFh
22	64/32	078000h–07FFFFh
21	64/32	070000h–077FFFh
20	64/32	068000h–067FFFh
19	64/32	060000h–067FFFh
18	64/32	058000h–05FFFFh
17	64/32	050000h–057FFFh
16	64/32	048000h–04FFFFh
15	64/32	040000h–047FFFh
14	64/32	038000h–03FFFFh
13	64/32	030000h–037FFFh
12	64/32	028000h–02FFFFh
11	64/32	020000h–027FFFh
10	64/32	018000h–01FFFFh
9	64/32	010000h–017FFFh
8	64/32	008000h–00FFFFh
7	8/4	007000h–007FFFh
6	8/4	006000h–006FFFh
5	8/4	005000h–005FFFh
4	8/4	004000h–004FFFh
3	8/4	003000h–003FFFh
2	8/4	002000h–002FFFh
1	8/4	001000h–001FFFh
0	8/4	000000h–000FFFh

Figure 3
Top Boot Block Device

Bank *a* = 16Mb		
Block	**Block Size (K-bytes/ K-words)**	**Address Range (x16)**
134	8/4	3FF000h–3FFFFFh
133	8/4	3FE000h–3FEFFFh
132	8/4	3FD000h–3FDFFFh
131	8/4	3FC000h–3FCFFFh
130	8/4	3FB000h–3FBFFFh
129	8/4	3FA000h–3FAFFFh
128	8/4	3F9000h–3F9FFFh
127	8/4	3F8000h–3F8FFFh
126	64/32	3F0000h–3F7FFFh
125	64/32	3E8000h–3EFFFFh
124	64/32	3E0000h–3E7FFFh
123	64/32	3D8000h–3DFFFFh
122	64/32	3D0000h–3D7FFFh
121	64/32	3C8000h–3CFFFFh
120	64/32	3C0000h–3C7FFFh
119	64/32	3B8000h–3BFFFFh
118	64/32	3B0000h–3B7FFFh
117	64/32	3A8000h–3AFFFFh
116	64/32	3A0000h–3A7FFFh
115	64/32	398000h–39FFFFh
114	64/32	390000h–397FFFh
113	64/32	388000h–38FFFFh
112	64/32	380000h–387FFFh
111	64/32	378000h–37FFFFh
110	64/32	370000h–377FFFh
109	64/32	368000h–36FFFFh
108	64/32	360000h–367FFFh
107	64/32	358000h–35FFFFh
106	64/32	350000h–357FFFh
105	64/32	348000h–34FFFFh
104	64/32	340000h–347FFFh
103	64/32	338000h–33FFFFh
102	64/32	330000h–337FFFh
101	64/32	328000h–32FFFFh
100	64/32	320000h–327FFFh
99	64/32	318000h–31FFFFh
98	64/32	310000h–317FFFh
97	64/32	308000h–30FFFFh
96	64/32	300000h–307FFFh

Bank *b* = 48Mb		
Block	**Block Size (K-bytes/ K-words)**	**Address Range (x16)**
95	64/32	2F8000h–2FFFFFh
94	64/32	2F0000h–2F7FFFh
93	64/32	2E8000h–2EFFFFh
92	64/32	2E0000h–2E7FFFh
91	64/32	2D8000h–2DFFFFh
90	64/32	2D0000h–2D7FFFh
89	64/32	2C8000h–2CFFFFh
88	64/32	2C0000h–2C7FFFh
87	64/32	2B8000h–2BFFFFh
86	64/32	2B0000h–2B7FFFh
85	64/32	2A8000h–2AFFFFh
84	64/32	2A0000h–2A7FFFh
83	64/32	298000h–29FFFFh
82	64/32	290000h–297FFFh
81	64/32	288000h–28FFFFh
80	64/32	280000h–287FFFh
79	64/32	278000h–27FFFFh
78	64/32	270000h–277FFFh
77	64/32	268000h–26FFFFh
76	64/32	260000h–267FFFh
75	64/32	258000h–25FFFFh
74	64/32	250000h–257FFFh
73	64/32	248000h–24FFFFh
72	64/32	240000h–247FFFh
71	64/32	238000h–23FFFFh
70	64/32	230000h–237FFFh
69	64/32	228000h–22FFFFh
68	64/32	220000h–227FFFh
67	64/32	218000h–21FFFFh
66	64/32	210000h–217FFFh
65	64/32	208000h–20FFFFh
64	64/32	200000h–207FFFh
63	64/32	1F8000h–1FFFFFh
62	64/32	1F0000h–1F7FFFh
61	64/32	1E8000h–1EFFFFh
60	64/32	1E0000h–1E7FFFh
59	64/32	1D8000h–1DFFFFh
58	64/32	1D0000h–1D7FFFh
57	64/32	1C8000h–1CFFFFh
56	64/32	1C0000h–1C7FFFh
55	64/32	1B8000h–1BFFFFh
54	64/32	1B0000h–1B7FFFh
53	64/32	1A8000h–1AFFFFh
52	64/32	1A0000h–1A7FFFh
51	64/32	198000h–19FFFFh
50	64/32	190000h–197FFFh
49	64/32	188000h–18FFFFh
48	64/32	180000h–187FFFh

Bank *b* = 48Mb		
Block	**Block Size (K-bytes/ K-words)**	**Address Range (x16)**
47	64/32	178000h–17FFFFh
46	64/32	170000h–177FFFh
45	64/32	168000h–16FFFFh
44	64/32	160000h–167FFFh
43	64/32	158000h–15FFFFh
42	64/32	150000h–157FFFh
41	64/32	148000h–14FFFFh
40	64/32	140000h–147FFFh
39	64/32	138000h–13FFFFh
38	64/32	130000h–137FFFh
37	64/32	128000h–12FFFFh
36	64/32	120000h–127FFFh
35	64/32	118000h–11FFFFh
34	64/32	110000h–117FFFh
33	64/32	108000h–10FFFFh
32	64/32	100000h–107FFFh
31	64/32	0F8000h–0FFFFFh
30	64/32	0F0000h–0F7FFFh
29	64/32	0E8000h–0EFFFFh
28	64/32	0E0000h–0E7FFFh
27	64/32	0D8000h–0DFFFFh
26	64/32	0D0000h–0D7FFFh
25	64/32	0C8000h–0CFFFFh
24	64/32	0C0000h–0C7FFFh
23	64/32	0B8000h–0BFFFFh
22	64/32	0B0000h–0B7FFFh
21	64/32	0A8000h–0AFFFFh
20	64/32	0A0000h–0A7FFFh
19	64/32	098000h–09FFFFh
18	64/32	090000h–097FFFh
17	64/32	088000h–08FFFFh
16	64/32	080000h–087FFFh
15	64/32	078000h–07FFFFh
14	64/32	070000h–077FFFh
13	64/32	068000h–06FFFFh
12	64/32	060000h–067FFFh
11	64/32	058000h–05FFFFh
10	64/32	050000h–057FFFh
9	64/32	048000h–04FFFFh
8	64/32	040000h–047FFFh
7	64/32	038000h–03FFFFh
6	64/32	030000h–037FFFh
5	64/32	028000h–02FFFFh
4	64/32	020000h–027FFFh
3	64/32	018000h–01FFFFh
2	64/32	010000h–017FFFh
1	64/32	008000h–00FFFFh
0	64/32	000000h–007FFFh

FLASH MEMORY OPERATING MODES

COMMAND STATE MACHINE

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between external microprocessors and the internal write state machine (WSM). The available commands are listed in Table 3, their definitions are given in Table 4 and their descriptions in Table 5. Program and erase algorithms are automated by the on-chip WSM. Table 7 shows the CSM transition states.

Once a valid PROGRAM/ERASE command is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally. A command is valid only if the exact sequence of WRITEs is completed. After the WSM completes its task, the write state machine status (WSMS) bit (SR7) (see Table 8) is set to a logic HIGH level (VIH), allowing the CSM to respond to the full command set again.

OPERATIONS

Device operations are selected by entering a standard JEDEC 8-bit command code with conventional microprocessor timings into an on-chip CSM through I/Os DQ0–DQ7. The number of bus cycles required to activate a command is typically one or two. The first operation is always a WRITE. Control signals F_CE# and F_WE# must be at a logic LOW level (VIL), and F_OE# and F_RP# must be at logic HIGH (VIH). The second operation, when needed, can be a WRITE or a READ depending upon the command. During a READ operation, control signals F_CE# and F_OE# must be at a logic LOW level (VIL), and F_WE# and F_RP# must be at logic HIGH (VIH).

Table 7 illustrates the bus operations for all the modes: write, read, reset, standby, and output disable.

When the device is powered up, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. For each one of the two Flash memory partitions, an on-chip status register is available. These two registers allow the monitoring of the progress of various operations that can take place on a memory bank. One of the two status registers is interrogated by entering a READ STATUS REGISTER command onto the CSM (cycle 1), specifying an address within the memory partition boundary, and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status register bits SR0-SR7 correspond to DQ0–DQ7 (see Table 8).

COMMAND DEFINITION

Once a specific command code has been entered, the WSM executes an internal algorithm, generating the necessary timing signals to program, erase, and verify data. See Table 4 for the CSM command definitions and data for each of the bus cycles.

STATUS REGISTER

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete. The status register is monitored by toggling F_OE# and F_CE# and reading the resulting status code on I/Os DQ0–DQ7. The high-order I/Os (DQ8–DQ15) are set to 00h internally, so only the low-order I/Os (DQ0–DQ7) need to be interpreted. Address lines select the status register pertinent to the selected memory partition.

Table 3
Command State Machine Codes For Device Mode Selection

COMMAND DQ0–DQ7	CODE ON DEVICE MODE
10h	Accelerated Programming Algorithm (APA)
20h	Block erase setup
40h	Program setup
50h	Clear status register
60h	Protection configuration setup
60h	Enable/disable deep power-down
70h	Read status register
90h	Read protection configuration register
98h	Read query
B0h	Program/erase suspend
C0h	Protection register program/lock
D0h	Program/erase resume – erase confirm
D1h	Check block erase confirm
FFh	Read array

Register data is updated and latched on the falling edge of F_OE# or F_CE#, whichever occurs last. The latest falling edge of either of these two signals updates the latch within a given READ cycle. Latching the data prevents errors from occurring if the register input changes during a status register read.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 8 defines the status register bits.

After monitoring the status register during a PROGRAM/ERASE operation, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

COMMAND STATE MACHINE OPERATIONS

The CSM decodes instructions for the commands listed in Table 3. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 4 for command definitions). During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested.

During a PROGRAM cycle, the WSM controls the program sequences and the CSM responds to a PROGRAM SUSPEND command only.

During an ERASE cycle, the CSM responds to an ERASE SUSPEND command only. When the WSM has completed its task, the WSMS bit (SR7) is set to a logic HIGH level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an ERASE or PROGRAM operation only when F_VPP is within its correct voltage range.

Table 4
Command Definitions

	FIRST BUS CYCLE			SECOND BUS CYCLE		
COMMAND	OPERATION	ADDRESS[1]	DATA	OPERATION	ADDRESS[1]	DATA[1]
READ ARRAY	WRITE	WA	FFh			
READ PROTECTION CONFIGURATION REGISTER	WRITE	IA	90h	READ	IA	ID
READ STATUS REGISTER	WRITE	BA	70h	READ	X	SRD
CLEAR STATUS REGISTER	WRITE	BA	50h			
READ QUERY	WRITE	QA	98h	READ	QA	QD
BLOCK ERASE SETUP	WRITE	BA	20h	WRITE	BA	D0h
PROGRAM SETUP	WRITE	WA	40h	WRITE	WA	WD
ACCELERATED PROGRAMMING ALGORITHM (APA)	WRITE	WA	10h	WRITE	WA	WD
PROGRAM/ERASE SUSPEND	WRITE	BA	B0h			
PROGRAM/ERASE RESUME – ERASE CONFIRM	WRITE	BA	D0h			
LOCK BLOCK	WRITE	BA	60h	WRITE	BA	01h
UNLOCK BLOCK	WRITE	BA	60h	WRITE	BA	D0h
LOCK DOWN BLOCK	WRITE	BA	60h	WRITE	BA	2Fh
CHECK BLOCK ERASE	WRITE	BA	20h	WRITE	BA	D1h
PROTECTION REGISTER PROGRAM	WRITE	PA	C0h	WRITE	PA	PD
PROTECTION REGISTER LOCK	WRITE	LPA	C0h	WRITE	LPA	FFFDh
ENABLE/DISABLE DEEP POWER-DOWN	WRITE	DPW	60h	WRITE	DPW	03h

NOTE: 1. BA: Address within the block
DPW: BBCFh = Disable deep power-down
BBDFh = Enable deep power-down
IA: Identification code address
ID: Identification code data
LPA: Lock protection register address
PA: Protection register address
PD: Data to be written at location PA
QA: Query code address
QD: Query code data
SRD: Data read from the status register
WA: Word address of memory location to be written, or read
WD: Data to be written at the location WA
X: "Don't Care"

Table 5
Command Descriptions

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
10h	APA	First	Prepares for an accelerated program operation.
20h	Erase Setup	First	Prepares the CSM for the ERASE command. If the next command is not a CHECK BLOCK ERASE OR ERASE CONFIRM command, the command will be ignored, and the device will go to read status mode and wait for another command.
40h	Program Setup	First	A two-cycle command: The first cycle prepares for a PROGRAM operation, the second cycle latches addresses and data and initiates the WSM to execute the program algorithm. The Flash outputs status register data on the falling edge of F_OE# or F_CE#, whichever occurs first.
50h	Clear Status Register	First	The WSM can set the program status (SR4), and erase status (SR5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0."
60h	Protection Configuration Setup	First	Prepares the CSM for changes to the block locking status. If the next command is not BLOCK UNLOCK, BLOCK LOCK or BLOCK LOCK DOWN, the command will be ignored, and the device will go to read status mode.
	Set Read Configuration Register	First	Puts the device into the set read configuration mode so that it will be possible to set the option bits related to burst read mode.
70h	Read Status Register	First	Places the device into read status register mode. Reading the device outputs the contents of the status register for the addressed bank. The device automatically enters this mode for the addressed bank after a PROGRAM or ERASE operation has been initiated.
90h	Read Protection Configuration	First	Puts the device into the read protection configuration mode so that reading the device outputs the manufacturer/device codes or block lock status.
98h	Read Query	First	Puts the device into the read query mode so that reading the device outputs common Flash interface information.
B0h	Program Suspend	First	Suspends the currently executing PROGRAM/ERASE/CHECK BLOCK ERASE operation. The status register indicates when the operation has been successfully suspended by setting either the program suspend (SR2) or erase suspend (SR6) and the WSMS bit (SR7) to a "1" (ready). The WSM continues to idle in the suspend state, regardless of the state of all input control pins except F_RP#, which immediately shuts down the WSM and the remainder of the chip if F_RP# is driven to V_{IL}.
	Erase Suspend	First	
	Check Block Erase Suspend	First	
C0h	Program Device Protection Register	First	Writes a specific code into the device protection register.
	Lock Device Protection Register	First	Locks the device protection register; data can no longer be changed.

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Table 5
Command Descriptions (continued)

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
D0h	Erase Confirm	Second	If the previous command was an ERASE SETUP command, then the CSM closes the address and data latches, and it begins erasing the block indicated on the address pins. During programming/erase, the device responds only to the READ STATUS REGISTER, PROGRAM SUSPEND, or ERASE SUSPEND commands and outputs status register data on the falling edge of F_OE# or F_CE#, whichever occurs last.
	Program/Erase/ Check Block Erase Resume	First	If a PROGRAM, ERASE or CHECK BLOCK ERASE operation was previously suspended, this command resumes the operation.
FFh	Read Array	First	During the array mode, array data is output on the data bus.
01h	Lock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and locks the block indicated on the address bus.
2Fh	Lock Down	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and locks down the block indicated on the address bus.
D0h	Unlock Block	Second	If the previous command was PROTECTION CONFIGURATION SETUP, the CSM latches the address and unlocks the block indicated on the address bus. If the block had been previously set to lock down, this operation has no effect.
00h	Invalid/Reserved		Unassigned command that should not be used.
D1h	Check Block Erase Confirm	Second	If the previous command was ERASE SETUP command, the CSM closes the address latches and checks that the block is completely erased.

CLEAR STATUS REGISTER

The internal circuitry can set, but not clear, the block lock status bit (SR1), the F_VPP status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to the internal operations. When the status bits are cleared, the device returns to the read array mode.

READ OPERATIONS

The following READ operations are available: READ ARRAY, READ PROTECTION CONFIGURATION REGISTER, READ QUERY and READ STATUS REGISTER.

READ ARRAY

The array is read by entering the command code FFh on DQ0–DQ7. Control signals F_CE# and F_OE# must be at a logic LOW level (VIL), and F_WE# and F_RP# must be at a logic HIGH level (VIH) to read data from the array. Data is available on DQ0–DQ15. Any valid address within any of the blocks selects that address and allows data to be read from that address. Upon initial power-up or device reset, the device defaults to the read array mode.

READ CHIP PROTECTION IDENTIFICATION DATA

The chip identification mode outputs three types of information: the manufacturer/device identifier, the block locking status, and the protection register. Two bus cycles are required for this operation: the chip identification data is read by entering the command code 90h on DQ0–DQ7 to the bank containing address 00h and the identification code address on the address lines. Control signals F_CE# and F_OE# must be at a logic LOW level (VIL), and F_WE# and F_RP# must be at a logic HIGH level (VIH) to read data from the protection configuration register. Data is available on DQ0–DQ15. After data is read from protection configuration register, the READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands. See Table 10 for further details.

READ QUERY

The read query mode outputs common flash interface (CFI) data when the device is read (see Table 12). Two bus cycles are required for this operation. It is possible to access the query by writing the read query command code 98h on DQ0–DQ7 to the bank containing address 0h. Control signals F_CE# and F_OE# must be at a logic LOW level (VIL), and F_WE# and F_RP# must be at a logic HIGH level (VIH) to read data from the query. The CFI data structure contains information such as block size, density, command set, and electrical specifications. To return to read array mode, write the read array command code FFh on DQ0–DQ7.

READ STATUS REGISTER

The status register is read by entering the command code 70h on DQ0–DQ7. Two bus cycles are required for this operation: one to enter the command code and a second to read the status register. In a READ cycle, the address is latched and register data is updated on the falling edge of F_OE# or F_CE#, whichever occurs last. Register data is updated and latched on the falling edge of F_OE# or F_CE#, whichever occurs last.

Table 6
Command State Machine Transition Table

Command input to the present partition (and next state of the present partition)													Present state of the present partition				Present state of the other partition	
2Fh Lock down confirm	01h Lock confirm	C0h OTP setup	60h Lock/Unlock /Lock down	98h Read query	90h Read device ID	50h Clear status register	70h Read status	B0h Program /Erase suspend	D0h BE confirm, P/E resume, ULB confirm	20h Erase setup	10h/40h APA/ Program setup	FFh Read array	SR7	Data when read	State	Mode		
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Array	Array	Read	1	Setup
																	2	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					3	Idle
Read array								Read array									4	Erase suspend
								Read array									5	Prog. suspend
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	CFI	Query		6	Setup
																	7	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					8	Idle
Read array								Read array									9	Erase suspend
								Read array									10	Prog. suspend
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	ID	Device ID		11	Setup
																	12	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					13	Idle
Read array								Read array									14	Erase suspend
								Read array									15	Prog. suspend
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Status		16	Setup
																	17	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					18	Idle
Read array								Read array									19	Erase suspend
								Read array									20	Prog. suspend
Protection register busy													1	Status	Setup	Protection register	21	Idle
Protection register busy													0	Status	Busy		22	Idle
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Done		23	Setup
																	24	Busy
Read array		OTP setup	Lock	Read query	Read ID	Read array	Read status	Read array		Erase setup	Program setup	Read array	1	Status	Done		25	Idle
Read array								Read array									26	Erase suspend
								Read array									27	Prog. suspend

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Table 6
Command State Machine Transition Table (continued)

Command input to the present partition (and next state of the present partition)													Present state of the present partition				Present state of the other partition	
2Fh Lock down confirm	01h Lock confirm	C0h OTP setup	60h Lock/Unlock /Lock down	98h Read query	90h Read device ID	50h Clear status register	70h Read status	B0h Program /Erase suspend	D0h BE confirm, P/E resume, ULB confirm	20h Erase setup	10h/40h APA/ Program setup	FFh Read array	SR7	Data when read	State	Mode		
LB/ULB		Lock						L	LB/ULB	Lock			1	Status	Setup	Lock	28	Any state
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Error		29	Setup
																	30	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					31	Idle
Read array								Read array									32	Erase suspend
								Read array									33	Prog. suspend
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Lock/ Unlock		34	Setup
																	35	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					36	Idle
Read array								Read array									37	Erase suspend
								Read array									38	Prog. suspend
Program Busy													1	Status	Setup	Program	39	Any state
Program Busy								PS read	Program busy				0	Status	Busy		40	Idle
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Done		41	Setup
																	42	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					43	Idle
Read array								Read array									44	Erase suspend
								Read array									45	Prog. suspend
Program suspend read array			Lock	Program suspend read query	Program suspend read ID	Program suspend read array	Program suspend read status	Program suspend read array	Program busy	Program suspend read array			1	Status	Read status	Program suspend	46	Setup
																	47	Idle
																	48	Erase suspend

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Table 6
Command State Machine Transition Table (continued)

Command input to the present partition (and next state of the present partition)													Present state of the present partition				Present state of the other partition	
2Fh Lock down confirm	01h Lock confirm	C0h OTP setup	60h Lock/Unlock /Lock down	98h Read query	90h Read device ID	50h Clear status register	70h Read status	B0h Program /Erase suspend	D0h BE confirm, P/E resume, ULB confirm	20h Erase setup	10h/40h APA/ Program setup	FFh Read array	SR7	Data when read	State	Mode		
Program suspend read array			Lock	Program suspend read query	Program suspend read ID	Program suspend read array	Program suspend read status	Program suspend read array	Program busy	Program suspend read array			1	Array	Read array	Program suspend	49	Setup
																	50	Idle
																	51	Erase suspend
Program suspend read array			Lock	Program suspend read query	Program suspend read ID	Program suspend read array	Program suspend read status	Program suspend read array	Program busy	Program suspend read array			1	ID	Read ID		52	Setup
																	53	Idle
																	54	Erase suspend
Program suspend read array			Lock	Program suspend read query	Program suspend read ID	Program suspend read array	Program suspend read status	Program suspend read array	Program busy	Program suspend read array			1	CFI	Read Query		55	Setup
																	56	Idle
																	57	Erase suspend
LB/ULB		Erase error						Erase error	Erase busy	Erase error			1	Status	Setup	Erase	58	Idle
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Error		59	Setup
																	60	Busy
Read array		OTP setup						Read array		Erase setup	Program setup	Read array					61	Idle
Read array								Read array									62	Erase suspend
								Read array									63	Prog. suspend
Read array			Lock	Read query	Read ID	Read array	Read status	Read array					1	Status	Done		64	Setup
																	65	Busy
Read array		OTP setup						Read array		Erase	Program setup	Read array					66	Idle
Read array								Read array									67	Erase suspend
								Read array									68	Prog. suspend
Block erase busy								ES read status	Erase busy				0	Status	Busy		69	Idle

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Table 6
Command State Machine Transition Table (continued)

Command input to the present partition (and next state of the present partition)													Present state of the present partition				Present state of the other partition	
2Fh Lock down confirm	`01h Lock confirm	C0h OTP setup	60h Lock/Unlock /Lock down	98h Read query	90h Read device ID	50h Clear status register	70h Read status	B0h Program /Erase suspend	D0h BE confirm, P/E resume, ULB confirm	20h Erase setup	10h/40h APA/ Program setup	FFh Read array	SR7	Data when read	State	Mode		
Erase suspend read array			Lock	Erase suspend read query	Erase suspend read ID	Erase suspend read array	Erase suspend read status	ES read array	Erase busy	Erase suspend read array			1	Status	Read status	Erase suspend	70	Setup
								Erase suspend read array									71	Busy
								ES read array	Erase busy	ES read array	Prog. setup	ES read array					72	Idle
								Erase suspend read array									73	Prog. suspend
Erase suspend read array			Lock	Erase suspend read query	Erase suspend read ID	Erase suspend read array	Erase suspend read status	ES read array	Erase busy	Erase suspend read array			1	Array	Read array		74	Setup
								Erase suspend read array									75	Busy
								ES read array	Erase busy	ES read array	Prog. setup	ES read array					76	Idle
								Erase suspend read array									77	Prog. suspend
Erase suspend read array			Lock	Erase suspend read query	Erase suspend read ID	Erase suspend read array	Erase suspend read status	ES read array	Erase busy	Erase suspend read array			1	ID	Read ID		78	Setup
								Erase suspend read array									79	Busy
								ES read array	Erase busy	ES read array	Prog. setup	ES read array					80	Idle
								Erase suspend read array									81	Prog. suspend
Erase suspend read array			Lock	Erase suspend read query	Erase suspend read ID	Erase suspend read array	Erase suspend read status	ES read array	Erase busy	Erase suspend read array			1	CFI	Read query		82	Setup
								Erase suspend read array									83	Busy
								ES read array	Erase busy	ES read array	Prog. setup	ES read array					84	Idle
								Erase suspend read array									85	Prog. suspend

Table 7
Bus Operations

MODE	F_RP#	F_CE#	F_OE#	F_WE#	ADDRESS	DQ0–DQ15
Read (array, status registers, device identification register, or query)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Standby	V_{IH}	V_{IH}	X	X	X	High-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Reset	V_{IL}	X	X	X	X	High-Z
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

PROGRAMMING OPERATIONS

There are two CSM commands for programming: PROGRAM SETUP and ACCELERATED PROGRAMMING ALGORITHM (see Table 3).

PROGRAM SETUP COMMAND

After the 40h command code is entered on DQ0–DQ7, the WSM takes over and correctly sequences the device to complete the PROGRAM operation. The WRITE operation may be monitored through the status register (see the Status Register section). During this time, the CSM will only respond to a PROGRAM SUSPEND command until the PROGRAM operation has been completed, after which time, all commands to the CSM become valid again. The PROGRAM operation can be suspended by issuing a PROGRAM SUSPEND command (B0h).

Once the WSM reaches the suspend state, it allows the CSM to respond only to READ ARRAY, READ STATUS REGISTER, READ PROTECTION CONFIGURATION, READ QUERY, PROGRAM SETUP, or PROGRAM RESUME. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the PROGRAM operation, a PROGRAM RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 4 for programming operation and Figure 5 for program suspend and program resume).

Taking RP# to V_{IL} during programming aborts the PROGRAM operation.

ACCELERATED PROGRAMMING ALGORITHM

The accelerated programming algorithm (APA) is intended for in-system and in-factory use. Its 32 single-word internal buffer enables fast data stream programming.

The APA is activated when the WSM executes command code 10h. Upon activation, the word address and the data sequences must be provided to the WSM, without polling SR7. The same starting address must be provided for each data word. After all 32 sequences are issued, the status register reports a busy condition. Figure 6 shows the APA flowchart.

If the data stream is shorter than 32 words, use FFFFh to fill in the missing data. Also, be sure the starting address is aligned with a 32-word boundary.

The APA is fully concurrent. For example, it can be interrupted and resumed during programming. When loading the programming buffer, only a read access in the other bank is allowed.

For in-factory programming, the APA, along with an optimized set of programming parameters, minimizes chip programming time when 11.4V ≤ F_V_{PP} ≤ 12.6V.

For in-system programming, when 0.9V ≤ F_V_{PP} ≤ 2.2V, the APA and the 32 single-word buffer significantly improve both the system throughput and the average programming time when compared with standard programming practices. The accelerated programming functionality executes and verifies the APA without microprocessor intervention. This relieves the microprocessor from constantly monitoring the progress of the programming and erase activity, freeing up valuable memory bus bandwidth. This increases the system throughput.

ERASE OPERATIONS

An ERASE operation must be used to initialize all bits in an array block to “1s.” After BLOCK ERASE confirm is issued, the CSM responds only to an ERASE SUSPEND command until the WSM completes its task.

Block erasure inside the memory array sets all bits within the address block to logic 1s. Erase is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Block erasure is initiated by a command sequence to the CSM: BLOCK ERASE SETUP (20h) followed by BLOCK ERASE CONFIRM (D0h) (see Table 5). A two-command erase sequence protects against accidental erasure of memory contents.

When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally verification is performed to ensure that all bits are correctly erased. Monitoring of the ERASE operation is possible through the status register (see the Status Register section).

During the execution of an ERASE operation, the ERASE SUSPEND command (B0h) can be entered to direct the WSM to suspend the ERASE operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, READ QUERY, READ CHIP PROTECTION CONFIGURATION, PROGRAM SETUP, PROGRAM RESUME, ERASE RESUME and LOCK SETUP (see the Block Locking section). During the ERASE SUSPEND operation, array data must be read from a block other than the one being erased. To resume the ERASE operation, an ERASE RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 8). It is also possible that an ERASE in any bank can be suspended and a WRITE to another block in the same bank can be initiated. After the completion of a WRITE, an ERASE can be resumed by writing an ERASE RESUME command.

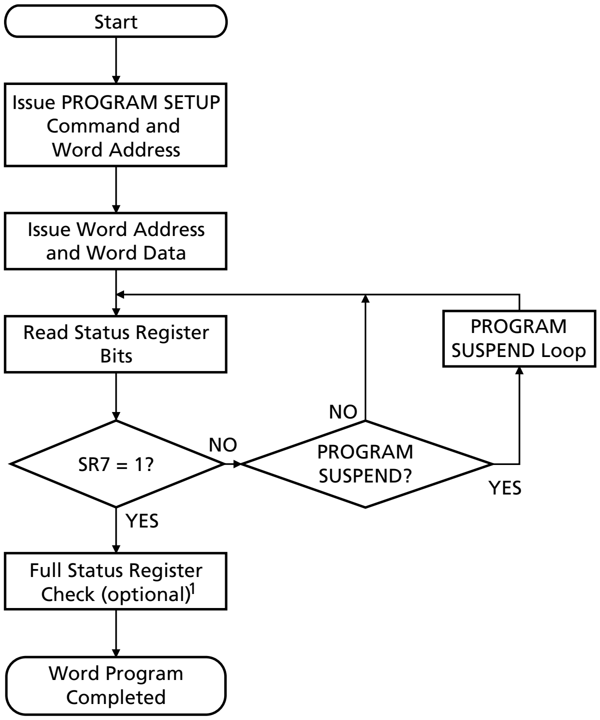
After an ERASE command completion, it is possible to check if the block has been erased successfully, using the CHECK BLOCK ERASE command. Two bus cycles are required for this operation: one to set up the CHECK BLOCK ERASE and the second one to start the execution of the command. If after the operation the bit SR5 is set to 0 the operation has been completed succesfully, if it is set to 1, there has been an error during the BLOCK ERASE operation.

Table 8
Status Register Bit Definition

WSMS	ESS	ES	PS	V_{PP}S	PSS	BLS	R
7	6	5	4	3	2	1	0

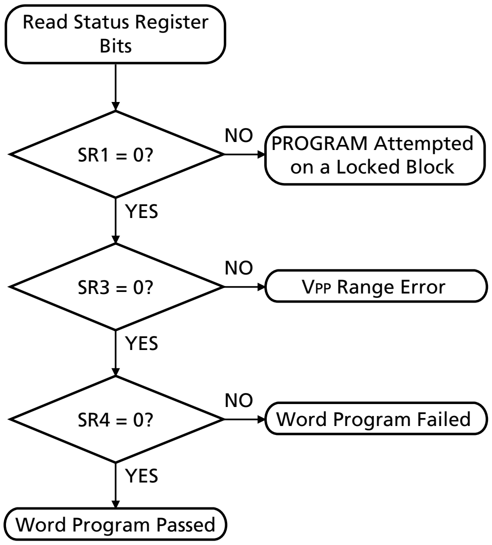
STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check write state machine bit first to determine word program or block erase completion, before checking program or erase status bits.
SR6	ERASE SUSPEND STATUS (ESS) 1 = BLOCK ERASE Suspended 0 = BLOCK ERASE in Progress/Completed	When ERASE SUSPEND is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an ERASE RESUME command is issued.
SR5	ERASE/CHECK BLOCK ERASE STATUS (ES) 1 = Error in BLOCK ERASE/ CHECK BLOCK ERASE 0 = Successful BLOCK ERASE	When this bit is set to "1" and ERASE CONFIRM is issued, WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure. When this bit is set to "1" and CHECK BLOCK ERASE CONFIRM is issued, WSM has checked the block for its erase state, and the block is not erased.
SR4	PROGRAM STATUS (PS) 1 = Error in PROGRAM 0 = Successful PROGRAM	When this bit is set to "1," WSM has attempted but failed to program a word.
SR3	F_V_{PP} STATUS (V_{PP}S) 1 = F_V_{PP} Low Detect, Operation Abort 0 = F_V_{PP} = OK	The F_V_{PP} status bit does not provide continuous indication of the F_V_{PP} level. The WSM interrogates the F_V_{PP} level only after the program or erase command sequences have been entered and informs the system if F_V_{PP} < 0.9V. The F_V_{PP} level is also checked before the PROGRAM/ERASE operation is verified by the WSM. A factory option allows PROGRAM or ERASE at 0V, in which case SR3 is held at "0."
SR2	PROGRAM SUSPEND STATUS (PSS) 1 = PROGRAM Suspended 0 = PROGRAM in Progress/Completed	When PROGRAM SUSPEND is issued, WSM halts execution and sets both WSM and PSS bits to "1." PSS bit remains set to "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS (BLS) 1 = PROGRAM/ERASE Attempted on a Locked Block; Operation Aborted 0 = No Operation to Locked Blocks	If a PROGRAM or ERASE operation is attempted to one of the locked blocks, this is set by the WSM. The operation specified is aborted, and the device is returned to read status mode.
SR0	RESERVED FOR FUTURE ENHANCEMENT	This bit is reserved for future use.

Figure 4
Automated Word Programming Flowchart


Start
Issue PROGRAM SETUP Command and Word Address
Issue Word Address and Word Data
Read Status Register Bits
PROGRAM SUSPEND Loop
SR7 = 1?
NO
PROGRAM SUSPEND?
NO
YES
YES
Full Status Register Check (optional)1
Word Program Completed

BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE PROGRAM SETUP	Data = 40h Addr = Address of word to be programmed
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word programming operation to reset the device to read array mode.		

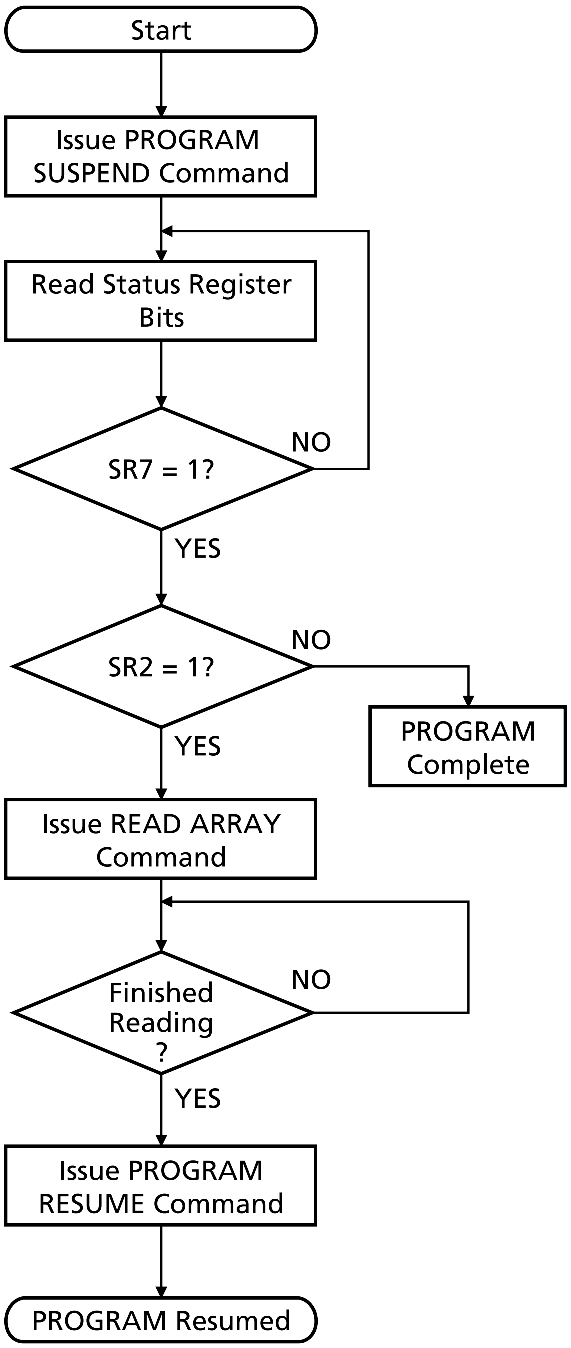
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect F_VPP low
Standby		Check SR4[3] 1 = Word program error

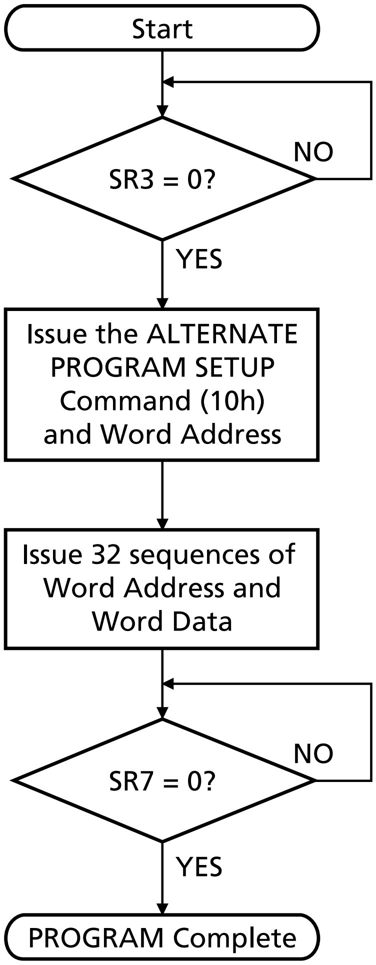
NOTE:
1. Full status register check can be done after each word or after a sequence of words.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR4 is cleared only by the CLEAR STATUS REGISTER command, but it does not prevent additional program operation attempts.

Figure 5
PROGRAM SUSPEND/ PROGRAM RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed.
WRITE	PROGRAM RESUME	Data = D0h

Figure 6
Accelerated Program Algorithm Flowchart

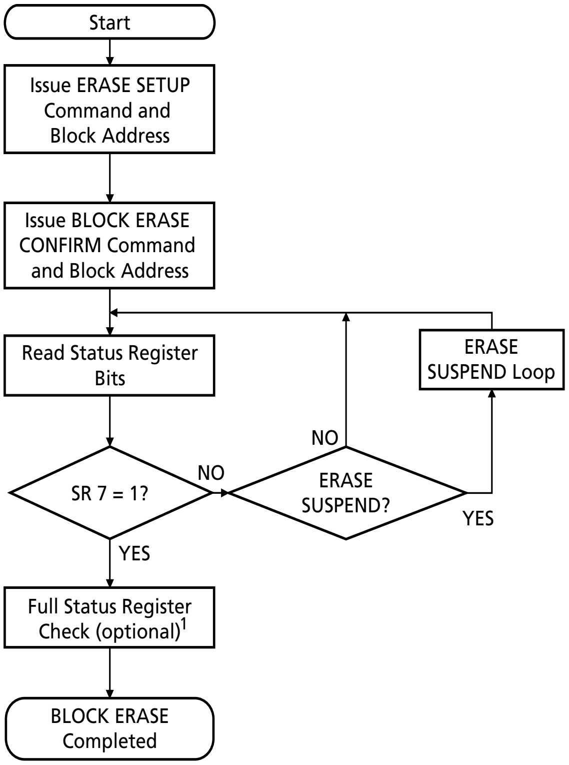

Start
SR3 = 0?
NO
YES
Issue the ALTERNATE PROGRAM SETUP Command (10h) and Word Address
Issue 32 sequences of Word Address and Word Data
SR7 = 0?
NO
YES
PROGRAM Complete

BUS OPERATION	COMMAND	COMMENTS

WRITE	WRITE ACCELERATED PROGRAM ALGORITHM SETUP	Data = 10h
		Addr = Start address

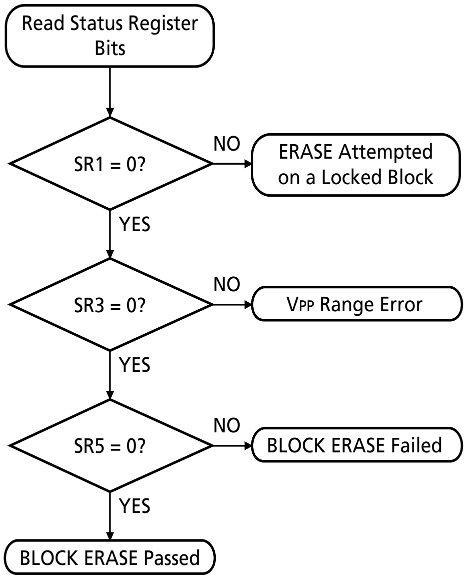
WRITE	WRITE DATA	Data = Word to be programmed Addr = Start address
READ		Status register data Toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy

Figure 7
BLOCK ERASE Flowchart


Start
Issue ERASE SETUP Command and Block Address
Issue BLOCK ERASE CONFIRM Command and Block Address
Read Status Register Bits
ERASE SUSPEND Loop
NO
SR 7 = 1?
NO
ERASE SUSPEND?
YES
YES
Full Status Register Check (optional)[1]
BLOCK ERASE Completed

BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Block Addr = Address within block to be erased
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last BLOCK ERASE operation to reset the device to read array mode.		

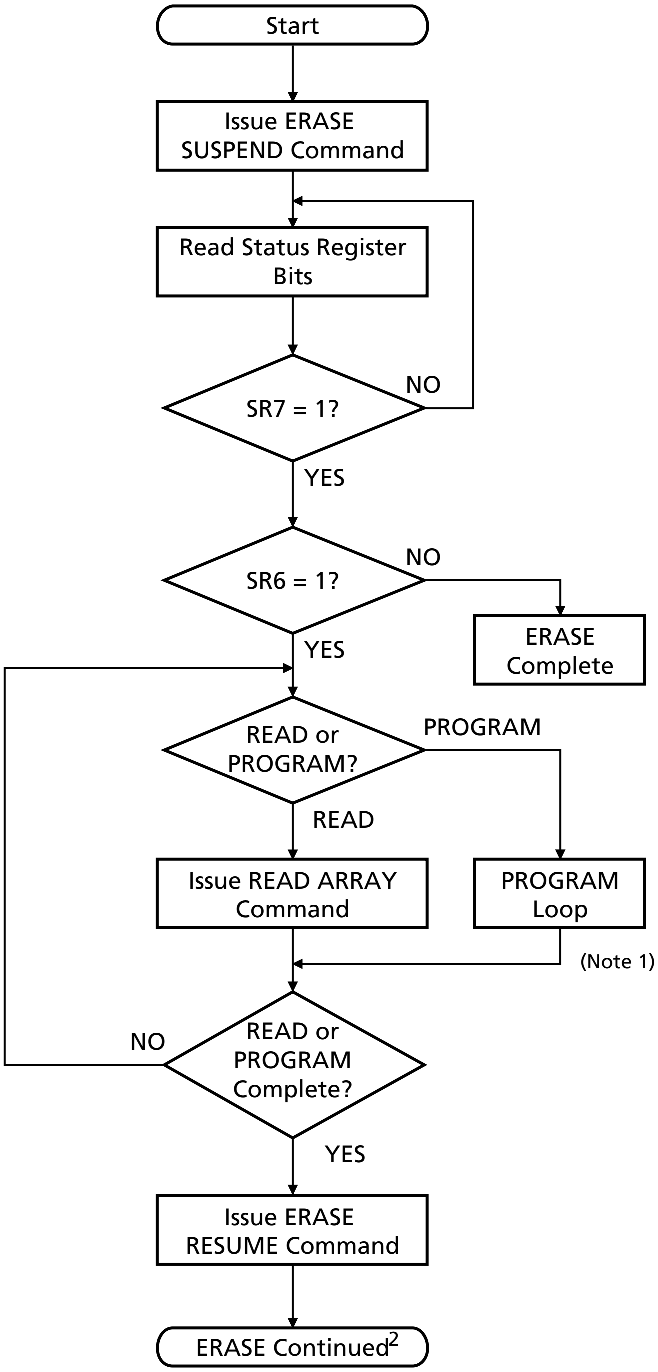
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect F_V_{PP} block
Standby		Check SR4 and SR5 1 = BLOCK ERASE command error
Standby		Check SR5[3] 1 = BLOCK ERASE error

NOTE:
1. Full status register check can be done after each block or after a sequence of blocks.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

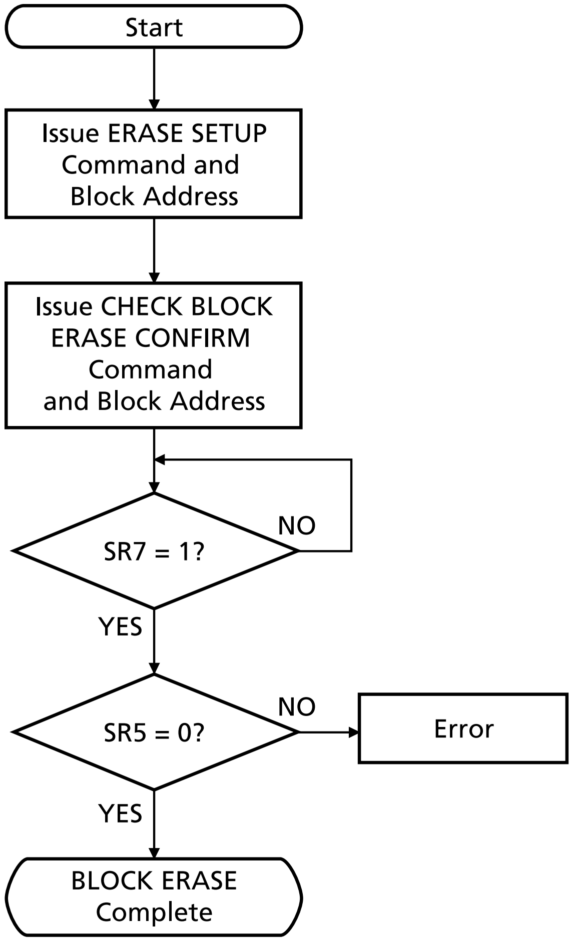
Figure 8
ERASE SUSPEND/ERASE RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR6 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being erased.
WRITE	ERASE RESUME	Data = D0h

NOTE: 1. See Word Programming Flowchart for complete programming procedure.
2. See BLOCK ERASE Flowchart for complete erasure procedure.

Figure 9
CHECK BLOCK ERASE Flowchart


Start
Issue ERASE SETUP Command and Block Address
Issue CHECK BLOCK ERASE CONFIRM Command and Block Address
SR7 = 1?
NO
YES
SR5 = 0?
NO
Error
YES
BLOCK ERASE Complete

BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SETUP	Data = 20h Block Addr = Address within block to be checked
WRITE	CHECK BLOCK ERASE CONFIRM	Data = D1 Block Addr = Address within block to be checked
READ		Status register data Toggle OE# or CE# to update status register
Standby		Check SR7 and SR5

READ-WHILE-WRITE/ERASE CONCURRENCY

It is possible for the device to read from one bank while erasing/writing to another bank. Once a bank enters the WRITE/ERASE operation, the other bank automatically enters read array mode. For example, during a READ CONCURRENCY operation, if a PROGRAM/ERASE command is issued in bank *a*, then bank *a* changes to the read status mode and bank *b* defaults to the read array mode. The device reads from bank *b* if the latched address resides in bank *b* (see Figure 10). Similarly, if a PROGRAM/ERASE command is issued in bank *b*, then bank *b* changes to read status mode and bank *a* defaults to read array mode. When returning to bank *a*, the device reads program/erase status if the latched address resides in bank *a*.

A correct bank address must be specified to read status register after returning from concurrent read in the other bank.

When reading the CFI or the chip protection register, concurrent operation is not allowed on the top boot device. Concurrent READ of the CFI or the chip protection register is only allowed when a PROGRAM or ERASE operation is performed on bank *b* on the bottom boot device. For a bottom boot device, reading of the CFI table or the chip protection register is only allowed if bank *b* is in read array mode. For a top boot device, reading of the CFI table or the chip protection register is only allowed if bank *a* is in read array mode.

BLOCK LOCKING

The Flash memory of the MT28C6428P20 and MT28C6428P18 devices provide a flexible locking scheme which allows each block to be individually locked or unlocked with no latency.

The devices offer two-level protection for the blocks. The first level allows software-only control of block locking (for data which needs to be changed frequently), while the second level requires hardware interaction before locking can be changed (code which does not require frequent updates).

Control signals F_WP#, DQ0, and DQ1 define the state of a block; for example, state [001] means F_WP# = 0, DQ0 = 0 and DQ1 = 1.

Table 9 defines all of the possible locking states.

NOTE: All blocks are software-locked upon completion of the power-up sequence.

LOCKED STATE

After a power-up sequence completion, or after a reset sequence, all blocks are locked (states [001] or [101]). This means full protection from alteration. Any PROGRAM or ERASE operations attempted on a locked block will return an error on bit SR1 of the status register. The status of a locked block can be changed to unlocked or lock down using the appropriate software commands. Writing the lock command sequence, 60h followed by 01h, can lock an unlocked block.

UNLOCKED STATE

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered down. An unlocked block can be locked or locked down using the appropriate software command sequence, 60h followed by D0h. (See Table 4.)

Figure 10
READ-While-WRITE Concurrency

Bank *a*	Bank *b*
1 - Erasing/writing to bank *a* 2 - Erasing in bank *a* can be suspended, and a WRITE to another block in bank *a* can be initiated. 3 - After the WRITE in that block is complete, an ERASE can be resumed by writing an ERASE RESUME command.	→ 1 - Reading from bank *b*
1 - Reading bank *a* ←	1 - Erasing/writing to bank *b* 2 - Erasing in bank *b* can be suspended, and a WRITE to another block in bank *b* can be initiated. 3 - After the WRITE in that block is complete, an ERASE can be resumed by writing an ERASE RESUME command.

Table 9
Block Locking State Transition

F_WP#	DQ1	DQ0	NAME	ERASE/PROGRAM ALLOWED	LOCK	UNLOCK	LOCK DOWN
0	0	0	Unlocked	Yes	To [001]	–	To [011]
0	0	1	Locked (Default)	No	–	To [000]	To [011]
0	1	1	Lock Down	No	–	–	–
1	0	0	Unlocked	Yes	To [101]	–	To [111]
1	0	1	Locked	No	–	To [100]	To [111]
1	1	0	Lock Down Disabled	Yes	To [111]	–	To [111]
1	1	1	Lock Down Disabled	No	–	To [110]	–

LOCKED DOWN STATE

Blocks locked down (state [011]) are protected from PROGRAM and ERASE operations, but their protection status cannot be changed using software commands alone. A locked or unlocked block can be locked down by writing the lock down command sequence, 60h followed by 2Fh. Locked down blocks revert to the locked state when the device is reset or powered down.

The LOCK DOWN function is dependent on the F_WP# input. When F_WP# = 0, blocks in lock down [011] are protected from program, erase, and lock status changes. When F_WP# = 1, the LOCK DOWN function is disabled ([111]) and locked down blocks can be individually unlocked by a software command to the [110] state, where they can be erased and programmed. These blocks can then be relocked [111] and unlocked [110], as desired, as long as F_WP# remains HIGH. When F_WP# goes LOW, blocks that were previously locked down return to the lock down state [011] regardless of any changes made while F_WP# was HIGH. Device reset or power-down resets all locks, including those in lock down, to the locked state (see Table 10).

READING A BLOCK'S LOCK STATUS

The lock status of every block can be read in the read device identification mode. To enter this mode, write 90h to the bank containing address 00h. Subsequent READs at block address +00002h will output the lock status of that block. The lowest two outputs, DQ0 and DQ1, represent the lock status. DQ0 indicates the block lock/unlock status and is set by the LOCK command and cleared by the UNLOCK command. It is also automatically set when entering lock down. DQ1 indicates lock down status and is set by the LOCK DOWN command. It can only be cleared by reset or power-down, not by software. Table 9 shows the block locking state transition scheme. The READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands.

LOCKING OPERATIONS DURING ERASE SUSPEND

Changes to block lock status can be performed during an ERASE SUSPEND by using the standard locking command sequences to unlock, lock, or lock down. This is useful in the case when another block needs to be updated while an ERASE operation is in progress.

To change block locking during an ERASE operation, first write the ERASE SUSPEND command (B0h), then check the status register until it indicates that the ERASE operation has been suspended. Next, write the desired lock command sequence to block lock, and the lock status will be changed. After completing any desired LOCK, READ, or PROGRAM operations, resume the ERASE operation with the ERASE RESUME command (D0h).

If a block is locked or locked down during an ERASE SUSPEND on the same block, the locking status bits are changed immediately. When the ERASE is resumed, the ERASE operation completes.

A locking operation cannot be performed during a PROGRAM SUSPEND.

STATUS REGISTER ERROR CHECKING

Using nested locking or program command sequences during ERASE SUSPEND can introduce ambiguity into status register results.

Following protection configuration setup (60h), an invalid command produces a lock command error (SR4 and SR5 are set to "1") in the status register. If a lock command error occurs during an ERASE SUSPEND, SR4 and SR5 are set to "1" and remain at "1" after the ERASE SUSPEND command is issued. When the ERASE is complete, any possible error during the ERASE cannot be detected via the status register because of the previous locking command error.

A similar situation happens if an error occurs during a program operation error nested within an ERASE SUSPEND.

CHIP PROTECTION REGISTER

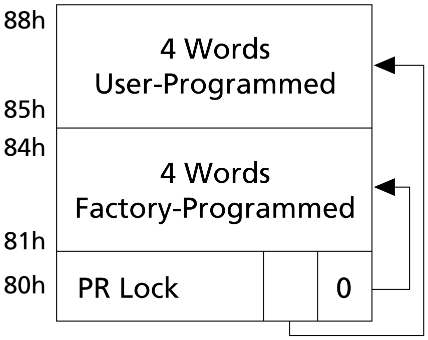
A 128-bit chip protection register can be used to fullfill the security considerations in the system (preventing device substitution).

The 128-bit security area is divided into two 64-bit segments. The first 64 bits are programmed at the manufacturing site with a unique 64-bit number. The other segment is left blank for customers to program as desired. (See Figure 12).

READING THE CHIP PROTECTION REGISTER

The chip protection register is read in the device identification mode. To enter this mode, load the 90h command the bank containing address 00h. Once in this mode, READ cycles from addresses shown in Table 10 retrieve the specified information. To return to the read array mode, write the READ ARRAY command (FFh). The READ ARRAY command, FFh, must be issued to the bank containing address 00h prior to issuing other commands.

Figure 12
Protection Register Memory Map



PAGE READ MODE

The initial portion of the page mode cycle is the same as the asynchronous access cycle. Holding CE# LOW and toggling addresses A0–A2 allows random access of other words in the page.

The page size can be customized at the factory to four or eight words as required; but if no specification is made, the normal size is four words.

ASYNCHRONOUS READ CYCLE

When accessing addresses in a random order or when switching between pages, the access time is given by ^{t}AA.

When F_CE# and F_OE# are LOW, the data is placed on the data bus and the processor can read the data.

Table 10
Chip Configuration Addressing[1]

ITEM	ADDRESS[2]	DATA
Manufacturer Code (x16)	00000h	002Ch
Device Code • Top boot configuration • Bottom boot configuration	00001h	 44B6h 44B7h

Block Lock Configuration
• Block is unlocked
• Block is locked
• Block is locked down
	XX002h	Lock
		DQ0 = 0
		DQ0 = 1
		DQ1 = 1

Chip Protection Register Lock	80h	PR Lock
Chip Protection Register 1	81h–84h	Factory Data
Chip Protection Register 2	85h–88h	User Data

NOTE: 1. Other locations within the configuration address space are reserved by Micron for future use.
2. "XX" specifies the block address of lock configuration.

STANDBY MODE

ICC supply current is reduced by applying a logic HIGH level on F_CE# and F_RP# to enter the standby mode. In the standby mode, the outputs are placed in High-Z. Applying a CMOS logic HIGH level on F_CE# and F_RP# reduces the current to ICC3 (MAX). If the device is deselected during an ERASE operation or during programming, the device continues to draw current until the operation is complete.

AUTOMATIC POWER SAVE (APS) MODE

Substantial power savings are realized during periods when the Flash array is not being read and the device is in the active mode. During this time the device switches to the automatic power save (APS) mode. When the device switches to this mode, ICC is reduced to a level comparable to ICC3. Further power savings can be realized by applying a logic HIGH level on CE# to place the device in standby mode. The low level of power is maintained until another operation is initiated. In this mode, the I/Os retain the data from the last memory address read until a new address is read. This mode is entered automatically if no addresses or control signals toggle.

DEEP POWER-DOWN MODE

By issuing an ENABLE DEEP POWER-DOWN command (see Table 3) it is possible to enable the DEEP POWER-DOWN function. In this configuration, applying a logic LOW to RST# reduces the current to ICC10, and resets all the internal registers with the exception of the individual block protection status. To exit this mode, a wait time of 100µs (^{t}RWHDP) must elapse after a logic HIGH is applied to RST#. During the wait time, the device performs a full power-up sequence, and the power consumption may exceed the standby current limits.

F_VPP/F_VCC PROGRAM AND ERASE VOLTAGES

The Flash memory devices provide in-system programming and erase with F_VPP in the 0.9V–2.2V range. In addition to the flexible block locking, the F_VPP programming voltage can be held LOW for absolute hardware write protection of all blocks in the Flash device. When F_VPP is below VPPLK, any PROGRAM or ERASE operation results in an error, prompting the corresponding status register bit (SR3) to be set.

A factory option provides in-system programming and erase with F_VPP in the 0.0V–2.2V range.

F_VPP at 12V ±5% (F_VPP2) is supported for a maximum of 100 cycles and 10 cumulative hours. The device can withstand 100,000 WRITE/ERASE operations when F_VPP = F_VCC.

During WRITE and ERASE operations, the WSM monitors the F_VPP voltage level. WRITE/ERASE operations are allowed only when F_VPP is within the ranges specified in Table 11.

When F_VCC is below VLKO or F_VPP is below VPPLK, any WRITE/ERASE operation is prevented.

DEVICE RESET

To correctly reset the device, the RST# signal must be asserted (RST# = VIL) for a minimum of ^{t}RP. After reset, the device can be accessed for a READ operation with a delayed access time of ^{t}RWH from the rising edge of RST#. The circuitry used for generating the RST# signal needs to be common with the rest of the system reset to ensure that correct system initialization occurs. Please refer to the timing diagram for further details.

POWER-UP SEQUENCE

The following power-up sequence is recommended to properly initialize internal chip operations:

- At power-up, RST# should be kept at VIL for 2µs after F_VCC reaches F_VCC (MIN).
- VCCQ should not come up before F_VCC.
- F_VPP should be kept at VIL to maximize data integrity.

When the power-up sequence is completed, RST# should be brought to VIH. To ensure proper power-up, the rise time of RST# (10%–90%) should be < 10µs.

Table 11
F_VPP Ranges (V)

DEVICE	MIN	MAX
In-System	0.9	2.2
In-Factory	11.4	12.6

FLASH ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage to Any Ball Except F_Vcc and F_Vpp
with Respect to Vss .... -0.5V to +2.45V
F_Vpp Voltage (for BLOCK ERASE and PROGRAM
with Respect to Vss) .... -0.5V to +13.5V**
F_Vcc and VccQ Supply Voltage
with Respect to Vss .... -0.3V to +2.45V
Output Short Circuit Current 100mA
Operating Temperature Range .... -40ºC to +85ºC
Storage Temperature Range .... -55ºC to +125ºC
Soldering Cycle .... 260ºC for 10s

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum DC voltage on F_Vpp may overshoot to +13.5V for periods <20ns.

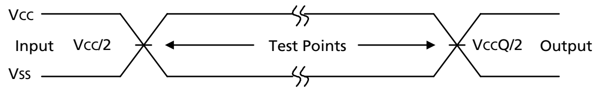
RECOMMENDED OPERATING CONDITIONS

($-40°C \leq T_A \leq +85°C$)

PARAMETER		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc supply voltage (MT28C6428P18)		F_Vcc, S_Vcc	1.70	1.90	V	
Vcc supply voltage (MT28C6428P20)		F_Vcc, S_Vcc	1.80	2.20	V	
I/O supply voltage (MT28C6428P18)		VccQ	1.70	1.90	V	
I/O supply voltage (MT28C6428P20)		VccQ	1.80	2.20	V	
F_Vpp voltage (when used as logic control)		F_Vpp1	0.9	2.2	V	
F_Vpp in-factory programming voltage		F_Vpp2	11.4	12.6	V	
Data retention supply voltage		S_Vdr	1.0	–	V	
Block erase cycling (F_Vpp1)	F_Vpp = F_Vpp1	F_Vpp1	–	100,000	Cycles	
	F_Vpp = F_Vpp2	F_Vpp2	–	100	Cycles	1

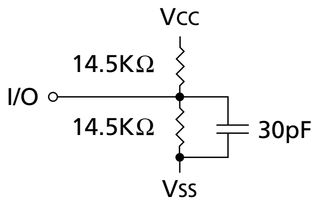
NOTE: 1. F_Vpp = F_Vpp2 is a maximum of 10 cumulative hours.

Figure 13
AC Input/Output Reference Waveform



AC test inputs are driven at Vcc for a logic 1 and Vss for a logic 0. Input timing begins at Vcc/2, and output timing ends at VccQ/2. Input rise and fall times (10% to 90%) < 5ns.

Figure 14
Output Load Circuit



COMBINED DC CHARACTERISTICS[1]

			F_V_{CC}/$V_{CC}Q$ = 1.70V–1.90V or 1.80V–2.20V				
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Input Low Voltage		V_{IL}	0.0	–	0.4	V	2
Input High Voltage		V_{IH}	$V_{CC}Q$ - 0.4	–	$V_{CC}Q$	V	2
Output Low Voltage I_{OL} = 100µA (Flash)		V_{OL}	–	–	0.10	V	
Output Low Voltage I_{OL} = 100µA (SRAM)		V_{OL}	–	–	0.3	V	
Output High Voltage I_{OH} = -100µA (Flash)		V_{OH}	$V_{CC}Q$ - 0.1	–	–	V	
Output High Voltage I_{OH} = -100µA (SRAM)		V_{OH}	$V_{CC}Q$ - 0.3	–	–	V	
F_V_{PP} Lockout Voltage		V_{PPLK}	–	–	0.4	V	
F_V_{PP} During PROGRAM/ERASE Operations		F_V_{PP1}	0.9	–	2.2	V	
		F_V_{PP2}	11.4	–	12.6	V	3
F_V_{CC} Program/Erase Lock Voltage		V_{LKO}	1.0	–	–	V	
Input Leakage Current		I_L	–	–	1.0	µA	
Output Leakage Current		I_{OZ}	–	–	1.0	µA	
F_V_{CC} Read Current Asynchronous Random Read, 100ns cycle		I_{CC1}	–	–	15	mA	4, 5
Asynchronous Page Read, 100ns/35ns cycle		I_{CC2}	–	–	5	mA	4, 5
F_V_{CC} plus S_V_{CC} Standby Current		I_{CC3}	–	25	70	µA	
F_V_{CC} Program Current		I_{CC4}	–	–	55	mA	
F_V_{CC} Erase Current		I_{CC5}	–	18	45	mA	
F_V_{CC} Erase Suspend Current		I_{CC6}	–	6	70	µA	6
F_V_{CC} Program Suspend Current		I_{CC7}	–	6	70	µA	6
Read-While-Write Current		I_{CC8}	–	–	80	mA	

NOTE:
1. All currents are in RMS unless otherwise noted.
2. V_{IL} may decrease to -0.4V and V_{IH} may increase to $V_{CC}Q$ + 0.3V for durations not to exceed 20ns.
3. 12V F_V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.
4. APS mode reduces I_{CC} to approximately I_{CC3} levels.
5. Test conditions: Vcc = V_{CC} (MAX), CE# = V_{IL}, OE# = V_{IH}. All other inputs = V_{IH} or V_{IL}.
6. I_{CC6} and I_{CC7} values are valid when the device is deselected. Any read operation performed while in suspend mode will add a current draw of I_{CC1} or I_{CC2}.

(continued on next page)

COMBINED DC CHARACTERISTICS[1] (continued)

			F_V_{CC}/$V_{CC}Q$ = 1.70V–1.90V or 1.80V–2.20V				
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
S_V_{CC} Read/Write Operating Supply Current – Random Access Mode	V_{IN} = V_{IH} or V_{IL} chip enabled, I_{OL} = 0	I_{CC9}	–	12	15	mA	
S_V_{CC} Read/Write Operating Supply Current – Page Access Mode	V_{IN} = V_{IH} or V_{IL} chip enabled, I_{OL} = 0	I_{CC10}	–	2	3	mA	
Deep Power-Down Current		I_{CC11}	–	35	45	µA	
F_V_{PP} Current	F_V_{PP} ≤ F_V_{CC}	I_{PP1}	0.5	–	1	µA	
(Read, Standby Erase Suspend, Program Suspend)	F_V_{PP} ≥ F_V_{CC}		50	–	200	µA	

NOTE:
1. All currents are in RMS unless otherwise noted.
2. V_{IL} may decrease to -0.4V and V_{IH} may increase to $V_{CC}Q$ + 0.3V for durations not to exceed 20ns.
3. 12V F_V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.
4. APS mode reduces I_{CC} to approximately I_{CC3} levels.
5. Test conditions: Vcc = V_{CC} (MAX), CE# = V_{IL}, OE# = V_{IH}. All other inputs = V_{IH} or V_{IL}.
6. I_{CC6} and I_{CC7} values are valid when the device is deselected. Any read operation performed while in suspend mode will add a current draw of I_{CC1} or I_{CC2}.

CAPACITANCE

(T_A = +25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS
Input Capacitance	C	7	12	pF
Output Capacitance	COUT	13	15	pF

FLASH READ CYCLE TIMING REQUIREMENTS

		-80		-85		
		F_VCC = 1.80V–2.20V		F_VCC = 1.70V–1.90V		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
Address to output delay	^{t}AA		80		85	ns
F_CE# LOW to output delay	^{t}ACE		80		85	ns
Page address access	^{t}APA		30		35	ns
F_OE# LOW to output delay	^{t}AOE		25		30	ns
F_RP# HIGH to output delay	^{t}RWH		200		250	ns
CE# or OE# HIGH to output High-Z	^{t}OD		20		25	ns
Output hold from address, CE# or OE# change	^{t}OH	0		0		ns
READ cycle time	^{t}RC		80		85	ns
RST# deep power-down	^{t}RWHOP		100		100	µs

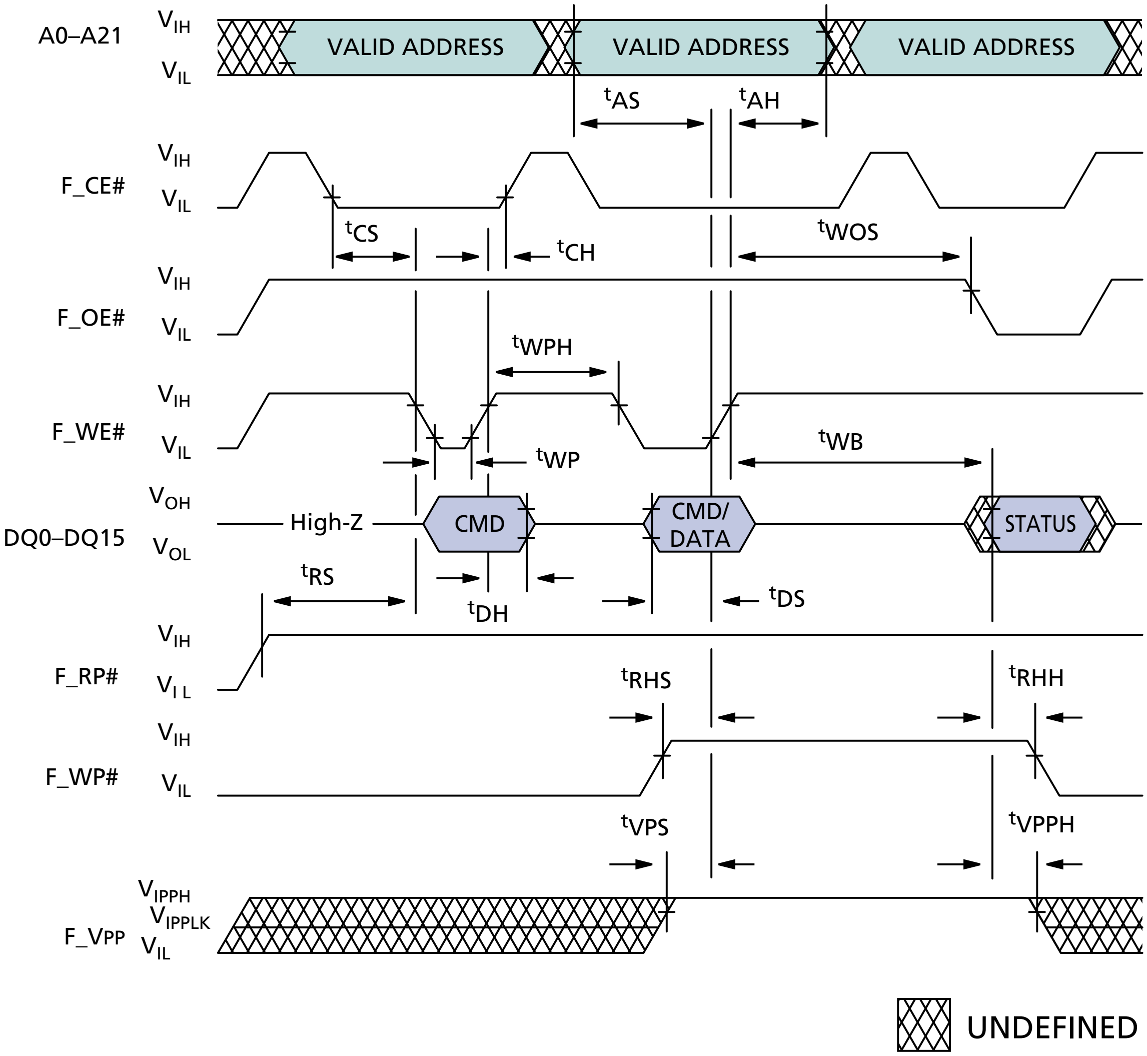
FLASH WRITE CYCLE TIMING REQUIREMENTS

		-80		-85		
		F_V$_{CC}$ = 1.80V–2.20V		F_V$_{CC}$ = 1.70V–1.90V		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Reset HIGH recovery to F_WE# going LOW	^{t}RS	150		150		ns
F_CE# setup to F_WE# going LOW	^{t}CS	0		0		ns
Write pulse width	^{t}WP	50		70		ns
Data setup to F_WE# going HIGH	^{t}DS	50		70		ns
Address setup to F_WE# going HIGH	^{t}AS	50		70		ns
F_CE# hold from F_WE# HIGH	^{t}CH	0		0		ns
Data hold from F_WE# HIGH	^{t}DH	0		0		ns
Address hold from F_WE# HIGH	^{t}AH	0		0		ns
Write pulse width HIGH	^{t}WPH	30		30		ns
F_WP# setup to F_WE# going HIGH	^{t}RHS	0		0		ns
F_V$_{PP}$ setup to F_WE# going HIGH	^{t}VPS	200		200		ns
Write recovery before READ	^{t}WOS	50		50		ns
Write recovery before READ in opposite bank	^{t}WOA	0		0		ns
F_WP# hold from valid SRD	^{t}RHH	0		0		ns
F_V$_{PP}$ hold from valid SRD	^{t}VPPH	0		0		ns
F_WE# HIGH to data valid	^{t}WB		^{t}AA + 50		^{t}AA + 50	ns

FLASH ERASE AND PROGRAM CYCLE TIMING REQUIREMENTS

	-80/-85		
PARAMETER	**TYP**	**MAX**	**UNITS**
4KW parameter block program time	40	800	ms
32KW parameter block program time	320	6,400	ms
Word program time	8	10,000	µs
4KW parameter block erase time	0.3	6	s
32KW parameter block erase time	0.5	6	s
Program suspend latency	5	10	µs
Erase suspend latency	5	20	µs
Chip programming time		20	S

TWO-CYCLE PROGRAMMING/ERASE OPERATION



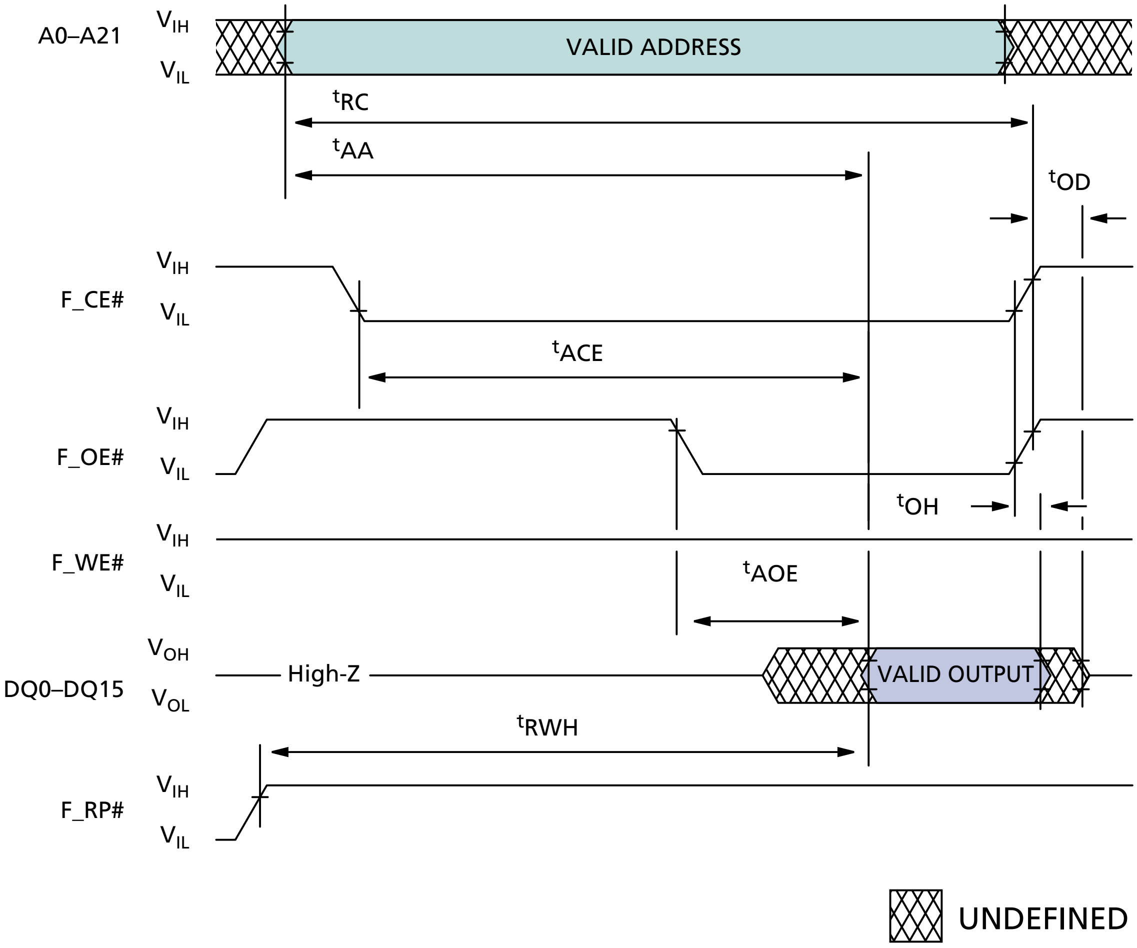
WRITE TIMING PARAMETERS

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^{t}RS	150		150		ns
^{t}CS	0		0		ns
^{t}WP	50		70		ns
^{t}DS	50		70		ns
^{t}AS	50		70		ns
^{t}CH	0		0		ns
^{t}DH	0		0		ns

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^{t}AH	0		0		ns
^{t}RHS	0		0		ns
^{t}VPS	200		200		ns
^{t}WOS	50		50		ns
^{t}RHH	0		0		ns
^{t}VPPH	0		0		ns
^{t}WB		^{t}AA + 50		^{t}AA + 50	ns

NOTE: 1. The WRITE cycles for the WORD PROGRAMMING command are followed by a READ ARRAY DATA cycle.

SINGLE ASYNCHRONOUS READ OPERATION

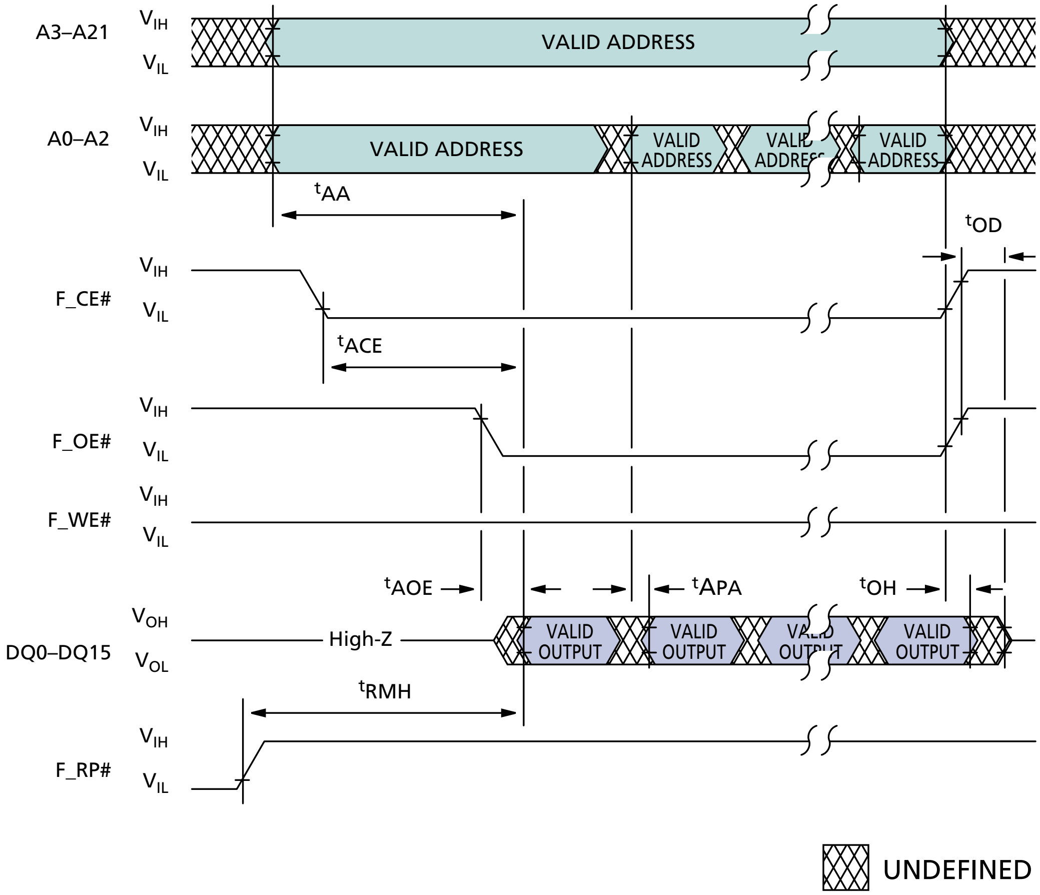


READ TIMING PARAMETERS

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^tAA		80		85	ns
^tACE		80		85	ns
^tAOE		25		30	ns
^tRWH		200		250	ns

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^tOD		20		25	ns
^tOH	0		0		ns
^tRC		80		85	ns

ASYNCHRONOUS PAGE MODE READ OPERATION

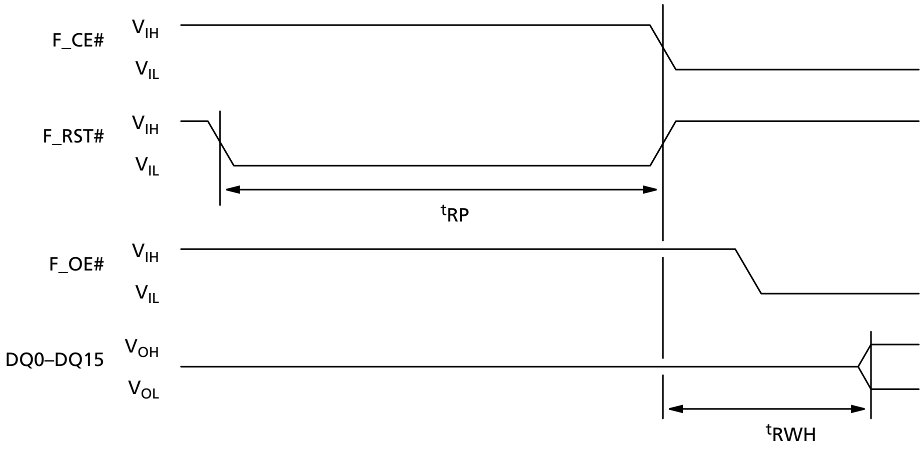


READ TIMING PARAMETERS

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^tAA		80		85	ns
^tACE		80		85	ns
^tAPA		30		35	ns
^tAOE		25		30	ns

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^tRWH		200		250	ns
^tOD		20		25	ns
^tOH	0		0		ns

RESET OPERATION



READ TIMING PARAMETERS

	-80		-85		
	F_Vcc = 1.80V–2.20V		F_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^tRWH		200		250	ns
^tRP	100		100		ns

Table 12
CFI

OFFSET	DATA	DESCRIPTION
00	2Ch	Manufacturer code
01	B6h	Top boot block device code
	B7h	Bottom boot block device code
02–0F	reserved	Reserved
10, 11	0051,0052	“QR”
12	0059	“Y”
13, 14	0003, 0000	Primary OEM command set
15, 16	0039, 0000	Address for primary extended table
17, 18	0000, 0000	Alternate OEM command set
19, 1A	0000, 0000	Address for OEM extended table
1B	0017	F_VCC MIN for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1C	0022	F_VCC MAX for Erase/Write; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
1D	00B4	F_VPP MIN for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD
1E	00C6	F_VPP MAX for Erase/Write; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD, 0000 = F_VPP ball
1F	0003	Typical timeout for single byte/word program, 2^n µs, 0000 = not supported
20	0000	Typical timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
21	0009	Typical timeout for individual block erase, 2^n ms, 0000 = not supported
22	0000	Typical timeout for full chip erase, 2^n ms, 0000 = not supported
23	000C	Maximum timeout for single byte/word program, 2^n µs, 0000 = not supported
24	0000	Maximum timeout for maximum size multiple byte/word program, 2^n µs, 0000 = not supported
25	0003	Maximum timeout for individual block erase, 2^n ms, 0000 = not supported
26	0000	Maximum timeout for full chip erase, 2^n ms, 0000 = not supported
27	0017	Device size, 2^n bytes
28	0001	Bus interface x8 = 0, x16 = 1, x8/x16 = 2
29	0000	Flash device interface description 0000 = async
2A, 2B	0000, 0000	Maximum number of bytes in multibyte program or page, 2^n
2C	0003	Number of erase block regions within device (4K words and 32K words)
2D, 2E	5F00, 0001	Top boot block device erase block region information 1, 8 blocks …
	0007, 0000	Bottom boot block device erase block region information 1, 8 blocks …
2F, 30	0000, 0001	Erase block region information 1, 8 blocks …
	0020, 0000	…of 8KB
31, 32	000E, 0000	15 blocks of ….
33, 34	0000, 0001	……64KB
35, 36	0007, 0000	Top boot block device ……96KB blocks of
	5F00, 0001	Bottom boot block device ……96KB blocks of

(continued on the next page)

Table 12
CFI (continued)

OFFSET	DATA	DESCRIPTION
37, 38	0020, 0000	Top boot block device……64KB
	0000, 0001	Bottom boot block device……64KB
39, 3A	0050, 0052	"PR"
3B	0049	"I"
3C	0030	Major version number, ASCII
3D	0031	Minor version number, ASCII
3E 3F 40 41	00E6 0002 0000 0000	Optional Feature and Command Support Bit 0 Chip erase supported no = 0 Bit 1 Suspend erase supported = yes = 1 Bit 2 Suspend program supported = yes = 1 Bit 3 Chip lock/unlock supported = no = 0 Bit 4 Queued erase supported = no = 0 Bit 5 Instant individual block locking supported = yes = 1 Bit 6 Protection bits supported = yes = 1 Bit 7 Page mode read supported = yes = 1 Bit 8 Synchronous read supported = yes = 1 Bit 9 Simultaneous operation supported = yes = 1
42	0001	Program supported after erase suspend = yes
43, 44	0003,0000	Bit 0 block lock status active = yes; Bit 1 block lock down active = yes
45	0018	F_VCC supply optimum; Bit7–Bit4 Volts in BCD; Bit3–Bit0 100mV in BCD
46	00C0	F_VPP supply optimum; Bit7–Bit4 Volts in Hex; Bit3–Bit0 100mV in BCD
47	0001	Number of protection register fields in JEDEC ID space
48, 49	0080, 0000	Lock bytes LOW address, lock bytes HIGH address
4A, 4B	0003, 0003	2^n factory programmed bytes, 2^n user programmable bytes
4C	0003	Background Operation 0000 = Not used 0001 = 4% block split 0002 = 12% block split 0003 = 25% block split 0004 = 50% block split
4D	0000	Burst Mode Type 0000 = No burst mode 00x1 = 4 words MAX 00x2 = 8 words MAX 00x3 = 16 words MAX 001x = Linear burst, and/or 002x = Interleaved burst, and/or 004x = Continuous burst
4E	0002	Page Mode Type 0000 = No page mode 0001 = 4-word page 0002 = 8-word page 0003 = 16-word page 0004 = 32-word page
4F	0008	SRAM density, 8Mb (512K x 16)

SRAM OPERATING MODES

SRAM READ ARRAY

The operational state of the SRAM is determined by S_CE1#, S_CE2, S_WE#, S_OE#, S_UB#, and S_LB#, as indicated in the Truth Table. To perform an SRAM READ operation, S_CE1#, and S_OE#, must be at VIL, and S_CE2 and S_WE# must be at VIH. When in this state, S_UB# and S_LB# control whether the lower byte is read (S_UB# VIH, S_LB# VIL), the upper byte is read (S_UB# VIL, S_LB# VIH), both upper and lower bytes are read (S_UB# VIL, S_LB# VIL), or neither are read (S_UB# VIH, S_LB# VIH) and the device is in a standby state.

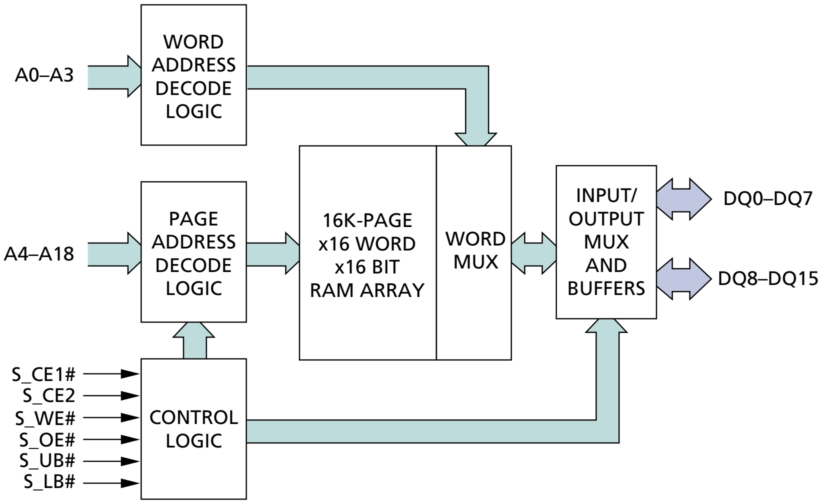
While performing an SRAM READ operation, current consumption may be reduced by reading within a 16-word page. This is done by holding S_CE1# and S_OE# at VIL, S_WE# and S_CE2 at VIH, and toggling addresses A0–A3. S_UB# and S_LB# control the data width as described above.

SRAM WRITE ARRAY

In order to perform an SRAM WRITE operation, S_CE1# and S_WE# must be at VIL, and S_CE2 and S_OE# must be at VIH. When in this state, S_UB# and S_LB# control whether the lower byte is written (S_UB# VIH, S_LB# VIL), the upper byte is written (S_UB# VIL, S_LB# VIH), both upper and lower bytes are written (S_UB# VIL, S_LB# VIL), or neither are written (S_UB# VIH, S_LB# VIH) and the device is in a standby state.

SRAM

SRAM FUNCTIONAL BLOCK DIAGRAM


A0–A3
WORD ADDRESS DECODE LOGIC
A4–A18
PAGE ADDRESS DECODE LOGIC
16K-PAGE x16 WORD x16 BIT RAM ARRAY
WORD MUX
INPUT/ OUTPUT MUX AND BUFFERS
DQ0–DQ7
DQ8–DQ15
S_CE1#
S_CE2
S_WE#
S_OE#
S_UB#
S_LB#
CONTROL LOGIC

TIMING TEST CONDITIONS

Input pulse levels........... 0.1V S_Vcc to 0.9V S_Vcc
Input rise and fall times 5ns
Input timing reference levels 0.5V
Output timing reference levels 0.5V
Operating Temperature .... -40°C to +85°C

NOTE: For input/output contacts, refer to the Capacitance Table.

SRAM READ CYCLE TIMING

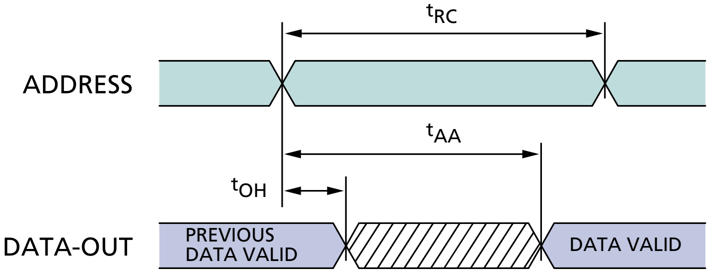
		-80		-85		
		S_Vcc = 1.80V–2.20V		S_Vcc = 1.70V–1.90V		
DESCRIPTION	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
READ cycle time	^{t}RC		80		85	ns
Address access time	^{t}AA		80		85	ns
Address access time (word mode)	^{t}AAW		25		25	ns
Chip enable to valid output	^{t}CO		80		85	ns
Output enable to valid output	^{t}OE		20		20	ns
Byte select to valid output	^{t}LB, ^{t}UB		80		85	ns
Chip enable to Low-Z output	^{t}LZ	0		0		ns
Output enable to Low-Z output	^{t}OLZ	0		0		ns
Byte select to Low-Z output	^{t}LBZ, ^{t}UBZ	0		0		ns
Chip enable to High-Z output	^{t}HZ	0	15	0	15	ns
Output disable to High-Z output	^{t}OHZ	0	15	0	15	ns
Byte select disable to High-Z output	^{t}LBHZ, ^{t}UBHZ	0	15	0	15	ns
Output hold from address change	^{t}OH	5		5		ns

SRAM WRITE CYCLE TIMING

		-80		-85		
		S_Vcc = 1.80V–2.20V		S_Vcc = 1.70V–1.90V		
DESCRIPTION	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
WRITE cycle time	^{t}WC		80		85	ns
Chip enable to end of write	^{t}CW		80		85	ns
Address valid to end of write	^{t}AW		80		85	ns
Byte select to end of write	^{t}LBW, ^{t}UBW		80		85	ns
Address setup time	^{t}AS	0		0		ns
Write pulse width	^{t}WP	50		50		ns
Write recovery time	^{t}WR	0		0		ns
Write to High-Z output	^{t}WHZ	0	15	0	15	ns
Data to write time overlap	^{t}DW	30		30		ns
Data hold from write time	^{t}DH	0		0		ns
End write to Low-Z output	^{t}OW	0		0		ns

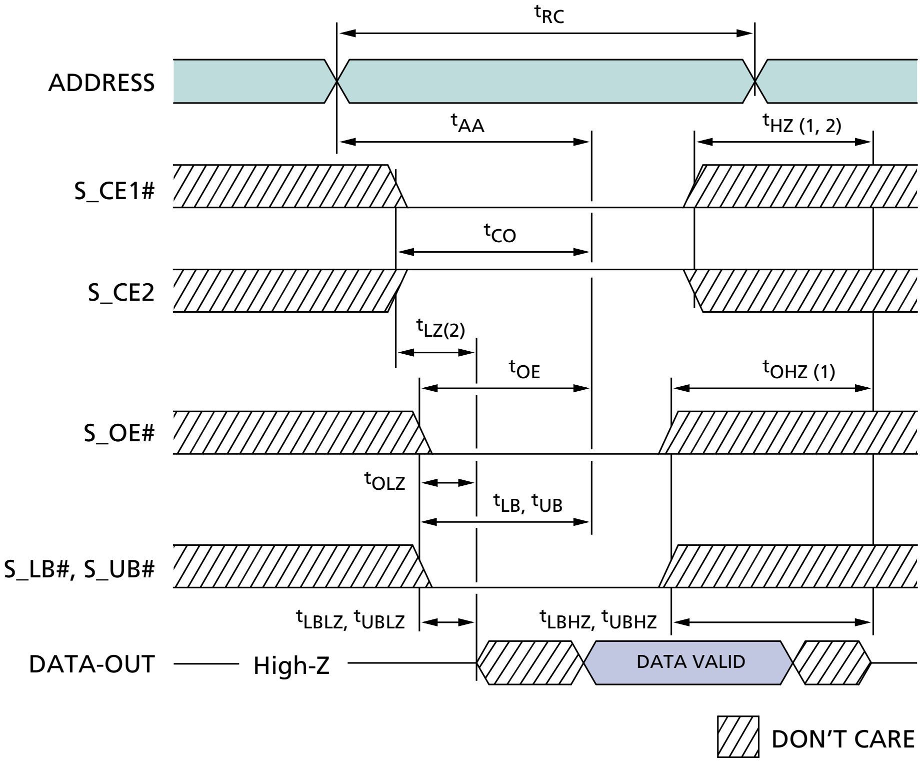
READ CYCLE 1

(S_CE1# = S_OE# = V$_{IL}$; S_CE2, S_WE# = V$_{IH}$)



READ CYCLE 2

(S_WE# = V$_{IH}$)

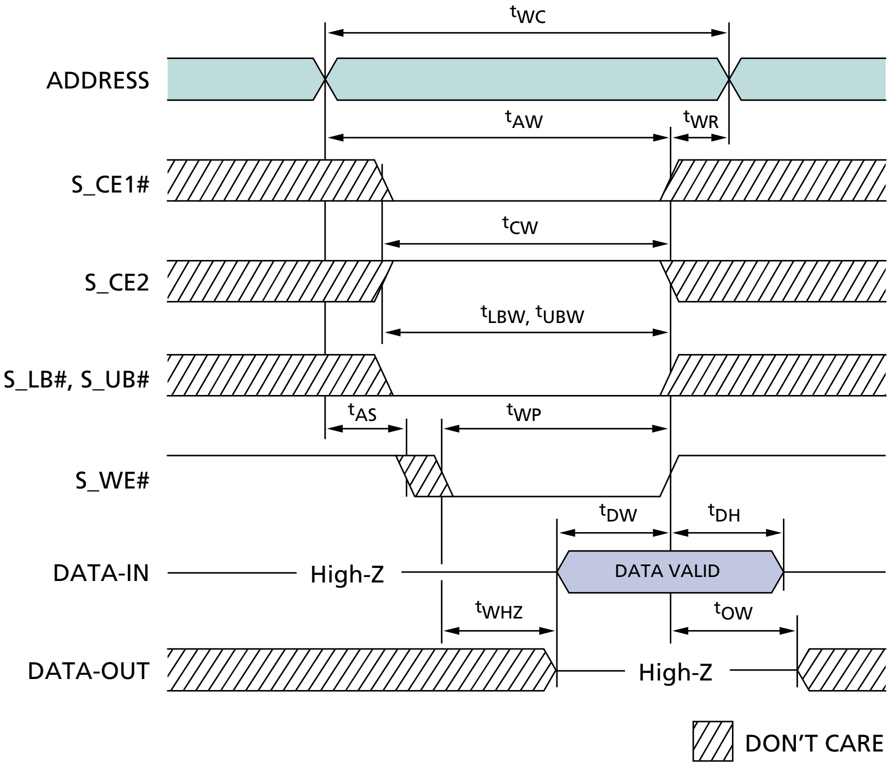


READ TIMING PARAMETERS

	-80		-85		
	S_V$_{CC}$ = 1.80V–2.20V		S_V$_{CC}$ = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^{t}RC		80		85	ns
^{t}AA		80		85	ns
^{t}CO		80		85	ns
^{t}OE		20		20	ns
^{t}LB, ^{t}UB		80		85	ns
^{t}LZ	0		0		ns

	-80		-85		
	S_V$_{CC}$ = 1.80V–2.20V		S_V$_{CC}$ = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
^{t}OLZ	0		0		ns
^{t}HZ	0	15	0	15	ns
^{t}OHZ	0	15	0	15	ns
^{t}LBHZ, ^{t}UBHZ	0	15	0	15	ns
^{t}OH	5		5		ns

WRITE CYCLE
(S_WE# CONTROL)

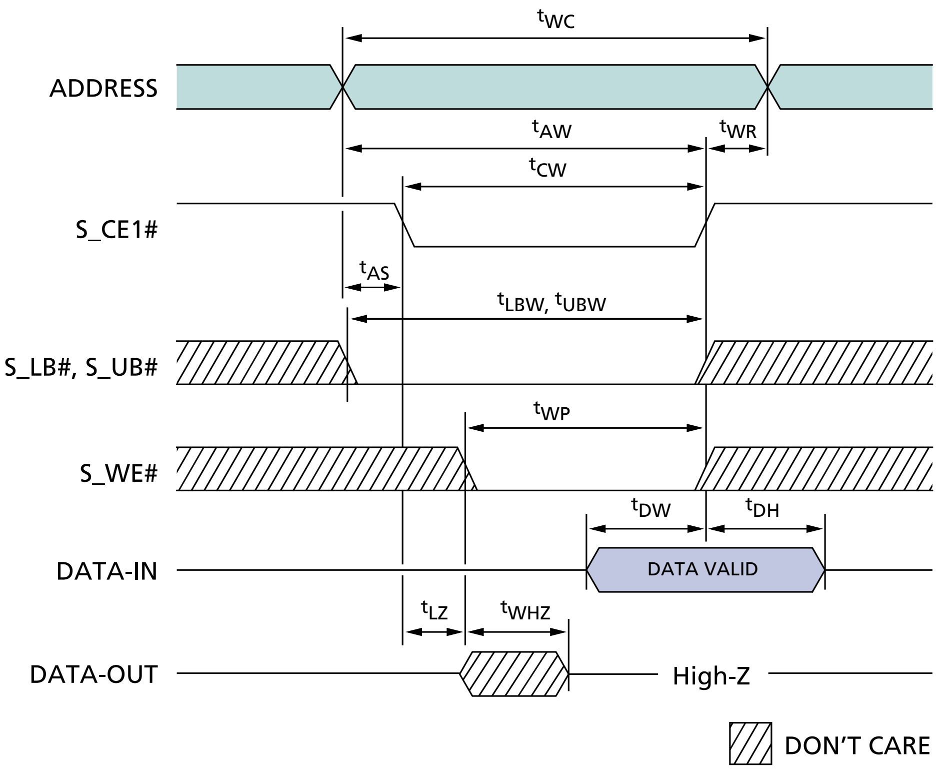


WRITE TIMING PARAMETERS

SYMBOL	-80		-85		UNITS
	S_VCC = 1.80V–2.20V		S_VCC = 1.70V–1.90V		
	MIN	MAX	MIN	MAX	
^{t}WC		80		85	ns
^{t}CW		80		85	ns
^{t}AW		80		85	ns
^{t}LBW, ^{t}UBW		80		85	ns
^{t}AS	0		0		ns

SYMBOL	-80		-85		UNITS
	S_VCC = 1.80V–2.20V		S_VCC = 1.70V–1.90V		
	MIN	MAX	MIN	MAX	
^{t}WP	50		50		ns
^{t}WR	0		0		ns
^{t}WHZ	0	15	0	15	ns
^{t}DW	30		30		ns
^{t}DH	0		0		ns
^{t}OW	0		0		ns

WRITE CYCLE 2
(S_CE1# CONTROL)

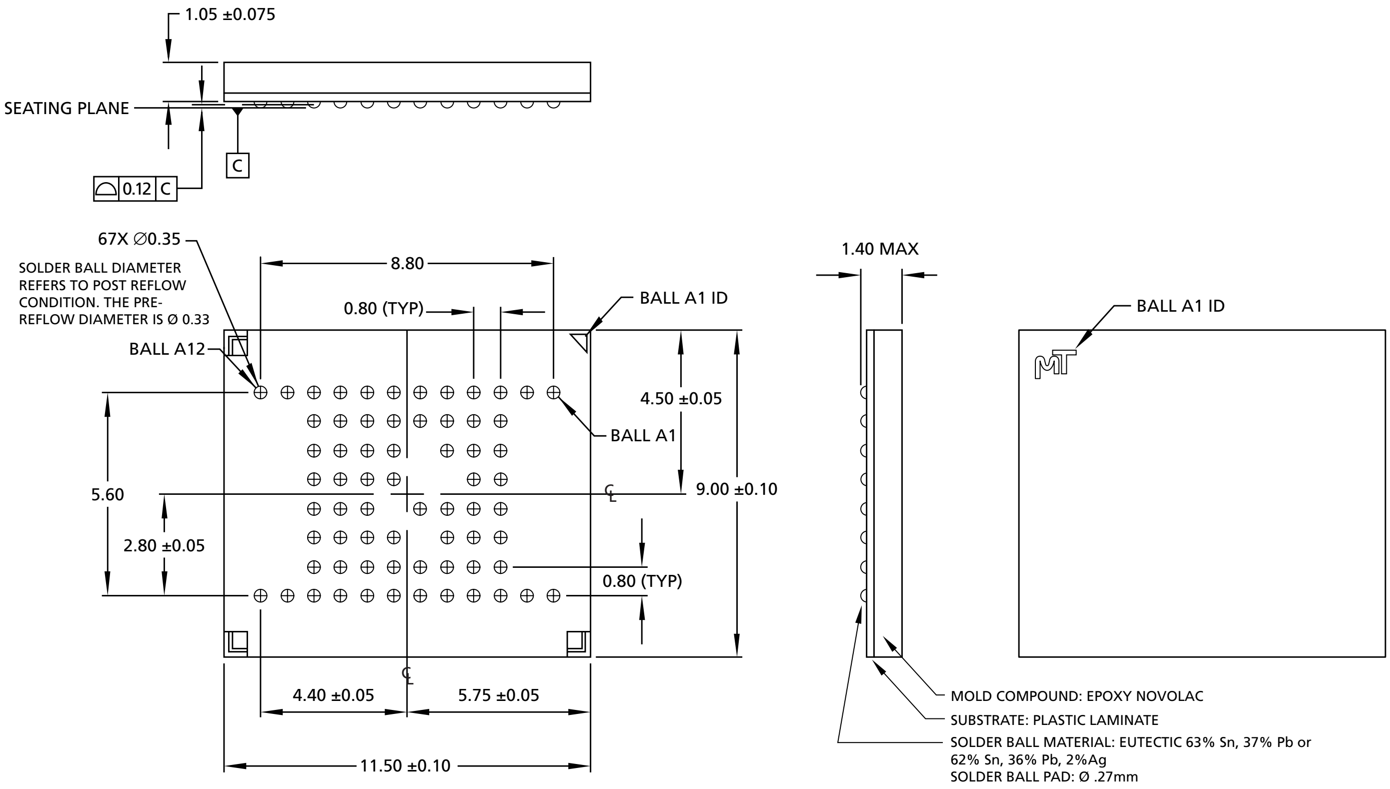


WRITE TIMING PARAMETERS

	-80		-85		
	S_Vcc = 1.80V–2.20V		S_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tWC		80		85	ns
tCW		80		85	ns
tAW		80		85	ns
tLBW, tUBW		80		85	ns
tAS	0		0		ns

	-80		-85		
	S_Vcc = 1.80V–2.20V		S_Vcc = 1.70V–1.90V		
SYMBOL	MIN	MAX	MIN	MAX	UNITS
tWP	50		50		ns
tWR	0		0		ns
tWHZ	0	15	0	15	ns
tDW	30		30		ns
tDH	0		0		ns
tOW	0		0		ns

67-BALL FBGA


1.05 ±0.075
SEATING PLANE
0.12 C
C
67X ∅0.35
SOLDER BALL DIAMETER REFERS TO POST REFLOW CONDITION. THE PRE-REFLOW DIAMETER IS Ø 0.33
8.80
0.80 (TYP)
BALL A1 ID
BALL A12
4.50 ±0.05
BALL A1
5.60
9.00 ±0.10
2.80 ±0.05
0.80 (TYP)
4.40 ±0.05
5.75 ±0.05
11.50 ±0.10
1.40 MAX
BALL A1 ID
MT
MOLD COMPOUND: EPOXY NOVOLAC
SUBSTRATE: PLASTIC LAMINATE
SOLDER BALL MATERIAL: EUTECTIC 63% Sn, 37% Pb or 62% Sn, 36% Pb, 2%Ag
SOLDER BALL PAD: Ø .27mm

NOTE: 1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.27mm per side.

DATA SHEET DESIGNATION

No Marking: This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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REVISION HISTORY

Rev. 4 .... 10/02
- ADVANCE designation removed.

Rev. 3, ADVANCE 7/02
- Corrected bottom boot block device address ranges
- Updated command descriptions
- Updated SR5 status register bit description
- Updated flowcharts
- Updated DC Characteristics
- Corrected Status Register section
- Updated the Read-While-Write/Erase Concurrency section
- Changed ^{t}RHS from 200ns (MIN) to 0ns (MIN)
- Changed C_{OUT} from 9 (TYP) and 12 (MAX) to 13 (TYP) and 15 (MAX)

Rev. 2, ADVANCE 4/02
- Updated the Combined DC Characteristics table
- Updated ^{t}AH and ^{t}RWH
- Updated the chip protection mode register information
- Updated the block locking information

Initial published release, ADVANCE, Rev. 1 .... 1/02